EMI-Optimized Design for the Isolated RS-485/RS-422 Transceiver

Introduction

This article examines how to achieve first-pass electromagnetic interference (EMI) success using a well-planned isolated RS-485/RS-422 transceiver solution design that takes the CA-IS3092W as an example and utilizes proper filter techniques, along with good PCB layout.

The CA-IS3092W is a fully integrated, isolated RS-485/RS-422 transceiver with a built-in isolated DC-DC converter, that eliminates the need for a separate isolated power supply in space constrained designs. The internal integrated DC-DC converter provides isolated 3.3V or 5V output (V_{ISO}) options programmed by pin SEL, can support up to 100mA load current. Integration of the isolated DC-DC converter along with the micro-power transformer into a single package makes a very compact solution. The DC-DC converter in the CA-IS3092W switches at about 70 MHz to reduce the size of the power transformer and enable integration in a small package. At this switching frequency, because of the fast dv/dt and di/dt, the spectral components of the switching converter fall into 30MHz to 1GHz spectrum that may be subjected to regulatory restrictions by some EMI standards like EN55032.

This article discusses design techniques and PCB layout guidelines for improving EMC/EMI performance and help designers to meet EN55032 radiated emissions Class A standard even without the use of shielding techniques.

Optimized Design and Layout

PCB layout and components selection are the key when designing a circuit for optimum EMC/EMI performance, even the internal isolated DC-DC converter of the CA-IS3902W has been optimized for robust communication in harsh industrial environments. In this section, we will discuss how to design and layout an EMI-optimized PCB for the isolated RS-485/RS-422 transceivers based on the CA-IS3902W.

Stitch capacitor between GNDA and GNDB

The CA-IS3902W does not require any additional external components to build an isolated RS-422/RS-485 transceiver, however, for the EMC/EMI sensitive applications, designers need to consider the noise resources to keep any noise coupling from the isolated power converter away from signal path and other circuits in the system. The internal switching controller is one of the key noise resources; another one is the micro-transformer operating at up to 70MHz frequency. For the compact design, the primary and secondary windings of the micro-transformer inside CA-IS3902W are very close to each other, hence, a parasitic capacitance is formed between those windings. Noise generated by the switching operation couple through this parasitic capacitance, can be in the form of conducted or radiated emissions. Also, conducted emissions can take the form of voltage or current, and each of these can be categorized as common-mode or differential-mode.

For an ideal transformer, only the current flowing through the primary coil of the transformer will be coupled to the secondary side. However, due to the parasitic parameters as mentioned above, the coupling capacitance between primary side and secondary side, and the inductance leakage of micro-transformer, interlayer capacitance of primary side, high dv/dt switching between the isolated barriers can cause current flow into parasitic capacitances and can be coupled to the secondary side. Then, the large PCB sizes might create large current loops and such large current loops may cause higher radiations which can then be picked-up by nearby systems in the end application. If a primary return path is provided for these parasitic currents in the design, it will help to reduce electromagnetic radiation. Without this path, the parasitic current will appear at the output of VISO and GNDB pins as common mode current, which form a dipole antenna and produce radiation interference, especially, if these unintended paths have a large loop area, current flowing through the loop can radiate, causing strong electromagnetic interference (EMI).

In general, a safety rated Y-capacitor is placed between GNDA and GNDB (across the isolation barrier) to help reduce this common mode noise. The Y-capacitor create a very short path with a small loop area for the parasitic current return to primary side, reducing the EMI generated on the board as shown in Figure 1. The larger capacitance value can better suppress EMI.

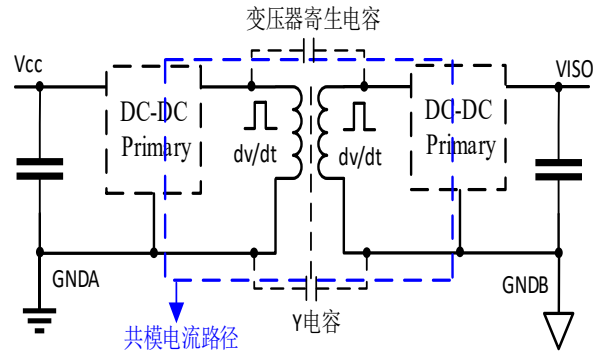


Figure 1. Common mode current route

Poor EMI performance is often found in boards with isolation barriers. Image charges are formed on the ground layer beneath a signal layer when a signal runs through traces on a PCB. When the charge image is forced to stop, for example, at an isolation barrier, differential currents and voltages are created in the PCB and generate EMI as well. The distributed inductance of the Y-capacitor will also reduce the high-frequency suppression performance.

A capacitor is formed when two layers in a PCB overlap. As shown in Figure 2 and Figure 3, PCB layers can be specially placed and sized to create capacitance, we call this a stitching capacitor. Stitching capacitors in the PCB allow image charges following the current path of signals to remain steady, reducing high-switching signals without adding additional cost to the PCB. Also, the inductance between the two parallel plates of this type of capacitor is very low and the capacitance is distributed over a large area.

The stitch capacitance of the board is calculated as,

$$C = \varepsilon_r \times \varepsilon_0 \times S/d$$

where ε_0 is a constant (8.854×10^{-12} F/m) and ε_r is dielectric constant determined by the PCB material, for FR4 board, ε_r = 4.5; S is the overlapping area of two PCB layers; D is the relative distance between the two layers.

The stitching capacitance is basically independent of the copper thickness, 1oz copper can be used in most applications. For example, if d = 456mm, S = 0.0022m^2, using the equation above, the stitching capacitance is approximately 181.9pF.

For the overlap stitching capacitance design between the primary ground (GNDA) layer and secondary ground (GNDB) layer of the micro-transformer, due to the requirements of creepage distance and external clearance distance, the relative distance between these two layers should not be less than 0.4mm. For a 4-layer PCB design, stitching capacitance is generally placed in the middle two layers, see Figure 2.

In addition to the Figure 2 overlapping solution, the stitching capacitor can also be formed by floating stitching, as shown in Figure 3. The total equivalent stitching capacitance is equivalent to C1 and C2 in series.

According to Chipanalog's radiated emissions test result as shown in the *EMI test comparative and analysis* section, any high frequency noise is eliminated with the use of the stitching capacitance.

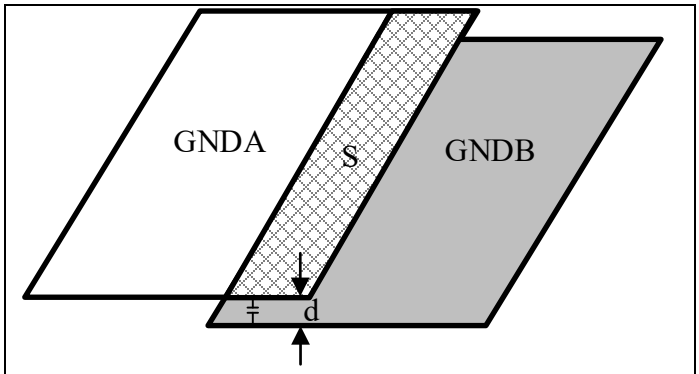


Figure 2. Overlap Stitch capacitance between GNDA and GNDB

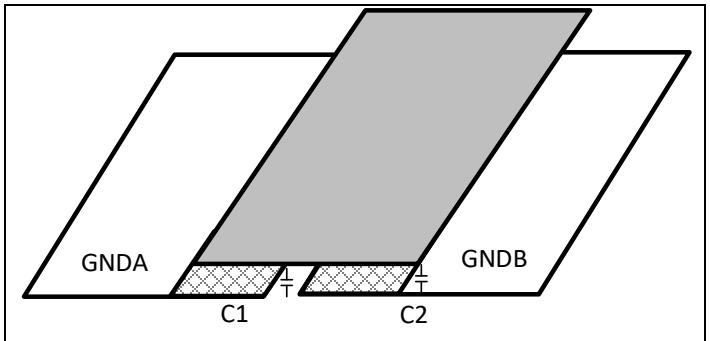


Figure 3. Floating Stitch capacitance between GNDA and GNDB

V_{CC} and V_{ISO} Decoupling capacitors

Since the operating frequency of the CA-IS3092W's built-in micro-transformer is up to 70MHz, higher dv/dt and di/dt will cause strong electromagnetic radiation. Therefore, the loop area of the primary current paths and secondary current paths outside of the micro- transformer directly

affects the intensity of radiation interference. The larger the current loop, the stronger the radiation. This can be an important concern for designers who need to meet strict electromagnetic compatibility (EMC) guidelines. The loop area of these current paths must be minimized in the PCB layout.

High frequency bypass capacitors (such as, 10nF) must be placed closer to VCC and VISO pins, less than 2 mm distance away from device pins, to reduce parasitic inductance and current loop. This is very essential for optimized radiated emissions performance. Also, the bulk capacitors of at least 10μF must be placed on power converter input (V_{CC}) and output (V_{ISO}) supply pins as shown in Figure 4 and Figure 5.

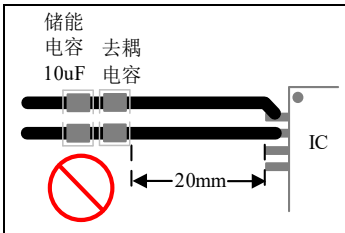


Figure 4. Not Recommended

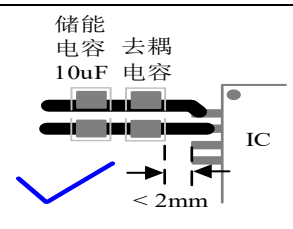


Figure 5. Recommended

If vias need to be placed on the power trace and ground trace, the vias must be placed outside of the decoupling capacitors rather than between the capacitors and the IC pins to reduce the influence of via parasitic inductance, as shown in Figure 6 and Figure 7. If the PCB space is available, multiple vias can be placed in parallel. In this way, the parasitic inductance of vias is equivalent to multiple inductors parallel, which can further reduce the parasitic inductance.

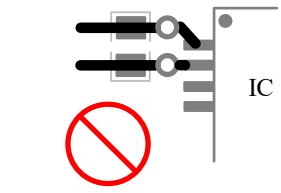


Figure 6. Not Recommended

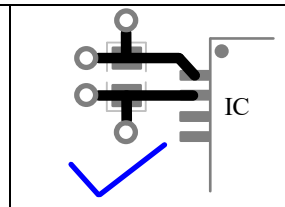


Figure 7. Recommended

Ensure that these decoupling capacitors are small size so that they offer least inductance (ESL). We recommend to use MLCC capacitor for most applications. Figure 8 shows the capacitor's equivalent circuit.

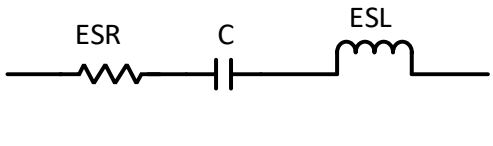


Figure 8. Capacitor's equivalent circuit

ESR: equivalent series resistance of capacitor;

ESL: distributed inductance of capacitor and parasitic inductance of PCB wiring.

$$Z(\Omega) = \sqrt{(ESR)^2 + (X_{ESL} + X_C)^2}$$

$$X_{ESL}(\Omega) = 2\pi f L$$

$$X_C(\Omega) = \frac{1}{2\pi f C}$$

$$f_{RES} = \frac{1}{2\pi\sqrt{LC}}$$

Figure 9 shows the impedance vs. frequency curve of a 10nf / 10V MLCC capacitor. In this figure, we can see that when the frequency is low, the equivalent inductance of the capacitor is much smaller than the capacitance, which shows the capacitive characteristic; As the frequency increased and greater than the self-resonant frequency, the equivalent inductance of this capacitor is greater than the capacitive reactance, which shows the inductive characteristic, and the impedance increases with the increase of frequency. For the decoupling capacitor selection, the self-resonant frequency should be near 70MHz and its low-frequency harmonics. If needed, designers can use multiple capacitors with different capacitance value in parallel to cover broader frequency range.

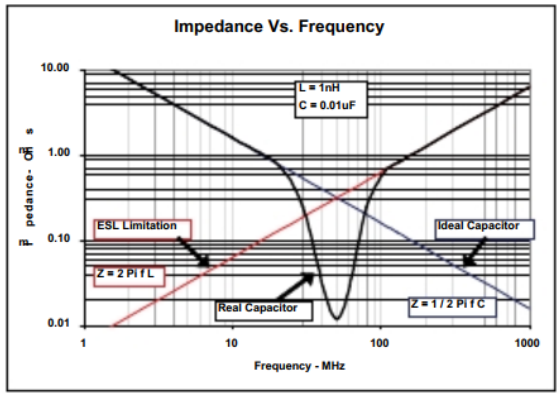


Figure 9. Impedance vs. frequency of a 10nf / 10V MLCC

In addition to using discrete capacitors, designers can add stitching bypass capacitors for V_{CC} and V_{ISO} on the PCB layout as well. These can be formed by overlap stitching capacitor between V_{CC} plane and A-side ground plane(GNDA), V_{ISO} plane and B-side ground plane(GNDB). The distributed inductance of PCB stitching capacitor is very small, can get better performance at high-frequency compared with the discrete capacitors, also cover wide frequency range. For example, the interval between GNDA of the first layer and V_{CC} of the second layer of PCB is 0.2mm, the overlapping area of V_{CC} and GNDA is 0.0021m^2. According to the calculation equation, the stitching capacitance is as below:

C = 4.5 x 8.544 x 0.0021 / 0.0002pF = 403.7 PF

Same PCB design can be used for the V_{ISO} plan and GNDB on the secondary side.

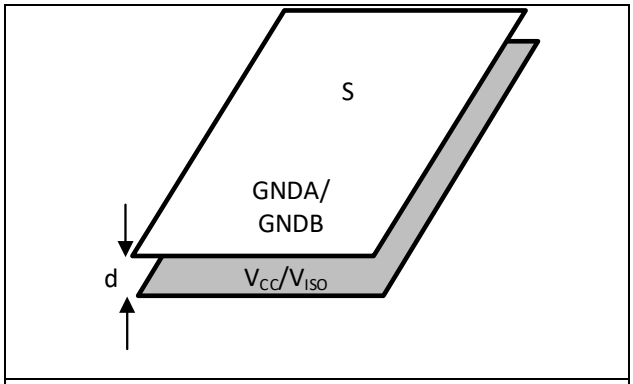


Figure 10. Overlap stitching capacitor between V_{CC}/V_{ISO} and GNDA/GNDB

Building the edge guarding

Noise on the ground and power layers in a PCB can radiate upon reaching the edge of the board. Using the edge guarding, or a via guard ring around the ground layers will be helpful to limit this radiation. Shrink the power layer (V_{CC} and V_{ISO}) to form the edge guarding, so that the electric field noise is only conducted in the ground layers(GNDA and GNDB), to reduce the radiation and interfere to the external system. For example, if the power supply plane edge relative to the ground plane edge shrinks more than 20 times the spacing of the two layers (i.e. 20H rule), the radiation can be effectively reduced, as shown in Figure 11.

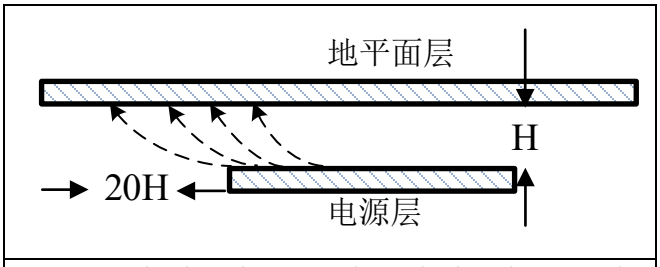


Figure 11. Shrinking the power plane edge based on 20H rule

A grounding vias can also be added around the PCB to form a via guard ring to return the noise to the ground and reduce external radiation, as shown in Figure 12. Please follow below guidelines to design the via guard ring:

- Place more than one row of vias;
- If there are more than two rows of vias, the vias placed in the two rows shall be staggered from each other;
- The spacing between vias in the same row shall not be less than the 1/20 of electromagnetic wave length λ. Usually, the 3mm via spacing is enough to block electromagnetic interference below 1GHz frequency.

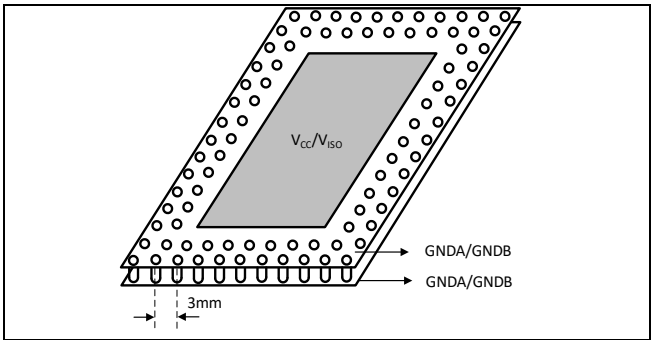


Figure 12. Vias guard ring around the edges of the GNDA and GNDB layers

While helpful, the use of edge guarding, or a via guard ring around the ground layers, has a significant tradeoff because edge guarding reduces the area on the stitching capacitor layer. In some cases, the board size might need to be slightly increased to obtain the optimum stitching capacitance.

Ferrite Bead

For the EMI input filter, consider of the inherent equivalent series inductance of the bypass capacitors as shown in Figure 8, a second filter stage is often essential to provide supplemental differential-mode noise attenuation at a high frequency using a ferrite bead, with impedance typically rated at 100 MHz. In general, the differential-mode noise filter inductance is sized to attenuate the fundamental and low-frequency harmonics. Use the minimum inductance possible to meet the low-frequency filtering demands, as a higher inductance with more turns increases the inductor's equivalent parallel capacitance and thus the self-resonant frequency, compromising its performance at high frequencies.

A ferrite bead is inserted between the input power supply and the CA-IS3092W's DC/DC converter input (VCC pin), thereby breaking the path of larger common-mode current loops, and offer high attenuation to select frequencies and block the switching noise.

Choose this ferrite bead such that it offers the highest impedance at the switching frequency and its harmonic frequencies. Here we recommend FBG1005-601Y which can cover wider frequency range, see Figure 13 impedance vs. frequency curve.

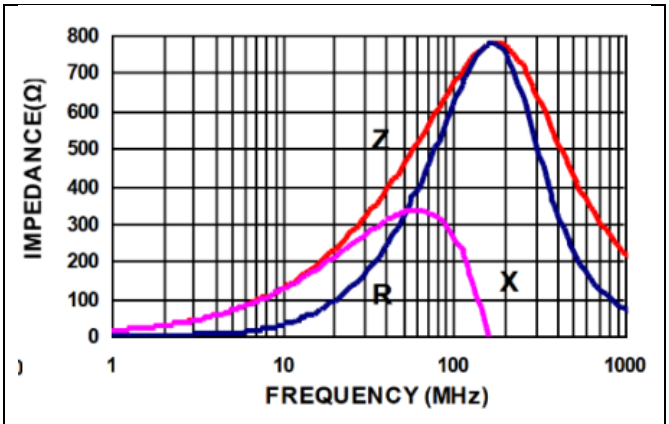


Figure 13 Impedance vs. frequency curve of FBG1005-601Y

Place the ferrite bead separate out the device from the rest of the PCB, ensure the power and ground planes before and after ferrite bead stay separated all through the PCB, see Figure 14 and Figure 15. The conducted emission can be further reduced by additional improvements using more small input ferrite bead, also using multiple capacitors with different capacitance value in parallel can cover broader frequency range.

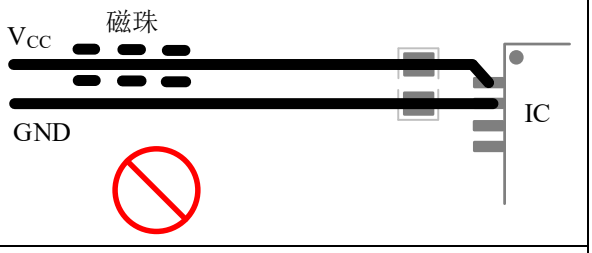


Figure 14. Not Recommended

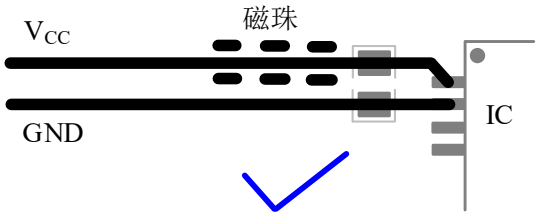
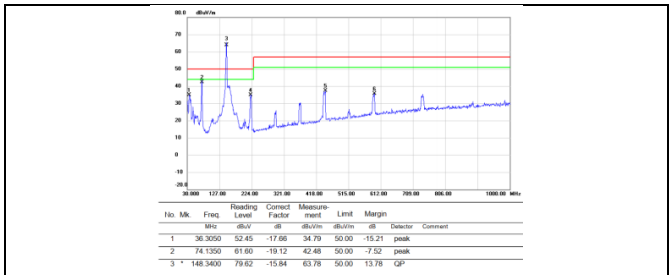


Figure 15. Recommended

EMI test comparative and analysis

1. Only a 10μF external bulk capacitor is used between V_{CC} and GNDA on primary-side, and between V_{ISO} and GNDB on secondary-side separately. There is no other discrete decoupling capacitors at pins VCC and VISO. The PCB overlapping stitch capacitor between GNDA and GNDB is 180pF; The stitching capacitance between V_{CC} and GNDA on primary side, and between V_{ISO} and GNDB on secondary-side are 500pF respectively (refer to Figure 10). The radiated emission test result is shown in Figure 16;

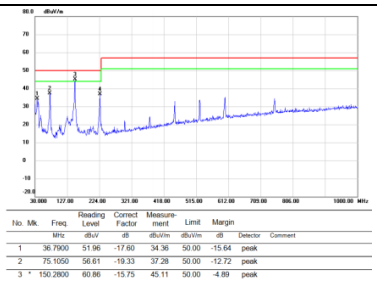


No.	Mk.	Freq.	Reading Level	Correct Factor	Measure-ment	Limit	Margin	Detector	Comment
		MHz	dBuV	dB	dBuV/m	dBuV/m	dB		
1		36.3050	52.45	-17.66	34.79	50.00	-15.21	peak	
2		74.1350	61.60	-19.12	42.48	50.00	-7.52	peak	
3	*	148.3400	79.62	-15.84	63.78	50.00	13.78	QP	

Figure 16. The stitching capacitors between V_{CC} and GNDA, V_{ISO} and GNDB are about 500pF respectively;; Input voltage is 5V. 5V output with 100mA load at V_{ISO}

2. Only a 10μF external bulk capacitor and 800pF PCB overlap stitching capacitors are used between V_{CC} and GNDA on primary-side, and between V_{ISO} and GNDB on secondary-side for the supply bypass (refer to Figure 10). There is no other discrete decoupling

capacitors at pins VCC and VISO. The PCB overlapping stitch capacitor between GNDA and GNDB is 180pF. The radiated emission test result is shown in Figure 17;



No.	Mk.	Freq.	Reading Level	Correct Factor	Measure-ment	Limit	Margin		
		MHz	dBuV	dB	dBuV/m	dBuV/m	dB	Detector	Comment
1		36.7900	51.96	-17.60	34.36	50.00	-15.64	peak	
2		75.1050	56.61	-19.33	37.28	50.00	-12.72	peak	
3	*	150.2800	60.86	-15.75	45.11	50.00	-4.89	peak	

Figure 17. The stitching capacitors between V_{CC} and GNDA, V_{ISO} and GNDB are 800pF respectively; Input voltage is 5V. 5V output with 100mA load at V_{ISO}

3. Keep 10μF external bulk capacitors and PCB overlap stitching capacitors between V_{CC} and GNDA on primary-side, between V_{ISO} and GNDB on secondary-side, and between GNDA and GNDB in above test. Add a 10nF and a 470pF high frequency ceramic capacitors between V_{CC} and GNDA, and between V_{ISO} and GNDB respectively (refer to Figure 18). The radiated emission test result is shown in Figure 19;

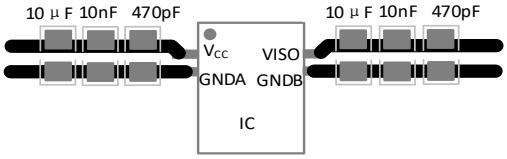
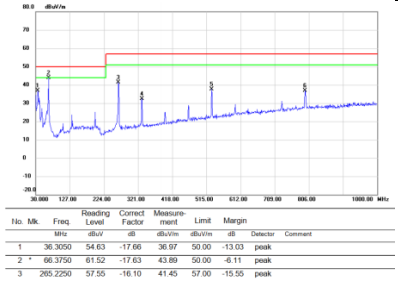


Figure 18. Add 10nF+470pF high frequency ceramic decoupling capacitors at pins VCC and VISO respectively.



No.	Mk.	Freq.	Reading Level	Correct Factor	Measure-ment	Limit	Margin		
		MHz	dBuV	dB	dBuV/m	dBuV/m	dB	Detector	Comment
1		36.3050	54.63	-17.66	36.97	50.00	-13.03	peak	
2	*	66.3750	61.52	-17.63	43.89	50.00	-6.11	peak	
3		265.2250	57.55	-16.10	41.45	57.00	-15.55	peak	

Figure 19. add 10 nF +470pF decoupling capacitors; Input voltage is 5V; 5V output with 100mA load at V_{ISO}

4. Keep all of bypass capacitors in #3 on the primary-side and secondary-side, also added a FBG1005-601Y ferrite bead connected in series at the supply input V_{CC}, see Figure 20. The radiated emission test result is shown in Figure 21.

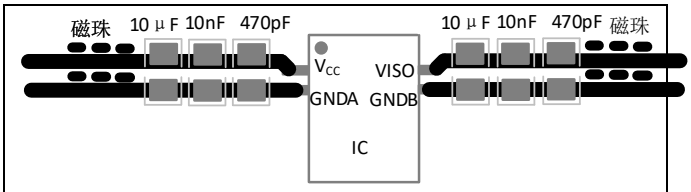
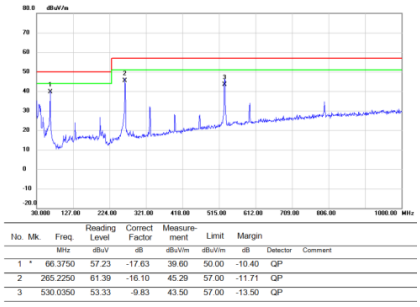


Figure 20. add 10 nF +470pF high frequency ceramic decoupling capacitors at pins of VCC and VISO respectively; add a ferrite bead at supply input.



No.	Mk.	Freq.	Reading Level	Correct Factor	Measure-ment	Limit	Margin		
		MHz	dBuV	dB	dBuV/m	dBuV/m	dB	Detector	Comment
1	*	66.3750	57.23	-17.63	39.60	50.00	-10.40	QP	
2		265.2250	61.39	-16.10	45.29	57.00	-11.71	QP	
3		530.0350	53.33	-9.83	43.50	57.00	-13.50	QP	

Figure 21. Add FBG1005-601Y ferrite bead at supply input. Input voltage is 5V; 5V output with 100mA load at V_{ISO}

Based on above test results, we can get below conclusions:

1. The overlap PCB stitching capacitance between the primary ground GNDA and the secondary ground GNDB greatly improve the radiation suppression performance in the 30MHz-1GHz frequency band by about 20dBμV/m attenuation;

2. The PCB overlap stitching capacitance between primary V_{CC} and GNDA, and between secondary V_{ISO} and GNDB can significantly improve the radiation suppression performance in 30MHz-1GHz frequency band by about 10dBμV/m attenuation;

3. The 10nF and 470pF high frequency ceramic capacitors, placed between primary V_{CC} and GNDA, and between secondary V_{ISO} and GNDB, provide 20dBμV/m attenuation at 150MHz frequency, also improve the radiation suppression performance for other frequencies;

4. FBG1005-601Y ferrite bead provides about 3dBμV/m attenuation at the 70MHz fundamental frequency.

Design example

In this section, we offer a design example based above discussion to optimize a PCB board for EMC/EMI testing. Figure 22 to Figure 25 show a fully tested PCB implementation of the CA-IS3092W and Figure 26 provides the schematic for this test board. This design use four-layer PCB layout, the PCB length and width are 99mm, copper thickness is 1.0mm. The insulation thickness between the top signal layer and the second signal layer is 0.2mm; the insulation thickness is 0.465mm between the second layer and third layers, and 0.2mm between the third layer and bottom signal layer.

The PCB overlapping stitch capacitor between GNDA and GNDB is 180pF; The stitching capacitance between V_{CC} and GNDA on primary side, and between V_{ISO} and GNDB on secondary-side are 800pF respectively. See below figures for the PCB layout with edge guarding.

In this design, FBL1 and FBL2 are FBG1005-601Y ferrite beads. $C_2 = C_5 = 10\mu F$, C3 = C6 = 10nF, C4 = C7 = 470pF, see Figure 26. The test result is shown in Figure 21, this solution meets EN55032 radiated emissions Class A standard, and also leave 10.4dBμV/m design margin.

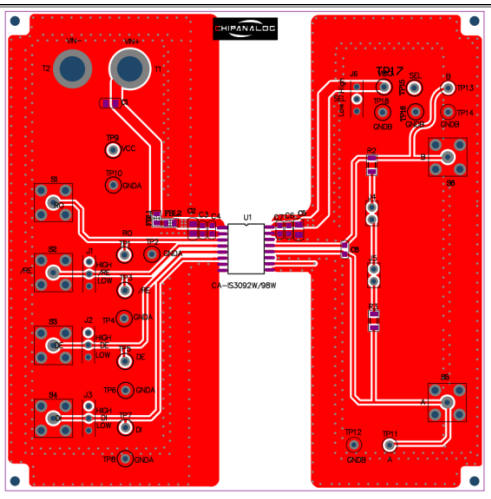


Figure 22. Top layer

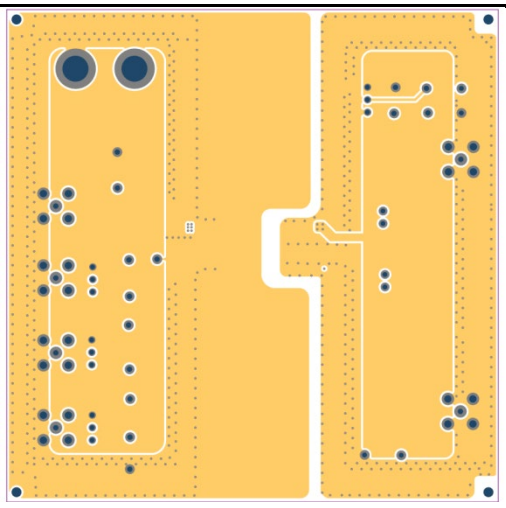


Figure 23. Layer 2

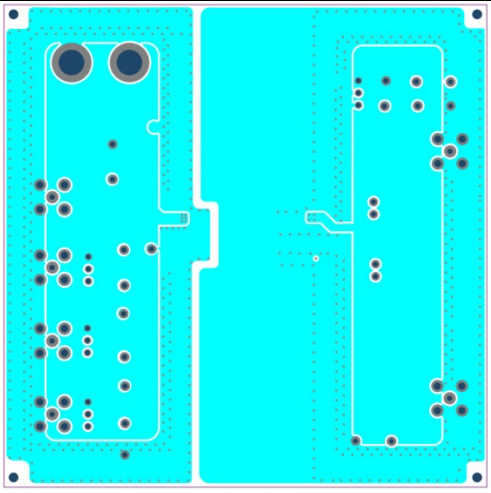


Figure 24. Layer 3

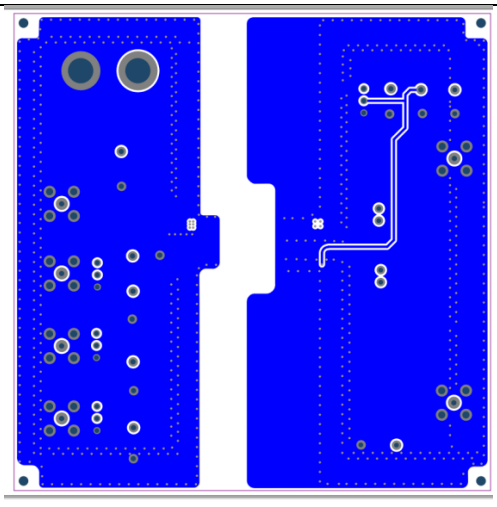


Figure 25. Bottom layer

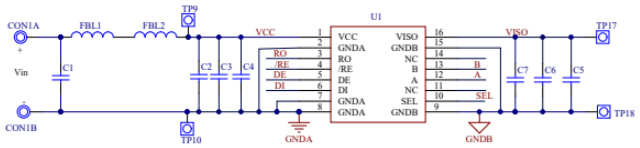


Figure 26. CA-IS3092W test board schematic

Conclusion

By considering how to control EMI in the early stage of design, the risk and trouble of certification of the isolated RS-485/RS-422 transceiver with internal DC-DC power converter can be reduced. Even the CA-IS3092W has optimized radiated emissions performance with built in low-emission DC-DC converter, designers can achieve further improvements in emissions by above suggested decoupling capacitors, stitching capacitors, ferrite bead filter and good PCB layout. To manage EMI, a metal case shield soldered to the PCB ground plane also effectively mitigates high-frequency emissions.

The guidelines discussed in this article can help to reduce the impact of large PCBs and long cables on radiated emissions results and enable the end-equipment to comply to EN55032 standard emissions limits.

Revision History

Revision Number	Description	Page Changed	Revision Date
Version 1.00	Initial version	All	Feb. 2022

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