# CA-IF428x Home Bus System (HBS) Compatible Transceiver

## 1. Features

- **Configurability Enables Flexible Design**
  - 9.6kbps to 200kbps Data Rate
  - Adjustable Receiver Thresholds and Internal Threshold Configuration Option
  - Large Receiver Hysteresis
  - Adjustable Slew Rate on Transmit Signals
  - Dynamic Cable Termination Improves Signal Quality for High-Speed Communication
  - Support Bus Polarity Detection (CA-IF4289 only)
- **Integrated Protection for Robust Communication**
  - IEC 61000-4-2 ±8kV Contact and ±15kV Air-Gap ESD Protection
  - IEC 61000-4-5 ±1kV Surge Protection with Selected External Components
- **Compact 4mm*4mm QFN Package**
- **Operation temperature range from -40°C to +105°C**

## 2. Applications

- HVAC
- Data over Power Applications (PoD)
- Digital Signage
- Industrial PLC
- Remote Monitoring and Sensing

## 3. General Description

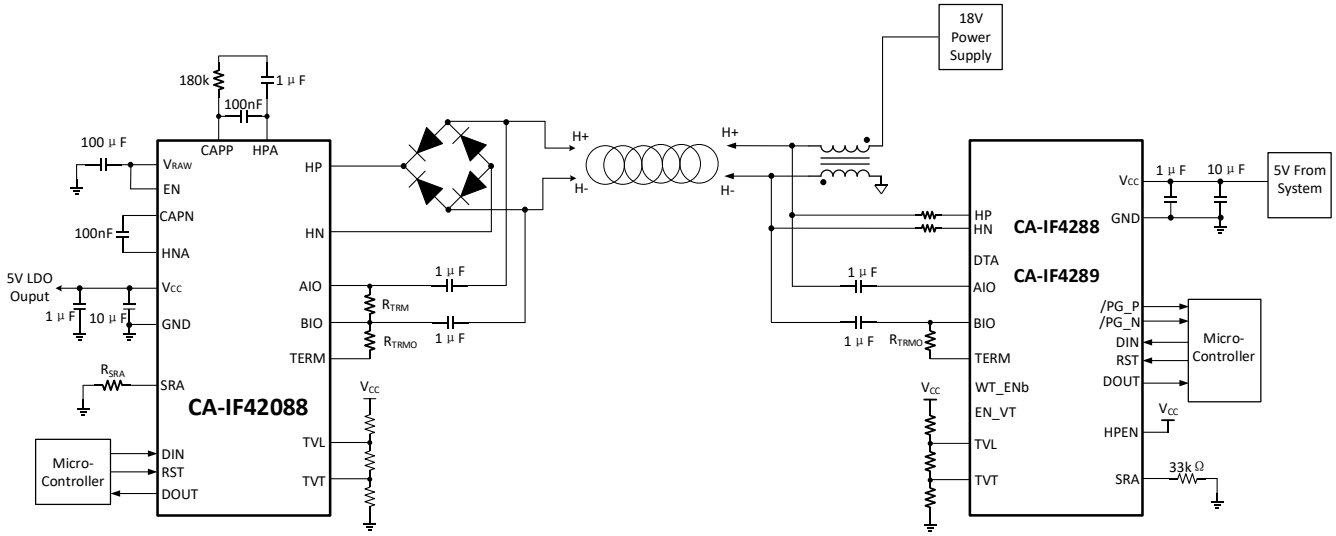
The CA-IF428x family of devices complies with the home bus standard requirements while improving communication in harsh environments and minimizing the need for external components. The home bus standard was designed to ease communication between multiple different devices connected to a single bus, where data and power are passed on one single pair of wires, to allow a mutual exchange of information at any time from any room in a home or building among various appliances, equipment, or security devices.

The CA-IF428x family is configurable to operate up to 200kbps with adjustable receiver thresholds and dynamic cable termination for improved communication with high data rates. This family of devices is rated for operation up to ±8kV contact discharge and ±15kV air gap ESD protection, and survives up to ±1kV surge events with selected external components. Additional features include adjustable receiver hysteresis and driver slew rate. Also, the CA-IF4289 features bus polarity detection, help to prevent incorrect bus connections. The CA-IF428x devices have been designed for operation in home bus systems but they are not only limited to those networks, can be used to transmit data over any compatible system.

All devices are specified over the -40°C to +105°C operating temperature range and are available in a compact 24-pin 4mm*4mm QFN package.

**DEVICE INFORMATION**

| Part Number | Package | Package Size |
|---|---|---|
| CA-IF4288 | QFN24 | 4mm*4mm |
| CA-IF4289 | QFN24 | 4mm*4mm |




**Simplified Home Bus System (HBS)**

## 4. Ordering Information

**Table 4-1. Ordering Information**

| Part Number | Temperature Range | Package |
|---|---|---|
| CA-IF4288 | -40°C to +105°C | QFN24 4mm*4mm |
| CA-IF4289 | -40°C to +105°C | QFN24 4mm*4mm |

# Contents

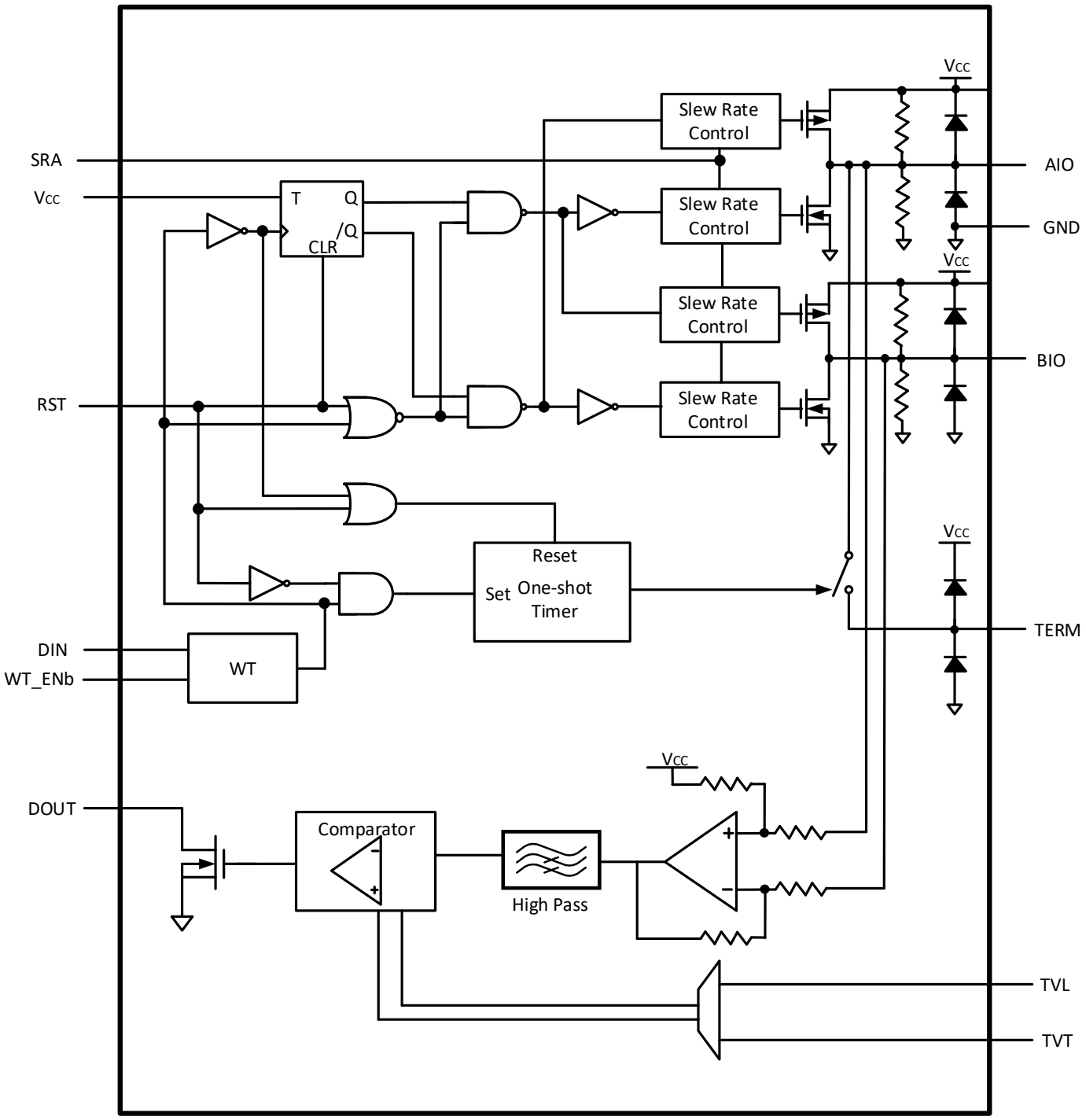


**Revision History**

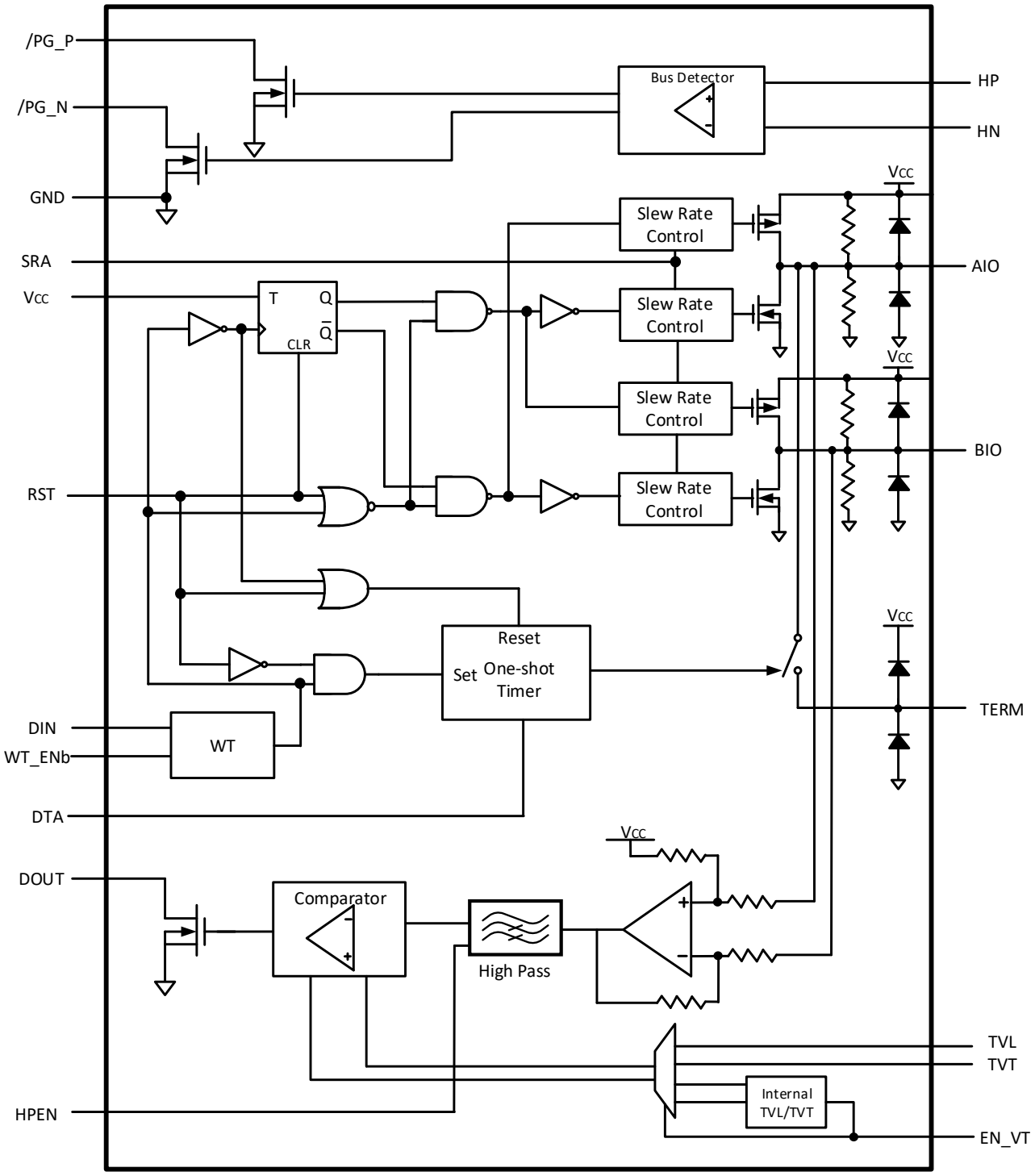
| Revision Number | Description | Page Changed | Revision Date |
|---|---|---|---|
| Version 1.00 | N/A | N/A | 2022/01/19 |
| Version 1.01 | Changed CA-IF4288 pin 20 definition, HPEN to NC. | 4, 6, 7, 14, 16 | 2022/04/19 |
| Version 1.02 | 1. Added Soldering Temperature Profile and Tape and Reel Information section.<br>2. Changed HBM ESD rating from ±4kV to ±6kV.<br>3. Changed package name to QFN. | 19, 20, 6<br>1, 2, 18, 19, 20 | 2022/11/29 |
| Version 1.03 | 4. Updata the test condition of $V_{LEAD}$ and $V_{TRAIL}$ | 7 | 2024/03/27 |

## 5. Simplified Block Diagram

### 5.1. CA-IF4288 simplified Block Diagram



## 5.2. CA-IF4288 simplified Block Diagram



## 6. Pin Configuration

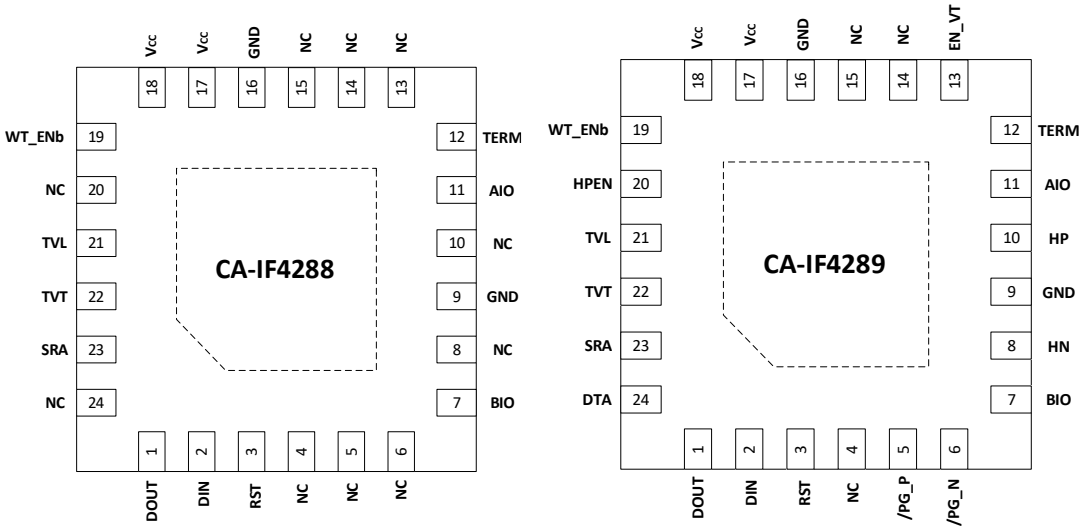



**Figure 6-1. CA-IF4288 / 4289 Pin Configuration**

**Table 6-1. CA-IF4288/ 4289 Pin Description**

| NAME | PIN NUMBER | | TYPE | DESCRIPTION |
|---|---|---|---|---|
| | CA-IF4288 | CA-IF4289 | | |
| DOUT | 1 | 1 | LOGIC I/O | Data output, open-drain output. Connect an external pull-up resistor to the logic voltage supply. |
| DIN | 2 | 2 | LOGIC I/O | Data input. |
| RST | 3 | 3 | LOGIC I/O | Bus reset control input. |
| N.C. | 4,5,6,8,10,13,14,15,20,24 | 4,14,15 | - | Not connected. |
| /PG_P | - | 5 | LOGIC I/O | Open-drain output, active low when bus polarity is positive ($V_{HP}$-$V_{HN}$ > 3V). |
| /PG_N | - | 6 | LOGIC I/O | Open-drain output, active low when bus polarity is negative ($V_{HN}$-$V_{HP}$ > 3V). |
| BIO | 7 | 7 | HOME BUS | Home bus data input and output. Connect BIO to home bus through a 1μF capacitor in series with a 4.7Ω resistor for 57.6kbps operation. |
| HN | - | 8 | HOME BUS | Home bus interface. Connect a 200Ω resistor between HN and home bus for surge protection. |
| GND | 9, 16 | 9, 16 | GND | Ground. |
| HP | - | 10 | HOME BUS | Home bus interface. Connect a 200Ω resistor between HN and home bus for surge protection. |
| AIO | 11 | 11 | HOME BUS | Home bus data input and output. Connect BIO to home bus through an external 1μF capacitor in series with a 4.7Ω resistor for 57.6kbps operation. |
| TERM | 12 | 12 | HOME BUS | Switched bus termination. Connect a resistor between TERM and BIO to adjust home bus cable termination for better signal quality. |
| EN_VT | - | 13 | LOGIC I/O | Enable control for internal threshold configuration, active high. Connect EN_VT to GND through an 1MΩ pull-down resistor. Leave the pin floating to disable internal threshold configuration. |
| $V_{CC}$ | 17, 18 | 17, 18 | POWER | Power supply input. Connect +5V to $V_{CC}$, and bypass $V_{CC}$ to GND with at least 1μF ceramic capacitor as close to the device as possible. |

| NAME | PIN NUMBER | | TYPE | DESCRIPTION |
|---|---|---|---|---|
| | CA-IF4288 | CA-IF4289 | | |
| WT_ENb | 19 | 19 | LOGIC I/O | Enable control for data input timeout protection, active low. Connect WT_ENb to GND through an 180kΩ pull-down resistor. Leave the pin floating to disable timeout detection. |
| HPEN | - | 20 | LOGIC | High pass filter enable input. Connect HPEN to $V_{CC}$ to enable the internal high pass filter on the receiver input. Connect HPEN to GND to disable the internal high pass filter. Do not leave HPEN open. |
| TVL | 21 | 21 | HOME BUS | Leading edge data threshold, see the Receiver Threshold Adjustment section for more information. |
| TVT | 22 | 22 | HOME BUS | Trailing edge data threshold, see the Receiver Threshold Adjustment section for more information. |
| SRA | 23 | 23 | LOGIC | Slew rate control input. Connect SRA to GND through a resistor to adjust the slew rate of AIO and BIO data output edges. |
| DTA | - | 24 | LOGIC | Dynamic termination time adjustment. For the CA-IF4289, Connect DTA to GND through a 10kΩ to 500kΩ resistor to adjust the dynamic termination turn on time; Leave DTA floating, the dynamic termination time is default of 34µs. For the CA-IF4288, the termination time is fixed at 34µs. |
| EP | - | - | - | Exposed pad, connect to Ground. |

# 7. Specifications

## 7.1. Absolute Maximum Ratings[1]

| PARAMETERS | MIN | MAX | UNITS |
|---|---|---|---|
| VCC to GND | -0.3 | 6.0 | V |
| AIO, BIO, TERM, SRA to GND | -0.3 | Vcc+0.3 | V |
| HP, HN to GND | -0.3 | +28 | V |
| HP to HN and HN to HP | -28 | +28 | |
| Continuous current into pins of $V_{CC}$, AIO, BIO, TERM | -100 | +100 | mA |
| Continuous current into all other pins | -50 | +50 | mA |
| Operating Temperature Range | -40 | +105 | °C |
| Junction Temperature | | +150 | °C |
| Storage Temperature Range | -40 | +150 | °C |
| Soldering Temperature (reflow) | | +260 | °C |

**Note:**

1. The stresses listed under "Absolute Maximum Ratings" are stress ratings only, not for functional operation condition. Exposure to absolute maximum rating conditions for extended periods may cause permanent damage to the device.

## 7.2. ESD Rating

| | | | VALUE | UNITS |
|---|---|---|---|---|
| $V_{ESD}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, AIO,BIO to GND. | ±30 | kV |
| | | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all other pins. | ±6 | kV |
| | | IEC 61000-4-2 air discharge, AIO,BIO,TERM to GND | ±15 | kV |
| | | IEC 61000-4-2 contact discharge, Electrostatic discharge | ±8 | kV |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins. | ±2 | kV |

## 7.3. Recommended Operating Conditions

| PARAMETERS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| $V_{CC}$ | | 4.5 | | 5.5 | V |
| $V_{TVT}$ | | | 1.5 | | V |
| $V_{TVL}$ | | | 2.5 | | V |
| $R_{SRA}$ | | | 33k | | Ohm |
| $T_A$ | Ambient temperature | -40 | 25 | 105 | °C |
| $T_J$ | Junction temperature | | | 150 | °C |

## 7.4. Thermal Information

| PARAMETERS | | QFN | UNITS |
|---|---|---|---|
| $R_{\theta JA}$ | IC Junction-to-Ambient Thermal Resistance | 52 | °C/W |

## 7.5. Electrical Characteristics

Over recommended operating conditions, $T_A$ = –40°C to 105°C (unless otherwise noted).

### 7.5.1. DC characteristics($V_{CC}$)

| Symbol | Parameter | Test Conditions | MIN | TYP | MAX | Units |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Power supply voltage | | 4.5 | 5.0 | 5.5 | V |
| $I_{CC}$ | Supply current | $V_{CC}$=5.0V, no loading, 57.6kbps, $C_L$=0pF | | 1.7 | 2.5 | mA |
| $V_{UV}$ | $V_{CC}$ undervoltage lockout | $V_{CC}$ voltage falling | 4.0 | 4.2 | 4.4 | V |
| $V_{UV\_hys}$ | $V_{CC}$ undervoltage lockout hysteresis | | | 100 | | mV |

### 7.5.2. DC characteristics /Transmit Channel

| Symbol | Parameter | Test Conditions | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| $V_{TOH}$ | Output voltage high | AIO, BIO to GND, $I_{load}$=45mA to GND | Vcc-0.6 | | | V |
| $V_{TOL}$ | Output voltage low | AIO, BIO to GND, $I_{load}$=45mA to $V_{CC}$ | | | 0.6 | V |
| $R_{TERM}$ | Termination switch on resistance | TERM to AIO | 2.5 | 5 | 10 | Ohm |
| $R_{IN}$ | AIO,BIO transmit input resistance | Input resistance of AIO and BIO when they are unconnected, DIN=$V_{CC}$ | 7 | 10 | 13 | K Ω |
| $V_{AIO}$/ $V_{BIO}$ | Bias voltage ratio matching | AIO, BIO unconnected | -1 | | +1 | % |

### 7.5.3. DC characteristics /Receive Channel

| Symbol | Parameter | Conditions | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| $V_{LEAD}$ | Receive threshold leading edge | $V_{TVL}$ = 1.0V, /HPEN = $V_{CC}$, EN_VT= low | 0.85 | 1 | 1.15 | V |
| $V_{TRAIL}$ | Receive threshold trailing edge | $V_{TVT}$ = 0.5V, /HPEN = $V_{CC}$, EN_VT= low | 0.35 | 0.5 | 0.65 | V |
| $V_{TVL}$ | Internal high-level threshold configuration | EN_VT= high | 1.8 | 2 | 2.2 | V |
| $V_{TVT}$ | Internal low-level threshold configuration | EN_VT= high | 1.3 | 1.5 | 1.7 | V |
| $I_{THLEAK}$ | TVL, TVT input leakage current | $V_{TVL}$= $V_{TVT}$ = 2.5V | -1 | | +1 | μA |

### 7.5.4. DC characteristics/Digital I/O

**(DIN, DOUT, RST, /PG_P, /PG_N, EN_VT, WT_ENb, HPEN)**

| Symbol | Parameter | Conditions | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input logic-high | | 1.4 | | | V |
| $V_{IL}$ | Input logic-low | | | | 0.4 | V |
| $I_{LEAK}$ | Input leakage current | | -1 | | +1 | μA |
| $V_{OL}$ | Open-drain logic-low | $I_{SINK}$=2mA | | | 0.3 | V |
| $V_{ODL}$ | Open-drain leakage | $V_{OUT}$ = 5V, output not asserted | | | 1 | μA |

### 7.5.5. AC characteristics/Transmit channel

| Symbol | Parameter | Conditions | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| $t_{RLD}$ | Output rise time leading edge | $R_{SRA}$= 62k Ω, $R_{LOAD}$=200Ω, see Figure8- 1 | | 1.4 | | μs |
| $t_{FLD}$ | Output fall time leading edge | $R_{SRA}$= 62kΩ, $R_{LOAD}$=200Ω, see Figure8- 1 | | 1.4 | | μs |
| $t_{RTR}$ | Output rise time trailing edge | $R_{SRA}$= 62kΩ, $R_{LOAD}$=200Ω, see Figure8- 1 | | 1.4 | | μs |
| $t_{FTR}$ | Output fall time trailing edge | $R_{SRA}$= 62kΩ, $R_{LOAD}$=200Ω, see Figure8- 1 | | 1.4 | | μs |
| $t_{TPROP}$ | Transmit propagation delay | $R_{SRA}$= 62kΩ, $R_{LOAD}$=200Ω, see Figure8- 1 | | 1.2 | | μs |
| $t_{SYM}$ | Transmission output symmetry | $R_{SRA}$= 62kΩ, $R_{LOAD}$=200Ω, see Figure8- 1 | -0.4 | 0 | +0.4 | μs |
| $t_{TERM}$ | Termination switching delay | $R_{SRA}$= 62kΩ, $R_{LOAD}$=200Ω, see Figure8- 2 | | 0.5 | | μs |
| $t_{TRMON}$ | Termination on-time (default) | $R_{SRA}$= 62kΩ, $R_{LOAD}$=200Ω, DTA is floating, see Figure8- 2 | 19 | 34 | 63 | μs |
| $t_{TRMON\_min}$ | Minimum value of termination on-time (external adjustment) | $R_{SRA}$= 62kΩ, $R_{LOAD}$=200Ω, connect DTA to GND through an 10kΩ resistor, see Figure8- 2 | 8 | 10 | 12 | μs |
| $t_{TRMON\_max}$ | Maximum value of termination on-time (External adjustment) | $R_{SRA}$= 62kΩ, $R_{LOAD}$=200Ω, connect DTA to GND through a 500k resistor, see Figure8- 2 | 400 | 500 | 600 | μs |

### 7.5.6. AC characteristics/Receive channel

| Symbol | Parameter | Conditions | MIN | TYP | MAX | Units |
|---|---|---|---|---|---|---|
| $t_{RPROP}$ | Receive propagation delay | HPEN = $V_{CC}$, see Figure8- 3 | | | 1 | μs |
| $t_{HP}$ | Receiver high pass filter time constant | HPEN = $V_{CC}$, see Figure8- 3 | | 500 | | μs |

### 7.5.7. Bus polarity detection[1]

| Symbol | Parameter | Conditions | MIN | TYP | MAX | Units |
|---|---|---|---|---|---|---|
| $V_{HIGH}$ | Bus polarity detection: logic high | $V_{HP}$-$V_{HN}$, /PG_P = low | 2.5 | 3 | 3.5 | V |
| $V_{LOW}$ | Bus polarity detection: logic low | $V_{HN}$-$V_{HP}$, /PG_N = low | 2.5 | 3 | 3.5 | V |

**Note:**
1. The CA-IF4289 features bus polarity detection only.

### 7.6. Typical Characteristics and Waveforms

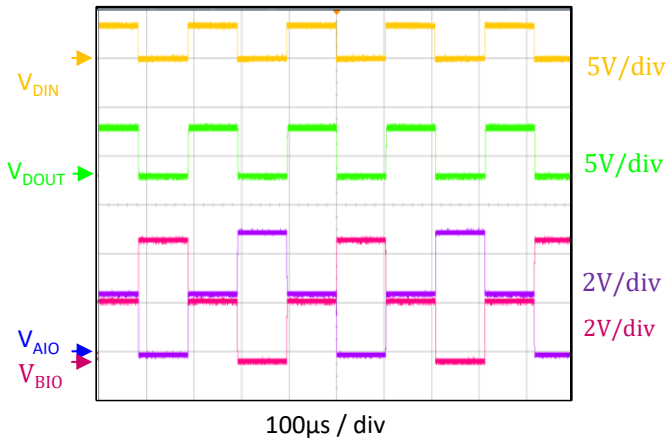



Figure 7-1. $V_{DIN}$=5V， $f_{DIN}$=4.8kHz， $R_{SRA}$=33KΩ

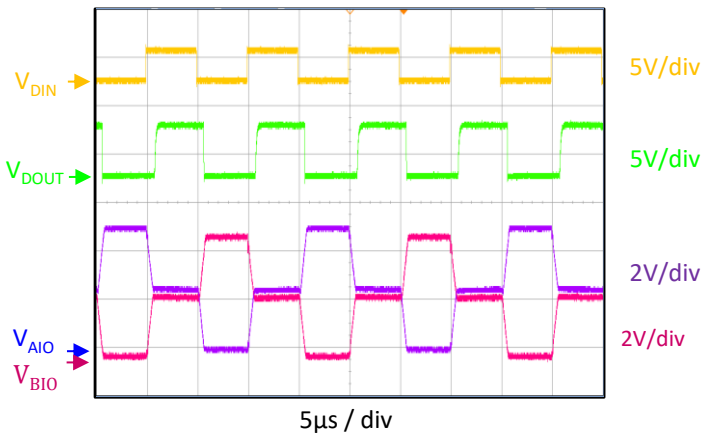



Figure 7-2. $V_{DIN}$=5V， $f_{DIN}$=100kHz， $R_{SRA}$=33kΩ

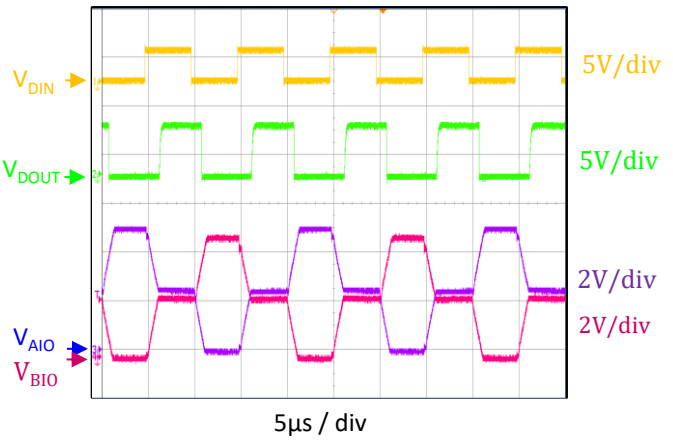



Figure 7-3. $V_{DIN}$=5V， $f_{DIN}$=100kHz， $R_{SRA}$=62kΩ

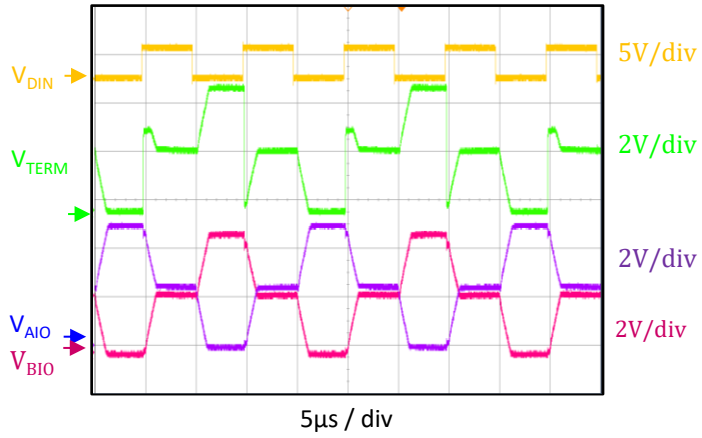



Figure 7-4. $V_{DIN}$=5V， $f_{DIN}$=100kHz， $R_{SRA}$=62kΩ

## 8. Parameter Measurement Information

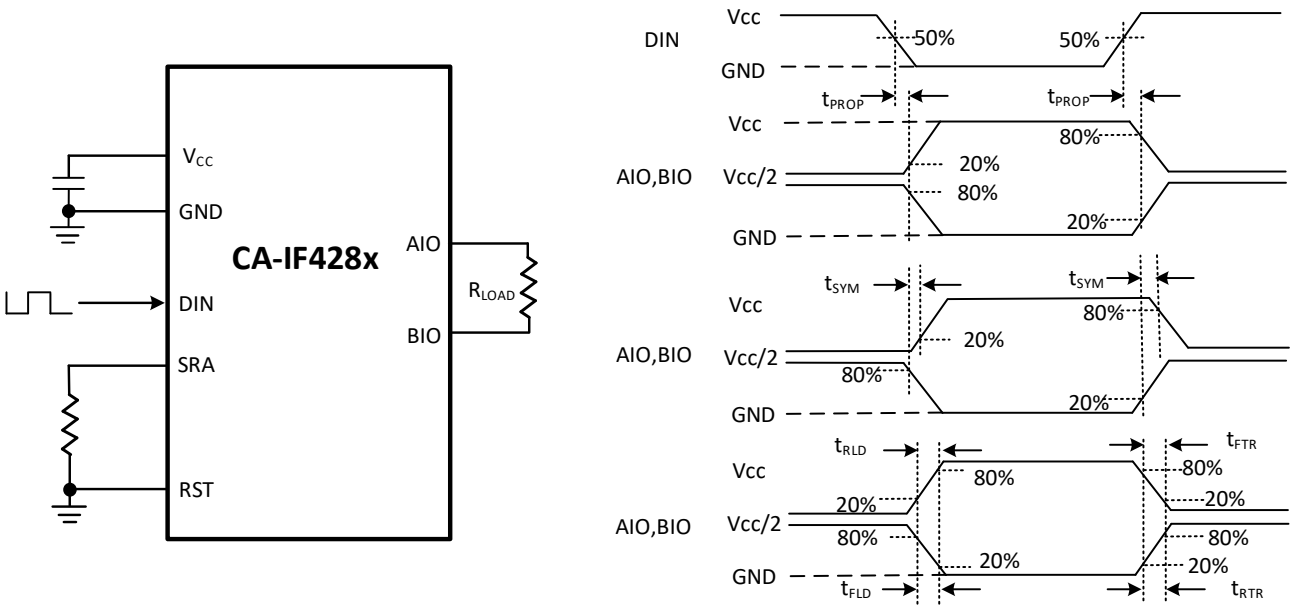



**Figure8- 1. Transmit Channel Timing Diagram**

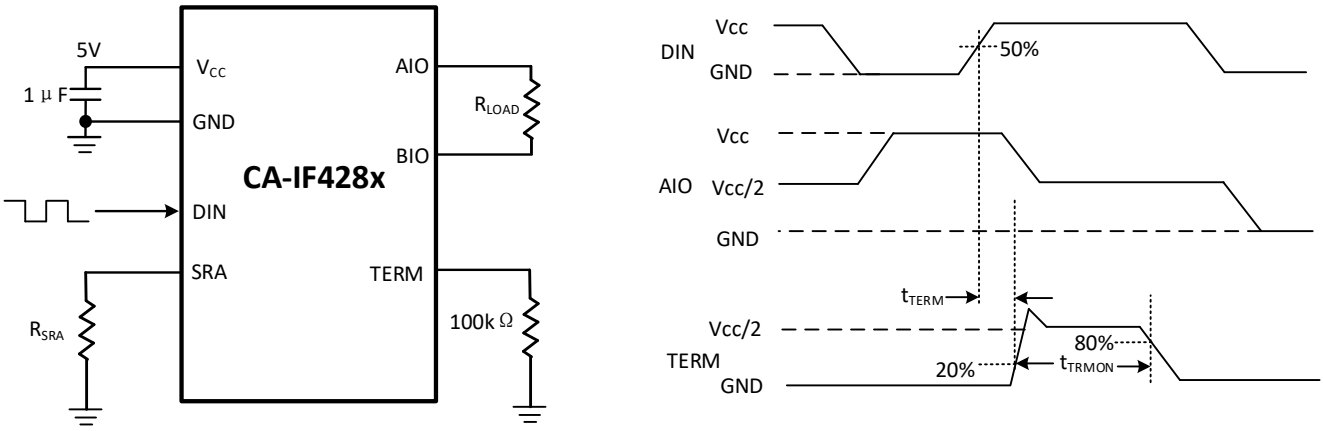



**Figure8- 2. Transmission Switch Delay and Termination On-Time**

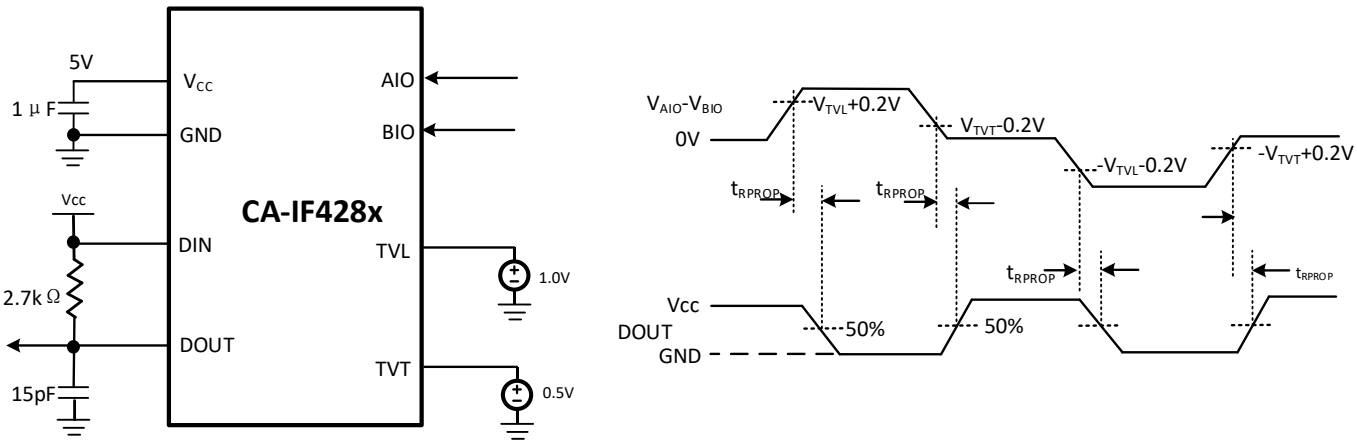



**Figure8- 3. Receive Propagation Delay**

## 9. Detailed Description

The CA-IF428x home bus transceiver complies with the home bus standard, where power and data are carried on a single pair of wires. All devices can operate with data rates up to 200kbps for bus-powered applications and feature dynamic cable termination, programmable receiver hysteresis and thresholds, and transmit driver slew rate adjustment for better signal quality and flexible design. See Figure 9-1 and Figure 9-2 functional block diagram for the CA-IF4288 and the CA-IF4289.

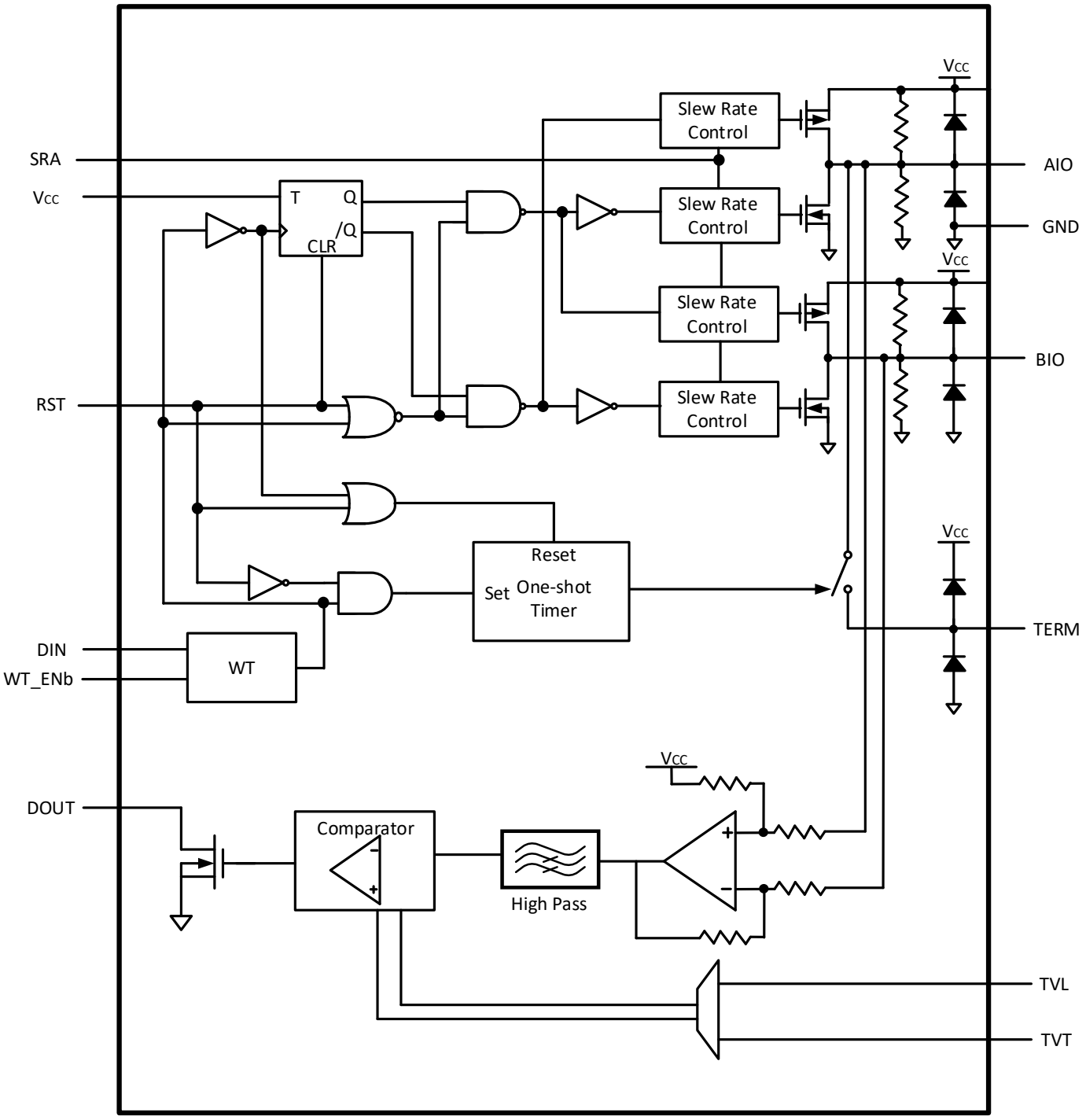



**Figure 9-1. The CA-IF4288 Functional Block Diagram**

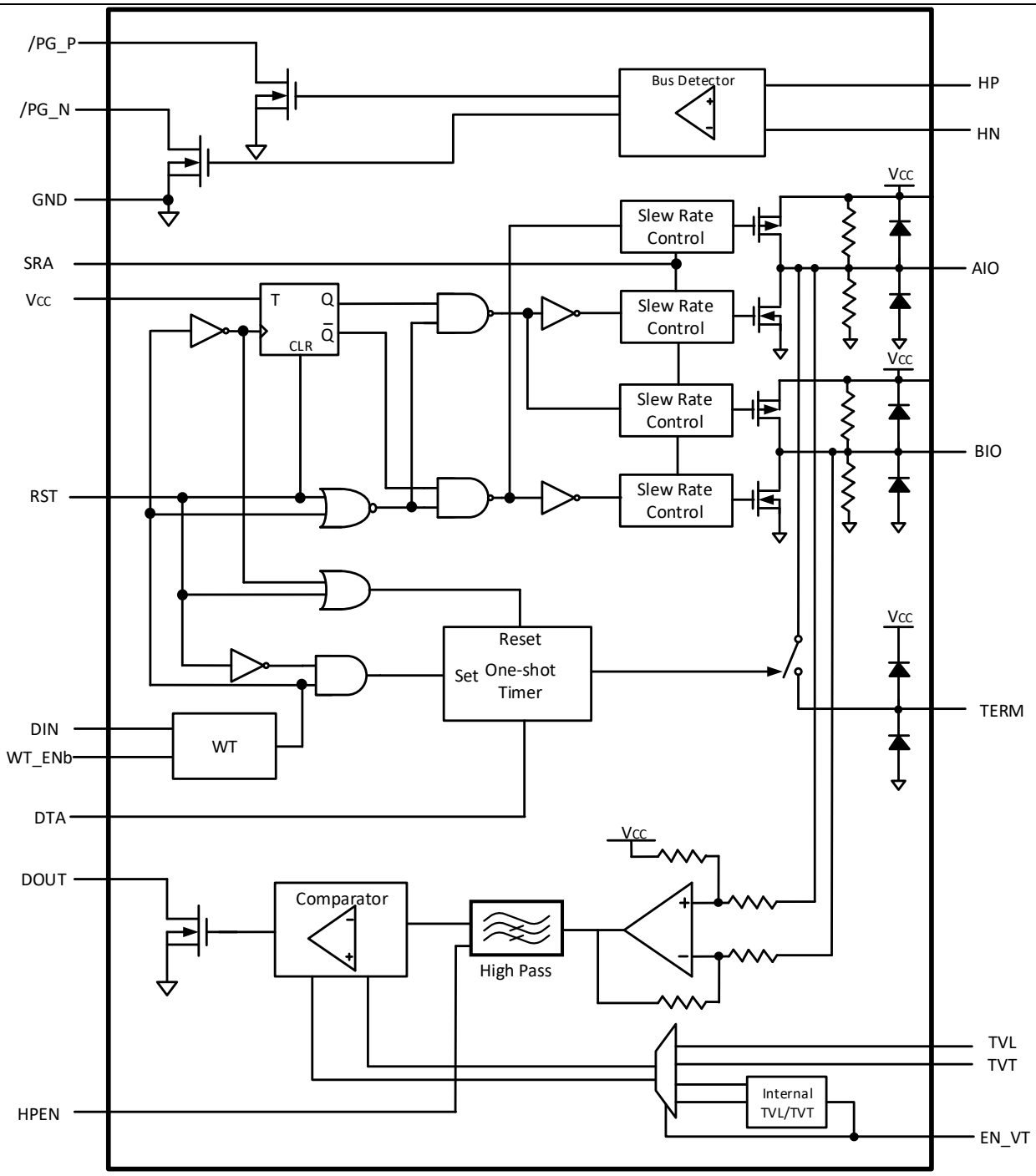



**Figure 9-2. The CA-IF4289 Functional Block Diagram**

### 9.1. Transceiver Operation

On the logic side, the CA-IF428x home bus transceivers have logic data input (DIN) and logic data output (DOUT); The reset control RST is used to enable or disable the bus transmitter: drive RST low to enable data transmission on AIO and BIO; drive RST high to disable the bus transmitter. The CA-IF428x home bus receiver is always active. In the typical applications, DIN, DOUT and RST logic pins are the interface with external micro-controller. Also, these devices feature an internal watchdog timer to avoid the bus being blocked by a long-zero. The timer is enabled by setting the logic input WT_ENb to low. The internal watchdog timer monitors the logic input DIN and if any long-zero input persists for more than the watchdog timeout and blocks the bus, sets the AIO and BIO outputs to high-impedance states. Any transition resets the watchdog timer.

On the bus side, AIO, BIO, and TERM connected to the home bus network. When DIN goes from high to low, the polarities of AIO and BIO invert; When DIN goes from low to high, put AIO and BIO pins to high-impedance. DOUT asserts low when the leading edge of $V_{AIO}$ - $V_{BIO}$ crosses $V_{TVL}$ or -$V_{TVL}$; DOUT is high-impedance when the trailing edge of $V_{AIO}$ - $V_{BIO}$ crosses $V_{TVT}$ or -$V_{TVT}$. See more details from Figure 9-3.

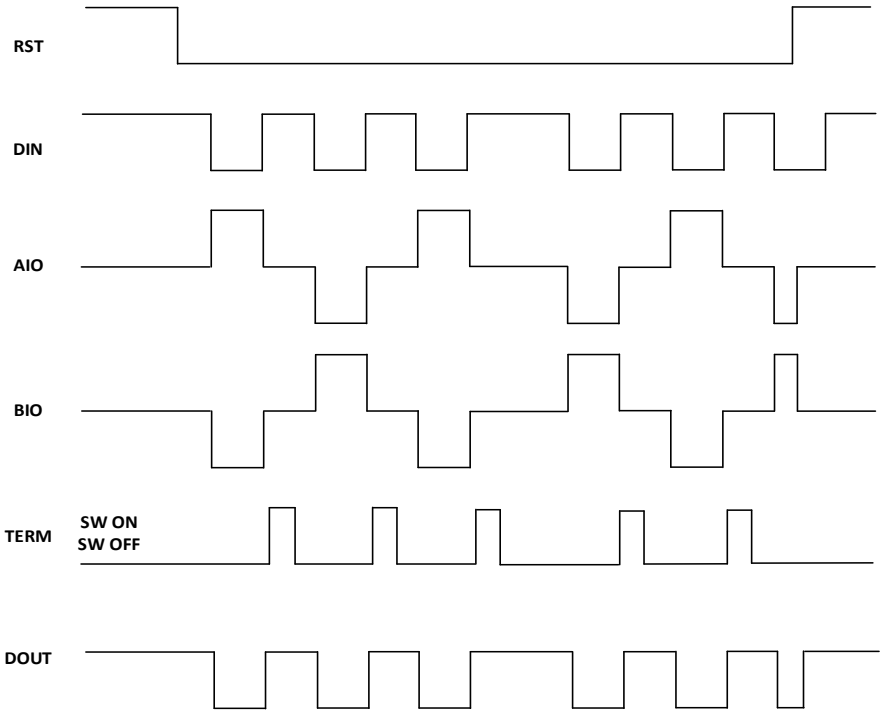



**Figure 9-3. Transceiver Operation**

## 9.2. Transmitter Control and Configuration

### 9.2.1. Dynamic Cable Termination

The CA-IF428x supports home bus signals at data rates up to 200kbps. When operating at high data rates, the mismatch between the home bus cable impedance and cable termination resistor can affect the signal transmission quality negatively. We recommend to connect a 200Ω to 1kΩ cable termination resistor($R_{TRM}$ in the typical application circuit) between AIO and BIO, and connect a resistor (100Ω, typ) between TERM and BIO ($R_{TRMO}$ in the typical application circuit), to absorb reflections on the bus. The CA-IF428x features dynamic cable termination to improve the signal quality for long distance transmission. When the driver transitions to high-impedance, an internal switch connects AIO to TERM and the external termination resistor($R_{TRMO}$) at TERM is connected between AIO and BIO in parallel with the cable termination resistor($R_{TRM}$). When DOUT asserts low, or when RST is driven high, the internal switch opens after 34μs (typ) fixed time for the CA-IF4288; For the CA-IF4289, the internal termination switch opens after 34μs with DTA pin floating, or opens after 10μs to 500μs with 10kΩ to 500kΩ of $R_{DTA}$, the external resistor connected between DTA and GND. Termination on-time calculation is as below equation:

$$t_{DTA} = R_{DTA} / 1k\Omega$$

Where $R_{DTA}$ is in kΩ, $t_{DTA}$ is in μs. When operating at lower data rate, we recommend to select larger $R_{DTA}$, for example, 120kΩ to 200kΩ $R_{DTA}$ at 9.6kbps data rate. Also, select a larger termination resistor between AIO and BIO, $R_{TRM}$ and increase the receiver threshold hysteresis when operating at low-speed transmission to reduce power consumption and improve system reliability. The optimized value of the dynamic termination resistor depends on the application. For typical applications, the value of the dynamic termination resistor is between 50Ω and 240Ω.

#### 9.2.2. Transmit Slew Rate Adjustment

Connect resistor $R_{SRA}$ between SRA and GND to control the slew rate of the transmit signals (AIO and BIO). The transmit rise ($t_{RLD}$, $t_{RTR}$)/fall time ($t_{FLD}$, $t_{FTR}$) is proportional to $R_{SRA}$ and is calculated using the following equation:

$$t_{rise/fall} = 17(pF) \times R_{SRA}(\Omega)$$

For most applications, it is recommended to use $R_{SRA}$ = 33kΩ resulting in 0.56μs (typ) output rise/fall time. Ensure that $R_{SRA}$ is in the range from 20kΩ to 120kΩ.

#### 9.2.3. RST (Reset) Control

The CA-IF428x family devices feature a bus reset control input. Drive RST low to enable the bus transmitter. Drive RST high to disable the bus transmitter. RST also controls the internal switch used for dynamic cable termination. Ensure that RST remains low for at least 34μs (typ) after the internal switch is closed when the driver transitions to high-impedance. The internal switch opens when put RST high.

#### 9.2.4. Data Input Timeout Detection

The CA-IF428x devices feature logic data input timeout detection that prevents erroneous controllers from clamping the bus to a low level by maintaining a continuous low input signal. Connect WT_ENb pin to low to enable timeout detection. In this case, when data input DIN remains in the low for greater than 21ms(typ), the transmitter is disabled that places the driver outputs (AIO/BIO) in a high-impedance state. To disable timeout detection, connect WT_ENb to logic high.

### 9.3. Receiver Control and Configuration

#### 9.3.1. Receiver Threshold Adjustment

The threshold levels of receiving signals are set by the voltages at TVL and TVT. The voltage at TVL sets the threshold for the pulse leading edge of receiving signals from the home bus($V_{AIO}$ - $V_{BIO}$). The voltage at TVT sets the threshold for the pulse trailing edge of receiving signals from home bus. Ensure that $V_{TVL} > V_{TVT}$. DOUT asserts low when $V_{AIO}$ - $V_{BIO}$ crosses $V_{TVL}$ or $-V_{TVL}$. DOUT is high impedance when $V_{AIO}$ - $V_{BIO}$ crosses $V_{TVT}$ or $-V_{TVT}$, see Figure 9-4. Receiver Thresholds. Connect a pull-up resistor between DOUT and the logic supply.

The CA-IF4289 provides internal threshold voltage configuration. Connect EN_VT to logic high, the threshold levels for the receiving signals are set internally, the default threshold voltage is $V_{TVL}$=2V and $V_{TVT}$=1.5V. Connect EN_VT to logic low, the threshold levels are set externally (see the typical application circuit), dependent on the voltage at pin TVL and TVT.

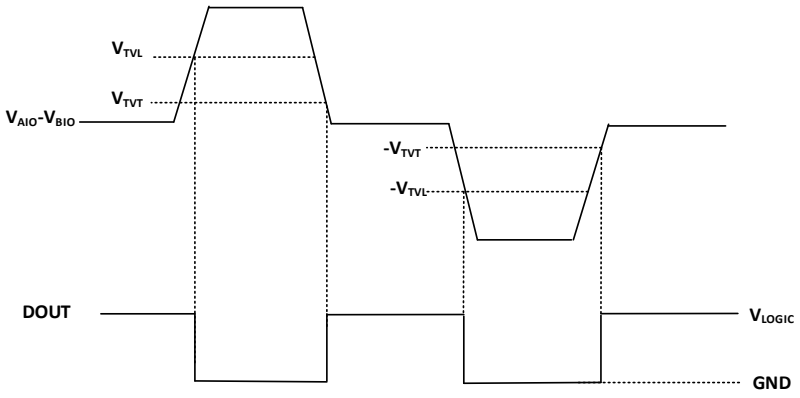



**Figure 9-4. Receiver Thresholds**

#### 9.3.2. High-Pass Filter

The CA-IF428x home bus transceivers have an internal high-pass filter on the receiver input to filter out the low frequency noise at AIO and BIO. The CA-IF4289 features high-pass filter enable control HPEN, connect HPEN to $V_{CC}$ to enable the internal high-pass filter on the receiver input; Connect HPEN to GND to disable the internal high pass filter. In any cases, don't leave the pin HPEN open. The CA-IF4288 doesn't have enable control HPEN, it's internal high-pass filter is always enabled.

### 9.4. Bus Polarity Detection

The CA-IF4289 device offers bus polarity detection that prevents wrong cable connection on the bus. When $V_{HP}$-$V_{HN}$ is greater than 3V (typ), /PG_P asserts to low level, indicates the bus polarity is positive; When $V_{HN}$-$V_{HP}$ is greater than 3V (typ), /PG_N asserts to low level, indicates that the bus polarity is negative. When the bus is not powered, both /PG_P and /PG_N assert to logic high via external pull-up resistors. Connect a 200Ω resistor between home bus and HP/HN pins for surge protection.

## 10. Application and Implementation

In the home bus standard, power and data are carried on a single pair of wires. The CA-IF428x family is powered by +5V system supply voltage at $V_{CC}$. An external AC-blocking inductor is required to superimpose the data on the home bus cable or to separate data from home bus cable, see Figure 10-1 to Figure 10-3 typical application circuits for the CA-IF4289 and the CA-IF4288.

### 10.1. Surge Protection

External components are required to protect the CA-IF428x home bus pins (HP, HN, AIO, BIO and TERM) from high voltage transient events (see Figure 10-1 to Figure 10-3). AIO, BIO and TERM must be protected with external TVS diodes and resistors from surge transients. Connect TVS diodes with a 5.8V maximum voltage rating from AIO to GND and BIO to GND, respectively. Connect a 4.7Ω serial resistor between each TVS diode and AIO/BIO to limit the surge current. Depending on the surge transients polarities, the residual current after the 4.7Ω resistor flows from AIO/BIO through the internal ESD clamping diodes to $V_{CC}$ or GND.

Connect a 200Ω resistor between the bus and HP, HN pins respectively for surge protection. Connect at least 1μF ceramic bypass capacitor as close to $V_{CC}$ pin as possible, and a minimum 10μF bulk capacitor between $V_{CC}$ and GND to limit the voltage overshoot on $V_{CC}$ pin.

### 10.1. PCB Layout Recommendations

Although impedance matching is not required on H+ and H- lines, route them together as much as possible. To reduce the parasitic capacitance on signal lines, do not route H+ and H- lines, or the connected components over the ground planes. To ensure proper protection, connect the ground return of the protection diodes directly to the ground plane. Use a star configuration to connect all grounds together as close to the GND as possible. Place the external protection components, TVS diodes and the diode bridge, as close to the home bus connector as possible.

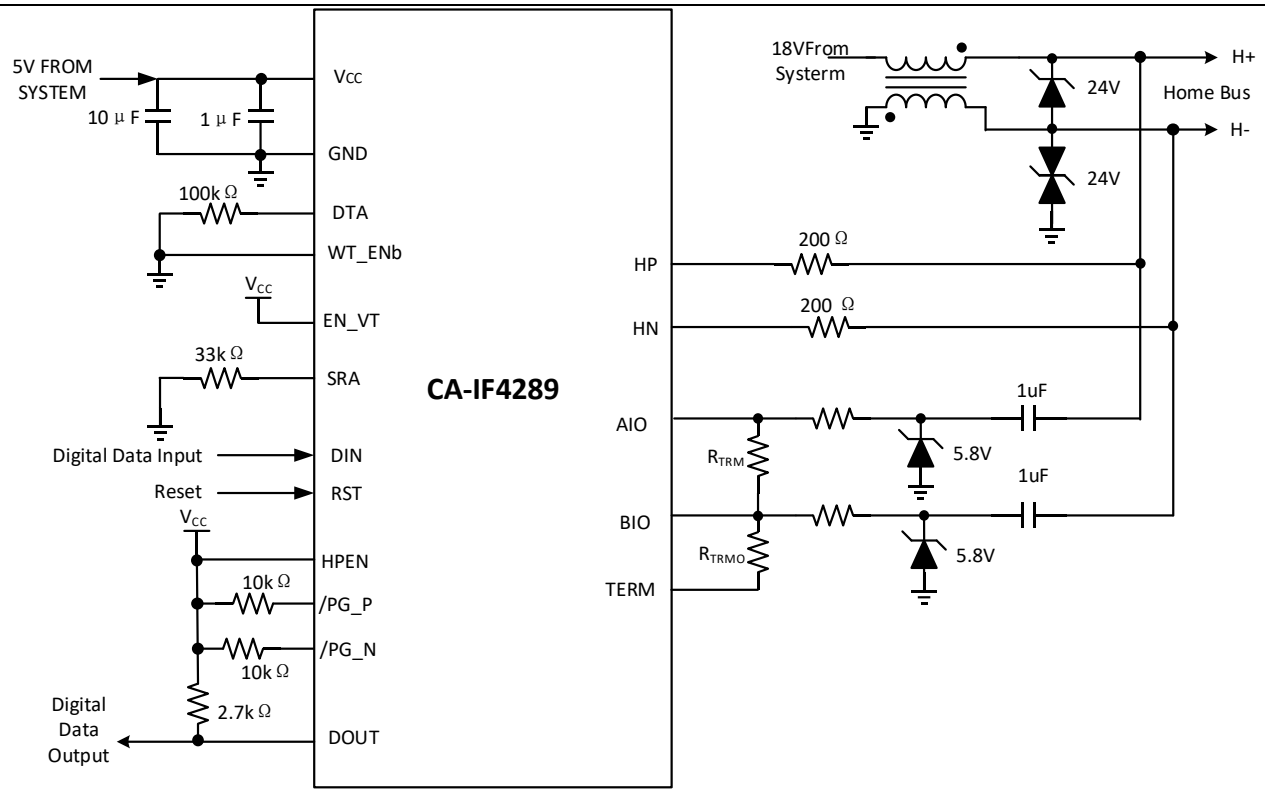



**Figure 10-1. The CA-IF4289 Typical Application Circuit with Internal Threshold Setup (connect EN_VT to $V_{CC}$)**

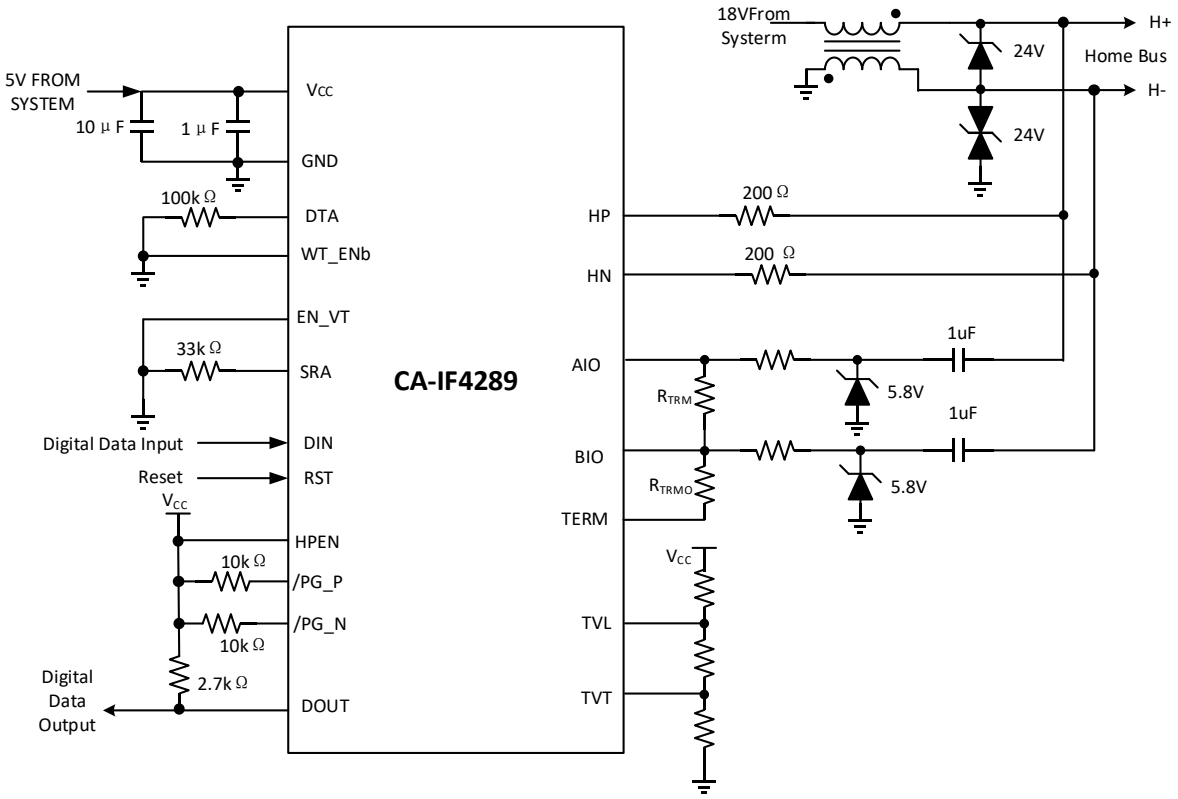



**Figure 10-2. The CA-IF4289Typical Application Circuit with External Threshold Setup(connect EN_VT to GND)**

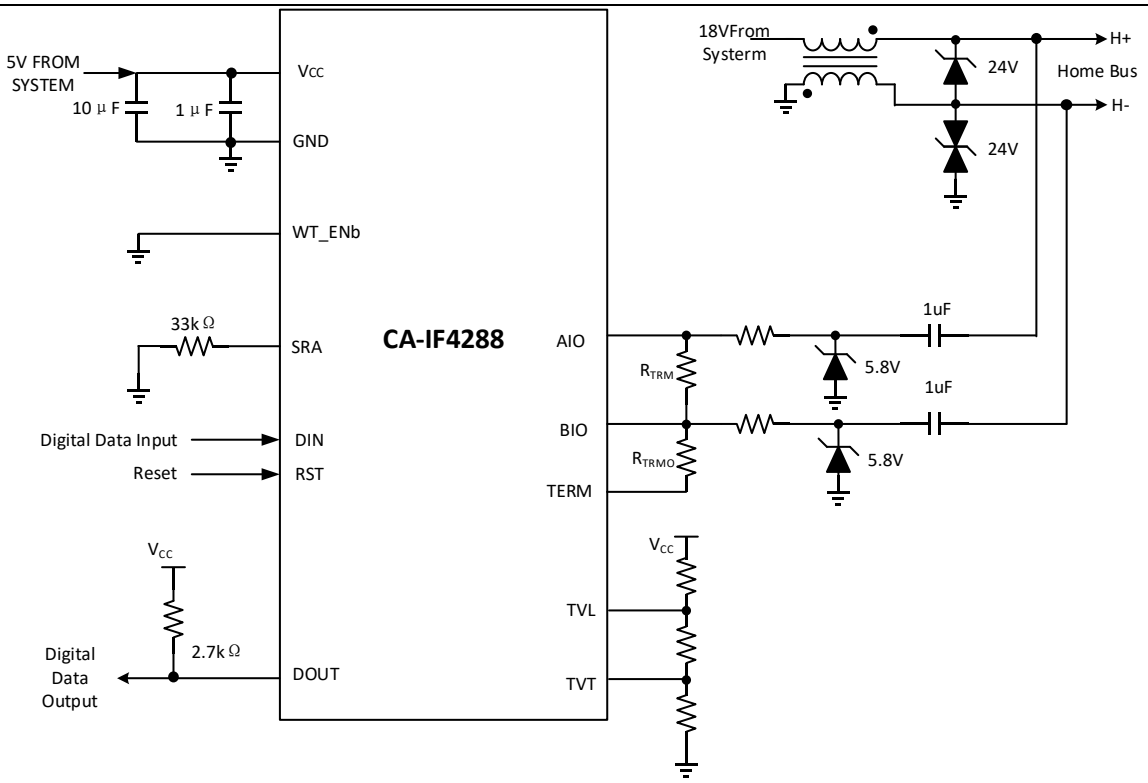
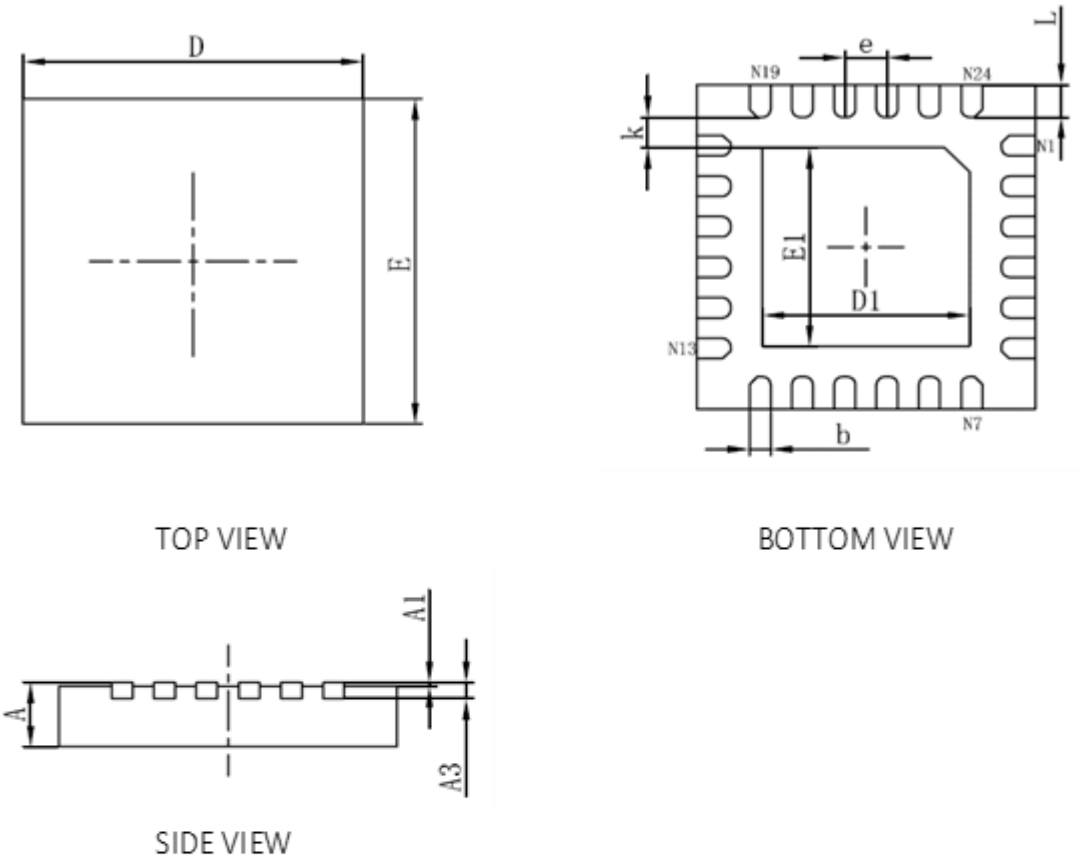



**Figure 10-3. The CA-IF4288 Typical Application Circuit**

## 11. Package Information

**QFN package outline**




| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|---|---|---|---|---|
| | Min. | Max. | Min. | Max. |
| A | 0.700 | 0.800 | 0.028 | 0.031 |
| A1 | 0.000 | 0.050 | 0.000 | 0.002 |
| A3 | 0.203REF. | | 0.008REF. | |
| D | 3.950 | 4.050 | 0.156 | 0.159 |
| E | 3.950 | 4.050 | 0.156 | 0.159 |
| E1 | 2.400 | 2.500 | 0.094 | 0.098 |
| D1 | 2.400 | 2.500 | 0.094 | 0.098 |
| k | 0.200MIN | | 0.008MIN | |
| b | 0.200 | 0.300 | 0.008 | 0.012 |
| e | 0.500TYP. | | 0.020TYP. | |
| L | 0.350 | 0.450 | 0.014 | 0.018 |

Note:

1. All dimensions are in millimeters, angles are in degrees.

**Figure 11-1. QFN packaging Information**

## 12. Soldering Temperature (reflow) Profile

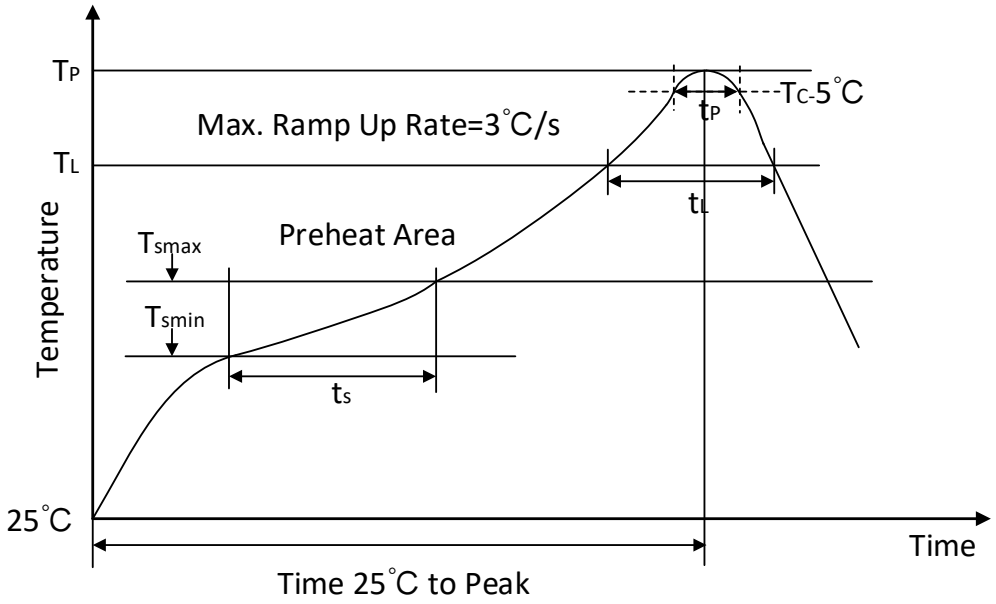


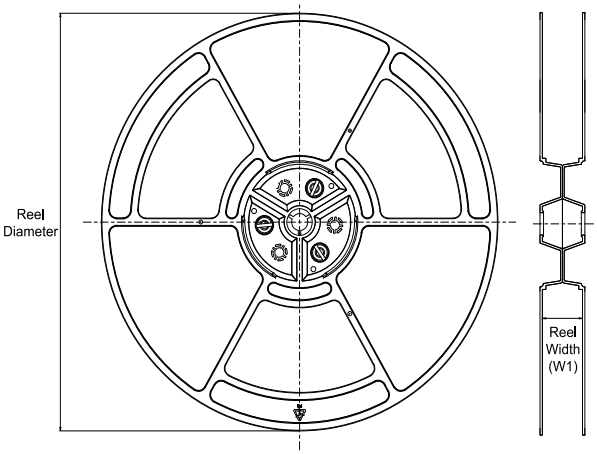

**Figure 12-1. Soldering Temperature (reflow) Profile**

**Table 12-1. Soldering Temperature Parameter**

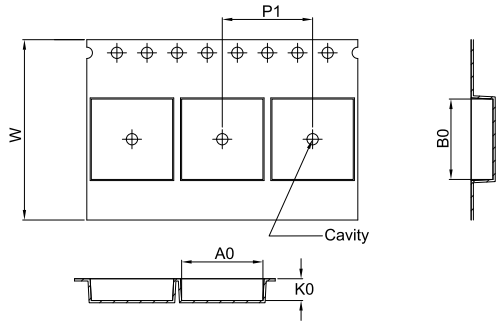
| **Profile Feature** | **Pb-Free Assembly** |
|---|---|
| Average ramp-up rate(217 ℃ to Peak) | 3℃/second max |
| Time of Preheat temp(from 150 ℃ to 200 ℃ | 60-120 second |
| Time to be maintained above 217 ℃ | 60-150 second |
| Peak temperature | 260 +5/-0 ℃ |
| Time within 5 ℃of actual peak temp | 30 second |
| Ramp-down rate | 6 ℃/second max. |
| Time from 25℃ to peak temp | 8 minutes max |

## 13. Tape and Reel Information

### REEL DIMENSIONS

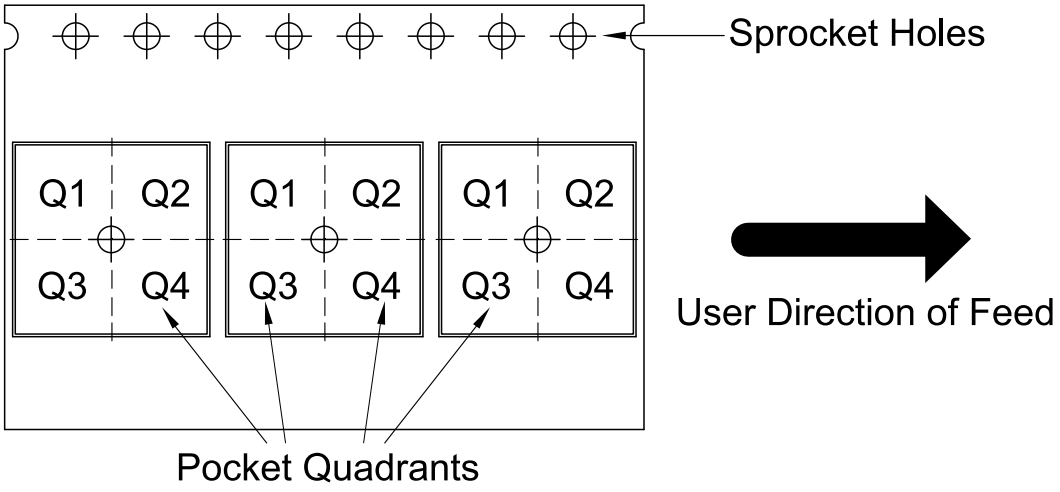



### TAPE DIMENSIONS




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **CA-IF4288** | QFN | F | 24 | 3000 | 330 | 12.4 | 4.3 | 4.3 | 1.1 | 8.0 | 12.0 | Q1 |
| **CA-IF4289** | QFN | F | 24 | 3000 | 330 | 12.4 | 4.3 | 4.3 | 1.1 | 8.0 | 12.0 | Q1 |

## 14. IMPORTANT NOTICE

The above information is for reference only and is used to assist Chipanalog customers in design and development. Chipanalog reserves the right to change the above information due to technological innovation without prior notice.

Chipanalog products are all factory tested. The customers shall be responsible for self-assessment and determine whether it is applicable for their specific application. Chipanalog's authorization to use the resources is limited to the development of related applications that the Chipanalog products involved in. In addition, the resources shall not be copied or displayed. And Chipanalog shall not be liable for any claim, cost, and loss arising from the use of the resources.

**Trademark Information**

Chipanalog Inc. ®, Chipanalog® are trademarks or registered trademarks of Chipanalog.

**http://www.chipanalog.com**