

# How to Isolate the I<sup>2</sup>C Interface Signal

### 1 Introduction

Inter-integrated circuit (I<sup>2</sup>C) bus communication is a short distance communication two-line half-duplex communication solution, which has been widely used in various applications because of its simplicity. The I<sup>2</sup>C bus is used to communicate between two modules, and isolation may be needed if there is a high voltage in the system. Isolation can be used to protect circuits and operators, as well as to isolate noise that may interfere with signal communication.

Since digital isolators are one-way communication, implementing bi-directional communication over the I<sup>2</sup>C bus presents many challenges for designers. This article will discuss different approaches to use the isolated I<sup>2</sup>C bus.

#### 2 Signal Isolation

Signal isolation of the I<sup>2</sup>C bus can be achieved in two ways. The first uses a digital isolator with an external circuit to separate the two-way data path into two one-way channels. The bi-directional data is separated into two uni-directional signals, and the digital isolator will modulate the input signals of each channel and pass the signals through the isolation gate before demodulation at output time. The design method of separating bi-directional I<sup>2</sup>C signals into uni-directional signals to interface with digital isolators is explained in detail.

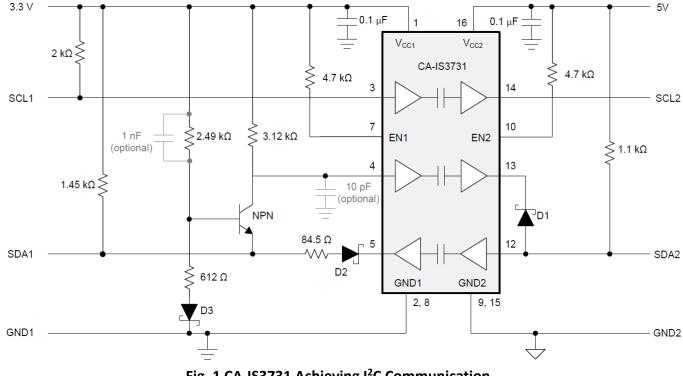


Fig. 1 CA-IS3731 Achieving I<sup>2</sup>C Communication

Fig. 1 shows an implementation of this approach in an application using bi-directional data and a uni-directional clock using a three-channel digital isolator, such as the CA-IS3731 device. Four-channel digital isolator (such as the CA-IS3742 device) can also be used for multi-host systems that require bi-directional data and clock signals.

The second is to use integrated solution such as the CA-IS302X series. This series of integrated circuit solutions use



#### Shanghai Chipanalog Microelectronics Co., Ltd.

## Rev1.0,Mar,2021

**AN003** 

internal circuit in combination with digital isolators to achieve equivalent device I<sup>2</sup>C buffering functions. The CA-IS3020 device is designed for systems with bi-directional data and clock signals, and the CA-IS3021 is designed for systems with bi-directional data and clock signals.

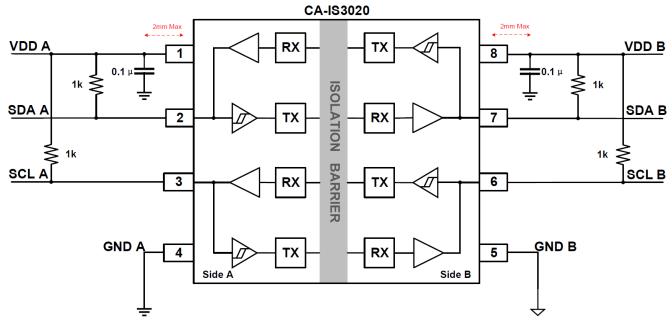


Fig. 2 CA-IS3020 Achieving I<sup>2</sup>C Communication

Fig. 2 shows how the bi-directional serial data (SDA) and serial clock (SCL) signals of the I<sup>2</sup>C bus of CA-IS3020 are internally separated into two uni-directional signals isolated by digital isolator channels. The CA-IS302x series I<sup>2</sup>C interface isolator internally divides the bi-directional SCL/SDA data into two uni-directional digital signal transmission channels. The output drives of each digital channel are I<sup>2</sup>C compatible open leakage outputs. The A side of the CA-IS302x chip is connected to the low-capacitance node on the I<sup>2</sup>C bus, supporting a maximum of 400pF load capacitance; side B connects to a high-capacitance node on the I<sup>2</sup>C bus, supporting a maximum of 400pF load capacitance. There is an I<sup>2</sup>C bus deadlock prevention circuit in the chip, which raises the low level of SCL/SDA output to about 700mV on side A of the chip. At the same time, the logic input on side A of the chip is judged by the internal hysterectomy comparator to determine whether the low level of 700mV that is driven by side A, so as to determine the signal transmission direction on the SCL/SDA line at this time.

Each solution for isolating signals in I<sup>2</sup>C system has pros and cons. Discrete solutions using digital isolators offer greater freedom in partial selection. Bothe CA-IS3731 and CA-IS3742 offer a variety of packages with different isolation grades to suit specific use conditions; however, the disadvantage of this solution is that it needs more board space and has more external circuits. The CA-IS302X integrated solution needs less board space, is designed more efficiently, and has a shorter product commissioning cycle.



## 上海川土微电子有限公司

## CA-IS3740, CA-IS3741, CA-IS3742 修订版 F

## **3** Version Information

Version	Date	State Description
Ver1.0	July.2021	Initial version

### 4 Important Statement

The above information is for reference only and used for helping Chipanalog customers with design, research and development. Chipanalog reserves the rights to change the above information due to technological innovation without advance notice.

