PCB Wiring Design Reference for Isolated Power Supply

PCB, short for Printed Circuit Board, can realize simple circuit connection and function of electronic components. For Chipanalog's isolated power supply series products, in PCB wiring design, besides following the basic rules of PCB wiring, there are other matters to pay attention to.

This document applies to isolating switching power supply, isolating RS485/422 with isolating switching power supply and isolating CAN. Chipanalog's material numbers are as follows:

Material No.	Function Description	Package
CA-IS3105W	0.65W isolated power supply	SOIC16(W)
CA-IS3090W	0.5Mbps isolated RS422 interface with integrated isolated power supply	SOIC16(W)
CA-IS3096W	10Mbps isolated RS422 interface with integrated isolated power supply	SOIC16(W)
CA-IS3092W	0.5Mbps isolated RS485 interface with integrated isolated power supply	SOIC16(W)
CA-IS3098W	10Mbps isolated RS485 interface with integrated isolated power supply	SOIC16(W)
CA-IS3090T	0.5Mbps isolated RS422 interface with integrated isolated power supply	SOIC20(T)
CA-IS3096T	10Mbps isolated RS422 interface with integrated isolated power supply	SOIC20(T)
CA-IS3062W	1Mbps isolated CAN interface with integrated isolated power supply	SOIC16(W)

PCB Design of the Pri-sec V_{CC} Ground Capacitance

When the isolated power supply is working, the V_{CC} and ground of the chip have a relatively large peak current. To provide this current continuously, the usual practice is to place a capacitor at the input of the power supply, a capacitor of about 10μF to filter low-frequency noise, and a capacitor of 0.001-0.1μF to filter high-frequency AC interference superimposed on the power line. However, the larger the capacitance used is not the better, because the actual capacitance is not ideal. The actual capacitor is equivalent to the resistance and inductance connected in series on the capacitor, due to the existence of parasitic parameters.

High frequency capacitors placed next to the pins of the isolated power supply chip serve two purposes:

1. Energy storage, replenish the peak current of the chip when in high-speed work to prevent input voltage down.
2. Decouple, filter out the high-frequency interference transmitted along the power line.

The position of the decoupling capacitor is very important. If the position is not reasonable, the decoupling effect will be lost. The position principle is: located close to the power supply pins, and with the minimum area enclosed by the power supply wire and ground wire of the capacitor. When the several capacitors are connected in parallel, the decoupling radius of the small-capacity capacitor is smaller, and should be as close to the chip pins as possible. The energy storage capacitor and coupling capacitor of input side V_{CC} and output side V_{ISO} should be placed as close to the chip pins as possible to reduce the loop area and the parasitic inductance of PCB wiring. The distance between the capacitor closest to the chip and the chip pin should be within 2mm. See Fig. 1 and Fig. 2.

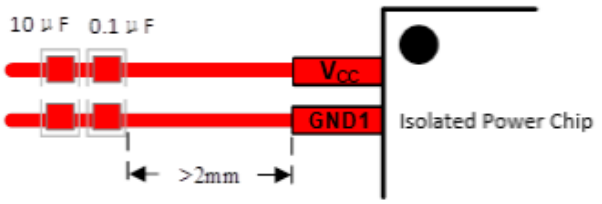

Fig. 1 Not Recommended

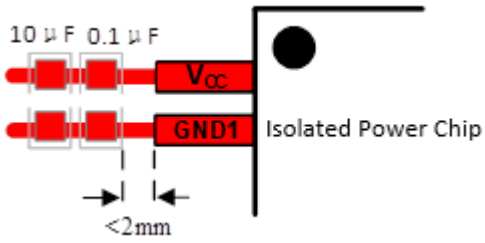

Fig. 2 Recommended

To reduce the impact of the parasitic inductance through the holes, place the holes on the power wire and ground wire outside the capacitor pins of the chip rather than between the capacitor and the chip, as shown in Fig. 3 and Fig. 4. If the PCB space allows, more holes can be placed, and the parasitic inductance of the holes is equivalent to parallel connection, to further reduce the impact of the parasitic inductance of the holes.

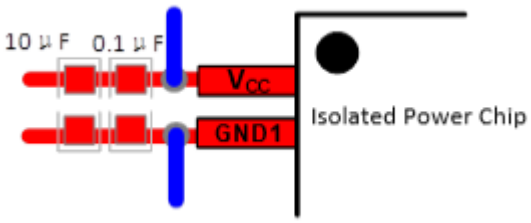

Fig. 3 Not Recommended

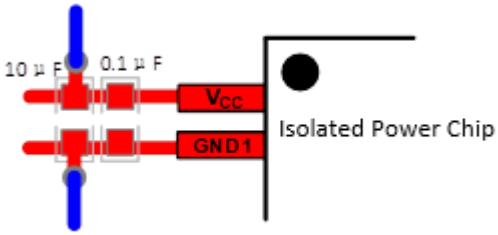

Fig. 4 Recommended

The following uses the CA-IS3062W device as an example to describe the capacitor placement position and PCB wiring next to the pin of the isolated switch power supply.

The CA-IS3062W device is a CAN transceiver with integrated isolated power supply, and its pins are shown in Fig. 5.

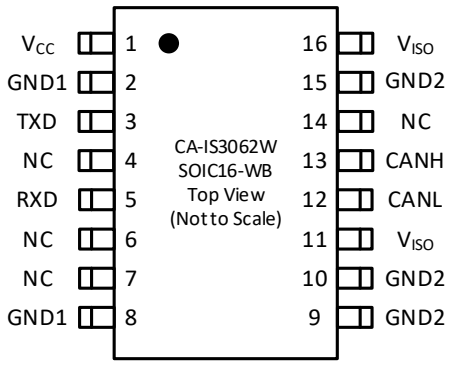

Fig. 5 The Pin Figure of CA-IS3062W

Among them, 11th pin V_{ISO} and 16th pin V_{ISO} are isolated power output, and these two pins need to be connected together in application. As the distance between 15th pin and 16th pin is the shortest when sealing and welding wires of the isolated power module inside the chip, it is recommended to place the capacitor between V_{ISO} and GND2 as close to 15th pin

GND2 and 16th pin V_{ISO} as possible, as shown in Fig. 7. Placement near 10th pin or 11th pin is not recommended, as shown in Fig. 6.

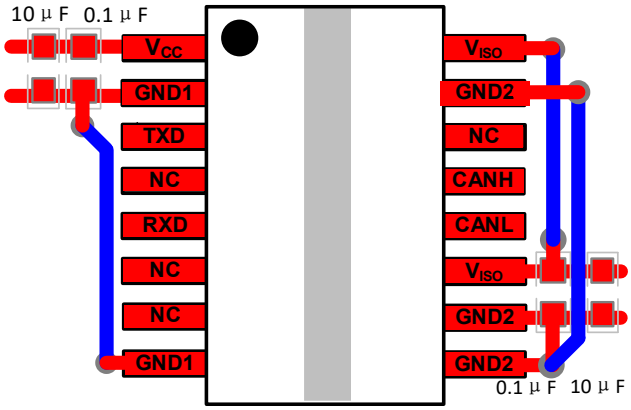

Fig. 6 Not Recommended

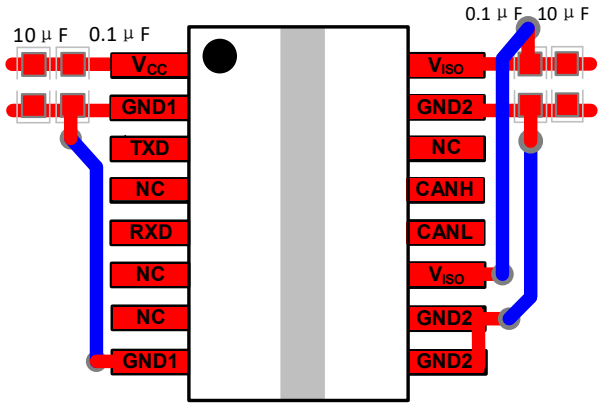

Fig. 7 Recommended

Improve EMI Radiation Interference

A capacitor is formed when the two signal layers of the PCB overlap with each other. This splicing capacitor, distributed inductance is very low, high frequency characteristics are better, can cover a wide frequency. This splicing capacitor can be used to improve EMI radiation interference. The following is a wiring method of 4-layer PCB. V_{CC} and V_{ISO} copper foil are added to the middle two layers of 4-layer PCB to increase its parasitic capacitance to GND1. GND1, GND2 overlapping capacitor improves RMI effect obviously, and pay attention to the PCB layer distance between GND1 and GND2, generally should be greater than 0.4mm.

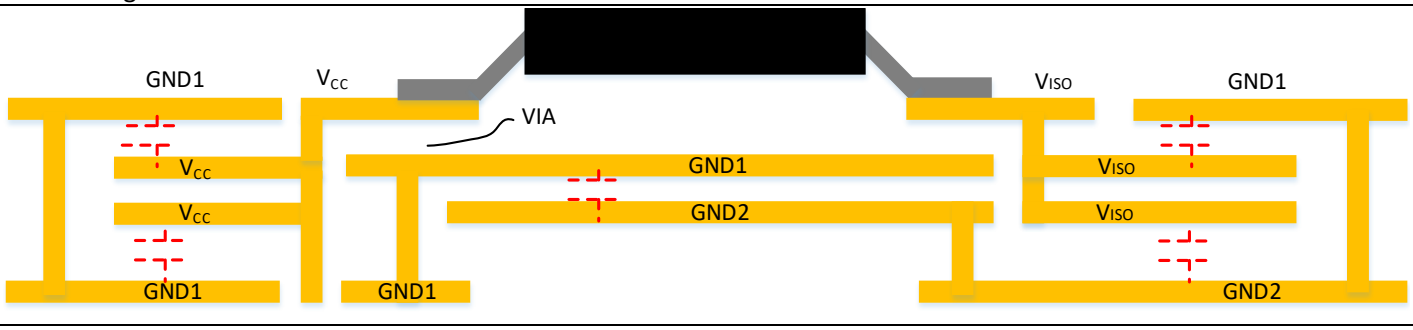

Fig. 8

The creepage distance of the copper foil between the primary ground GND1 and the secondary ground GND2 should not be lower than the distance between the primary and secondary chips, and is recommended to be greater than 8mm.

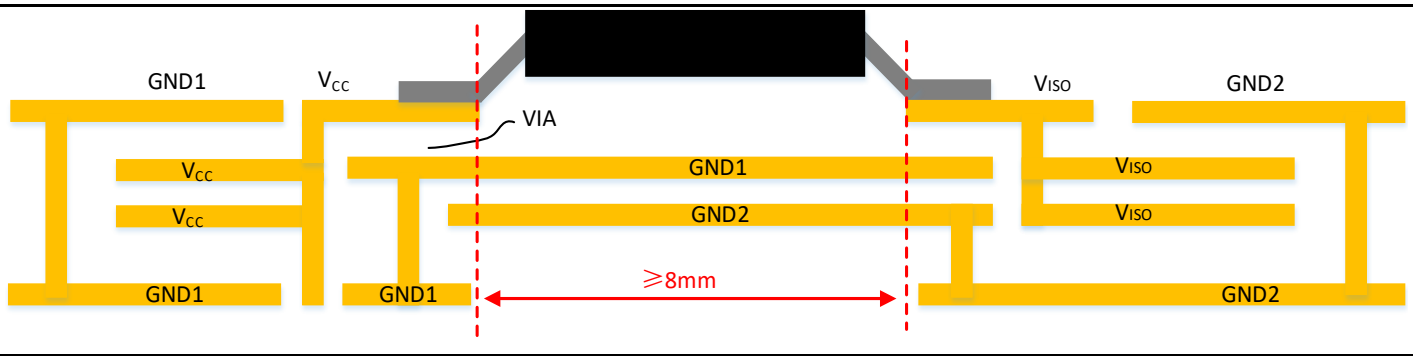

Fig. 9

The shield wall is built by the holes, and the edge protection is constructed for the inner power layer.

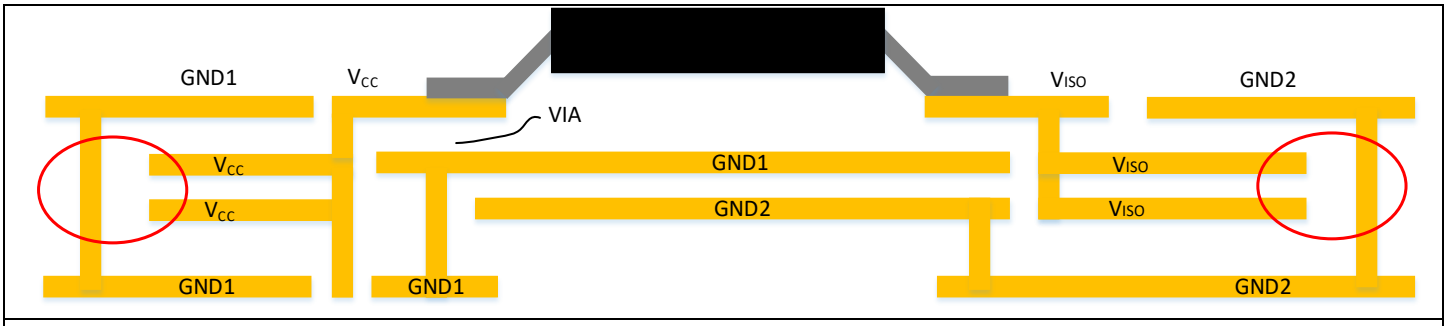

Fig. 10

For more detailed methods of EMI characteristic optimization of the isolated power supply, please log in to the official website of Chipanalog, and check *the Radiation Suppression Design Reference of the Isolated Power Supply* in "Technology and Support – Technical Documentation".

Revision History

Version	Date	State Description
Ver1.0	Jan.2021	Initial version

Important Statement

The above information is for reference only and used for helping Chipanalog customers with design, research and development. Chipanalog reserves the rights to change the above information due to technological innovation without advance notice.

http://www.chipanalog.com