Application of Isolated Current Detection Amplifier in PFC Boost System

1 Introduction

PFC, short for Power Factor Correction, is defined as the ratio of effective power to total power consumption (apparent power). When used in medium and large power switching power supply, improving the power factor can reduce the loss in power grid transmission and improve the transmission efficiency of electric energy. Therefore, it is of great significance to improve the power factor.

This article introduces the PFC application of the CA-IS120x and CA-IS130x series products of Chipanalog, and puts forward the application method and control suggestions for practical application.

2 Definition of Power Factor

Power factor is defined as the ratio of AC circuit active power P(W) to apparent power S(V*A). When the AC voltage and current phase are different, the power factor is less than 1. Under certain voltage and power, the higher the value, the better the benefit, and the more fully the power generation equipment can be used. Power factor is usually expressed as $\cos\theta$, and $\cos\theta = \frac{P}{S}$.

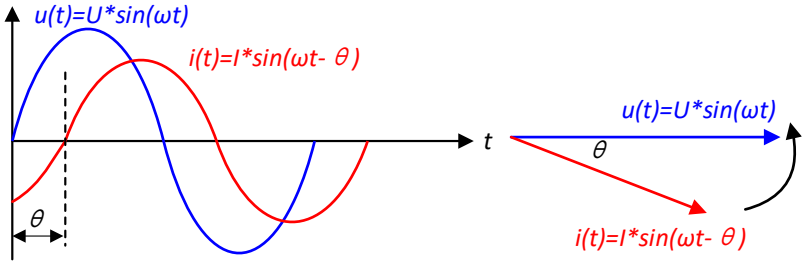

Fig. 1 Definition of Power Factor

For the boost circuit without PFC, it is mainly composed of rectifier bridge circuit, boost power and control circuit, as shown in Fig. 2. The rectifying circuit converts the mains power (220V/50Hz) into direct current. After rectifying, there is a peak current due to the large capacitor (C_{BULK}) in the boost circuit input. In addition, at this time, the input mains side produces distortion current i_{oc}, which contains fundamental wave component and harmonic component. In this circuit, the boost circuit only controls the output voltage V_{OUT} and has no regulation on the input current. The waveform is shown in Fig. 3.

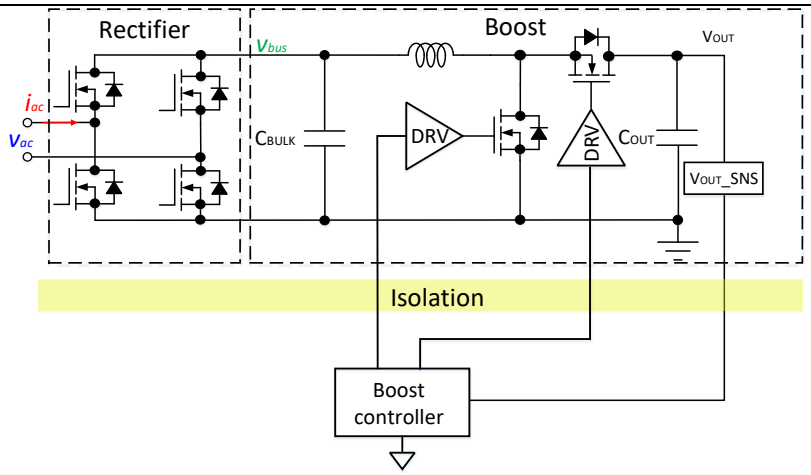

Fig. 2 Rectifier Bridge + Boost Circuit

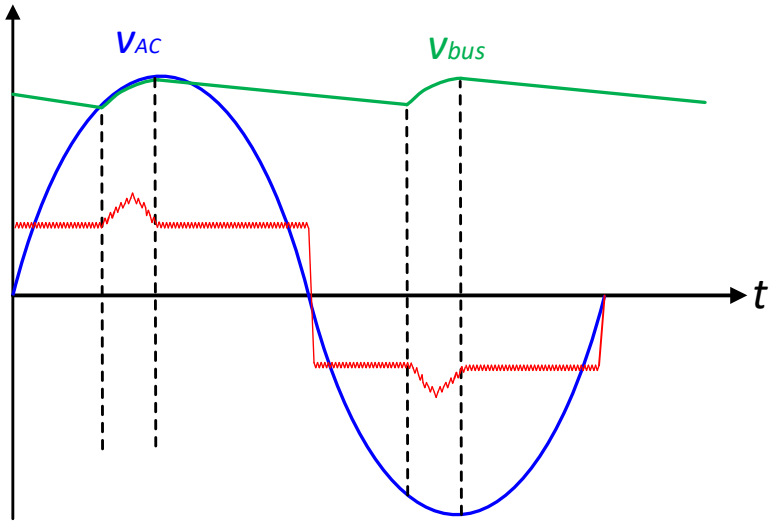

Fig. 3 Rectifier Bridge + Boost Circuit Typical Waveform

The PFC circuit also adds the input side current into the control loop to adjust the current waveform and phase, so as to realize the control of improving power factor.

See Fig. 4. Compare the detected output voltage and reference output voltage, magnify the output error through PI or PID, and multiply the amplified signal by the input bus voltage Vbus, thus the reference envelope of the current at DC bus side is obtained. Finally, the bus current can track the bus voltage under the condition that the output voltage can reach the index value through the controller. The controller has a variety of control methods and structures, and will be described in later section.

Note: Ignoring the voltage conversion problem caused by low input bus voltage at the DC side, there is a valley-fill circuit.

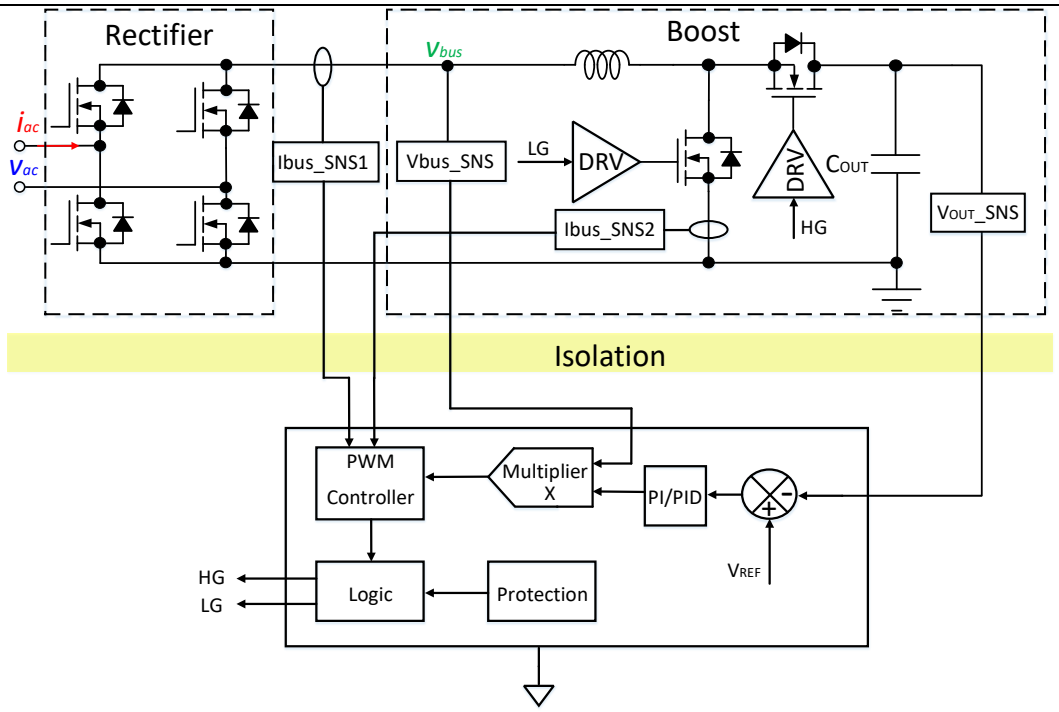

Fig. 4 Rectifier Bridge + PFC Boost Circuit

3 High-side Current Sampling

Current sampling is generally divided into high-side sampling and low-side sampling. High-side sampling has a relatively high common mode voltage to the ground, which can use the Chipanalog's products.

The CA-IS3105W device is used as the isolation power supply. R_SNS is a high-side sampling resistor. When the current flows through the resistor, the voltage drop will be generated on the resistor, and the current amplifier is used.

The CA-IS1200/CA-IS1300 device transmits the voltage drop to the low voltage side, which is converted into digital signals by ADC and sent to DSP or MCU. The CA-IS1204, CA-IS1305/06 devices can also be used to transmit differential voltage signals to the low side and read the digital signals from the low side directly through MCU.

High-side sampling is shown in Fig. 5 and Fig. 6.

The high-side current sampling mode has the following characteristics:

1. The power supply is complicated and must use isolation power supply.
2. The output ground of the isolation power supply is connected to the low voltage end of the sampling side, and cannot be connected to the power level GND.
3. When using isolation power supply, LDO or filter should be used on the input and output sides to prevent voltage ripple on the input and output sides from interfering with other signals.
4. When in normal work, the voltage withstand of the high-side power supply isolation grid is the bus voltage, so it is a test for the voltage withstand of the isolator, and ultimately affect the working life of the chip.
5. For the boost circuit, high-side sampling can monitor and control the current in the full switching cycle of the inductor. The control modes of PFC boost circuit are flexible.

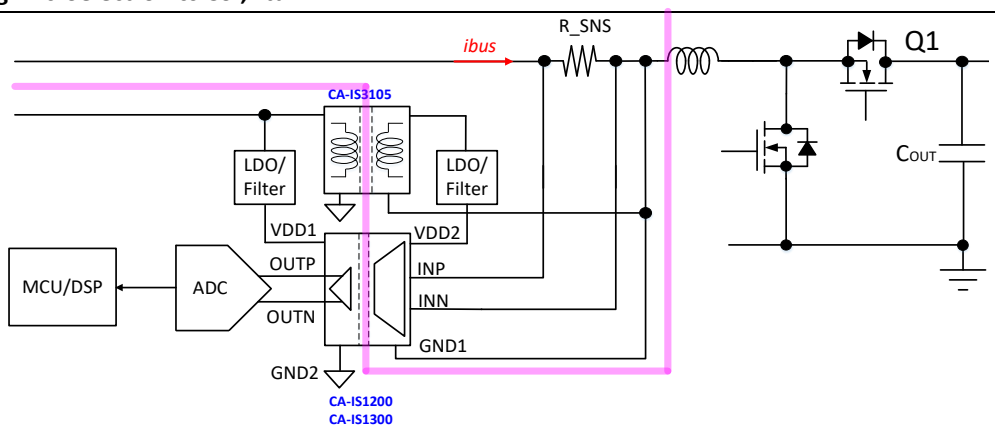

Fig. 5 Schematic Diagram 1 of High-side Current Sampling

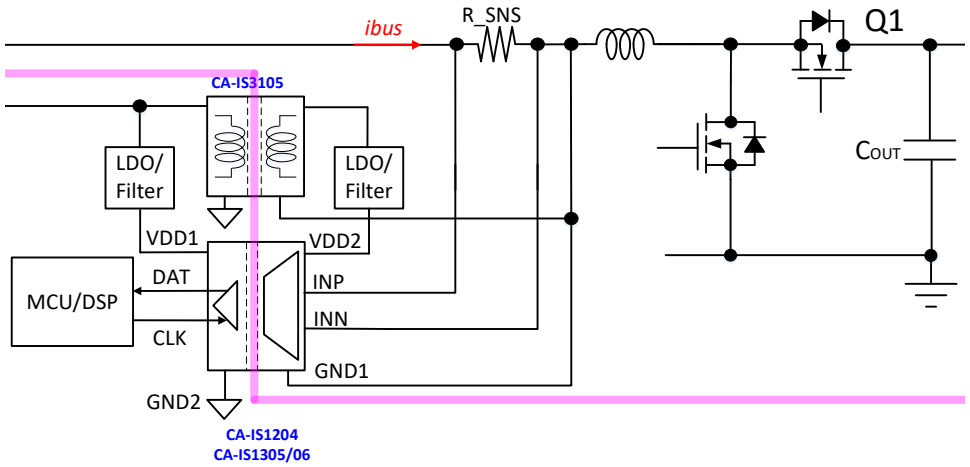

Fig. 6 Schematic Diagram 2 of High-side Current Sampling

3.1 Control Method of High-side Sampling PFC Boost Circuit

3.1.1 Fixed Frequency Peak Current Control

Inductance peak current, fixed frequency control, as is shown in Fig. 7. The output voltage and reference voltage are compared and amplified by PI/PID, and the bus current instruction value is obtained by multiplying the input DC bus voltage. The control logic is generated by comparator U2 and trigger U1. If the switch tube Q2 is on and Q1 is off, the inductance current i_{bus} increases. K_i_{bus} indicates the enlarged conversion value of i_{bus}. When the current K_i_{bus} reaches the instruction peak V_{COMP}, the comparator U2 outputs the high level and resets the trigger U1. At this time, the switch tube Q2 is off and Q1 is on, the inductance current discharges until the trigger is set high due to the fixed frequency pulse.

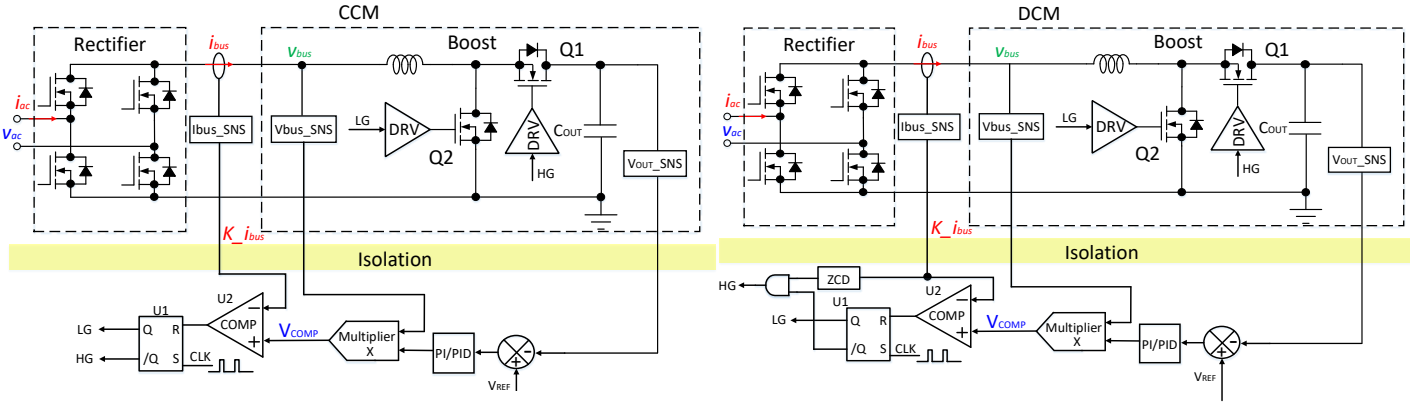

Fig. 7 Fixed Frequency Peak Current Control PFC Boost Circuit

As shown in Fig. 8, for boost circuit working in the continuous current mode (CCM), when the inductance current reaches the command current, the inductance current stops charging and starts discharging, and the envelope formed by the inductive current is sinusoidal. The mean value of the envelope approximates the sinusoidal waveform. For boost voltage working in the discontinuous current mode (DCM), when the inductance current reaches the command current, the inductance current stops charging and starts discharging. When the current drops to zero, the current zero crossing detection logic is triggered. The switch tube Q1 is off and remains until the clock signal triggers the switch tube on and off in the next switching cycle. When working in the peak current control mode, the switch frequency remains constant.

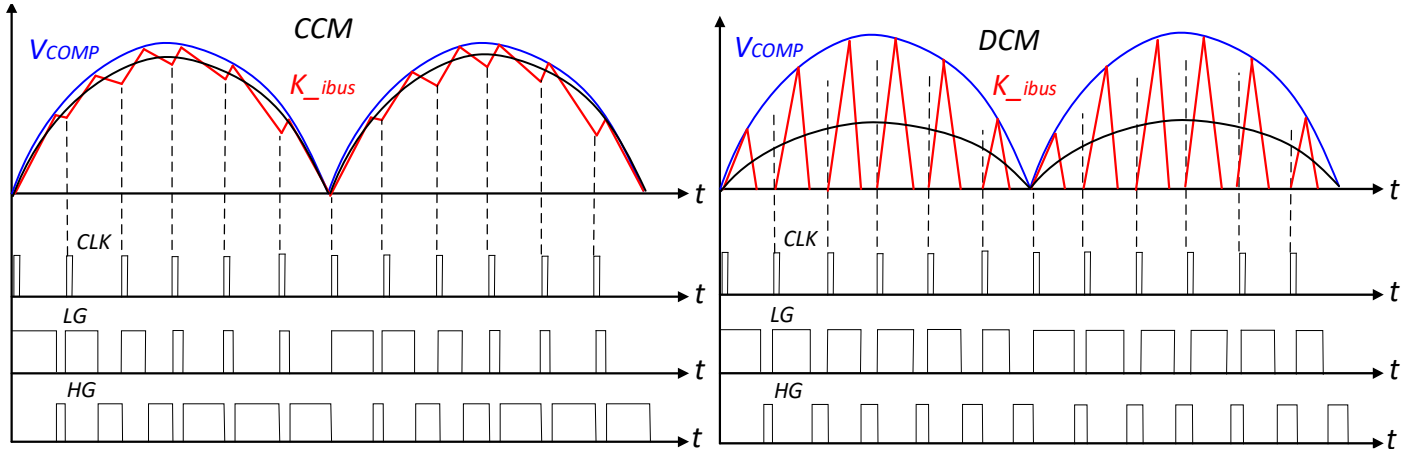

Fig. 8 Fixed Frequency Peak Control CCM/DCM PFC Boost Circuit Waveform

There is another mode called boundary current mode (BCM) between DCM and CCM, that is, when the inductance discharge reaches zero crossing, the on and off of the next switching cycle is started, so the circuit needs the current zero crossing detection (ZCD). In this mode, the switching frequency is variable, and varies with input, output and load conditions. The circuit and waveform are shown in Fig. 9 and Fig. 10.

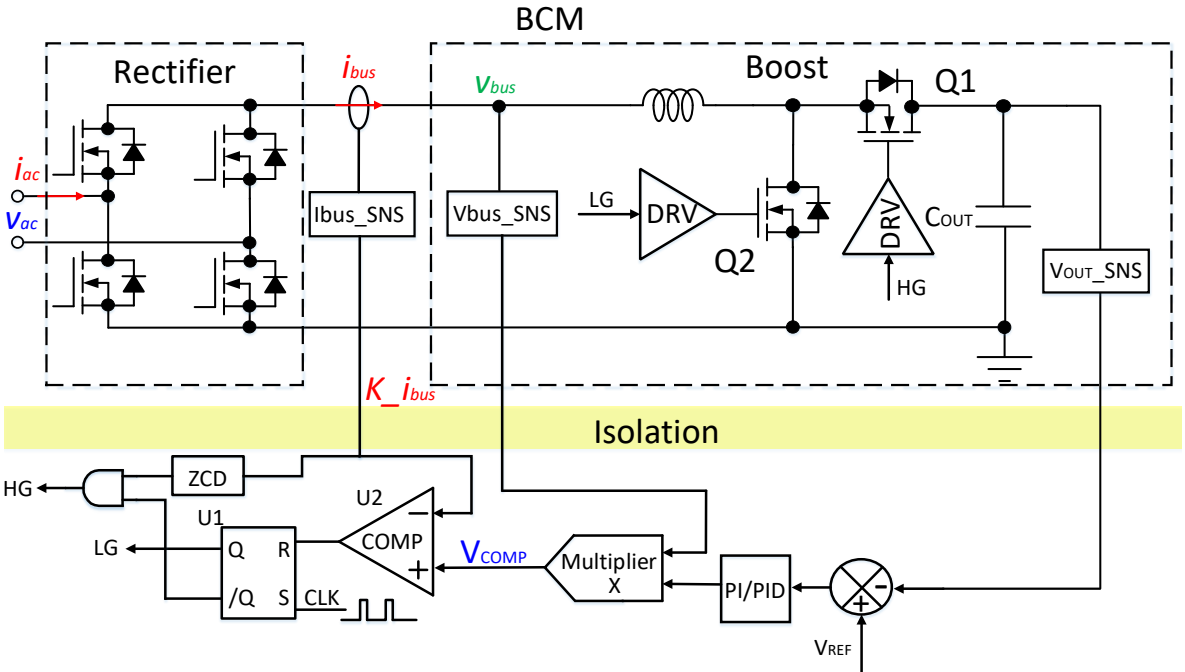

Fig. 9 BCM Peak Control PFC Boost Circuit

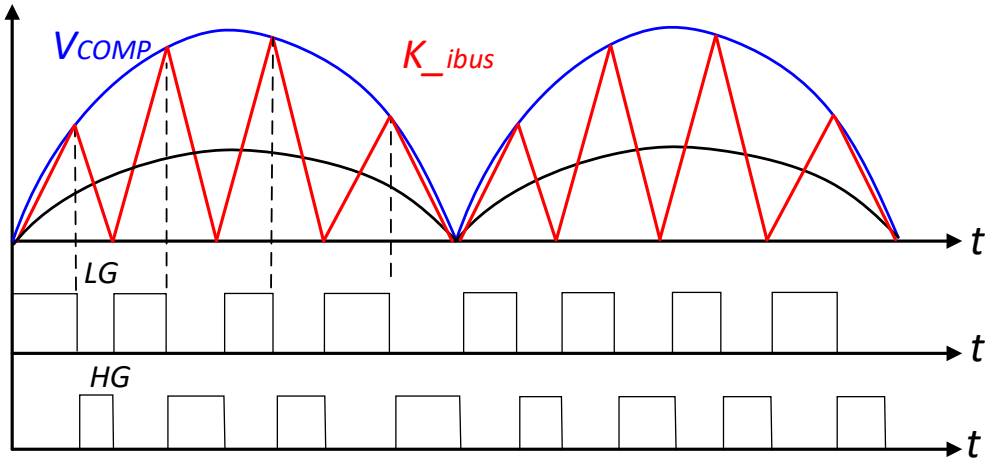

Fig. 10 BCM Peak Control PFC Boost Circuit Waveform

3.1.2 Hysteresis Control

Hysteresis control takes the upper and lower limits of the controlled quantity as control parameters. When the current reaches the upper limit of the target control quantity, the inductance current starts to discharge until it reaches the lower limit of the control quantity. This control will control the controlled quantity within a certain range, the control is relatively simple, the frequency is not fixed, the control circuit is shown in Fig. 11, and the waveform is shown in Fig. 12.

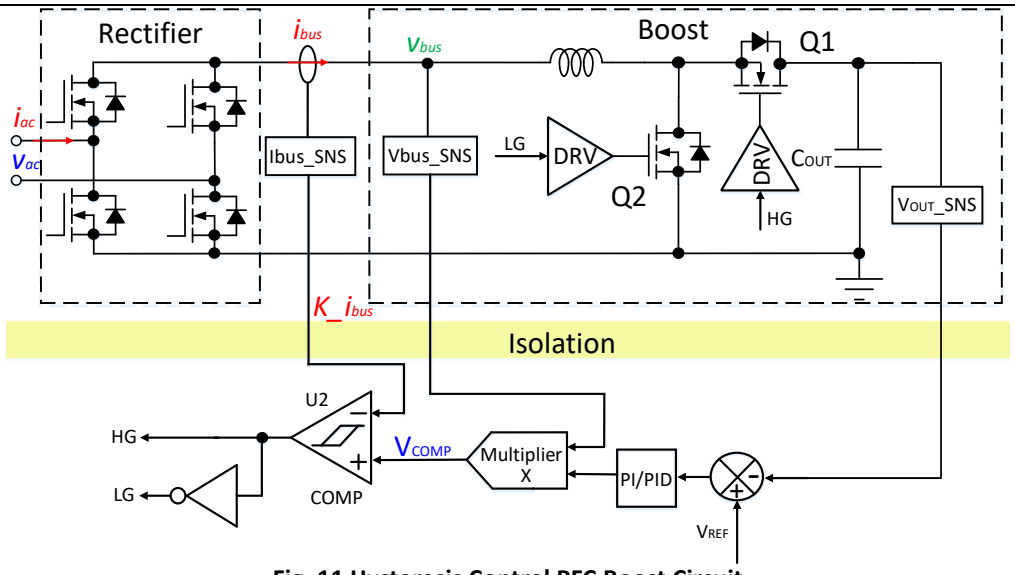

Fig. 11 Hysteresis Control PFC Boost Circuit

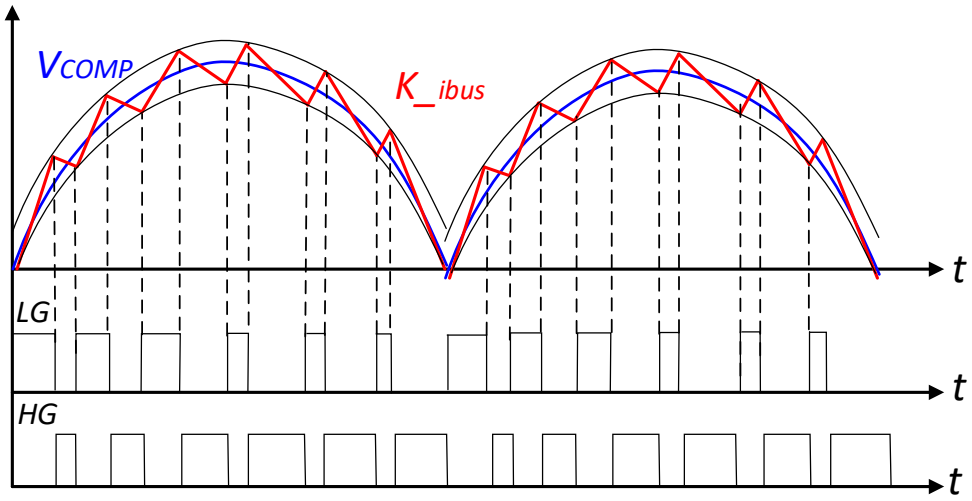

Fig. 12 Hysteresis Control PFC Boost Circuit Waveform

4 Low-side Current Sampling

If the sampling resistor is connected in series to the switch tube, it is low-side current sampling, as shown in Fig. 13 and Fig. 14.

Low-side sampling has low common mode voltage to the ground, and R_SNS is the high-side sampling resistance. When the current flows through the resistance, the voltage drop will be generated on the resistance. The current amplifier CA-IS1200/CA-IS1300 transmits the voltage drop to the low voltage side, which is converted into digital signals by ADC and sent to DSP or MCU, as shown in Fig. 13. The CA-IS1204 and CA-IS1305/06 can also be used to transmit differential voltage signals to the low side and read the digital signals on the low side directly through MCU, as shown in Fig. 14. For this sampling mode, the isolation power supply CA-IS3105W can be used because the high voltage side is referenced to the ground. However, it is recommended that the isolation power input and output be connected to VDD2 through serial LDO or filter, which still has a certain cost. Another way is that the resistance and regulator tube are connected in series, which is more economic.

Low-side current sampling mode has the following characteristics:

1. Power supply is relatively simple, and isolation power supply is not necessary.
2. When using isolation power supply, LDO or filter should be used on the input and output sides to prevent voltage ripple on the input and output sides from interfering with other signals.
3. The gate voltage is very low during normal operation, so the gate stress is very small under normal conditions.
4. High-side sampling for boost circuit, only the inductance charging current can be monitored and controlled within the switching cycle, and the control mode of PFC boost circuit is limited.

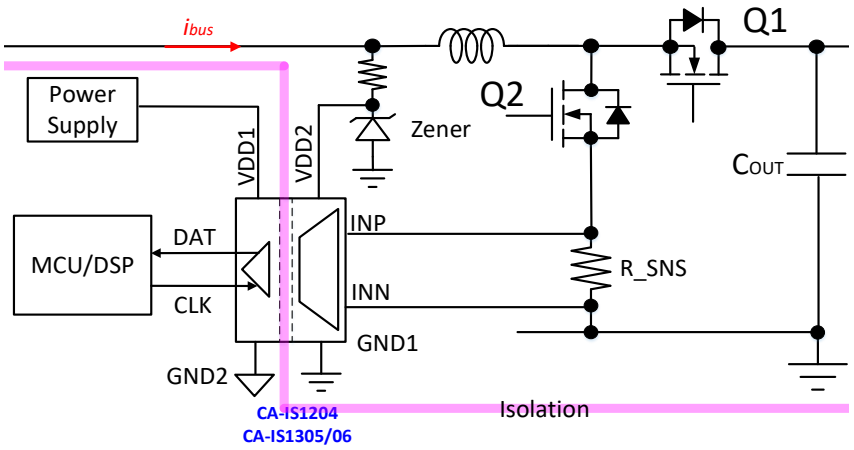

Fig. 13 Schematic Diagram 1 of Low-side Current Sampling

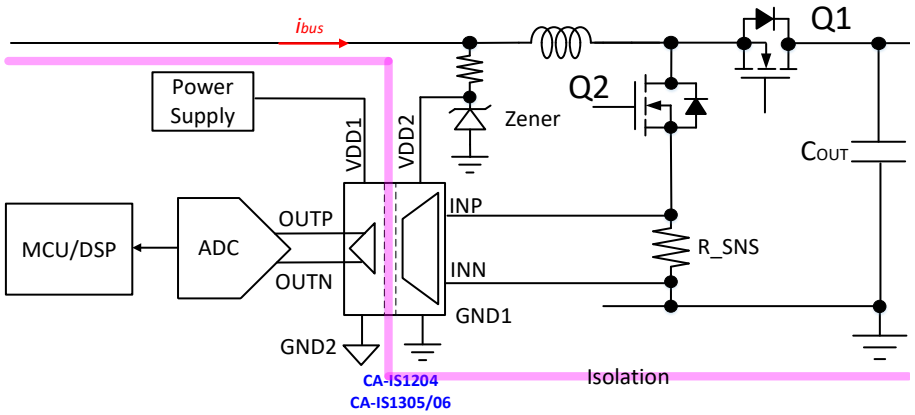

Fig. 14 Schematic Diagram 2 of Low-side Current Sampling

4.1 Control Method of Low-side Sampling PFC Boost Circuit

4.1.1 Fixed Switching Time Control COT (Constant OFF Time)

When the inductance current reaches the command current, the inductance current stops charging and starts discharging, which generates a fixed discharge time, or a fixed pulse width, through One-shot logic. When this fixed time is complete, the inductance current starts charging until the inductance current reaches the command current again. The envelope formed by the inductance current is sinusoidal. The mean value of the envelope approximates the sinusoidal waveform. In this mode, the switching frequency is variable, and varies with input, output and load conditions.

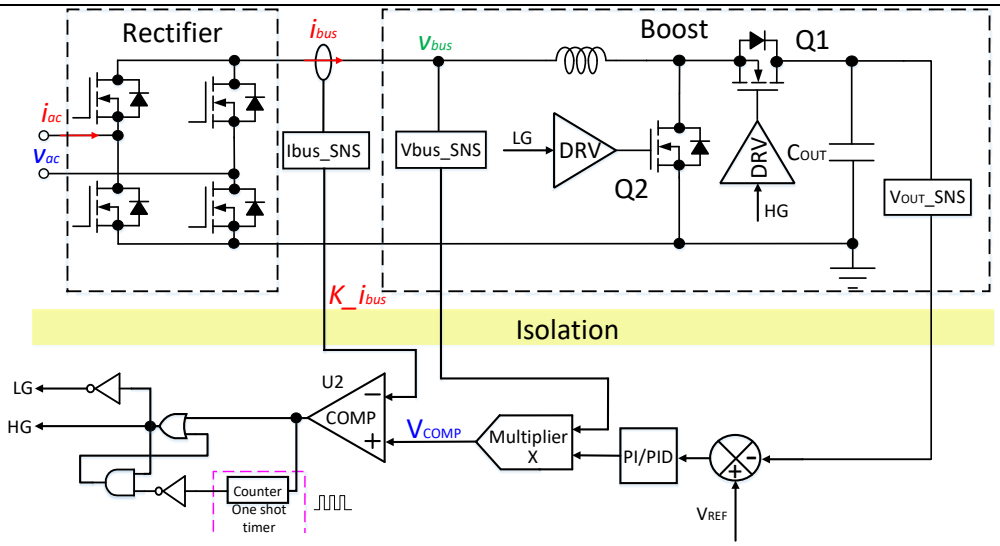

Fig. 15 Fixed On/off Time Control Circuit

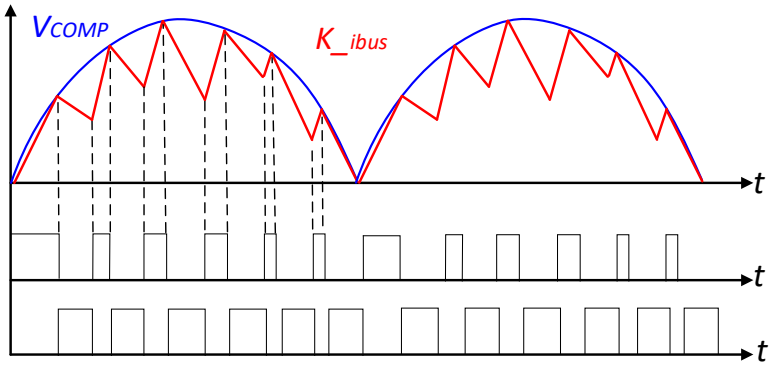

Fig. 16 Fixed On/off Time Control Waveform

In addition to the above control modes, there are other control modes such as average current mode control, valley current control, constant on time, voltage control mode, etc., which will not be described in detail in this chapter.

4.2 Comparative Analysis of High-side Sampling and Low-side Sampling

	High-side Current Sampling	Low-side Current Sampling	Note
Isolation barrier withstand voltage	High	Low	Ultimately affects chip life
High-side power supply	Require additional isolation power supply, need to add filter	Power supply circuit relatively simple, resistors and voltage regulator tubes will be OK	Additional circuits affect cost and circuit complexity
Control mode	Various	Limited	High-side current sampling includes all low-side control modes
Current Detecting	Full-cycle detection	Detection in part time of the cycle	

5 Voltage Sampling

The PFC circuit needs to sampling the input bus and output voltage. Sampling the input bus voltage is used to obtain the phase information of the input voltage, and sampling the output voltage is used in the negative feedback loop, as shown in Fig. 15. When voltage sampling is required, pay attention to the input voltage range to ensure that the common mode and differential mode voltage obtained by the input sampling are within the normal working range of the amplifier. Using the divider resistor to scale down the input voltage before feeding the current amplifier, the following conditions must be met:

$$\mathrm{VRange} \geq \frac{R2}{\mathrm{R1+R2}} \cdot Vbus \quad \text{(Formula 1)}$$

$$\mathrm{R1//R2} = R3 \quad \text{(Formula 2)}$$

$$\frac{1}{2 \cdot \pi \cdot (\mathrm{R1//R2+R3}) \cdot \mathrm{C1}} \geq 10 \cdot f\_Vbus \quad \text{(Formula 3)}$$

Note: Formula 3 is not a must. DSP or MCU filter algorithm can also realize digital filtering function.

V_{Range} is the maximum input differential voltage of the amplifier, Vbus is the maximum input DC bus voltage, and f_Vbus is the voltage frequency of the input DC bus.

R3=R2//R1 is used to offset the offset voltage of the amplifier dut to the input current. C1, R1, R2 and R3 form a low-pass filter to filter the input voltage of the amplifier. For details, please refer to Chipanalog's "Voltage Detection Based on the CA1200/1300 Device".

Sampling the output voltage to obtain the output voltage is used for negative feedback control, as shown in Fig. 15. When output voltage sampling is required, pay attention to the range of the output voltage to ensure that the common mode and differential mode voltage obtained by the input sampling are within the normal working range of the current amplifier. Using the divider resistor to scale down the input voltage before feeding the current amplifier, the following conditions must be met:

$$V_{Range} \geqslant \frac{R5}{\mathrm{R4+R5}} \cdot VOUT$$

$$\mathrm{R4//R5} = R6$$

V_{Range} is the maximum input differential voltage of the amplifier, V_{OUT} is the output voltage, and fs is the switching frequency of the converter.

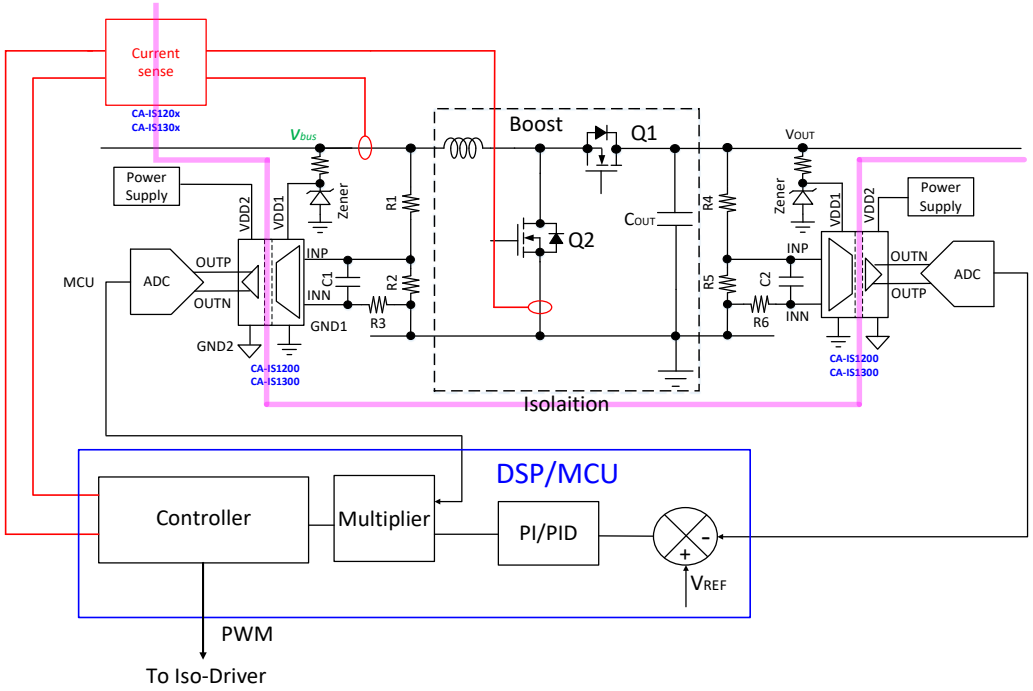

Fig. 17 PFC Boost Circuit Voltage Sampling Diagram

6 PCB Design Examples

6.1 Matters when Current Detection Amplifier is Used to Detect Current

When the current detection amplifier is used to detect current, the following matters must be paid attention to, as shown in Fig. 18:

1. C1 and C2 provide energy storage and filtering functions for power supply of the chip, so C1 and C2 are placed next to VDD1 and VDD2 pins of the chip.
2. R_SNS is the current detection resistor. When the current flows through this resistor, the voltage drop is generated, and the voltage drop is fed into the current detection amplifier. Use differential wiring as far as possible in design. When the differential wiring is long, R1, R2 and C2 can be used as filters, which can also reduce the detection error caused by impedance deviation of the differential wiring, so R1=R2.
3. INP/INN and OUTP/OUTN differential pairs are easy to be interfered, so keep away from the interference sources in design. Generally, they are high $\frac{dV}{dt}$ or $\frac{di}{dt}$ signals.
4. If the output is OUTP or OUTN, suggest to design equal length differential wiring. If the wiring is long, it is recommended to connect ohm resistance in series to reduce the detection error caused by impedance deviation of the differential wiring.
5. If the output is CLKIN or DOUT on the secondary side, the signal is the strong interference signal and should be kept away from the other signals. Copper foil is connected to GND2 through VIA hole near the wiring.
6. Keep more than 8mm distance between the top and bottom layers of PCB on both sides to prevent high voltage creepage, as shown in Fig. 19.

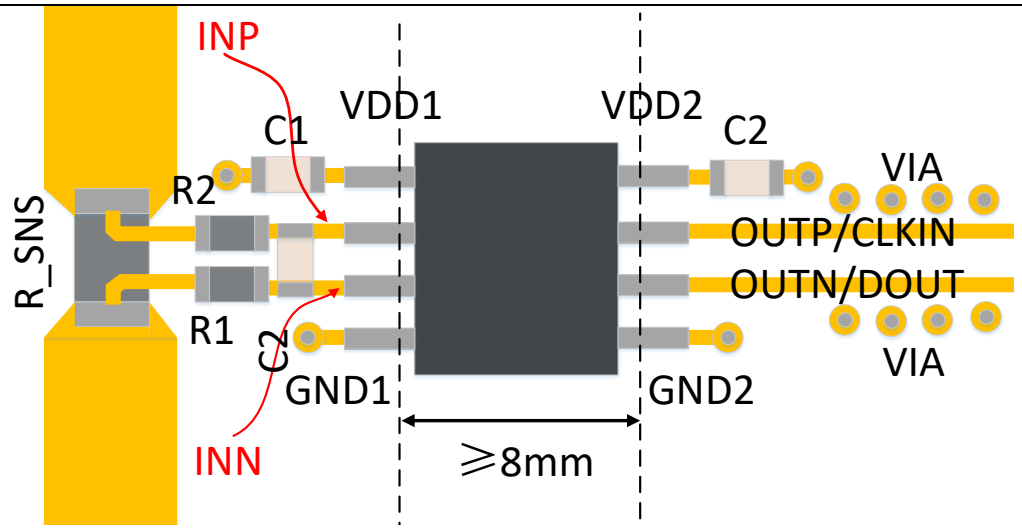

Fig. 18 PCB Design Example for Current Detection Application

Fig. 19 Keep Sufficient Distance Between the Two Isolation Layers to Prevent Creepage

6.2 Matters when Current Detection Amplifier is Used to Detect Voltage

When the current detection amplifier is used to detect voltage, the following matters must be paid attention to, as shown in Fig. 20:

1. C1 and C2 provide energy storage and filtering functions for power supply of the chip, so C1 and C2 are placed next to VDD1 and VDD2 pins of the chip.
2. R_top and R_bot are the voltage detection divider resistors used to detect the voltage on the output capacitor Bull Cap. The two components are placed as close to the chip as possible in wiring mode. When voltage detecting, suggest to wire the two capacitor voltages to the divider to improve the detection accuracy. If the detection voltage is very high, it is recommended that multiple divider resistors be connected in series to reduce the power consumption of a single resistor.
3. INP/INN and OUTP/OUTN differential pairs are easy to be interfered, so keep away from the interference sources in design. Generally, they are high $\frac{dV}{dt}$ or $\frac{di}{dt}$ signals.
4. If the output is OUTP or OUTN, suggest to design equal length differential wiring. If the wiring is long, it is recommended to connect ohm resistance in series to reduce the detection error caused by impedance deviation of the differential wiring.
5. If the output is CLKIN or DOUT on the secondary side, the signal is the strong interference signal and should be kept away from the other signals. Copper foil is connected to GND2 through VIA hole near the wiring.

6. Keep more than 8mm distance between the top and bottom layers of PCB on both sides to prevent high voltage creepage, as shown in Fig. 19.

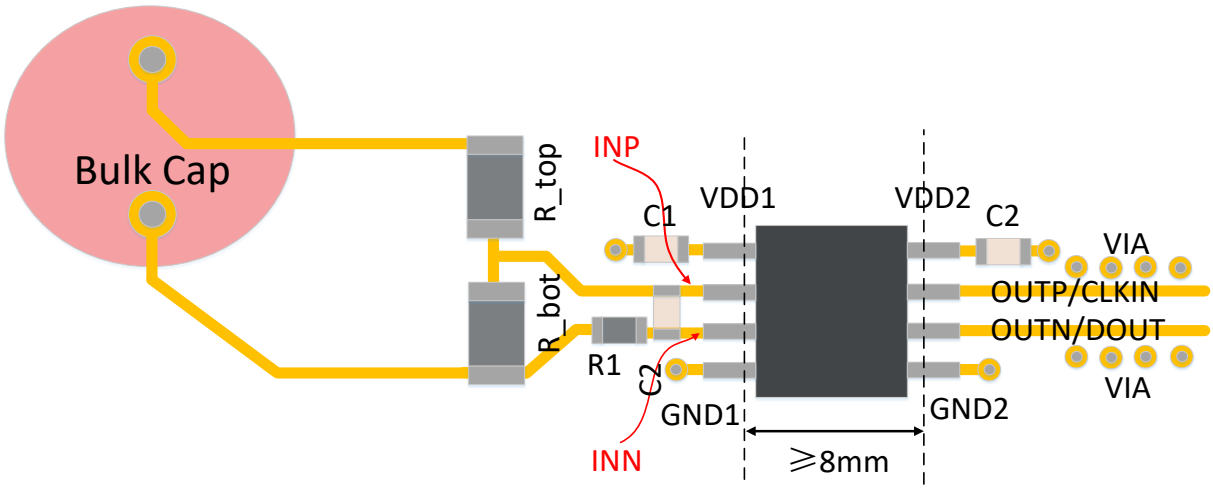

Fig. 20 PCB Design Example for Voltage Detection Application

7 Version Information

Version	Date	State Description
Ver1.0	Apr. 2022	Initial version

8 Important Statement

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