CA-IS3531 High-Speed Triple-Channel Digital Isolators

1. Features

- **Meets IR46 Physical Layer Standards**
- **Data Rate is up to 10Mbps**
- **Robust Galvanic Isolation of Digital Signals**
  - High lifetime: >40 years
  - Up to 5.0kV$_{RMS}$ isolation rating
  - ±150 kV/µs typical CMTI
  - ±8kV Human body model ESD protection
  - ±10 kV surge tolerant
  - Schmitt trigger inputs for high noise immunity
  - High electromagnetic immunity
- **Low Power Consumption**
  - 1.6mA per channel at 1Mbps with $V_{DD\_}$ = 5.0V
  - 2.5mA per channel at 10Mbps with $V_{DD\_}$ = 5.0V
  - Shutdown current is as low as 40 µA@5.0V
- **Best in Class Propagation Delay and Skew**
  - 10ns typical propagation delay
  - 1ns pulse width distortion
  - 2ns propagation delay skew (chip -to-chip)
- **Enable Control Input with Internal Pull-up**
- **2.375V to 5.5V Wide Operating Supply Voltage**
- **Wide Operating Temperature Range: -40°C to 125°C**
- **No Start-up Initialization Required**
- **Push-pull Output with Default Output High**
- **RoHS-Compliant Package:**
  - SOIC16(W) wide-body
- **Safety Regulatory Approvals**
  - VDE 0884-11 Reinforced Isolation (pending)
  - UL According to UL1577
  - IEC 62368-1, IEC 61010-1, GB 4943.1-2011 and GB 8898-2011 certifications

2. Applications

- Smart meters
- Data concentrators
- Circuit breakers

3. General Description

The CA-IS3531 is high-performance, low-power triple-channel digital isolators specially developed for smart electricity meters (IR46). This family devices feature up to ±10kV surge tolerant and ±8kV HBM ESD protection. The digital isolator is based on Chipanalog's advanced isolation architecture with up to ±5kV$_{RMS}$ isolation rating and ±150kV/µs CMTI, that provides a robust isolated data path between the different power domain and requires no special considerations or initialization at start-up. A simplified block diagram for a single CA-IS3531 channel is shown in the figure below.

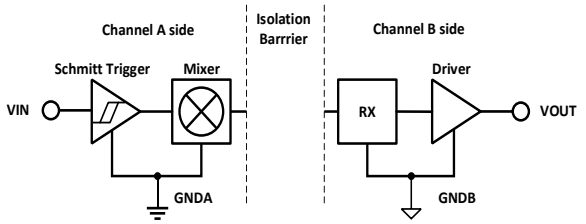
The CA-IS3531 has 2 forward and 1 reverse-direction channels. All of devices in this family come with enable control pins which can be used to put the driver outputs in high-impedance for the multi-master driving applications. Also, for the CA-IS3531HWPA, the enable control input can be used to put the device into shutdown mode to reduce power consumption as low as 40µA. The CA-IS3531 provides push-pull output with default output high, that means when the input is either not powered or is open-circuit, the default output is high for CA-IS3531HWPD and CA-IS3531HDPA.

The CA-IS3531 family devices are specified over the -40°C to +125°C operating temperature range. They are available in 16-pin SOIC wide body package.

Device information

Part number	Package	Package size (NOM)
CA-IS3531	SOIC16-WB(W)	10.30 mm × 7.50 mm

Simplified Channel Structure



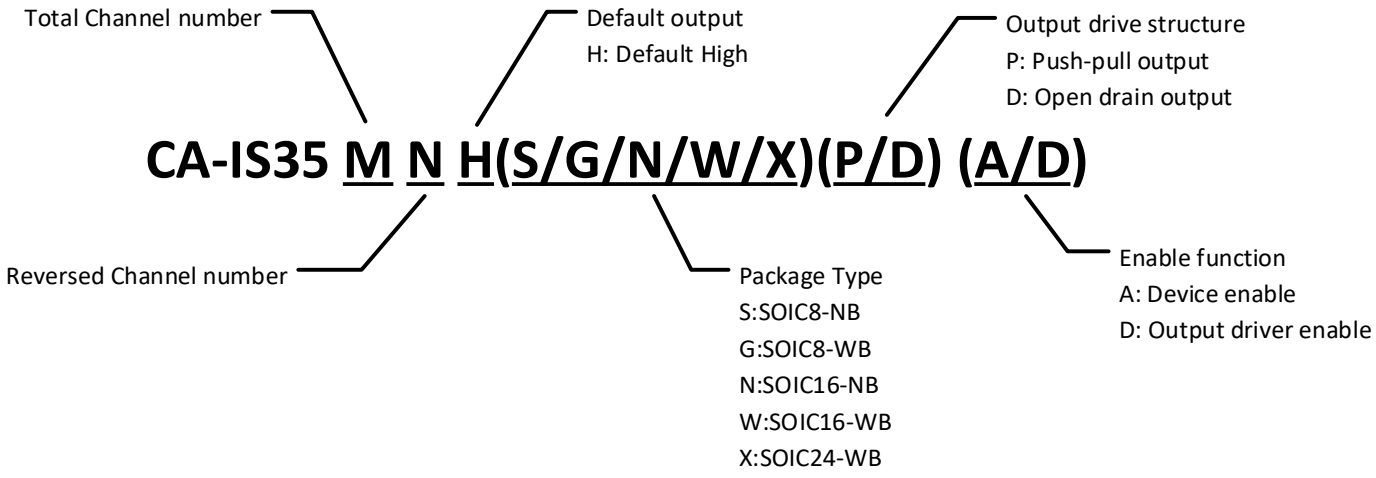
GNDA and GNDB are the isolated grounds for A side and B side respectively.

4. Ordering Information

Table 4-1. Ordering Information

Part Number	Number of Inputs A Side	Number of Inputs B Side	Output Type	Default Output	Isolation Rating (kV)	Output Enable	Package
CA-IS3531HWPD	2	1	Push-pull	High	5.0	Driver output enable control	SOIC16-WB
CA-IS3531HWPA	2	1	Push-pull	High	5.0	Device enable control	SOIC16-WB

5. Naming Rules



Contents

6. Revision History

Revision Number	Description	Page Changed
Preliminary Version	Initial version	N/A
Version A	• Update Safety-Related Certifications • Update Electrical Characteristics, leakage current maximum value	8 - 12
Version B	• Update part number	2
Version C	• Changed tape data • Added Soldering Temperature (reflow) Profile information	21 - 23
Version 1.00	Update document format	All
Version 1.01	Update POD	20

7. Pin Configuration and Functions

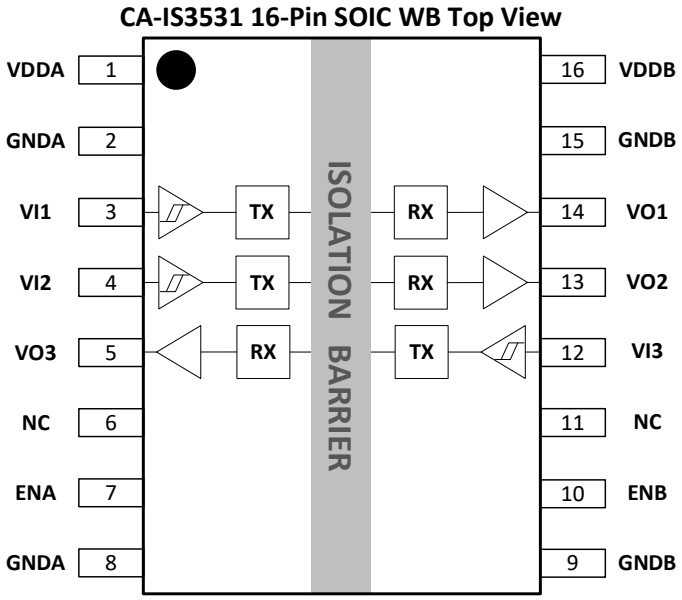


Figure 7-1. CA-IS3531 pin configuration

Table 7-1. CA-IS3531 pin description and function

CA-IS3531	Name	Type	Description
1	VDDA	Supply	Power supply for side A.
2, 8	GNDA	Ground	Ground reference for side A.
3	VI1	Digital I/O	Digital input 1 on side A, corresponds to logic output 1 on side B.
4	VI2	Digital I/O	Digital input 2 on side A, corresponds to logic output 2 on side B.
5	VO3	Digital I/O	Digital output 3 on side A, VO3 is the logic output for the VI3 input on side B.
6	NC	No Connect	Not internally connected. It can be left floating or tied to GNDA.
7	ENA	Digital I/O	Enable control input for side A, see Table 10-2 for more details.
9, 15	GNDB	Ground	Ground reference for side B.
10	ENB	Digital I/O	Enable control input for side B, see Table 10-2 for more details.
11	NC	No Connect	Not internally connected. It can be left floating or tied to GNDB.
12	VI3	Digital I/O	Digital input 3 on side B, corresponds to logic output 3 on side A.
13	VO2	Digital I/O	Digital output 2 on side B, VO2 is the logic output for the VI2 input on side A.
14	VO1	Digital I/O	Digital output 1 on side B, VO1 is the logic output for the VI1 input on side A.
16	VDDB	Supply	Power supply for side B.

8. Specifications

8.1. Absolute Maximum Ratings[1]

Parameters		Minimum value	Maximum value	Unit
V_{DDA}, V_{DDB}	Power supply voltage [2]	-0.5	7.0	V
V_{IN}	Input voltage at VI_X, EN_X	-0.5	V_{DDI}+0.5 [3]	V
I_O	Output current	-20	20	mA
T_J	Junction temperature	-40	150	°C
T_{STG}	Storage temperature range	-65	150	°C

Notes:

1. The stresses listed under "Absolute Maximum Ratings" are stress ratings only, not for functional operation condition. Exposure to absolute maximum rating conditions for extended periods may cause permanent damage to the device.
2. All voltage values are with respect to the local ground terminal (GNDA or GNDB) and are peak voltage values.
3. Maximum voltage must not be exceed 7 V, V_{DDI} = Input-side supply V_{DD}.

8.2. ESD Ratings

Parameters			Numerical value	Unit
V_{ESD} Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins [1]		±8000	V
	Charged device model (CDM), per JEDEC Specification JESD22-C101, all pins[2]		±2000	V

Notes:

1. Per JEDEC document JEP155, 500V HBM allows safe manufacturing of standard ESD control process.
2. JEDEC document JEP157, 250V HBM allows safe manufacturing of standard ESD control process.

8.3. Recommended Operating Conditions

	Parameters		MIN	Type	MAX	Unit
V_{DDA}, V_{DDB}	Supply voltage on side A, B		2.375	3.30	5.50	V
$V_{DD\ (UVLO+)}$	V_{DD} Undervoltage-Lockout Threshold When Supply Voltage is Rising		1.95	2.24	2.375	V
$V_{DD\ (UVLO-)}$	V_{DD} Undervoltage-Lockout Threshold When Supply Voltage is Falling		1.88	2.10	2.325	V
$V_{HYS\ (UVLO)}$	V_{DD} Undervoltage-Lockout Threshold Hysteresis		70	140	250	mV
I_{OH}	High-level Output Current	V_{DDO}[1] = 5V	-4			mA
		V_{DDO}[1] = 3.3V	-2			
		V_{DDO}[1] = 2.5V	-1			
I_{OL}	Low-level Output Current	V_{DDO}[1] = 5V			4	mA
		V_{DDO}[1] = 3.3V			2	
		V_{DDO}[1] = 2.5V			1	
V_{IH}	High-level Input Voltage		2.0			V
V_{IL}	Low-level Input Voltage				0.8	V
DR	Data Rate		0		10	Mbps
T_A	Ambient Temperature		-40	27	125	°C

Note:

1. V_{DDO} = Output-side supply V_{DD}.

8.4. Thermal Information

Thermal Metric		CA-IS3531 SOIC16-WB(W)	Unit
$R_{\theta JA}$	Junction-to-ambient thermal resistance	83.4	°C/W

8.5. Power Rating

Parameters		Test conditions	MIN	TYPE	MAX	Unit
CA-IS3531						
P_D	Maximum Power Dissipation	V_{DDA} = V_{DDB} = 5.5 V, C_L = 15 pF, T_J = 150°C, Input a 75-MHz 50% duty cycle square wave.			49	mW
P_{DA}	Maximum Power Dissipation on Side-A				17	mW
P_{DB}	Maximum Power Dissipation on Side-B				32	mW

8.6. Insulation Specifications

Parameters		Test Conditions	Value	Unit
			W	
CLR	External clearance	Shortest terminal-to-terminal distance through air	8	mm
CPG	External creepage	Shortest terminal-to-terminal distance across the package surface	8	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	32	µm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11)； IEC 60112	>600	V
	Material group	Per IEC 60664-1	I	
Overvoltage category per IEC 60664-1		Rated mains voltage ≤ 300 V_{RMS}	I-IV	
		Rated mains voltage ≤ 400 V_{RMS}	I-IV	
		Rated mains voltage ≤ 600 V_{RMS}	I-III	
DIN V VDE V 0884-11:2017-01[1]				
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	849	V_{PK}
V_{IOWM}	Maximum operating isolation voltage	AC voltage; time-dependent dielectric breakdown (TDDB) test	600	V_{RMS}
		DC voltage	849	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t=60 s (certified); $V_{TEST} = 1.2 \times V_{IOTM}$, t=1 s (100% product test)	7070	V_{PK}
V_{IOSM}	Maximum surge isolation voltage[2]	Test method per IEC 60065, 1.2/50 µs waveform, $V_{TEST} = 1.6 \times V_{IOSM}$ (production test)	6250	V_{PK}
q_{pd}	Apparent charge[3]	Method a, after input/output safety test of the subgroup 2/3, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)} = 1.2 \times V_{IORM}$, t_m = 10 s	≤5	pC
		Method a, after environmental test of the subgroup 1, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)} = 1.6 \times V_{IORM}$, t_m = 10 s	≤5	
		Method b, at routine test (100% production test) and preconditioning (type test) $V_{ini} = 1.2 \times V_{IOTM}$, t_{ini} = 1 s; $V_{pd(m)} = 1.875 \times V_{IORM}$, t_m = 1 s	≤5	
C_{IO}	Barrier capacitance, input to output[4]	V_{IO} = 0.4 × sin (2πft), f = 1 MHz	~0.5	pF
R_{IO}	Isolation resistance[4]	V_{IO} = 500 V, T_A = 25°C	$>10^{12}$	Ω
		V_{IO} = 500 V, 100°C ≤ T_A ≤ 125°C	$>10^{11}$	
		V_{IO} = 500 V at T_S = 150°C	$>10^{9}$	
	Pollution degree		2	
UL 1577				
V_{ISO}	Maximum withstanding isolation voltage	$V_{TEST} = V_{ISO}$, t = 60 s (qualification) $V_{TEST} = 1.2 \times V_{ISO}$, t = 1 s (100% production test)	5000	V_{RMS}

Notes:

1. This coupler is suitable for “safe electrical insulation” only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
2. Devices are immersed in oil during surge characterization.
3. The characterization charge is discharging charge (pd) caused by partial discharge.
4. Capacitance and resistance are measured with all pins on field-side and logic-side tied together.

8.7. Safety-Related Certifications

VDE (pending)	UL	CQC	TUV
Certified according to DIN VDE V 0884-11:2017-01	Certified according to UL 1577 Component Recognition Program	Certified according to GB 4943.1-2011 and GB 8898-2011	Certified according to EN/IEC 61010-1:2010 (3rd Ed) and EN /IEC 62368-1:2014+A11:2017
Maximum transient isolation voltage: 7070V_{pk} (SOIC16-W)	SOP16-W: 5000 V_{RMS}	SOP16-W: Reinforced insulation, 1000 V_{RMS} maximum working voltage (Altitude ≤ 5000 m)	5000 V_{RMS}(SOP16-W) insulation per EN/IEC 61010-1:2010 (3rd Ed) and EN /IEC 62368-1:2014+A11:2017, working voltage is up to 1000 V_{RMS}(SOP16-W)
	Certificate number：E511334	Certificate number : SOP16-W: CQC20001251466	CB Certificate number: JPTUV-112091; DE 2-028028 AK Certificate number: AK 50476717 0001; AK 50476719 0001

8.8. Electrical Characteristics

8.8.1. Electrical Characteristics at 5.0V

V_{DDA} = V_{DDB} = 5 V ± 10%, T_A = -40 to 125°C

Parameters		Test Conditions	MIN	TYPE	MAX	UNIT
V_{OH}	High-level Output Voltage	I_{OH} = -4mA; See Figure 9-2	V_{DDO}[1]-0.4	4.8		V
V_{OL}	Low-level Output Voltage	I_{OL} = 4mA; See Figure 9-2		0.2	0.4	V
$V_{IT+(IN)}$	Rising input switching threshold		1.4	1.67	1.9	V
$V_{IT-(IN)}$	Falling input switching threshold		1.0	1.23	1.4	V
$V_{I(HYS)}$	Input Threshold Hysteresis		0.30	0.44	0.50	V
I_{IH}	High-Level Input Leakage Current	V_{IH} = V_{DDA} at INx or ENx			20	µA
I_{IL}	Low-Level Input Leakage Current	V_{IL} = 0 V at INx	-20			µA
Z_O	Output Impedance[2]			50		Ω
CMTI	Common-mode Transient Immunity	V_I = V_{DDI}[1] or 0 V, V_{CM} = 1200 V; See Figure 9-4	100	150		kV/µs
C_I	Input Capacitance[3]	V_I = V_{DD}/ 2 + 0.4×sin(2πft), f = 1 MHz, V_{DD} = 5 V		2		pF

Notes:
1. V_{DDI} = Input-side supply V_{DD}, V_{DDO} = Output-side supply V_{DD}.
2. The nominal output impedance of each isolator driver is 50 Ω ± 40%.
3. Measured from pin to Ground.

8.8.2. Electrical Characteristics at 3.3V

V_{DDA} = V_{DDB} = 3.3 V ± 10%, T_A = -40 to 125°C

Parameters		Test Conditions	MIN	TYPE	MAX	UNIT
V_{OH}	High-level Output Voltage	I_{OH} = -4mA; See Figure 9-2	V_{DDO}[1]-0.4	3.1		V
V_{OL}	Low-level Output Voltage	I_{OL} = 4mA; See Figure 9-2		0.2	0.4	V
$V_{IT+(IN)}$	Rising input switching threshold		1.4	1.67	1.9	V
$V_{IT-(IN)}$	Falling input switching threshold		1.0	1.23	1.4	V
$V_{I(HYS)}$	Input Threshold Hysteresis		0.30	0.44	0.50	V
I_{IH}	High-Level Input Leakage Current	V_{IH} = V_{DDA} at INx or ENx			20	µA
I_{IL}	Low-Level Input Leakage Current	V_{IL} = 0 V at INx	-20			µA
Z_O	Output Impedance[2]			50		Ω
CMTI	Common-mode Transient Immunity	V_I = V_{DDI}[1] or 0 V, V_{CM} = 1200 V; See Figure 9-4	100	150		kV/µs
C_I	Input Capacitance[3]	V_I = V_{DD}/ 2 + 0.4×sin(2πft), f = 1 MHz, V_{DD} = 3.3 V		2		pF

Notes:
1. V_{DDI} = Input-side supply V_{DD}, V_{DDO} = Output-side supply V_{DD}.
2. The nominal output impedance of each isolator driver is 50 Ω ± 40%.
3. Measured from pin to Ground.

8.8.3. Electrical Characteristics at 2.5V

V_{DDA} = V_{DDB} = 2.5 V ± 10%, T_A = -40 to 125°C

Parameters		Test Conditions	MIN	TYPE	MAX	UNIT
V_{OH}	High-level Output Voltage	I_{OH} = -4mA; See Figure 9-2	V_{DDO}[1]-0.4	2.3		V
V_{OL}	Low-level Output Voltage	I_{OL} = 4mA; See Figure 9-2		0.2	0.4	V
$V_{IT+(IN)}$	Rising input switching threshold		1.4	1.67	1.9	V
$V_{IT-(IN)}$	Falling input switching threshold		1.0	1.23	1.4	V
$V_{I(HYS)}$	Input Threshold Hysteresis		0.30	0.44	0.50	V
I_{IH}	High-Level Input Leakage Current	V_{IH} = V_{DDA} at INx or ENx			20	µA
I_{IL}	Low-Level Input Leakage Current	V_{IL} = 0 V at INx	-20			µA
Z_O	Output Impedance[2]			50		Ω
CMTI	Common-mode Transient Immunity	V_I = V_{DDI}[1] or 0 V, V_{CM} = 1200 V; See Figure 9-4	100	150		kV/µs
C_I	Input Capacitance[3]	V_I = V_{DD}/ 2 + 0.4×sin(2πft), f = 1 MHz, V_{DD} = 2.5 V		2		pF

Notes:
1. V_{DDI} = Input-side supply V_{DD}, V_{DDO} = Output-side supply V_{DD}.

2. The nominal output impedance of each isolator driver is 50 Ω ± 40%.
3. Measured from pin to Ground.

8.9. Supply Current Characteristics

8.9.1. Supply Current Characteristics at 5.0V

V_{DDA} = V_{DDB} = 5 V ± 10%, T_A = -40 to 125°C

Parameters	Test Conditions		Supply Current	MIN	TYP	MAX	Unit
CA-IS3531							
Supply Current – Device shutdown	ENA = ENB = 0 V;		I_{DDA}	25	37	56	µA
			I_{DDB}	25	37	56	
Supply Current – Outputs disabled	ENA = ENB = 0 V; V_{IN} = V_{DDI}[1]		I_{DDA}		1.4	2.1	mA
			I_{DDB}		1.8	2.7	
	ENA = ENB = 0 V; V_{IN} = 0V		I_{DDA}		2.9	4.5	
			I_{DDB}		2.6	3.9	
Supply Current – DC Signal	ENA = ENB = V_{DDI}; V_{IN} = V_{DDI}		I_{DDA}		1.5	2.2	
			I_{DDB}		2.0	2.9	
	ENA = ENB = V_{DDI}; V_{IN} = 0V		I_{DDA}		3.0	4.5	
			I_{DDB}		2.8	4.2	
Supply Current – AC Signal	ENA = ENB = V_{DDI}; All Channels Switching with 50% Duty Cycle Square Wave Clock Input with 5V Amplitude; C_L = 15 pF for Each Channel.	1Mbps (500kHz)	I_{DDA}		2.3	3.4	
			I_{DDB}		2.5	3.7	
		10Mbps (5MHz)	I_{DDA}		2.8	4.1	
			I_{DDB}		3.4	5.1	

Note:
1. V_{DDI} = Input-side supply voltage V_{DD}.

8.9.2. Supply Current Characteristics at 3.3V

V_{DDA} = V_{DDB} = 3.3 V ± 10%, T_A = -40 to 125°C

Parameters	Test conditions		Supply Current	MIN	TYP	MAX	Unit
CA-IS3531							
Supply Current – Device shutdown	ENA = ENB = 0 V;		I_{DDA}	25	37	56	µA
			I_{DDB}	25	37	56	
Supply Current – Outputs disabled	ENA = ENB = 0 V; V_{IN} = V_{DDI}[1]		I_{DDA}		1.4	2.1	mA
			I_{DDB}		1.8	2.7	
	ENA = ENB = 0 V; V_{IN} = 0V		I_{DDA}		2.9	4.5	
			I_{DDB}		2.6	3.9	
Supply Current – DC Signal	ENA = ENB = V_{DDI}; V_{IN} = V_{DDI}		I_{DDA}		1.5	2.2	
			I_{DDB}		2.0	2.9	
	ENA = ENB = V_{DDI}; V_{IN} = 0V		I_{DDA}		3.0	4.5	
			I_{DDB}		2.8	4.2	
Supply Current – AC Signal	ENA=ENB = V_{DDI}; All Channels Switching with 50% Duty Cycle Square Wave Clock Input with 3.3V Amplitude; C_L = 15 pF for Each Channel.	1Mbps (500kHz)	I_{DDA}		2.3	3.4	
			I_{DDB}		2.5	3.7	
		10Mbps (5MHz)	I_{DDA}		2.6	3.9	
			I_{DDB}		3.2	4.8	

Note:
1. V_{DDI} = Input-side supply voltage V_{DD}.

8.9.3. Supply Current Characteristics at 2.5V

V_{DDA} = V_{DDB} = 2.5 V ± 10%, T_A = -40 to 125°C

Parameters	Test Conditions		Supply Current	MIN	TYP	MAX	Unit
CA-IS3531							
Supply Current – Device shutdown	ENA = ENB = 0 V;		I_{DDA}	25	37	56	µA
			I_{DDB}	25	37	56	
Supply Current – Disable	ENA = ENB = 0 V; V_{IN} = V_{DDI}[1]		I_{DDA}		1.4	2.1	mA
			I_{DDB}		1.8	2.7	
	ENA = ENB = 0 V; V_{IN} = 0V		I_{DDA}		2.9	4.5	
			I_{DDB}		2.6	3.9	
Supply Current – DC Signal	ENA = ENB = V_{DDI}; V_{IN} = V_{DDI}		I_{DDA}		1.5	2.2	
			I_{DDB}		2.0	2.9	
	ENA = ENB = V_{DDI}; V_{IN} = 0V		I_{DDA}		3.0	4.5	
			I_{DDB}		2.8	4.2	
Supply Current – AC Signal	ENA=ENB = V_{DDI}; All Channels Switching with 50% Duty Cycle Square Wave Clock Input with 2.5V Amplitude; CL = 15 pF for Each Channel.	1Mbps (500kHz)	I_{DDA}		2.3	3.4	
			I_{DDB}		2.5	3.7	
		10Mbps (5MHz)	I_{DDA}		2.5	3.8	
			I_{DDB}		3.0	4.5	

Note:

1. V_{DDI} = Input-side supply V_{DD}.

8.10. Timing Characteristics

8.10.1. Timing Characteristics at 5.0V

V_{DDA} = V_{DDB} = 5 V ± 10%, T_A = -40 to 125°C

Parameters		Test Conditions	MIN	TYP	MAX	Unit
DR	Data Rate		0		10	Mbps
t_{PLH}, t_{PHL}	Propagation Delay Time	See Figure 9-1	5.0	10.0	15.0	ns
PWD	Pulse Width Distortion |t_{PLH} - t_{PHL}|			1.0	4.5	ns
t_{sk}	Channel-to-Channel Output Skew Time[1]	Same-direction channels		1.0	4.5	ns
t_r	Output Signal Rise Time	See Figure 9-1		2.5	4.0	ns
t_f	Output Signal Fall Time	See Figure 9-1		2.5	4.0	ns
t_{PHZ}	Disable Propagation Delay, High to High Impedance Output	See Figure 9-2		8	12	ns
t_{PLZ}	Disable Propagation Delay, Low to High Impedance Output			8	12	ns
t_{PZH}	Enable Propagation Delay, High Impedance to High Output			5	10	µs
t_{PZL}	Enable Propagation Delay, High Impedance to Low Output			10	20	ns
t_{DO}	Default Output Delay Time from Input Power Loss	See Figure 9-3		8	12	µs
t_{SU}	Start-up Time			15	40	µs

Note:

1. tsk is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.

8.10.2. Timing Characteristics at 3.3V

V_{DDA} = V_{DDB} = 3.3 V ± 10%, T_A = -40 to 125°C

Parameters		Test Conditions	MIN	TYP	MAX	Unit
DR	Data Rate		0		10	Mbps
t_{PLH}, t_{PHL}	Propagation Delay Time	See Figure 9-1	5.0	10.0	15.0	ns
PWD	Pulse Width Distortion $\|t_{PLH} - t_{PHL}\|$			1.0	4.5	ns
t_{sk}	Channel-to-Channel Output Skew Time[1]	Same-direction channels		1.0	4.5	ns
t_r	Output Signal Rise Time	See Figure 9-1		2.5	4.0	ns
t_f	Output Signal Fall Time	See Figure 9-1		2.5	4.0	ns
t_{PHZ}	Disable Propagation Delay, High to High Impedance Output	See Figure 9-2		8	12	ns
t_{PLZ}	Disable Propagation Delay, Low to High Impedance Output			8	12	ns
t_{PZH}	Enable Propagation Delay, High Impedance to High Output			5	10	µs
t_{PZL}	Enable Propagation Delay, High Impedance to Low Output			10	20	ns
t_{DO}	Default Output Delay Time from Input Power Loss	See Figure 9-3		8	12	µs
t_{SU}	Start-up Time			15	40	µs

Note:

1. tsk is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.

8.10.3. Timing Characteristics at 2.5V

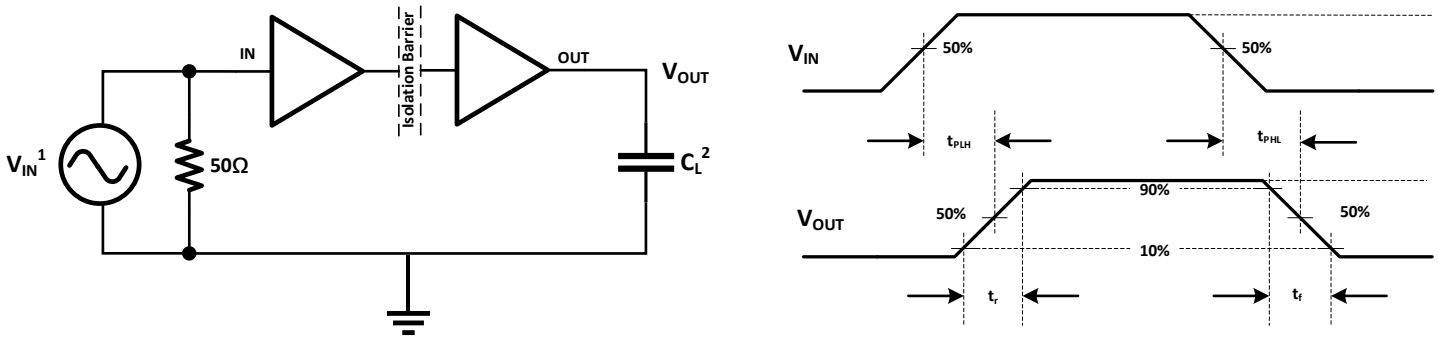
V_{DDA} = V_{DDB} = 2.5 V ± 10%, T_A = -40 to 125°C

Parameters		Test Conditions	MIN	TYP	MAX	UNIT
DR	Data Rate		0		10	Mbps
t_{PLH}, t_{PHL}	Propagation Delay Time	See Figure 9-1	5.0	10.0	15.0	ns
PWD	Pulse Width Distortion $\|t_{PLH} - t_{PHL}\|$			1.0	4.5	ns
t_{sk}	Channel-to-Channel Output Skew Time[1]	Same-direction channels		1.0	4.5	ns
t_r	Output Signal Rise Time	See Figure 9-1		2.5	4.0	ns
t_f	Output Signal Fall Time	See Figure 9-1		2.5	4.0	ns
t_{PHZ}	Disable Propagation Delay, High to High Impedance Output	See Figure 9-2		8	12	ns
t_{PLZ}	Disable Propagation Delay, Low to High Impedance Output			8	12	ns
t_{PZH}	Enable Propagation Delay, High Impedance to High Output			5	10	µs
t_{PZL}	Enable Propagation Delay, High Impedance to Low Output			10	20	ns
t_{DO}	Default Output Delay Time from Input Power Loss	See Figure 9-3		8	12	µs
t_{SU}	Start-up Time			15	40	µs

Note:

1. tsk is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.

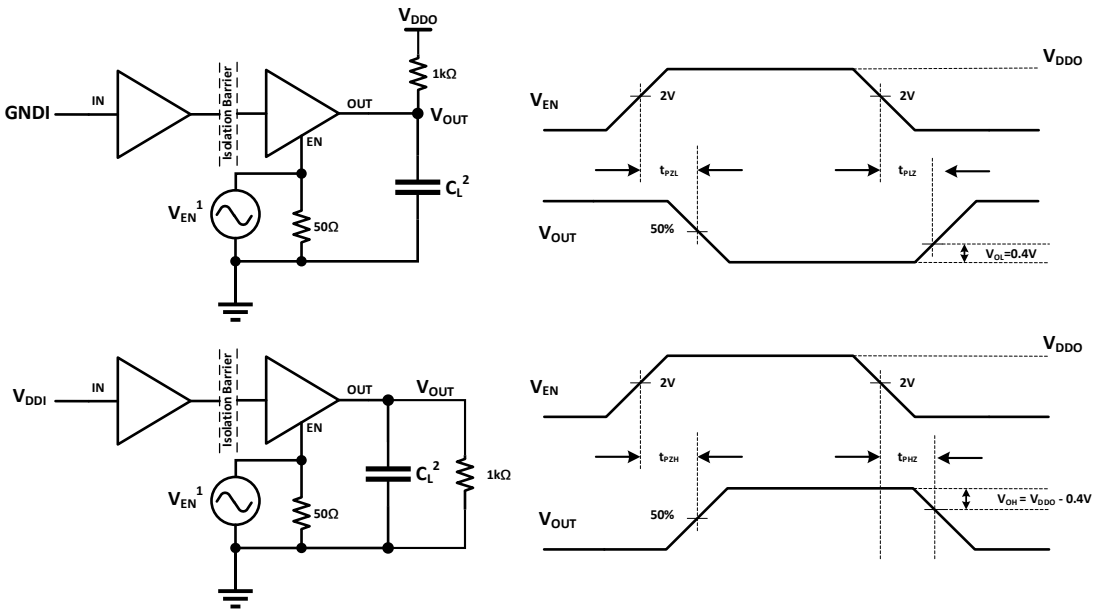
9. Parameter Measurement Information



Notes:

1. A square wave generator provide VIN input signal with characteristics: frequency ≤100kHz, 50% duty cycle, tr≤3ns, t_f≤3ns, Zout = 50Ω. At the input, 50 Ω resistor is required to terminate input generator signal. It is not needed in actual application.
2. C_L = 15pF and includes external circuit (instrumentation and fixture etc.) capacitance. Since the load capacitance influence the output rising time, it's a key factor in the timing characteristic measurement.

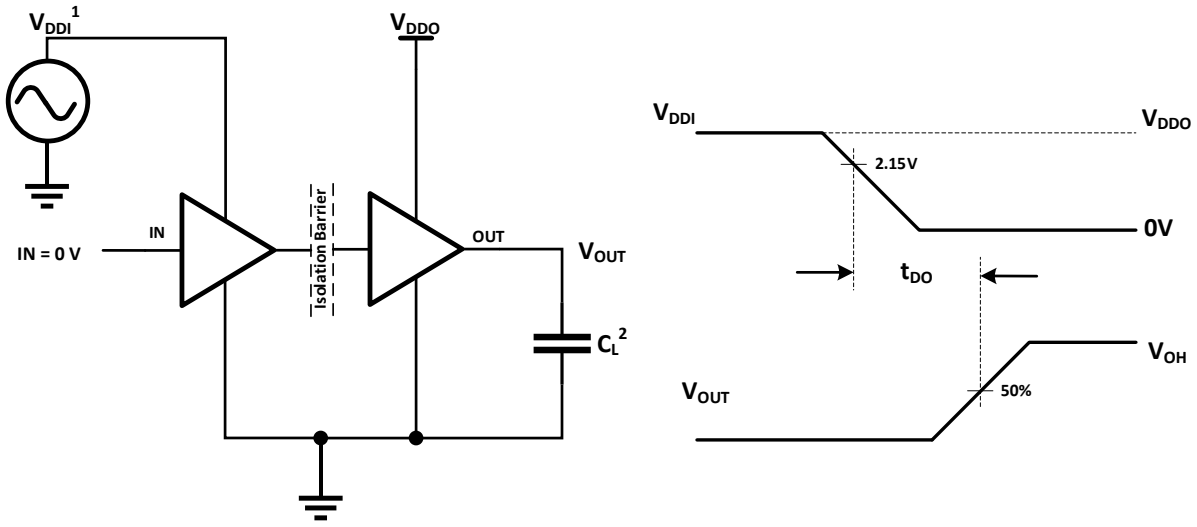
Figure 9-1. Switching Characteristics Test Circuit and Voltage Waveforms



Notes:

1. A square wave generator provide V_{IN} input signal with characteristics: frequency ≤10kHz, 50% duty cycle, t_r≤3ns, t_f≤3ns, Z_{out} = 50Ω. At the input, 50 Ω resistor is required to terminate input generator signal. It is not needed in actual application.
2. C_L = 15pF and includes external circuit (instrumentation and fixture etc.) capacitance. Since the load capacitance influence the output rising time, it's a key factor in the timing characteristic measurement.

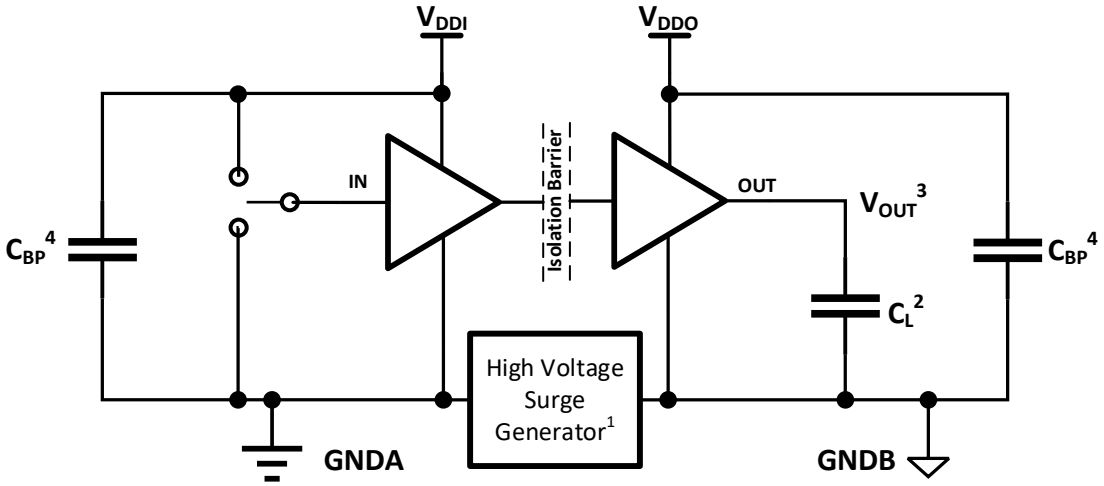
Figure 9-2. Enable/Disable Propagation Delay Time Test Circuit and Waveform



Notes:

1. Power Supply Ramp Rate = 10 mV/ns. V_{DDI} should ramp over 2.375V, and less than 5.5V.
2. C_L = 15pF and includes external circuit (instrumentation and fixture etc.) capacitance. Since the load capacitance influence the output rising time, it's a key factor in the timing characteristic measurement.

Figure 9-3. Default Output Delay Time Test Circuit and Voltage Waveforms



NOTE:

1. The High Voltage Surge Generator generates repetitive high voltage surges with > 1kV amplitude, rise time <10ns and fall time <10ns, to reach common-mode transient noise with > 150kV/μs slew rate.
2. C_L = 15pF and includes external circuit (instrumentation and fixture etc.) capacitance.
3. Pass-fail criteria: the output must remain stable.
4. C_{BP} (0.1 ~ 1uF) is bypass capacitance.

Figure 9-4. Common-Mode Transient Immunity Test Circuit

10. Detailed Description

10.1. Overview

The CA-IS3531 is three-channel digital galvanic isolator that incorporates advanced full differential capacitive isolation technology from Chipanalog to maximize the CMTI performance and minimize the radiated emissions due the high frequency carrier and IO buffer switching. These devices have an ON-OFF keying (OOK) modulation scheme to transfer digital signals across the SiO_2 based isolation barrier between circuits with different power domains. The transmitter sends a high frequency carrier across the barrier to represent one digital state and sends no signal to represent the other digital state. The receiver demodulates the signal and recovery input signal at output through a buffer stage. With this OOK architecture, the CA-IS3531 family of devices build a robust data transmission path between different power domains without any special start-up initialization requirements. All of devices in this family come with enable control pins. For the CA-IS3531HWPD, if EN_ pin is low then the corresponding driver output goes to high impedance; For the CA-IS3531HWPA, if EN_ pin is low then put the corresponding side into shutdown and place the driver output on corresponding side into high impedance.

10.2. Functional Block Diagram

The conceptual block diagram of a digital capacitive isolator, Figure 10-1, shows a functional block diagram of a typical channel; Figure 10-2 shows the operating waveform of a typical channel. Each channel of the CA-IS3531 is unidirectional, only passes data in one direction, as indicated in the functional diagram. Each device features three unidirectional channels that operate independently with guaranteed data rates from DC up to 10Mbps

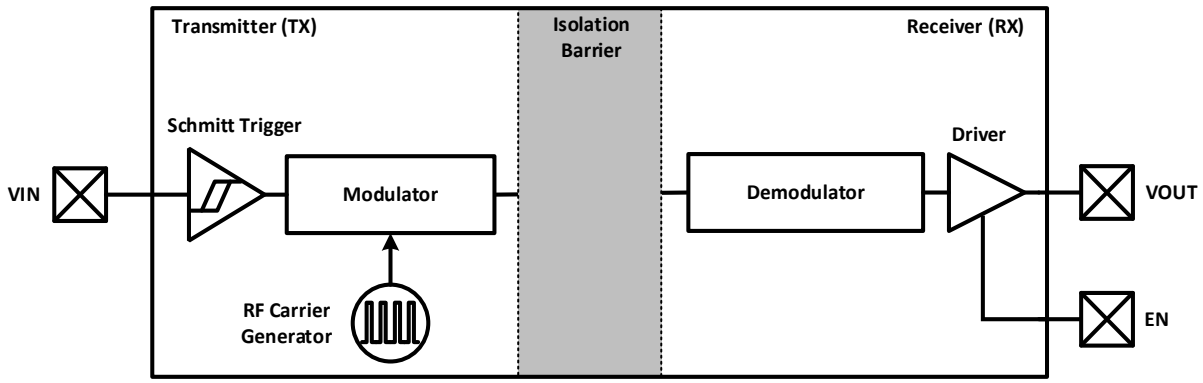


Figure 10-1. Functional Block Diagram of a Single Channel

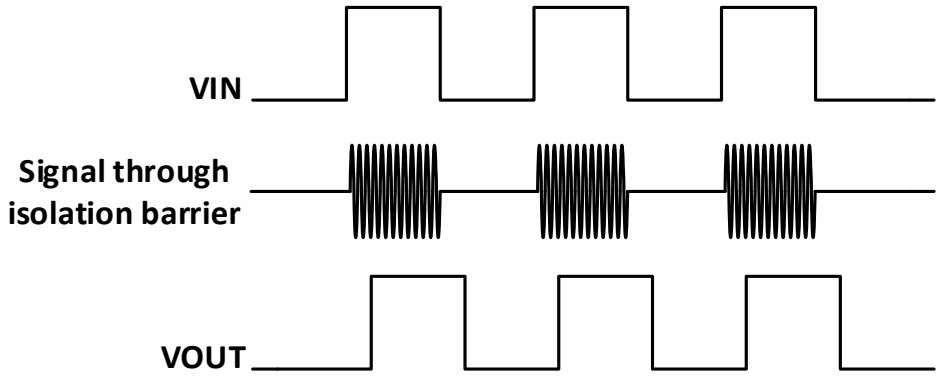


Figure 10-2. Conceptual Operation Waveforms of a Single Channel

10.3. Input and Output Equivalent Circuit

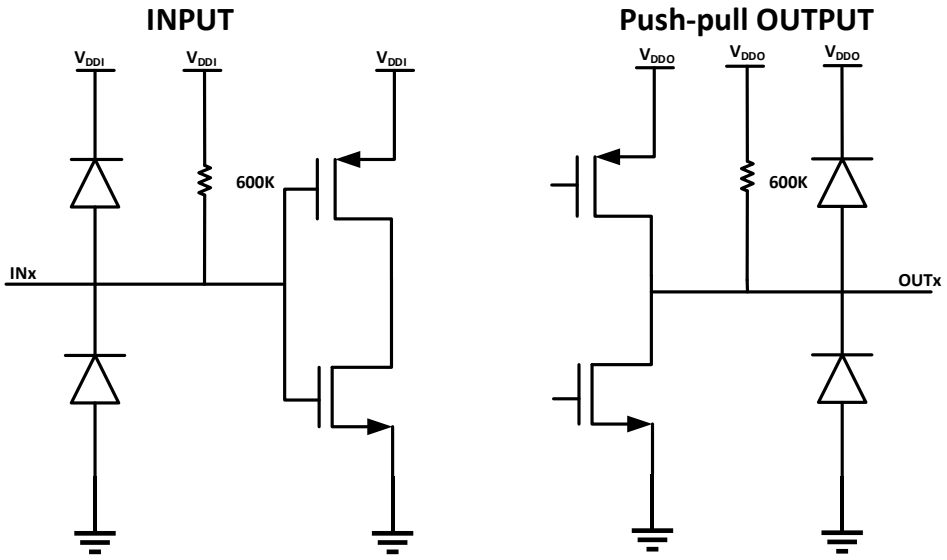


Figure 10-3. Input and output equivalent circuit

10.4. Device Operation Modes

Table 10-1 is the truth table for the CA-IS3531 devices. It shows the different operation modes with enable control input.

Table 10-1. Operation Mode Table

V_{DDI}[1]	V_{DDO}[1]	INPUT (VIx)[2]	ENABLE (EN_)[3]	OUTPUT (VOx)	OPERATION
PU	PU	H	H or open	H	Normal operation mode: Each channel output follows the logic state of its input.
		L	H or open	L	
		Open	H or open	Default	Default output mode: When input VIx is open, the corresponding channel output goes to its default logic state. Default is *High* for CA-IS3531HWPD and CA-IS3531HWPA.
X	PU	X	L	Z	High impedance mode: A low level of Enable pin causes the output to be high impedance.
PD	PU	X	H or open	Default	Default output mode: When VDDI is unpowered, a channel output assumes the logic state based on its default option. Default is *High* for CA-IS3531HWPD and CA-IS3531HWPA.
X	PD	X	X	Undetermined	If the output side V_{DDO} is unpowered, a channel output is undetermined.[4]

Notes:

1. V_{DDI} = Input-side V_{DD}; V_{DDO} = Output-side V_{DD}; PU = Powered up (V_{DD} ≥2.375); PD = Powered down (V_{DD} ≤2.24V); X = Irrelevant; H = High level; L = Low level; Z = High Impedance.
2. A strongly driven input signal can weakly power the floating V_{DD} through an internal protection diode and cause undetermined output.
3. It is recommended to connect the enable inputs to external logic high or low level when the CA-IS3531 operates in noisy environments.
4. The outputs are in undetermined state when $V_{DD(UVLO+)}$ > 2.25V, V_{DDO} < 2.375V.

Table 10-2 lists the operation modes under enable control input. The CA-IS3531 devices come with enable control on both side A and side B for the multi-master driving application, also the enable pins help to reduce system power consumption. The driver output on side A (or B) is enabled when ENA (or ENB) is high or floating; and the driver output on side A(or B) is in high-impedance state when ENA (or ENB) is low. See Table 10-2 for more details.

Table 10-2. Enable Control

PART NUMBER	ENA[1,2]	ENB[1,2]	STATUS
CA-IS3531HWPD	H	X	A-side output VO3 is enabled and follows the logic state of its input.
	L	X	A-side output VO3 is disabled and goes to high impedance state.
	X	H	B-side outputs VO1, VO2 are enabled and each output follows the logic state of its input.
	X	L	B-side outputs VO1, VO2 are disabled and go to high impedance state.
CA-IS3531HWPA	H	X	A-side circuit is enabled and each output on A-side follows the logic state of its input.
	L	X	A-side circuit is disabled and is placed into shutdown mode, each output on A-side goes to high impedance state.
	X	H	B-side circuit is enabled and each output on B-side follows the logic state of its input.
	X	L	B-side circuit is disabled and is placed into shutdown mode, each output on B-side goes to high impedance state.

Notes:

1. Enable inputs ENA and ENB can be used to put the respective outputs in high impedance for multi master driving applications, external clock synchronization etc. With internal pull-up resistors, these pins can be connected to logic high or left floating to enable the outputs. If ENA, ENB are unused, it is recommended to connect these pins to a logic level, especially in the noisy environment.

2. X = Irrelevant; H = High level; L = Low level.

11. Application and Implementation

11.1. Typical Operation Circuit

Isolation ICs provide complete galvanic isolation between two power domains, protecting circuits from high common-mode transients and faults, also eliminating ground loops. In many applications, the digital isolators, like CA-IS3531, are replacing optocouplers because they can reduce the power requirements and take up less board space while offering the same isolation capability. Unlike optocouplers, which require external components to improve performance, provide bias, or limit current, the CA-IS3531 only requires two external bypass capacitors to operate. To reduce ripple and the chance of introducing data errors, bypass VDDA and VDDB pins with 0.1μF to 1μF low-ESR ceramic capacitors to GNDA and GNDB, respectively. Place the bypass capacitors as close to the power supply input pins as possible. Figure 11-1 shows typical operating circuit of the CA-IS3531. The CA-IS3531 does not require special power supply sequencing and the output logic level is set independently on either side by V_{DDA} and V_{DDB} supply voltage.

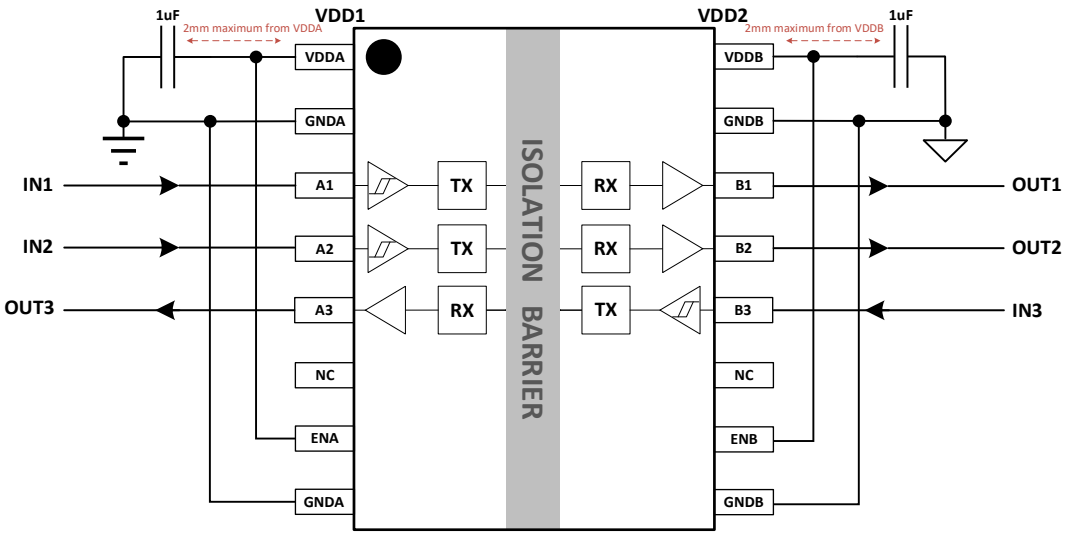


Figure 11-1. Typical Application Circuit of CA-IS3531

When designing with digital isolators, keep in mind that because of the single-ended design structure, digital isolators do not conform to any specific interface standard and are only intended for isolating single-ended CMOS or TTL digital signal lines. The isolator is typically placed between the data controller (that is, MCU or FPGA), and a data converter or a line transceiver, regardless of the interface type or standard. The PCB designer should follow some critical recommendations in order to get the best performance. For high-speed signal circuit boards, we recommend to use the standard FR4 PCB material and a minimum of four layers is required to accomplish a low EMI PCB design. Also, keep the input/output traces as short as possible, avoid using vias to make low-inductance paths for the signals. Keep the area underneath the digital isolator ICs free from ground and signal planes.

11.2. Typical Application in IR46 Smart Meters

According to the dual-chip electricity meter standard promoted by the State Grid, the next-generation dual-chip solution not only meets the requirements of smart grid but also meets the IR46 standard to achieve the independent operation of metering SOC and management MCU. It meets the new requirements of the State Grid meters, also takes into account the development of future (version 2.0) four-meter reading and data acquisition.

A key feature of dual-chip solution is high-speed data-rate. The highest communication baud rate has been increased to 115200bps from 9600bps. The traditional optocoupler can not support this requirement, so the high-speed digital isolator is ideal choice in this kind applications. The CA-IS35xx series of low-power, high-speed digital isolators are optimized for the next-generation smart meters, which is designed based on the new standards and requirements. Figure 11-2 shows the application block diagram in IR46 single-phase/three-phase smart meters for the CA-IS35xx family of digital isolators.

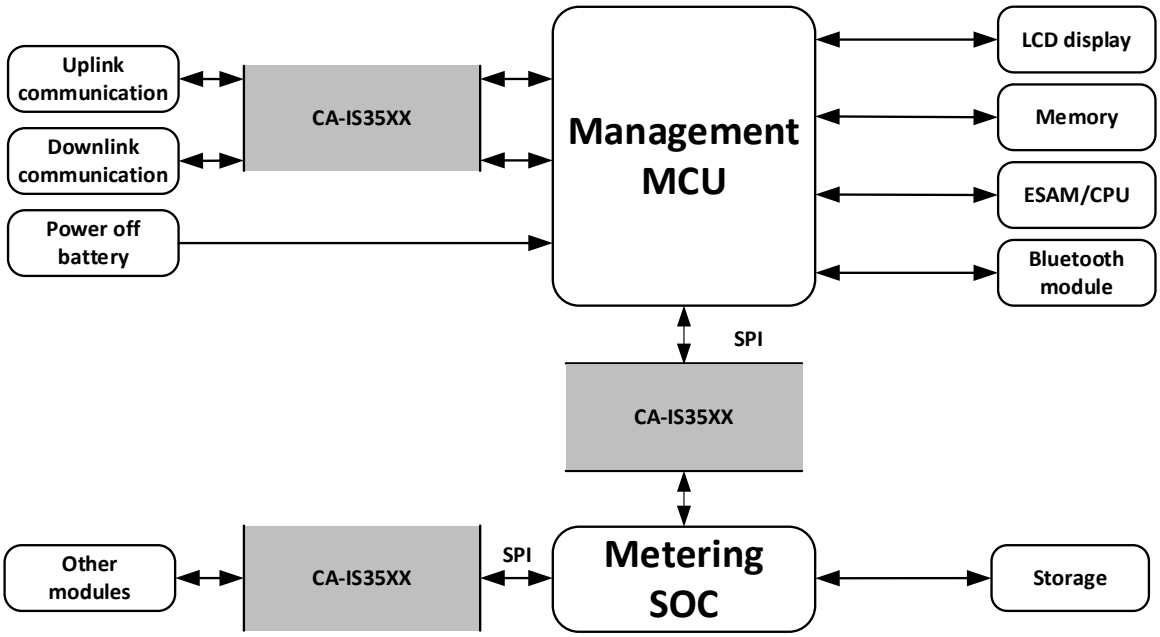
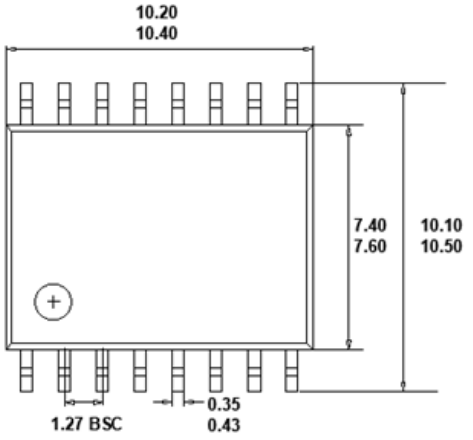


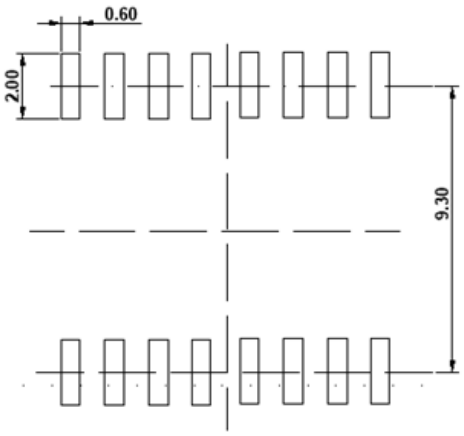
Figure 11-2. CA-IS35xxTypical Application Circuit in IR46 Single-phase/Polyphase Electricity Meters

12. Package Information

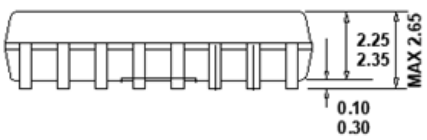
16-Pin Wide Body SOIC Package Outline



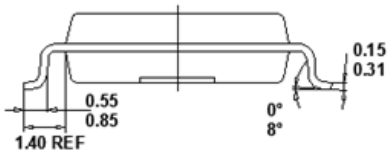
TOP VIEW



RECOMMMENDED LAND PATTERN



FRONT VIEW



LEFT SIDE VIEW

Note:

1. All dimensions are in millimeters, angles are in degrees.

13. Soldering Temperature (reflow) Profile

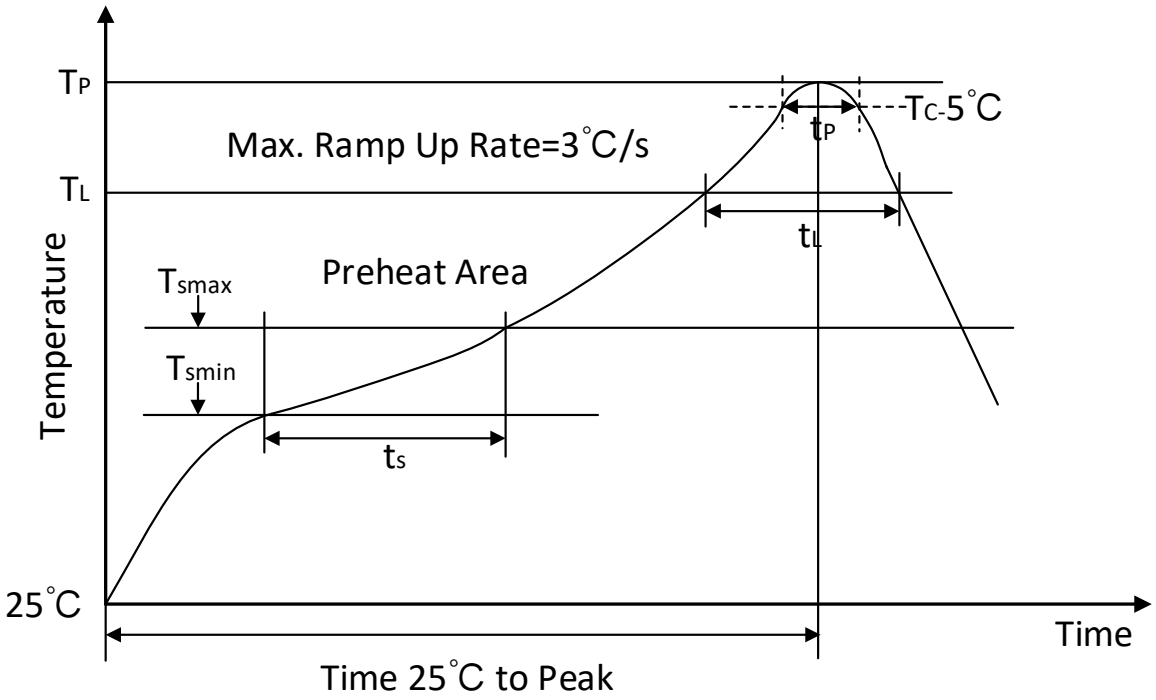


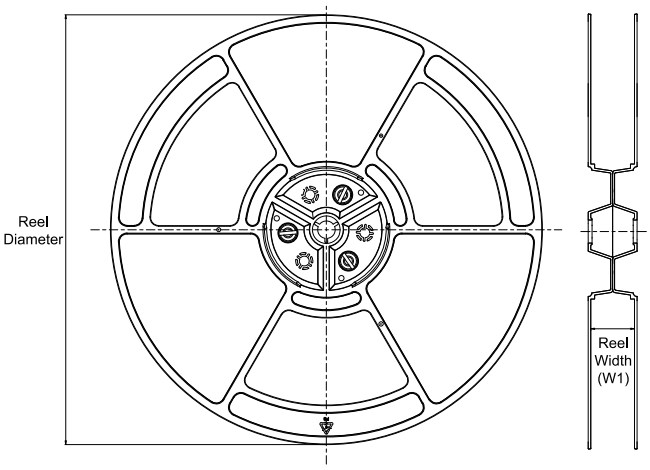
Figure. 13-1 Soldering Temperature (reflow) Profile

Tab. 13-1 Soldering Temperature Parameter

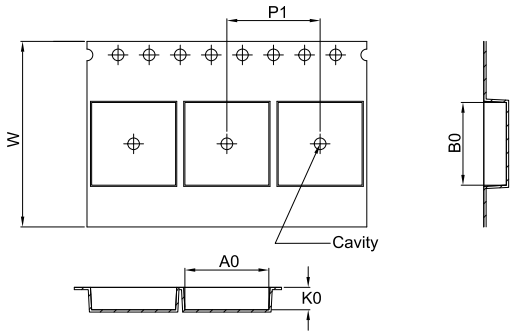
Profile Feature	Pb-Free Assembly
Average ramp-up rate(217 □ to Peak)	3□/second max
Time of Preheat temp(from 150 □ to 200 □	60-120 second
Time to be maintained above 217 □	60-150 second
Peak temperature	260 +5/-0 □
Time within 5 □of actual peak temp	30 second
Ramp-down rate	6 □/second max.
Time from 25□ to peak temp	8 minutes max

14. Tape and Reel Information

REEL DIMENSIONS

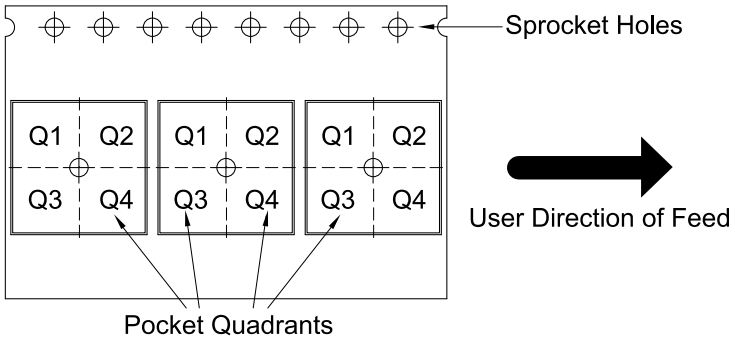


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CA-IS3531HWPD	SOIC	W	16	1000	330	16.4	10.9	10.7	3.2	12.0	16.0	Q1
CA-IS3531HWPA	SOIC	W	16	1000	330	16.4	10.9	10.7	3.2	12.0	16.0	Q1

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