

CA-IS3541 High-Speed Four-Channel Digital Isolators

1. Features

- **Meets IR46 Physical Layer Standards**
- **Data Rate is up to 10Mbps**
- **Robust Galvanic Isolation of Digital Signals**
 - High lifetime: >40 years
 - Up to 5.0kV_{RMS} isolation rating
 - ±150 kV/μs typical CMTI
 - ±8kV Human body model ESD protection
 - ±10 kV surge tolerant
 - Schmitt trigger inputs for high noise immunity
 - High electromagnetic immunity
- **Low Power Consumption**
 - 1.6mA per channel at 1Mbps with V_{DD} = 5.0V
 - 2.5mA per channel at 10Mbps with V_{DD} = 5.0V
 - Shutdown current is as low as 40 μA@5.0V
- **Best in Class Propagation Delay and Skew**
 - 10ns typical propagation delay
 - 1ns pulse width distortion
 - 2ns propagation delay skew (chip -to-chip)
- **Enable Control Input with Internal Pull-up**
- **2.375V to 5.5V Wide Operating Supply Voltage**
- **Wide Operating Temperature Range: -40°C to 125°C**
- **No Start-up Initialization Required**
- **Open-drain and Push-pull Output Options with Default Output High**
- **RoHS-Compliant Package:**
 - SOIC16(W) wide-body
- **Safety Regulatory Approvals**
 - VDE 0884-11 Reinforced Isolation (pending)
 - UL According to UL1577
 - IEC 62368-1, IEC 61010-1, GB 4943.1-2011 and GB 8898-2011 certifications

2. Applications

- Smart meters
- Data concentrators
- Circuit breakers

3. General Description

The CA-IS3541 is high-performance, low-power four-channel digital isolators specially developed for smart electricity meters (IR46). This family of devices features up to ±10kV surge tolerant and ±8kV HBM ESD protection. The digital isolator is based on Chipanalog's advanced isolation architecture with up to ±5kV_{RMS} isolation rating and ±150kV/μs CMTI, that provides a robust isolated data path between the different power domain and requires no special considerations or initialization at start-up. A simplified block diagram for a single CA-IS3541 channel is shown in the figure below.

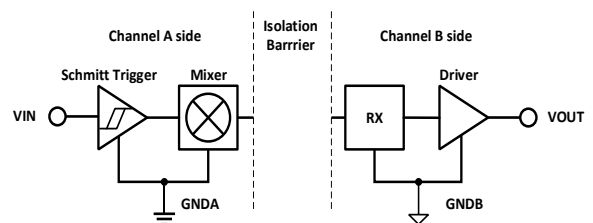
The CA-IS3541 has 3 forward and 1 reverse-direction channels. All of devices in this family come with enable control pins which can be used to put the driver outputs in high-impedance for the multi-master driving applications. Also, for the CA-IS3541HWPA and CA-IS3541HWDA, enable control inputs can be used to put the device into shutdown mode to reduce power consumption as low as 40μA. The CA-IS3541 devices provide open-drain and push-pull output options with default output high, that means when the input is either not powered or is open-circuit, the default output is high level.

The CA-IS3541 family devices are specified over the -40°C to +125°C operating temperature range. They are available in 16-pin SOIC wide body package.

Device information

Part number	Package	Package size (NOM)
CA-IS3541	SOIC16-WB(W)	10.30 mm × 7.50 mm

Simplified Channel Structure



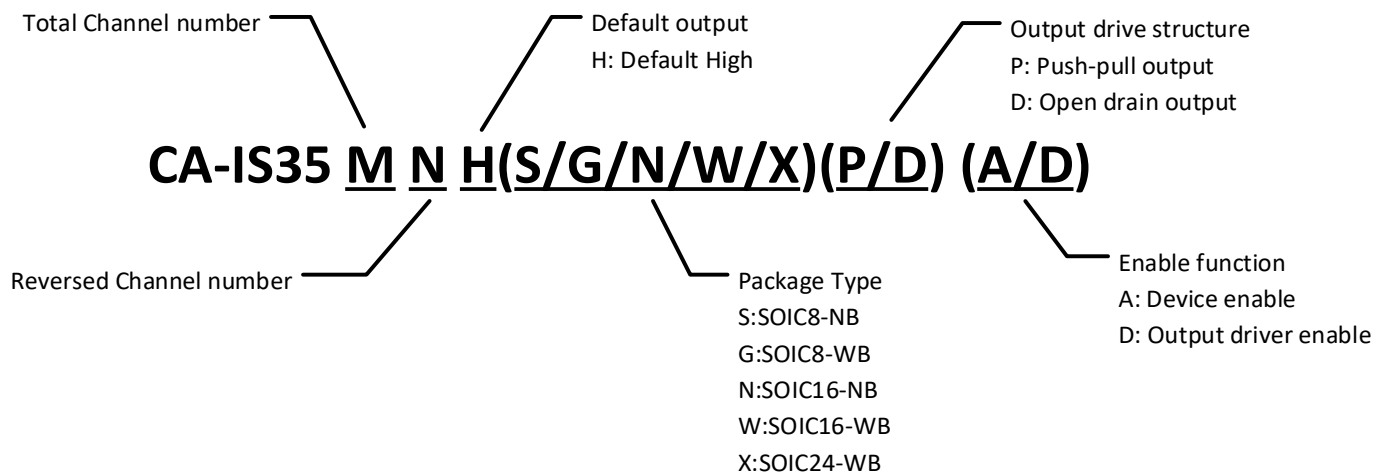
GND A and GND B are the isolated grounds for A side and B side respectively.

4. Ordering Information

Table 0-1. Ordering Information

Part Number	Number of Inputs A Side	Number of Inputs B Side	Output Type	Default Output	Isolation Rating (kV)	Output Enable	Package
CA-IS3541HWPD	3	1	Push-pull	High	5.0	Driver output enable control	SOIC16-WB
CA-IS3541HWPA	3	1	Push-pull	High	5.0	Device enable control	SOIC16-WB
CA-IS3541HWDD	3	1	Open-drain	High	5.0	Driver output enable control	SOIC16-WB
CA-IS3541HWDA	3	1	Open-drain	High	5.0	Device enable control	SOIC16-WB

5. Naming Rules

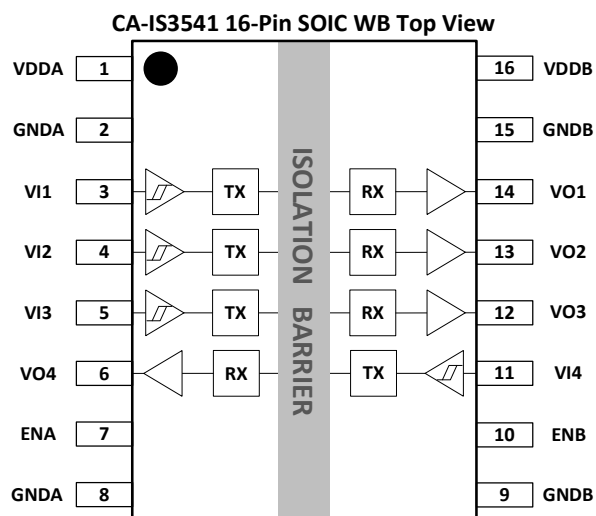


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6. Revision History

Revision Number	Description	Page Changed
Preliminary Version	Initial version	N/A
Version A	<ul style="list-style-type: none"> • Update Safety-Related Certifications • Update Electrical Characteristics, leakage current maximum value 	8 - 12
Version B	<ul style="list-style-type: none"> • Update part number 	2
Version C	<ul style="list-style-type: none"> • Changed tape data • Added Soldering Temperature (reflow) Profile information 	20 - 21
Version 1.00	Update document format	All
Version 1.01	Update POD	20

7. Pin Configuration and Functions

Figure 7-1. CA-IS3541 pin configuration
Table 7-1. CA-IS3541 pin description and function

CA-IS3541	Name	Type	Description
1	VDDA	Supply	Power supply for side A.
2, 8	GNDA	Ground	Ground reference for side A.
3	VI1	Digital I/O	Digital input 1 on side A, corresponds to logic output 1 on side B.
4	VI2	Digital I/O	Digital input 2 on side A, corresponds to logic output 2 on side B.
5	VI3	Digital I/O	Digital input 3 on side A, corresponds to logic output 3 on side B.
6	VO4	Digital I/O	Digital output 4 on side A, VO4 is the logic output for the VI4 input on side B.
7	ENA	Digital I/O	Enable control input for side A, see Table 10-2 for more details.
9, 15	GNDB	Ground	Ground reference for side B.
10	ENB	Digital I/O	Enable control input for side B, see Table 10-2 for more details.
11	VI4	Digital I/O	Digital input 4 on side B, corresponds to logic output 4 on side A.
12	VO3	Digital I/O	Digital output 3 on side B, VO3 is the logic output for the VI3 input on side A.
13	VO2	Digital I/O	Digital output 2 on side B, VO2 is the logic output for the VI2 input on side A.
14	VO1	Digital I/O	Digital output 1 on side B, VO1 is the logic output for the VI1 input on side A.
16	VDDDB	Supply	Power supply for side B.

8. Specifications

8.1. Absolute Maximum Ratings¹

Parameters		Minimum value	Maximum value	Unit
V_{DDA}, V_{DDB}	Power supply voltage ²	-0.5	7.0	V
V_{IN}	Input voltage at V_{Ix}, EN_x	-0.5	$V_{DDI}+0.5$ ³	V
I_O	Output current	-20	20	mA
T_J	Junction temperature	-40	150	°C
T_{STG}	Storage temperature range	-65	150	°C

Notes:

- The stresses listed under “Absolute Maximum Ratings” are stress ratings only, not for functional operation condition. Exposure to absolute maximum rating conditions for extended periods may cause permanent damage to the device.
- All voltage values are with respect to the local ground terminal (GNDA or GNDB) and are peak voltage values.
- Maximum voltage must not be exceed 7 V, $V_{DDI} =$ Input-side supply V_{DD} .

8.2. ESD Ratings

Parameters		Numerical value	Unit
V_{ESD} Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ¹	±8000	V
	Charged device model (CDM), per JEDEC Specification JESD22-C101, all pins ²	±2000	V

Notes:

- Per JEDEC document JEP155, 500V HBM allows safe manufacturing of standard ESD control process.
- JEDEC document JEP157, 250V HBM allows safe manufacturing of standard ESD control process.

8.3. Recommended Operating Conditions

Parameters		MIN	Type	MAX	Unit
V_{DDA}, V_{DDB}	Supply voltage on side A, B	2.375	3.30	5.50	V
$V_{DD} (UVLO+)$	V_{DD} Undervoltage-Lockout Threshold When Supply Voltage is Rising	1.95	2.24	2.375	V
$V_{DD} (UVLO-)$	V_{DD} Undervoltage-Lockout Threshold When Supply Voltage is Falling	1.88	2.10	2.325	V
$V_{HYS} (UVLO)$	V_{DD} Undervoltage-Lockout Threshold Hysteresis	70	140	250	mV
I_{OH}	High-level Output Current	$V_{DDO}^1 = 5V$	-4		mA
		$V_{DDO}^1 = 3.3V$	-2		
		$V_{DDO}^1 = 2.5V$	-1		
I_{OL}	Low-level Output Current	$V_{DDO}^1 = 5V$		4	mA
		$V_{DDO}^1 = 3.3V$		2	
		$V_{DDO}^1 = 2.5V$		1	
V_{IH}	High-level Input Voltage	2.0			V
V_{IL}	Low-level Input Voltage			0.8	V
DR	Data Rate	0		10	Mbps
T_A	Ambient Temperature	-40	27	125	°C

Note:

- $V_{DDO} =$ Output-side supply V_{DD} .

8.4. Thermal Information

Thermal Metric		CA-IS3541	Unit
		SOIC16-WB(W)	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	77.7	°C/W

8.5. Power Rating

Parameters		Test conditions	MIN	TYPE	MAX	Unit
CA-IS3541						
P_D	Maximum Power Dissipation	$V_{DDA} = V_{ddb} = 5.5 \text{ V}$, $C_L = 15 \text{ pF}$, $T_j = 150^\circ\text{C}$, Input a 75-MHz 50% duty cycle square wave.			65	mW
P_{DA}	Maximum Power Dissipation on Side-A				27	mW
P_{DB}	Maximum Power Dissipation on Side-B				38	mW

8.6. Insulation Specifications

Parameters		Test Conditions	Value	Unit
			W	
CLR	External clearance	Shortest terminal-to-terminal distance through air	8	mm
CPG	External creepage	Shortest terminal-to-terminal distance across the package surface	8	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	32	μm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	>600	V
	Material group	Per IEC 60664-1	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 300 V _{RMS}	I-IV	
		Rated mains voltage ≤ 400 V _{RMS}	I-IV	
		Rated mains voltage ≤ 600 V _{RMS}	I-III	
DIN V VDE V 0884-11:2017-01¹				
V _{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	849	V _{PK}
V _{IOWM}	Maximum operating isolation voltage	AC voltage; time-dependent dielectric breakdown (TDDB) test	600	V _{RMS}
		DC voltage	849	V _{DC}
V _{IOTM}	Maximum transient isolation voltage	V _{TEST} = V _{IOTM} , t = 60 s (certified); V _{TEST} = 1.2 × V _{IOTM} , t = 1 s (100% product test)	7070	V _{PK}
V _{IOSM}	Maximum surge isolation voltage ²	Test method per IEC 60065, 1.2/50 μs waveform, V _{TEST} = 1.6 × V _{IOSM} (production test)	6250	V _{PK}
Q _{pd}	Apparent charge ³	Method a, after input/output safety test of the subgroup 2/3, V _{ini} = V _{IOTM} , t _{ini} = 60 s; V _{pd(m)} = 1.2 × V _{IORM} , t _m = 10 s	≤5	pC
		Method a, after environmental test of the subgroup 1, V _{ini} = V _{IOTM} , t _{ini} = 60 s; V _{pd(m)} = 1.6 × V _{IORM} , t _m = 10 s	≤5	
		Method b, at routine test (100% production test) and preconditioning (type test) V _{ini} = 1.2 × V _{IOTM} , t _{ini} = 1 s; V _{pd(m)} = 1.875 × V _{IORM} , t _m = 1 s	≤5	
C _{IO}	Barrier capacitance, input to output ⁴	V _{IO} = 0.4 × sin(2πft), f = 1 MHz	~0.5	pF
R _{IO}	Isolation resistance ⁴	V _{IO} = 500 V, T _A = 25°C	>10 ¹²	Ω
		V _{IO} = 500 V, 100°C ≤ T _A ≤ 125°C	>10 ¹¹	
		V _{IO} = 500 V at T _S = 150°C	>10 ⁹	
	Pollution degree		2	
UL 1577				
V _{ISO}	Maximum withstanding isolation voltage	V _{TEST} = V _{ISO} , t = 60 s (qualification) V _{TEST} = 1.2 × V _{ISO} , t = 1 s (100% production test)	5000	V _{RMS}
Notes:				
1. This coupler is suitable for “safe electrical insulation” only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits. 2. Devices are immersed in oil during surge characterization. 3. The characterization charge is discharging charge (pd) caused by partial discharge. 4. Capacitance and resistance are measured with all pins on field-side and logic-side tied together.				

8.7. Safety-Related Certifications

VDE (pending)	UL	CQC	TUV
Certified according to DIN VDE V 0884-11:2017-01	Certified according to UL 1577 Component Recognition Program	Certified according to GB 4943.1-2011 and GB 8898-2011	Certified according to EN/IEC 61010-1:2010 (3rd Ed) and EN /IEC 62368-1:2014+A11:2017
Maximum transient isolation voltage: 7070V _{pk} (SOIC16-W)	SOP16-W: 5000 V _{RMS}	SOP16-W: Reinforced insulation, 1000 V _{RMS} maximum working voltage (Altitude ≤ 5000 m)	5000 V _{RMS} (SOP16-W) insulation per EN/IEC 61010-1:2010 (3rd Ed) and EN /IEC 62368-1:2014+A11:2017, working voltage is up to 1000 V _{RMS} (SOP16-W)
	Certificate number : E511334	Certificate number : SOP16-W: CQC20001251466	CB Certificate number: JPTUV-112091; DE 2-028028 AK Certificate number: AK 50476717 0001; AK 50476719 0001

8.8. Electrical Characteristics

8.8.1. Electrical Characteristics at 5.0V

 $V_{DDA} = V_{DDB} = 5\text{ V} \pm 10\%$, $T_A = -40$ to 125°C

Parameters	Test conditions	MIN	TYPE	MAX	UNIT
V_{OH}	High-level Output Voltage $I_{OH} = -4\text{mA}$; See Figure 9-2	$V_{DDO}^{1-0.4}$	4.8		V
V_{OL}	Low-level Output Voltage $I_{OL} = 4\text{mA}$; See Figure 9-2		0.2	0.4	V
$V_{IT+(IN)}$	Rising input switching threshold	1.4	1.7	1.9	V
$V_{IT-(IN)}$	Falling input switching threshold	1.0	1.3	1.5	V
$V_{I(HYS)}$	Input Threshold Hysteresis	0.30	0.44	0.50	V
I_{IH}	High-Level Input Leakage Current $V_{IH} = V_{DDA}$ at INx or ENx			20	μA
I_{IL}	Low-Level Input Leakage Current $V_{IL} = 0\text{ V}$ at INx	-20			μA
Z_O	Output Impedance ²		50		Ω
CMTI	Common-mode Transient Immunity $V_I = V_{DDI}^1$ or 0 V , $V_{CM} = 1200\text{ V}$; See Figure 9-4	100	150		$\text{kV}/\mu\text{s}$
C_i	Input Capacitance ³ $V_I = V_{DD}/2 + 0.4 \times \sin(2\pi ft)$, $f = 1\text{ MHz}$, $V_{DD} = 5\text{ V}$		2		pF

Notes:

- V_{DDI} = Input-side supply V_{DD} , V_{DDO} = Output-side supply V_{DD} .
- The nominal output impedance of each isolator driver is $50\ \Omega \pm 40\%$.
- Measured from pin to Ground.

8.8.2. Electrical Characteristics at 3.3V

 $V_{DDA} = V_{DDB} = 3.3\text{ V} \pm 10\%$, $T_A = -40$ to 125°C

Parameters	Test conditions	MIN	TYPE	MAX	UNIT
V_{OH}	High-level Output Voltage $I_{OH} = -4\text{mA}$; See Figure 9-2	$V_{DDO}^{1-0.4}$	3.1		V
V_{OL}	Low-level Output Voltage $I_{OL} = 4\text{mA}$; See Figure 9-2		0.2	0.4	V
$V_{IT+(IN)}$	Rising input switching threshold	1.4	1.7	1.9	V
$V_{IT-(IN)}$	Falling input switching threshold	1.0	1.3	1.5	V
$V_{I(HYS)}$	Input Threshold Hysteresis	0.30	0.44	0.50	V
I_{IH}	High-Level Input Leakage Current $V_{IH} = V_{DDA}$ at INx or ENx			20	μA
I_{IL}	Low-Level Input Leakage Current $V_{IL} = 0\text{ V}$ at INx	-20			μA
Z_O	Output Impedance ²		50		Ω
CMTI	Common-mode Transient Immunity $V_I = V_{DDI}^1$ or 0 V , $V_{CM} = 1200\text{ V}$; See Figure 9-4	100	150		$\text{kV}/\mu\text{s}$
C_i	Input Capacitance ³ $V_I = V_{DD}/2 + 0.4 \times \sin(2\pi ft)$, $f = 1\text{ MHz}$, $V_{DD} = 3.3\text{ V}$		2		pF

Notes:

- V_{DDI} = Input-side supply V_{DD} , V_{DDO} = Output-side supply V_{DD} .
- The nominal output impedance of each isolator driver is $50\ \Omega \pm 40\%$.
- Measured from pin to Ground.

8.8.3. Electrical Characteristics at 2.5V

 $V_{DDA} = V_{DDB} = 2.5\text{ V} \pm 10\%$, $T_A = -40$ to 125°C

Parameters	Test conditions	MIN	TYPE	MAX	UNIT
V_{OH}	High-level Output Voltage $I_{OH} = -4\text{mA}$; See Figure 9-2	$V_{DDO}^{1-0.4}$	2.3		V
V_{OL}	Low-level Output Voltage $I_{OL} = 4\text{mA}$; See Figure 9-2		0.2	0.4	V
$V_{IT+(IN)}$	Rising input switching threshold	1.4	1.7	1.9	V
$V_{IT-(IN)}$	Falling input switching threshold	1.0	1.3	1.5	V
$V_{I(HYS)}$	Input Threshold Hysteresis	0.30	0.44	0.50	V
I_{IH}	High-Level Input Leakage Current $V_{IH} = V_{DDA}$ at INx or ENx			20	μA
I_{IL}	Low-Level Input Leakage Current $V_{IL} = 0\text{ V}$ at INx	-20			μA
Z_O	Output Impedance ²		50		Ω
CMTI	Common-mode Transient Immunity $V_I = V_{DDI}^1$ or 0 V , $V_{CM} = 1200\text{ V}$; See Figure 9-4	100	150		$\text{kV}/\mu\text{s}$
C_i	Input Capacitance ³ $V_I = V_{DD}/2 + 0.4 \times \sin(2\pi ft)$, $f = 1\text{ MHz}$, $V_{DD} = 2.5\text{ V}$		2		pF

Notes:

- V_{DDI} = Input-side supply V_{DD} , V_{DDO} = Output-side supply V_{DD} .

2. The nominal output impedance of each isolator driver is $50\ \Omega \pm 40\%$.
3. Measured from pin to Ground.

8.9. Supply Current Characteristics

8.9.1. Supply Current Characteristics at 5.0V

 $V_{DDA} = V_{DDB} = 5\ \text{V} \pm 10\%$, $T_A = -40\ \text{to}\ 125^\circ\text{C}$

Parameters	Test Conditions	Supply Current	MIN	TYP	MAX	Unit
CA-IS3541						
Supply Current – Device shutdown	ENA = ENB = 0 V;	I_{DDA}	25	37	56	μA
		I_{DDB}	25	37	56	
Supply Current – Outputs disabled	ENA = ENB = 0 V; $V_{IN} = V_{DDI}^1$	I_{DDA}		1.7	2.9	mA
		I_{DDB}		2.5	3.9	
	ENA = ENB = 0 V; $V_{IN} = 0\text{V}$	I_{DDA}		5.5	7.2	
		I_{DDB}		3.8	5.4	
Supply Current – DC Signal	ENA = ENB = V_{DDI} ; $V_{IN} = V_{DDI}$	I_{DDA}		5.6	7.3	
		I_{DDB}		4.0	5.5	
	ENA = ENB = V_{DDI} ; $V_{IN} = 0\text{V}$	I_{DDA}		1.8	3.0	
		I_{DDB}		2.7	4.0	
Supply Current – AC Signal	ENA = ENB = V_{DDI} ; All Channels Switching with 50% Duty Cycle Square Wave Clock Input with 5V Amplitude; $C_L = 15\ \text{pF}$ for Each Channel.	1Mbps (500kHz)	I_{DDA}	3.7	6.2	
		I_{DDB}	3.7	6.2		
	10Mbps (5MHz)	I_{DDA}	4.5	7.5		
		I_{DDB}	6.0	9.9		
Note:						
1. V_{DDI} = Input-side supply voltage V_{DD} .						

8.9.2. Supply Current Characteristics at 3.3V

 $V_{DDA} = V_{DDB} = 3.3\ \text{V} \pm 10\%$, $T_A = -40\ \text{to}\ 125^\circ\text{C}$

Parameters	Test Conditions	Supply Current	MIN	TYP	MAX	Unit
CA-IS3541						
Supply Current – Device shutdown	ENA = ENB = 0 V;	I_{DDA}	10	15	23	μA
		I_{DDB}	10	15	23	
Supply Current – Outputs disabled	ENA = ENB = 0 V; $V_{IN} = V_{DDI}^1$	I_{DDA}		1.6	2.6	mA
		I_{DDB}		2.5	3.4	
	ENA = ENB = 0 V; $V_{IN} = 0\text{V}$	I_{DDA}		5.5	6.5	
		I_{DDB}		3.7	4.7	
Supply Current – DC Signal	ENA = ENB = V_{DDI} ; $V_{IN} = V_{DDI}$	I_{DDA}		1.7	2.6	
		I_{DDB}		2.6	3.5	
	ENA = ENB = V_{DDI} ; $V_{IN} = 0\text{V}$	I_{DDA}		5.5	6.5	
		I_{DDB}		4.0	4.8	
Supply Current – AC Signal	ENA=ENB = V_{DDI} ; All Channels Switching with 50% Duty Cycle Square Wave Clock Input with 3.3V Amplitude; $C_L = 15\ \text{pF}$ for Each Channel.	1Mbps (500kHz)	I_{DDA}	3.6	5.6	
		I_{DDB}	3.6	6.3		
	10Mbps (5MHz)	I_{DDA}	4.1	6.5		
		I_{DDB}	5.1	7.8		
Note:						
1. V_{DDI} = Input-side supply voltage V_{DD} .						

8.9.3. Supply Current Characteristics at 2.5V

 $V_{DDA} = V_{DDB} = 2.5\text{ V} \pm 10\%$, $T_A = -40\text{ to }125^\circ\text{C}$

Parameters	Test Conditions	Supply Current	MIN	TYP	MAX	Unit
CA-IS3541						
Supply Current – Device shutdown	ENA = ENB = 0 V;	I_{DDA}	5	7.4	12	μA
		I_{DDB}	5	7.4	12	
Supply Current – Disable	ENA = ENB = 0 V; $V_{IN} = V_{DDI}^1$	I_{DDA}		1.6	2.9	mA
		I_{DDB}		2.5	3.9	
	ENA = ENB = 0 V; $V_{IN} = 0\text{V}$	I_{DDA}		5.4	7.2	
		I_{DDB}		3.7	5.4	
Supply Current – DC Signal	ENA = ENB = V_{DDI} ; $V_{IN} = V_{DDI}$	I_{DDA}		5.5	7.3	mA
		I_{DDB}		3.8	5.5	
	ENA = ENB = V_{DDI} ; $V_{IN} = 0\text{V}$	I_{DDA}		1.7	3.0	
		I_{DDB}		2.6	4.0	
Supply Current – AC Signal	ENA=ENB = V_{DDI} ; All Channels Switching with 50% Duty Cycle Square Wave Clock Input with 2.5V Amplitude; CL = 15 pF for Each Channel.	1Mbps (500kHz)		1.5	4.7	mA
		I_{DDB}		2.5	5.3	
	10Mbps (5MHz)	I_{DDA}		1.6	5.4	
		I_{DDB}		3.8	6.5	
Note:						
1. V_{DDI} = Input-side supply V_{DD} .						

8.10. Timing Characteristics

8.10.1. Timing Characteristics at 5.0V

 $V_{DDA} = V_{DDB} = 5\text{ V} \pm 10\%$, $T_A = -40\text{ to }125^\circ\text{C}$

Parameters	Test Conditions	MIN	TYP	MAX	UNIT
DR Data Rate		0		10	Mbps
t_{PLH} , t_{PHL} Propagation Delay Time	See Figure 9-1	5.0	8.0	15.0	ns
PWD Pulse Width Distortion $ t_{PLH} - t_{PHL} $			0.2	4.5	ns
t_{sk} Channel-to-Channel Output Skew Time ¹	Same-direction channels		0.4	4.5	ns
t_r Output Signal Rise Time	See Figure 9-1		2.5	4.0	ns
t_f Output Signal Fall Time	See Figure 9-1		2.5	4.0	ns
t_{PHZ} Disable Propagation Delay, High to High Impedance Output	See Figure 9-2		8	13	ns
t_{PLZ} Disable Propagation Delay, Low to High Impedance Output			8	17	ns
t_{PZH} Enable Propagation Delay, High Impedance to High Output			15	30	μs
t_{PZL} Enable Propagation Delay, High Impedance to Low Output			15	30	ns
t_{DO} Default Output Delay Time from Input Power Loss	See Figure 9-3		8	12	μs
t_{SU} Start-up Time			15	40	μs
Note:					
1. t_{sk} is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.					

8.10.2. Timing Characteristics at 3.3V
 $V_{DDA} = V_{DDB} = 3.3\text{ V} \pm 10\%$, $T_A = -40\text{ to }125^\circ\text{C}$

Parameters		Test Conditions	MIN	TYP	MAX	UNIT
DR	Data Rate		0		10	Mbps
t_{PLH} , t_{PHL}	Propagation Delay Time	See Figure 9-1	5.0	8.0	13.0	ns
PWD	Pulse Width Distortion $ t_{PLH} - t_{PHL} $			0.2	4.5	ns
t_{sk}	Channel-to-Channel Output Skew Time ¹	Same-direction channels		0.4	4.5	ns
t_r	Output Signal Rise Time	See Figure 9-1		2.5	4.0	ns
t_f	Output Signal Fall Time	See Figure 9-1		2.5	4.0	ns
t_{PHZ}	Disable Propagation Delay, High to High Impedance Output	See Figure 9-2		12	19	ns
t_{PLZ}	Disable Propagation Delay, Low to High Impedance Output			14	26	ns
t_{PZH}	Enable Propagation Delay, High Impedance to High Output			8	15	μs
t_{PZL}	Enable Propagation Delay, High Impedance to Low Output			10	20	ns
t_{DO}	Default Output Delay Time from Input Power Loss	See Figure 9-3		8	12	μs
t_{SU}	Start-up Time			15	40	μs

Note:

1. t_{sk} is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.

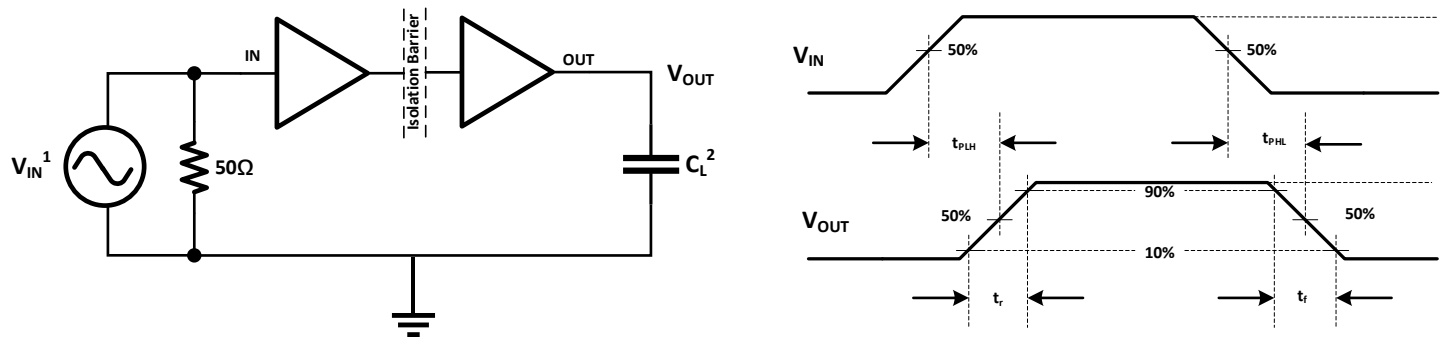
8.10.3. Timing Characteristics at 2.5V
 $V_{DDA} = V_{DDB} = 2.5\text{ V} \pm 10\%$, $T_A = -40\text{ to }125^\circ\text{C}$

Parameters		Test Conditions	MIN	TYP	MAX	UNIT
DR	Data Rate		0		10	Mbps
t_{PLH} , t_{PHL}	Propagation Delay Time	See Figure 9-1	5.0	8.0	13.0	ns
PWD	Pulse Width Distortion $ t_{PLH} - t_{PHL} $				0.2	5.0
t_{sk}	Channel-to-Channel Output Skew Time ¹	Same-direction channels		0.4	2.5	ns
t_r	Output Signal Rise Time	See Figure 9-1		2.5	4.0	ns
t_f	Output Signal Fall Time	See Figure 9-1		2.5	4.0	ns
t_{PHZ}	Disable Propagation Delay, High to High Impedance Output	See Figure 9-2		16	26	ns
t_{PLZ}	Disable Propagation Delay, Low to High Impedance Output			16	26	ns
t_{PZH}	Enable Propagation Delay, High Impedance to High Output			10	20	μs
t_{PZL}	Enable Propagation Delay, High Impedance to Low Output			10	20	ns
t_{DO}	Default Output Delay Time from Input Power Loss	See Figure 9-3		8	12	μs
t_{SU}	Start-up Time			15	40	μs

Note:

1. t_{sk} is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.

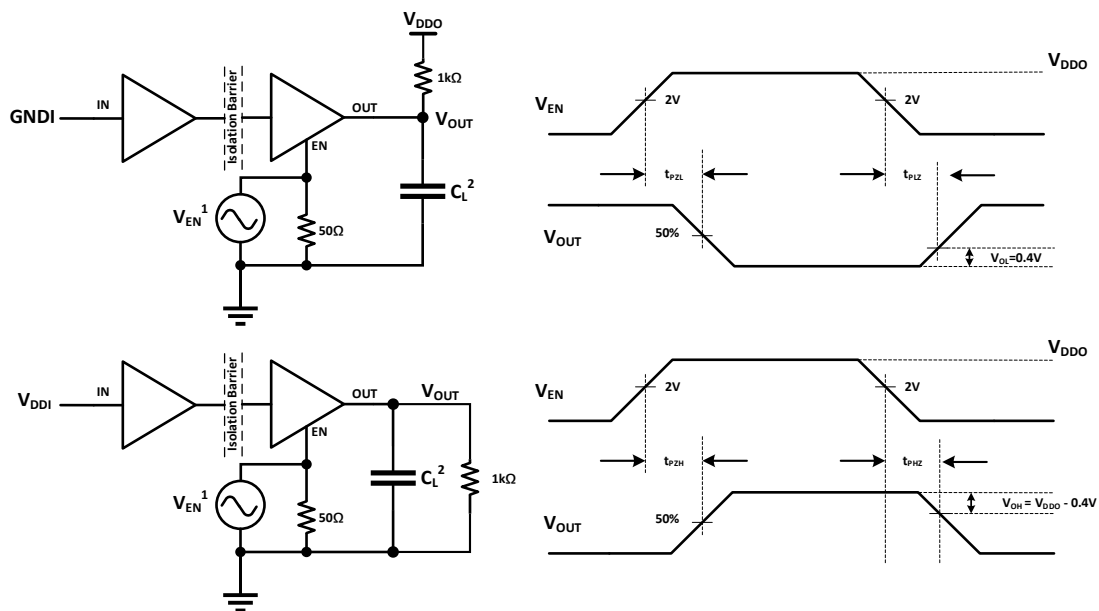
9. Parameter Measurement Information



Notes:

1. A square wave generator provide V_{IN} input signal with characteristics: frequency $\leq 100\text{kHz}$, 50% duty cycle, $t_r \leq 3\text{ns}$, $t_f \leq 3\text{ns}$, $Z_{out} = 50\Omega$. At the input, 50Ω resistor is required to terminate input generator signal. It is not needed in actual application.
2. $C_L = 15\text{pF}$ and includes external circuit (instrumentation and fixture etc.) capacitance. Since the load capacitance influence the output rising time, it's a key factor in the timing characteristic measurement.

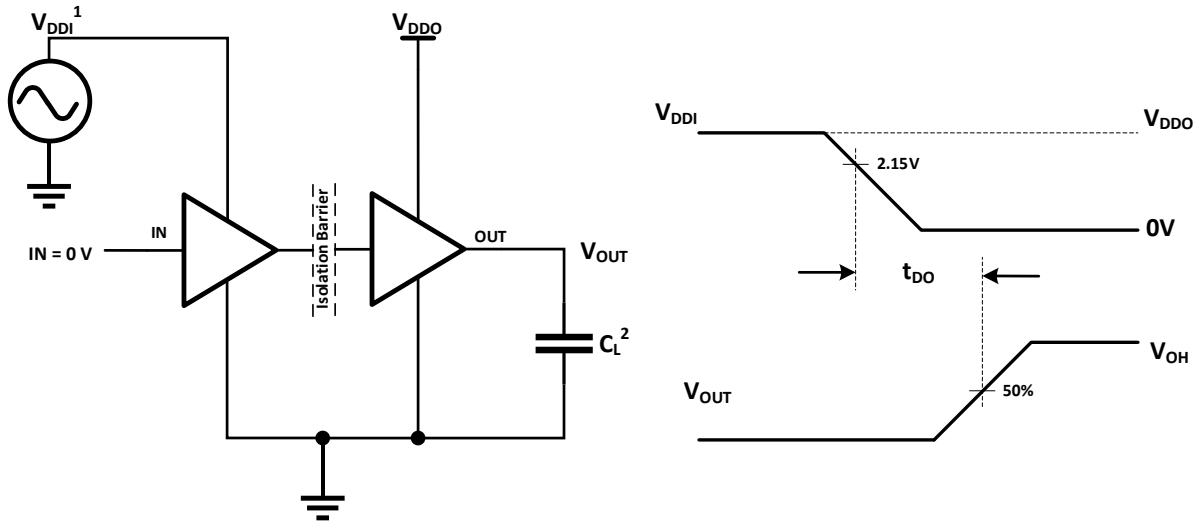
Figure 9-1. Switching Characteristics Test Circuit and Voltage Waveforms



Notes:

1. A square wave generator provide V_{IN} input signal with characteristics: frequency $\leq 10\text{kHz}$, 50% duty cycle, $t_r \leq 3\text{ns}$, $t_f \leq 3\text{ns}$, $Z_{out} = 50\Omega$. At the input, 50Ω resistor is required to terminate input generator signal. It is not needed in actual application.
2. $C_L = 15\text{pF}$ and includes external circuit (instrumentation and fixture etc.) capacitance. Since the load capacitance influence the output rising time, it's a key factor in the timing characteristic measurement.

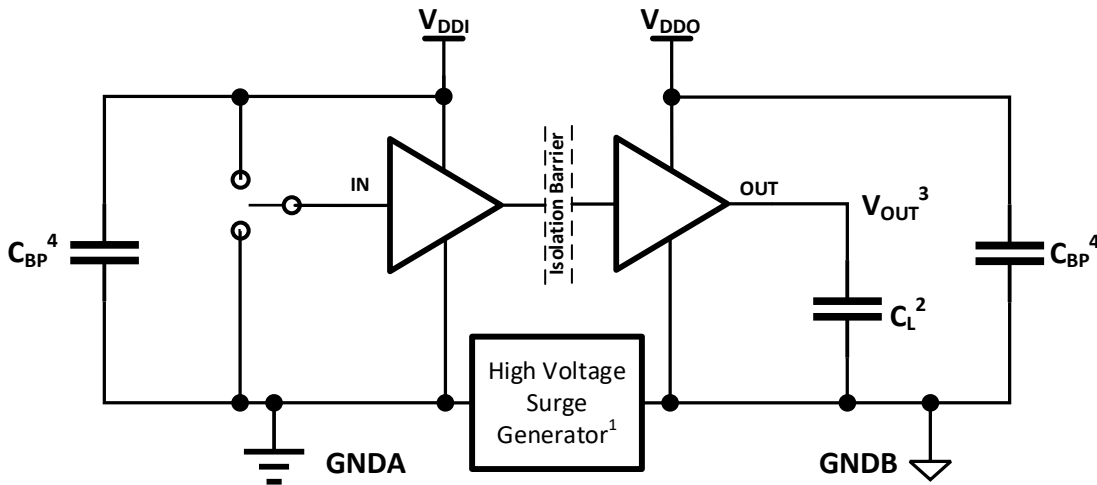
Figure 9-2. Enable/Disable Propagation Delay Time Test Circuit and Waveform



Notes:

1. Power Supply Ramp Rate = 10 mV/ns. V_{DD1} should ramp over 2.375V, and less than 5.5V.
2. C_L = 15pF and includes external circuit (instrumentation and fixture etc.) capacitance. Since the load capacitance influence the output rising time, it's a key factor in the timing characteristic measurement.

Figure 9-3. Default Output Delay Time Test Circuit and Voltage Waveforms



NOTE:

1. The High Voltage Surge Generator generates repetitive high voltage surges with > 1kV amplitude, rise time <10ns and fall time <10ns, to reach common-mode transient noise with > 150kV/ μ s slew rate.
2. C_L = 15pF and includes external circuit (instrumentation and fixture etc.) capacitance.
3. Pass-fail criteria: the output must remain stable.
4. C_{BP} (0.1 ~ 1uF) is bypass capacitance.

Figure 9-4. Common-Mode Transient Immunity Test Circuit

10. Detailed Description

10.1. Overview

The CA-IS3541 is four-channel digital galvanic isolator that incorporates advanced full differential capacitive isolation technology from Chipanalog to maximize the CMTI performance and minimize the radiated emissions due the high frequency carrier and IO buffer switching. These devices have an ON-OFF keying (OOK) modulation scheme to transfer digital signals across the SiO₂ based isolation barrier between circuits with different power domains. The transmitter sends a high frequency carrier across the barrier to represent one digital state and sends no signal to represent the other digital state. The receiver demodulates the signal and recovery input signal at output through a buffer stage. With this OOK architecture, the CA-IS3541 family of devices builds a robust data transmission path between different power domains without any special start-up initialization requirements. All of devices in this family come with enable control pins. For the CA-IS3541HWPD/CA-IS3541HWDD, if EN_ pin is low then the corresponding driver output goes to high impedance; For the CA-IS3541HWPA/CA-IS3541HWDA, if EN_ pin is low then put the corresponding side into shutdown mode and place the driver output on corresponding side into high impedance.

10.2. Functional Block Diagram

The conceptual block diagram of a digital capacitive isolator, Figure 10-1, shows a functional block diagram of a typical channel; Figure 10-2 shows the operating waveform of a typical channel. Each channel of the CA-IS3541 is unidirectional, only passes data in one direction, as indicated in the functional diagram. Each device features four unidirectional channels that operate independently with guaranteed data rates from DC up to 10Mbps

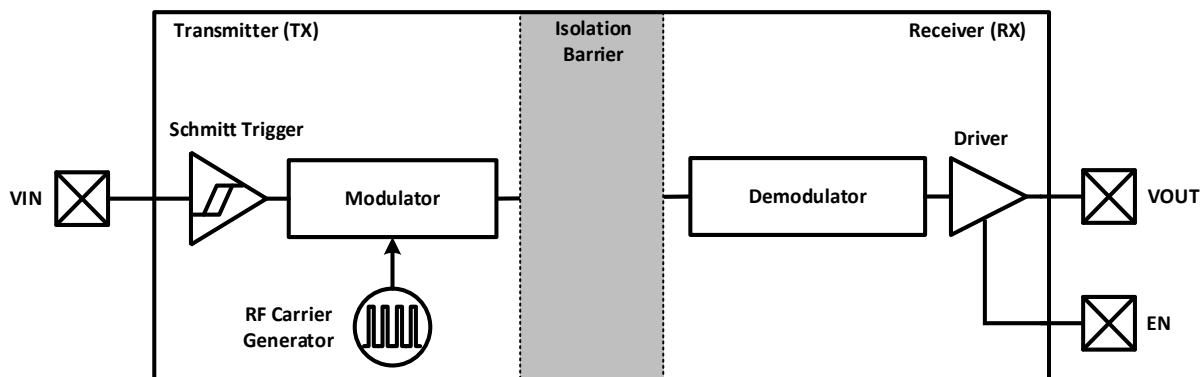


Figure 10-1. Functional Block Diagram of a Single Channel

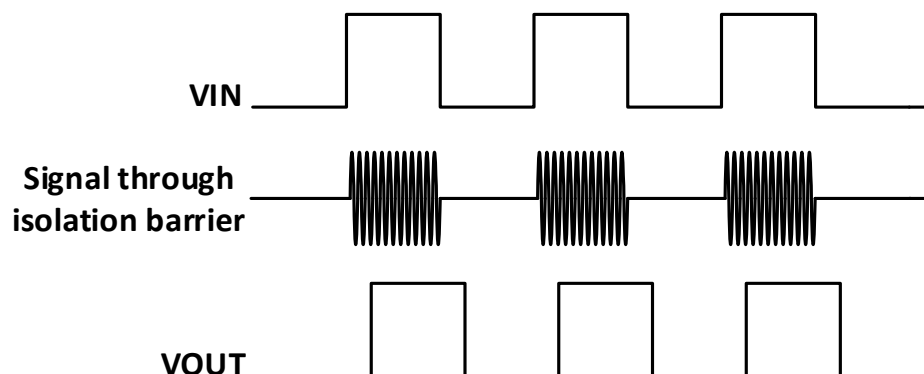


Figure 10-2. Conceptual Operation Waveforms of a Single Channel

10.3. Input and Output Equivalent Circuit

The CA-IS3541 provides different output options. The CA-IS3541HWDD/CA-IS3541HWDA features open-drain output and the CA-IS3541HWPD/CA-IS3541HWPA features push-pull output. See the Ordering Information and Naming Rules for suffixes associated with each option.

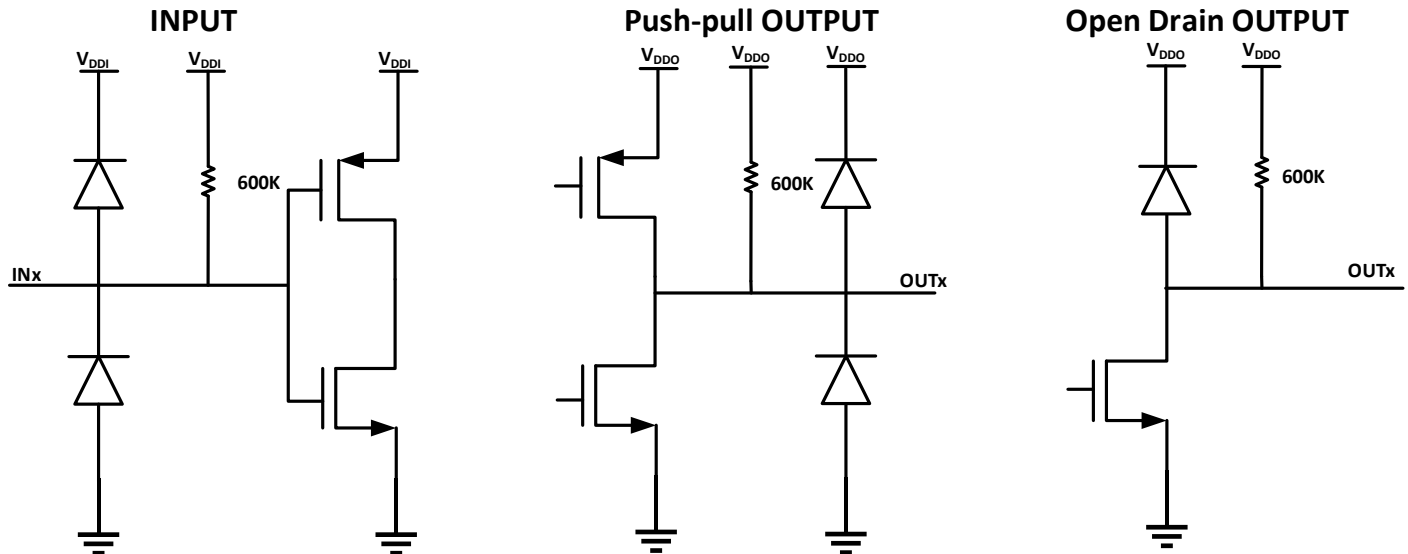

Figure 10-3. Input and output equivalent circuit
10.4. Device Operation Modes

Table 10-1 is the truth table for the CA-IS3541 devices. It shows the different operation modes with enable control input.

Table 10-1. Operation Mode Table

V_{DDI}^1	V_{DDO}^1	INPUT (V_{Ix}) ²	ENABLE ($EN_$) ³	OUTPUT (VOx)	OPERATION
PU	PU	H	H or open	H	Normal operation mode: Each channel output follows the logic state of its input.
		L	H or open	L	
		Open	H or open	Default	Default output mode: When input V_{Ix} is open, the corresponding channel output goes to its default logic state. Default is <i>High</i> for the CA-IS3541HWPD/CA-IS3541HWDD/CA-IS3541HWPA/CA-IS3541HWDA.
X	PU	X	L	Z	High impedance mode: A low level of Enable pin causes the output to be high impedance.
PD	PU	X	H or open	Default	Default output mode: When V_{DDI} is unpowered, a channel output assumes the logic state based on its default option. Default is <i>High</i> for the CA-IS3541HWPD/CA-IS3541HWDD/CA-IS3541HWPA/CA-IS3541HWDA.
X	PD	X	X	Undetermined	If the output side V_{DDO} is unpowered, a channel output is undetermined. ⁴

Notes:

- V_{DDI} = Input-side V_{DD} ; V_{DDO} = Output-side V_{DD} ; PU = Powered up ($V_{DD} \geq 2.375$); PD = Powered down ($V_{DD} \leq 2.24V$); X = Irrelevant; H = High level; L = Low level; Z = High Impedance.
- A strongly driven input signal can weakly power the floating V_{DD} through an internal protection diode and cause undetermined output.
- It is recommended to connect the enable inputs to external logic high or low level when the CA-IS3541 operates in noisy environments.
- The outputs are in undetermined state when $V_{DD(UVLO+)} > 2.25V$, $V_{DDO} < 2.375V$.

Table 10-2 lists the operation modes under enable control input. The CA-IS3541 devices come with enable control on both side A and side B for the multi-master driving application, also reduce system power consumption. The driver output on side A (or B) is enabled when ENA (or ENB) is high or floating; and the driver output on side A(or B) is in high-impedance state when ENA (or ENB) is low. See Table 10-2 for more details.

Table 10-2. Enable Control

PART NUMBER	ENA ^{1,2}	ENB ^{1,2}	STATUS
CA-IS3541HWPD	H	X	A-side output VO4 is enabled and follows the logic state of its input.
	L	X	A-side output VO4 is disabled and goes to high impedance state.
CA-IS3541HWDD	X	H	B-side outputs VO1, VO2 and VO3 are enabled and each output follows the logic state of its input.
	X	L	B-side outputs VO1, VO2 and VO3 are disabled and go to high impedance state.
CA-IS3541HWPA	H	X	A-side circuit is enabled and each output on A-side follows the logic state of its input.
	L	X	A-side circuit is disabled and is placed into shutdown mode, each output on A-side goes to high impedance state.
CA-IS3541HWDA	X	H	B-side circuit is enabled and each output on B-side follows the logic state of its input.
	X	L	B-side circuit is disabled and is placed into shutdown mode, each output on B-side goes to high impedance state.

Notes:

1. Enable inputs ENA and ENB can be used to put the respective outputs in high impedance for multi master driving applications, external clock synchronization etc. With internal pull-up resistors, these pins can be connected to logic high or left floating to enable the outputs. If ENA, ENB are unused, it is recommended to connect these pins to a logic level, especially in the noisy environment.
2. X = Irrelevant; H = High level; L = Low level.

11. Application and Implementation

11.1. Typical Operation Circuit

Isolation ICs provide complete galvanic isolation between two power domains, protecting circuits from high common-mode transients and faults, also eliminating ground loops. In many applications, the digital isolators, like CA-IS3541, are replacing optocouplers because they can reduce the power requirements and take up less board space while offering the same isolation capability. Unlike optocouplers, which require external components to improve performance, provide bias, or limit current, the CA-IS3541 only requires two external bypass capacitors to operate. To reduce ripple and the chance of introducing data errors, bypass VDDA and VDDB pins with 0.1 μ F to 1 μ F low-ESR ceramic capacitors to GNDA and GNDB, respectively. Place the bypass capacitors as close to the power supply input pins as possible. Figure 11-1 shows typical operating circuit of the CA-IS3541. The CA-IS3541 does not require special power supply sequencing and the output logic level is set independently on either side by VDDA and VDDB supply voltage.

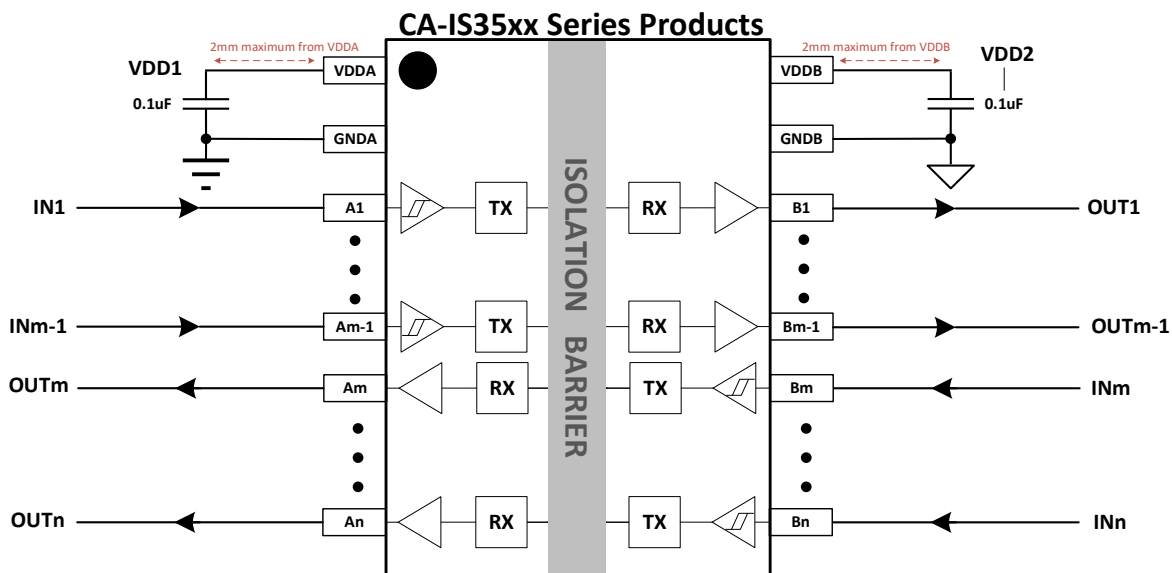


Figure 11-1. Typical Application Circuit of CA-IS3541

When designing with digital isolators, keep in mind that because of the single-ended design structure, digital isolators do not conform to any specific interface standard and are only intended for isolating single-ended CMOS or TTL digital signal lines. The isolator is typically placed between the data controller (that is, MCU or FPGA), and a data converter or communication bus interface, regardless of the interface type or standard. The PCB designer should follow some critical recommendations in order to get the best performance. For high-speed signal circuit boards, we recommend to use the standard FR4 PCB material and a minimum of four layers is required to accomplish a low EMI PCB design. Also, keep the input/output traces as short as possible, avoid using vias to make low-inductance paths for the signals. Keep the area underneath the digital isolator ICs free from ground and signal planes.

11.2. Typical Application in IR46 Smart Meters

According to the dual-chip electricity meter standard promoted by China State Grid, the next-generation dual-chip solution not only meets the requirements of smart grid but also meets the IR46 standard to achieve the independent operation of metering SoC and management MCU. It meets the new requirements of the State Grid meters, also takes into account the development of future (version 2.0) four-meter reading and data acquisition.

A key feature of dual-chip solution is high-speed data-rate. The highest communication baud rate has been increased to 115,200bps from 9,600bps. The traditional optocoupler can not support this requirement, so the high-speed digital isolator is ideal choice in this kind applications. The CA-IS35xx series of low-power, high-speed digital isolators are optimized for the next-generation smart meters, which is designed based on the new standards and requirements. Figure 11-2 shows the application block diagram in IR46 single-phase/three-phase smart meters for the CA-IS35xx family of digital isolators.

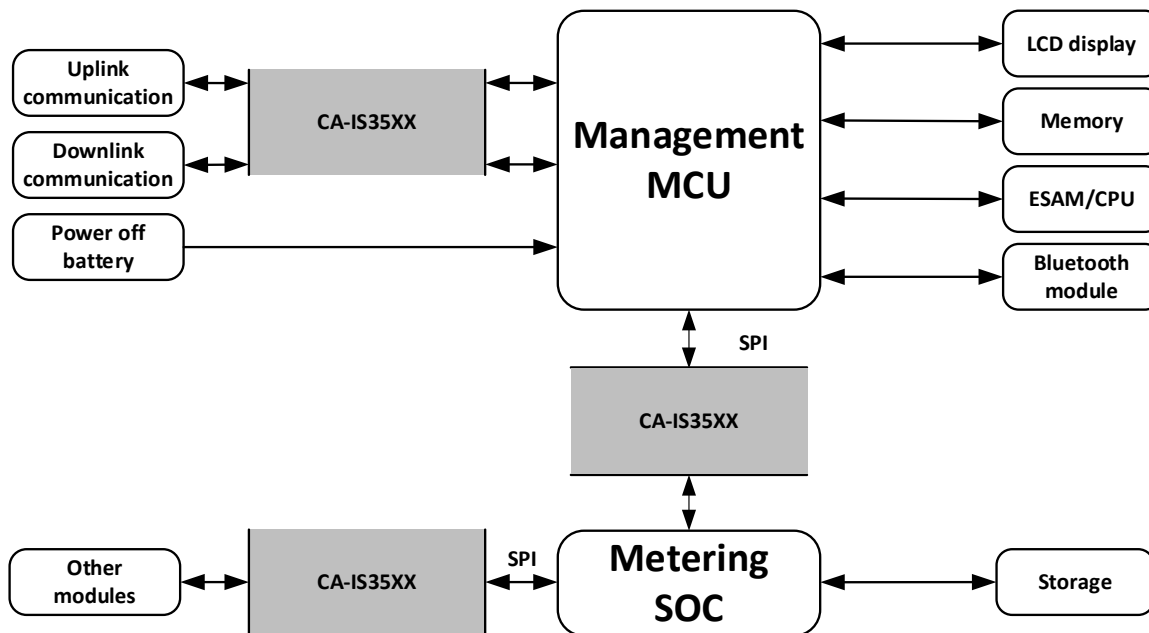
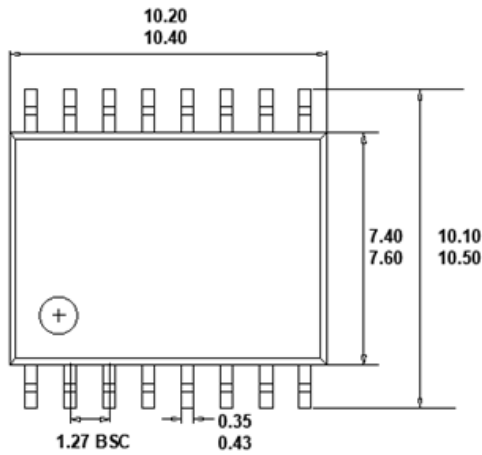


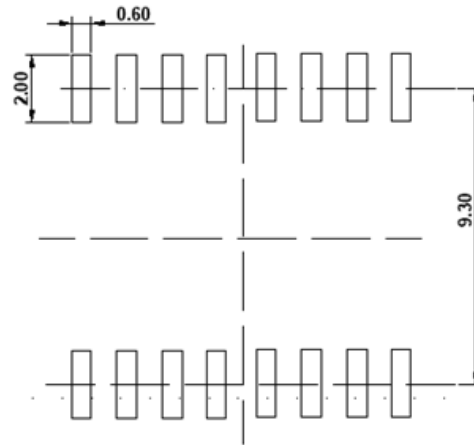
Figure 11-2. CA-IS35xx Typical Application Circuit in IR46 Single-phase/Polyphase Electricity Meters

12. Package Information

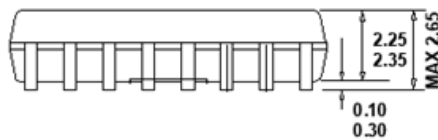
16-Pin Wide Body SOIC Package Outline



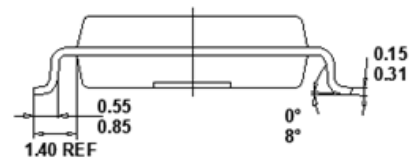
TOP VIEW



RECOMMENDED LAND PATTERN



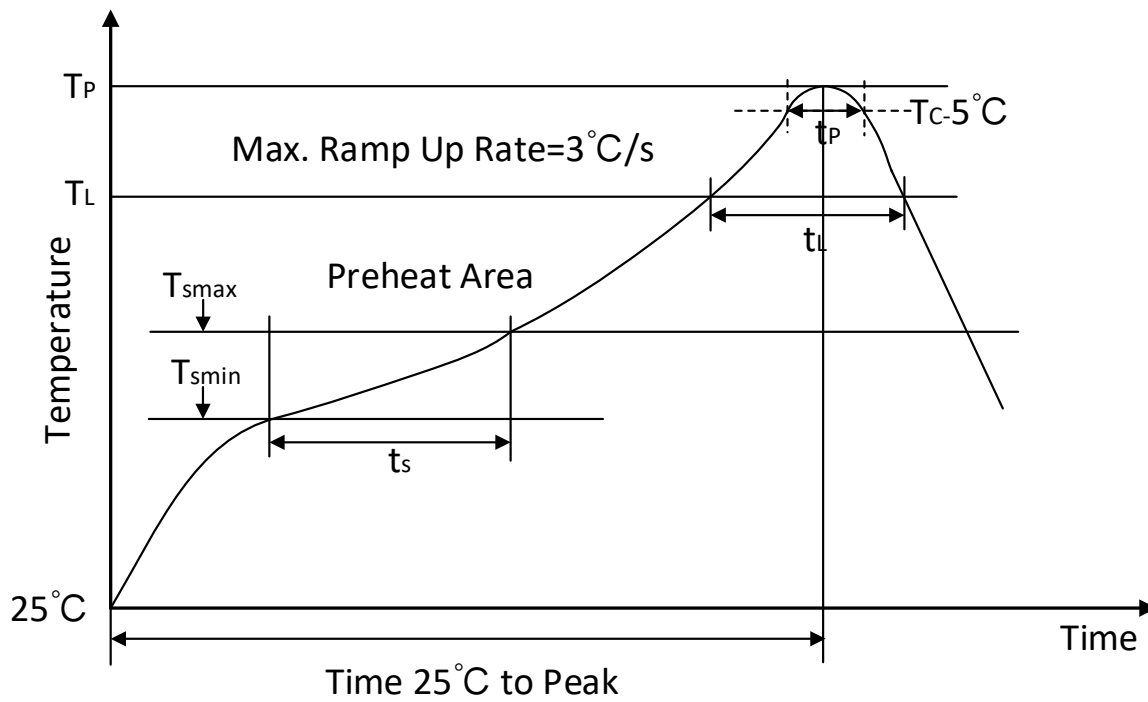
FRONT VIEW



LEFT SIDE VIEW

Note:

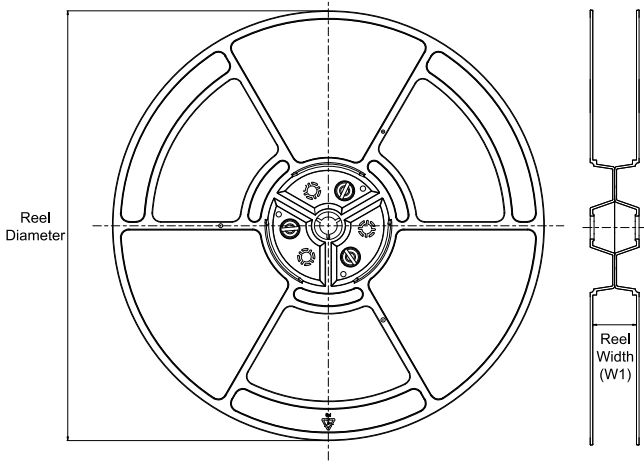
1. All dimensions are in millimeters, angles are in degrees.

13. Soldering Temperature (reflow) Profile

Figure. 13-1 Soldering Temperature (reflow) Profile
Tab. 13-1 Soldering Temperature Parameter

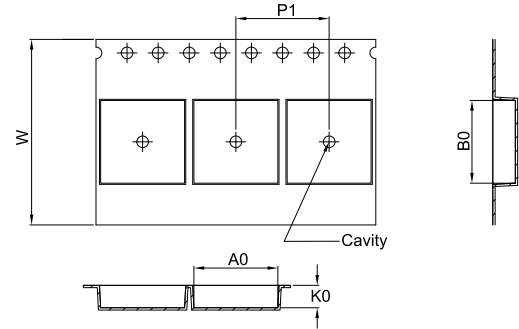
Profile Feature	Pb-Free Assembly
Average ramp-up rate(217 ℃ to Peak)	3℃/second max
Time of Preheat temp(from 150 ℃ to 200 ℃)	60-120 second
Time to be maintained above 217 ℃	60-150 second
Peak temperature	260 +5/-0 ℃
Time within 5 ℃of actual peak temp	30 second
Ramp-down rate	6 ℃/second max.
Time from 25℃ to peak temp	8 minutes max

14. Tape and Reel Information

REEL DIMENSIONS

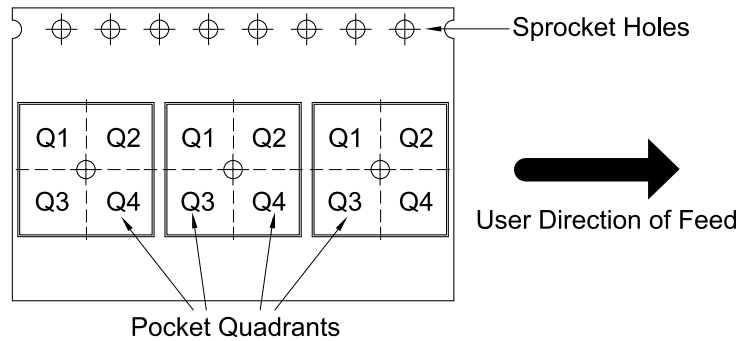


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CA-IS3541HWP	SOIC	W	16	1000	330	16.4	10.9	10.7	3.2	12.0	16.0	Q1
CA-IS3541HWPA	SOIC	W	16	1000	330	16.4	10.9	10.7	3.2	12.0	16.0	Q1
CA-IS3541HWDD	SOIC	W	16	1000	330	16.4	10.9	10.7	3.2	12.0	16.0	Q1
CA-IS3541HWDA	SOIC	W	16	1000	330	16.4	10.9	10.7	3.2	12.0	16.0	Q1

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