3.0V to 5.5V RS485/RS422 Transceivers with ±20kV ESD Protection

1. Features

- **High-Performance and Compliant with RS-485 EIA/ TIA-485 Standard**
  - Low EMI 500kbps Data Rate (CS48505x) and up to 20Mbps (CS48520x) High-Speed Data Rate
  - 50 Nodes on the Same Bus
- **Integrated Protection for Robust Communication**
  - -7V to +12V Common-Mode Voltage Range
  - ±20kV Human Body Model ESD Protection and ±4kV Contact Discharge IEC 61000-4-2 ESD Protection on A/B pins
  - 1/2 Unit Load Enables up to 64 Nodes on the Same Bus
  - Short-Circuit Protection
  - Thermal Shutdown
  - True Fail-Safe Guarantees Known Receiver Output State
  - Glitch-free during Power on/Power off
- **Output Level is Compatible with Profibus Standard**
  - $|V_{OD}|$ > 2.1V @ 5V Supply Voltage
- **Low Power**
  - Low Supply Current (0.95mA, typ.)
  - Shutdown Current < 5μA
- **3V to 5.5V Supply Voltage Range**
- **Wide Operating Temperature Range: –40°C to 125°C**
- **8 pin SOIC, 8 pin MSOP and 8 pin DFN Packages**

2. Applications

- Factory Automation & Control
- Grid Infrastructure
- Home and Building Automation
- Video Surveillance
- Smart Meters
- Process Control
- Telecommunication Equipment

3. General Description

The CS485xx family of devices are low-power half-duplex transceivers for RS-485/RS-422 communications in harsh environments. All devices feature ±20kV electro-static discharge (ESD) protection for the bus pins (A and B), eliminating the need for additional system level protection components.

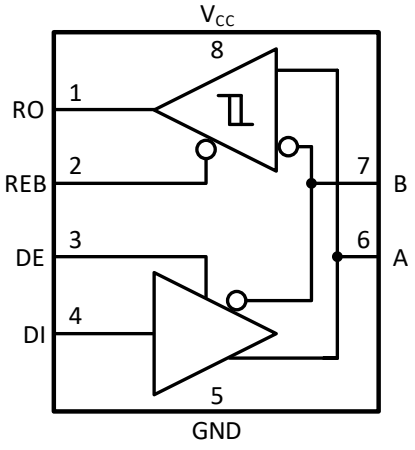
The CS485xx family of devices contain one driver(T_X) and one receiver(R_X), operates over the +3V to +5.5V supply range, making these devices convenient for designers to use one part with either +3.3V or +5V supply systems. The CS48520x devices can transmit and receive at data rates up to 20Mbps, while the CS48505x devices are specified for data rates up to 500kbps. These devices also include fail-safe circuitry, guaranteeing a logic-high receiver output when the receiver inputs are shorted or open.

All devices are specified over the -40°C to +125°C wide operating temperature range and are available in small 8-pin MSOP, 8-pin DFN packages for space constrained applications and 8-pin SOIC for drop-in compatibility design.

Device Information

Part number	Package	Package size (NOM)
CS48505S CS48520S	SOIC8	3.9mm*4.9mm
CS48505M CS48520M	MSOP8	3mm*3mm
CS48505D CS48520D	DFN8	3mm*3mm

Simplified Block Diagram



4. Ordering Information

Table 4-1. Ordering Information

Part Number	Full/Half-Duplex	Data Rate(Mbps)	Number of Nodes on Bus	Package
CS48505S	Half-Duplex	0.5	50	SOIC8(S)
CS48520S	Half-Duplex	20	50	SOIC8(S)
CS48505M	Half-Duplex	0.5	50	MSOP8(M)
CS48520M	Half-Duplex	20	50	MSOP8(M)
CS48505D	Half-Duplex	0.5	50	DFN8(D)
CS48520D	Half-Duplex	20	50	DFN8(D)

Table of Contents

5. Revision History

Revision Number	Description	Page Changed
Version 1.00	N/A	N/A
Version 1.01	Change the maximum number of nodes supported by the bus to 64； Change the minimum value of bus input impedance	P1 P6
Version 1.02	Update EFT items	P5
	Increase the absolute maximum rated value of the differential voltage between buses A and B	P5
	Remarks on adding test conditions for RI bus input impedance	P6

6. Pin Configuration and Descriptions

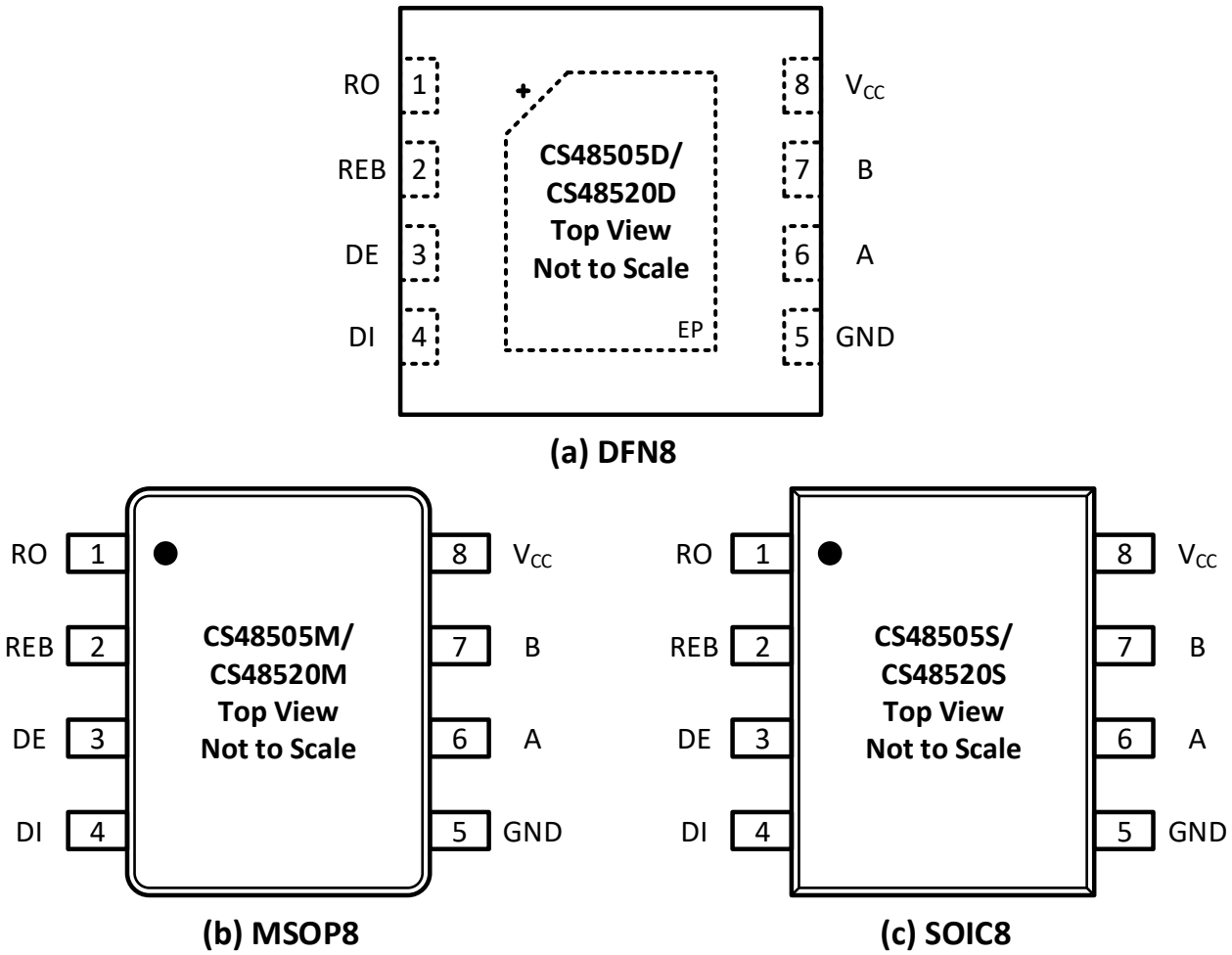


Figure 6-1. CS485xx pin configuration

Table 6-1 CS485xx pin description

Pin Name	Pin Number	Description
RO	1	Receiver data output. With REB low, RO is high when (V_A –V_B) > V_{TH+} and is low when (V_A – V_B) < V_{TH-}. RO is high impedance when REB is high. See *Table 9-2* for details.
REB	2	Receiver output enable. Drive REB low or connect to GND to enable RO. Drive REB high or leave open to disable the receiver and put RO in high impedance. Drive REB high and DE low to force the IC into low-power shutdown mode.
DE	3	Driver output enable. Drive DE high to enable the driver. Drive DE low or leave open to disable the driver. Drive REB high and DE low to force the IC into low-power shutdown mode.
DI	4	Driver data input. With DE high, a logic low on DI forces the noninverting output (A) low and the inverting output (B) high; a logic high on DI forces the noninverting output high and the inverting output low. See *Table 9-1* for details.
GND	5	Ground.
A	6	Noninverting RS-485/RS-422 driver output/receiver input.
B	7	Inverting RS-485/RS-422 driver output/receiver input.
V_{CC}	8	Power supply input. Bypass V_{CC} to GND with at least 0.1μF capacitor as close to the device as possible.
EP	--	Exposed Pad (DFN8 package Only). Connect EP to GND.

7. Specification

7.1. Absolute Maximum Ratings[1]

Parameters		Minimum value	Maximum value	Unit
V_{CC}[2]	Power supply voltage	-0.5	7.0	V
A, B[2]	Voltage on the bus	-8	13	V
A-B	Differential voltage between A and B	-8	13	V
DE, DI, REB	Logic control voltage	-0.3	V_{CC}+0.3[3]	V
RO	Logic voltage at RO	-0.3	V_{CC}+0.3[3]	V
T_J	Junction temperature		150	℃
T_{STG}	Storage temperature range	-65	150	℃

Notes:

1. The stresses listed under "Absolute Maximum Ratings" are stress ratings only, not for functional operation condition. Exposure to absolute maximum rating conditions for extended periods may cause permanent damage to the device.
2. All voltage values are with respect to the ground terminal (GND) and are peak voltage values unless otherwise specified.
3. Maximum voltage must not be exceed 7V.

7.2. ESD Ratings

Parameters			Value	Unit
V_{ESD}	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, bus pins (A, B) to GND [1]	±20	kV
		Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all other pins [1]	±8	
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[2]	±2	
		Contact Discharge, per IEC 61000-4-2, bus pins (A, B) to GND	±4	
V_{EFT}		per IEC 61000-4-4, bus pins (A, B) to GND	±4	

Notes:

1. Per JEDEC document JEP155, 500V HBM allows safe manufacturing of standard ESD control process.
2. Per JEDEC document JEP157, 250V CDM allows safe manufacturing of standard ESD control process.

7.3. Recommended Operating Conditions

	Parameters	Minimum value	Typical value	Maximum value	Unit
V_{CC}	Power supply	3	5	5.5	V
V_{IN}	Input voltage at any bus terminal	-7		12	V
V_{IL}	Low-level input voltage	0		0.8	V
V_{IH}	High-level input voltage	2.0		V_{CC}	V
R_L	Differential load resistance	54			Ohm
$1/t_{UI}$	Signaling rate：CS48505x			500	kbps
$1/t_{UI}$	Signaling rate：CS48520x			20	Mbps
T_A	Operating ambient temperature	-40		125	℃
T_J	Junction temperature	-40		150	℃

7.4. Thermal Information

THERMAL METRIC		SOIC8	MSOP8	DFN8	Unit
$R_{\theta JA}$	Junction-to-ambient thermal resistance	120	160	45	℃/W

7.5. Electrical Characteristics

All typical specs are at V_{CC} = 5V, T_A = 25°C, Min/Max specs are over recommended operating conditions unless otherwise specified.

Parameters		Test conditions		Minimum value	Typical value	Maximum value	Unit
Driver							
$\|V_{OD}\|$	Differential output voltage	R_L =60 Ω, -7 V ≤ V_{test} ≤ 12 V , see Figure8-1		1.5	3.2		V
		R_L =60 Ω, -7 V ≤ V_{test} ≤ 12 V , 4.5 V ≤ V_{CC} ≤ 5.5 V , see Figure 8-1		2.1	3.2		
		R_L = 100 Ω, C_L = 50pF , see Figure8- 2		1.8	3.6		V
		R_L = 54 Ωm C_L = 50pF , see Figure8- 2		1.5	3.2		V
$\Delta\|V_{OD}\|$	Change in differential output voltage	RL = 54 Ω or 100Ω， CL = 50pF, see Figure8- 2		–50		50	mV
V_{OC}	Common-mode output voltage			1	V_{CC}/2	3.3	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage			–200		200	mV
$\Delta V_{OC(pp)}$	Change in steady-state common-mode output voltage, peak to peak				450		
I_{OS}	Short-circuit output current	DE = V_{CC}, -7 V ≤ V_O ≤ 12 V			90	150	mA
Receiver							
I_I	Bus input current	DE = 0 V, V_{CC} = 0 V or 5 V	V_I = 12V		70	600	µA
			V_I = -7V	–200	–40		µA
R_I	Receiver Input Resistance	V_A = –7V， V_B = 12V[1] or V_A = 12V， V_B = –7V[1]		24			kΩ
V_{TH+}	Receiver differential threshold voltage rising	Over common-mode range			–110	–50	mV
V_{TH-}	Receiver differential threshold voltage falling			–200	–140		mV
V_{HYS}[2]	Receiver input hysteresis				30		mV
V_{OH}	Output high voltage	I_{OH} = –4mA		V_{CC} – 0.5	V_{CC} – 0.3		V
V_{OL}	Output low voltage	I_{OH} = 4mA			0.2	0.4	V
I_{OZR}	Output high-impedance current	V_O = 0 V or V_{CC}, REB = V_{CC}		-1		1	µA
I_{OSR}	Receiver output short current	REB = DE = 0V, see Figure8- 3				95	mA
Input Logic							
I_{IN}	Logic Input current	3 V ≤ V_{CC} ≤ 5.5 V, 0 V ≤ V_{IN} ≤ V_{CC}		-5		5	µA
Device							
I_{CC}	Supply current (quiescent)	Driver and receiver enabled REB=0V, DE = V_{CC}, No load			0.95	1.5	mA
		Driver enabled, receiver Disabled REB=V_{CC}, DE = V_{CC}, No load			0.55	1	mA
		Driver disabled, receiver enabled REB=0V, DE = 0V, No load			0.7	1.1	mA
		Driver and receiver disabled REB=V_{CC}, DE = 0V, D=open, No load				5	µA
T_{SD}	Thermal shutdown temperature				200		°C
T_{SDHYS}	T_{SD} hysteresis				25		

Note:

1. The absolute voltage difference between A and B cannot exceed the maximum rated value of 13V. During testing, apply A/B single terminal voltage separately.
2. Under any condition, ensure that V_{TH+} is at least V_{HYS} higher than V_{TH-}.

7.6. Switching Characteristics

All typical specs are at V_{CC} = 5V, T_A = 25°C, Min/Max specs are over recommended operating conditions unless otherwise specified.

Parameter		Test Conditions	Minimum value	Typical value	Maximum value	Unit
Driver						
t_r, t_f	Driver differential output rise/fall time	RL = 54 Ω, CL = 50 pF, see Figure8- 4		5	12	ns
t_{PHL},t_{PLH}	Propagation delay			5	12	ns
$t_{SK(P)}$	Pulse skew $\lvert t_{PHL} - t_{PLH} \rvert$				3.5	ns
t_{PHZ},t_{PLZ}	Disable time	See Figure8- 5, Figure8- 6		10	30	ns
t_{PZH},t_{PZL}	Enable time	REB = 0V, See Figure8- 5, Figure8- 6		10	30	ns
		REB = V_{CC}, See Figure8- 5, Figure8- 6		6	12	us
Receiver						
t_r, t_f	Output rise/fall time	CL = 15 pF[1], see Figure8- 7		4	8	ns
t_{PHL},t_{PLH}	Propagation delay			40	80	ns
$t_{SK(P)}$	Pulse skew $\lvert t_{PHL} - t_{PLH} \rvert$				4	ns
t_{PHZ}, t_{PLZ}	Disable time	see Figure8- 8		7	20	ns
$t_{PZH(1)}$,$t_{PZL(1)}$,		DE = VCC, see Figure8- 8, Figure8- 9		30	70	ns
$t_{PZH(2)}$,$t_{PZL(2)}$,	Enable time	DE = 0 V, see Figure8- 8, Figure8- 9		6	12	µs

Note:

1. C_L includes external circuit (fixture and instrumentation etc.) capacitance.

7.7. Typical Characteristics

All typical specs are at V_{CC} = 5V, T_A = 25°C, Min/Max specs are over recommended operating conditions unless otherwise specified.

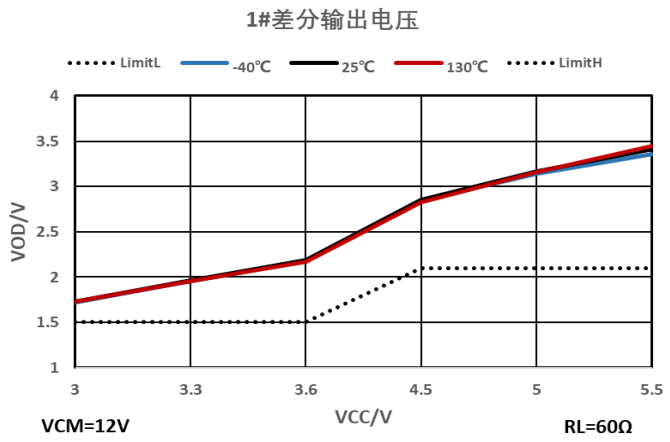


Figure 7-1 Driver Differential Output Voltage @ V_{CM} = 12V

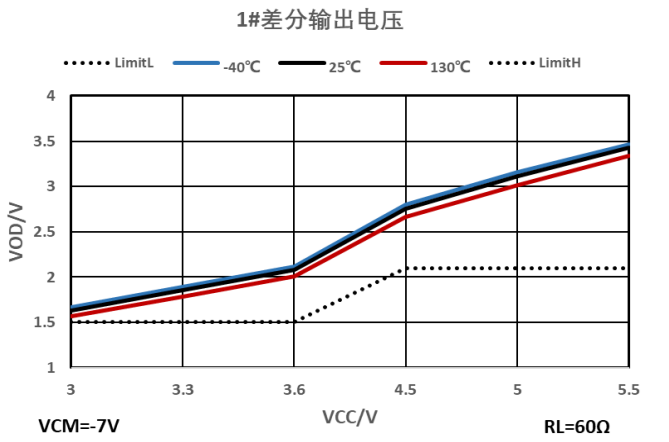


Figure 7-2 Driver Differential Output Voltage @V_{CM} = -7V

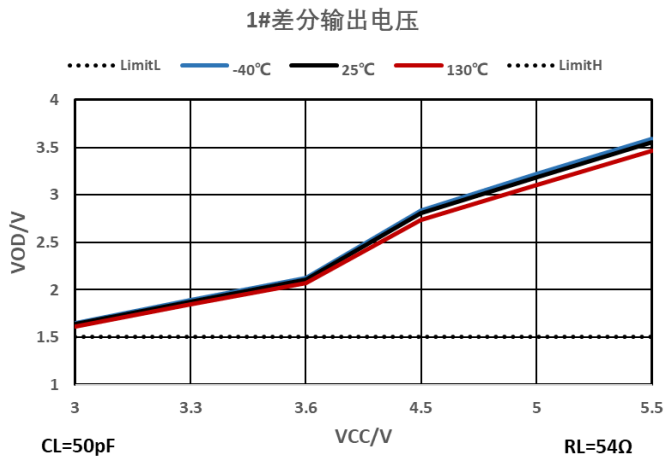


Figure 7-3 Driver Differential Output Voltage with 54Ω Load

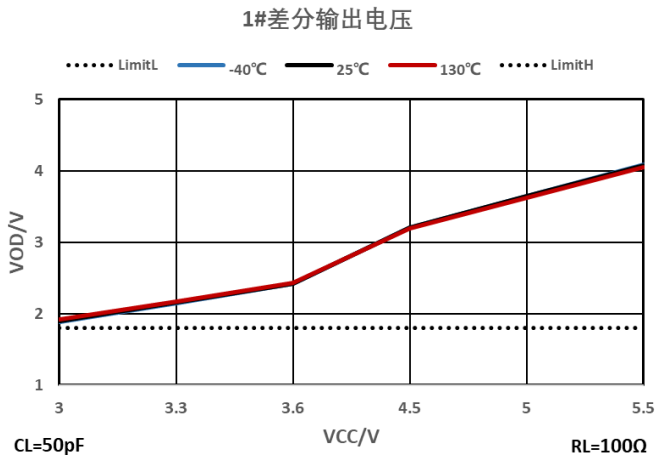


Figure 7-4 Driver Differential Output Voltage with 100Ω Load

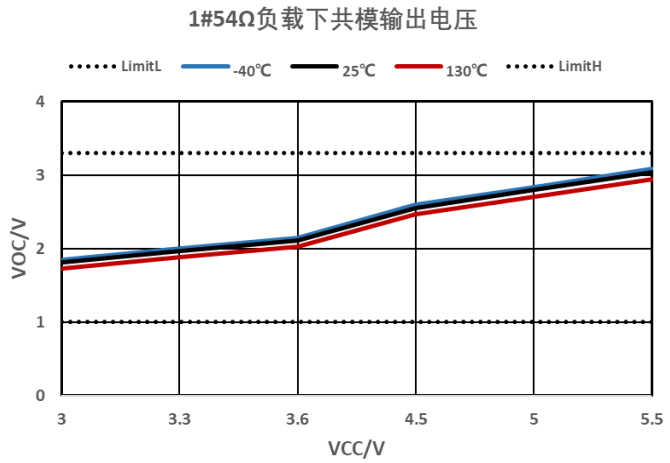


Figure 7-5 Driver Common-mode Output Voltage with 54Ω Load

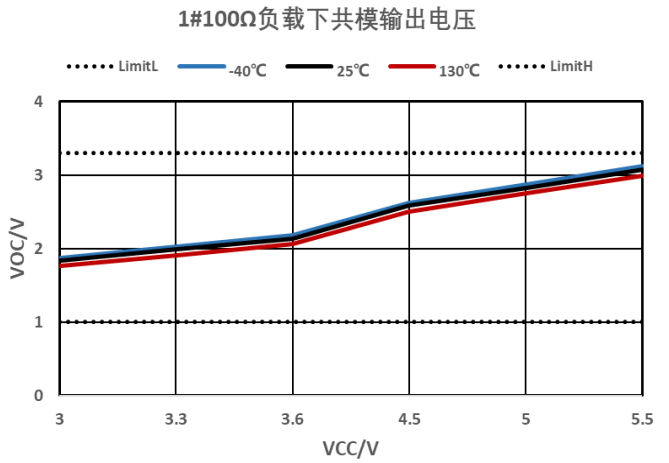


Figure 7-6 Driver Common-mode Output Voltage with 100Ω Load

Typical Characteristics (continued)

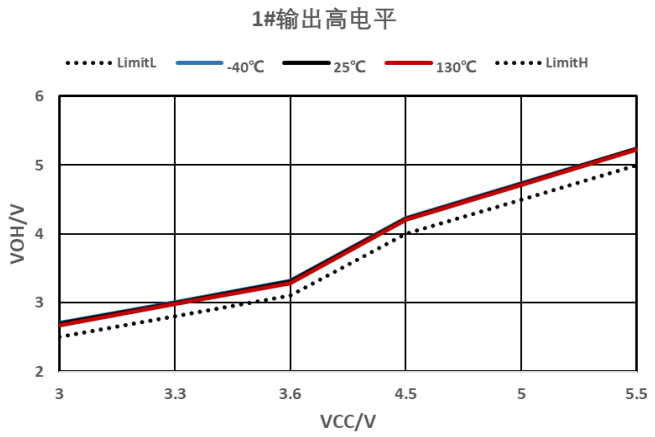


Figure 7-7 Receiver Output @ Logic-high

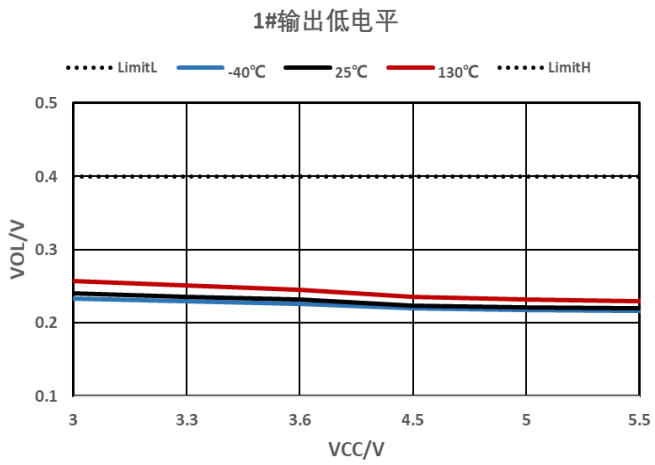


Figure 7-8 Receiver Output @ Logic-low

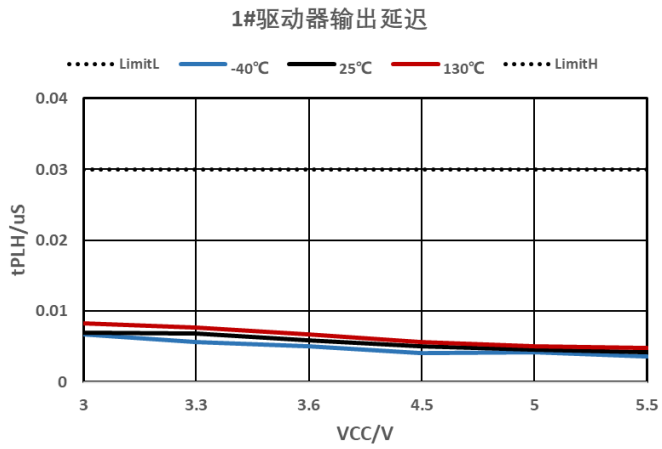


Figure 7-9 Driver Propagation Delay vs. Supply Voltage(L to H)

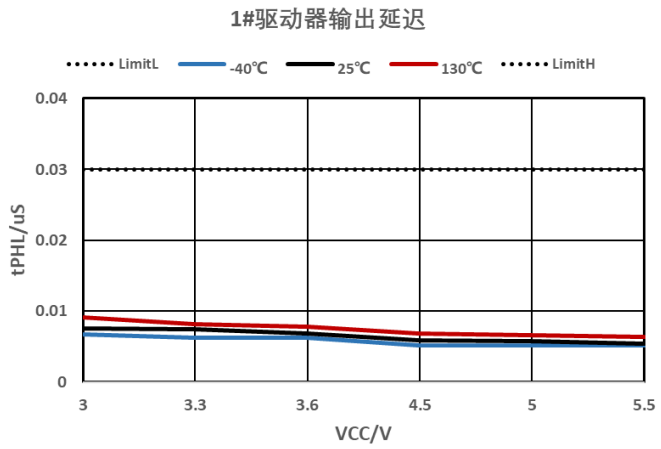


Figure 7-10 Driver Propagation Delay vs. Supply Voltage(H to L)

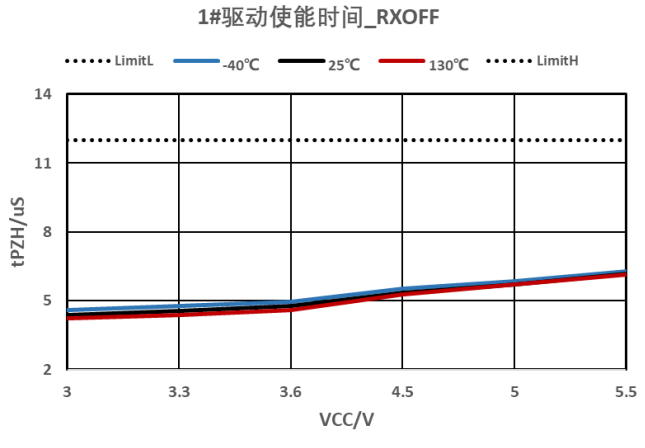


Figure 7-11 Driver Enable Time vs. Supply Voltage: t_{PZH}

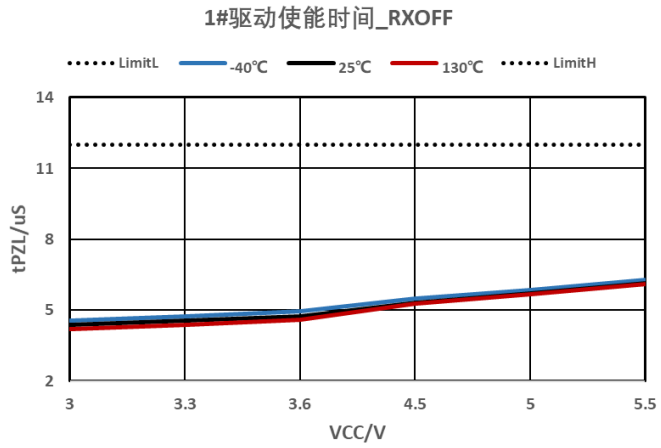


Figure 7-12 Driver Enable Time vs. Supply Voltage: t_{PZL}

Typical Characteristics (continued)

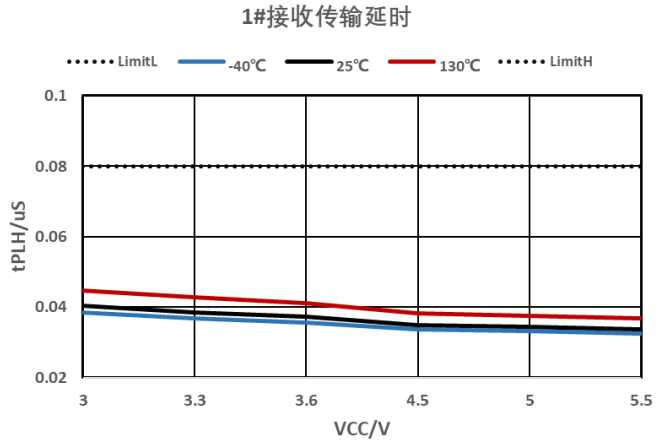


Figure 7-133 Receiver Propagation Delay vs. Supply Voltage(L to H)

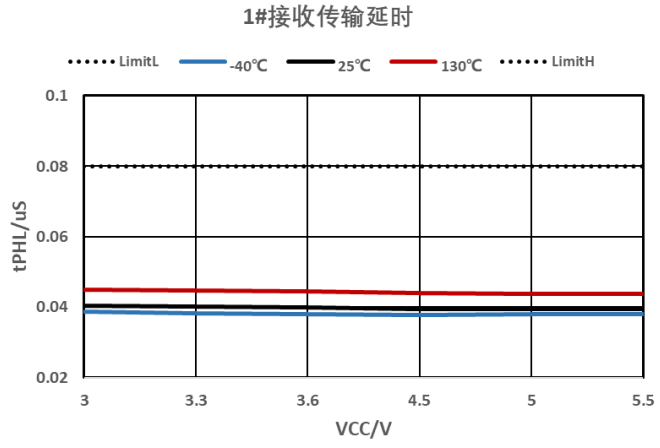


Figure 7-14 Receiver Propagation Delay vs. Supply Voltage(H to L)

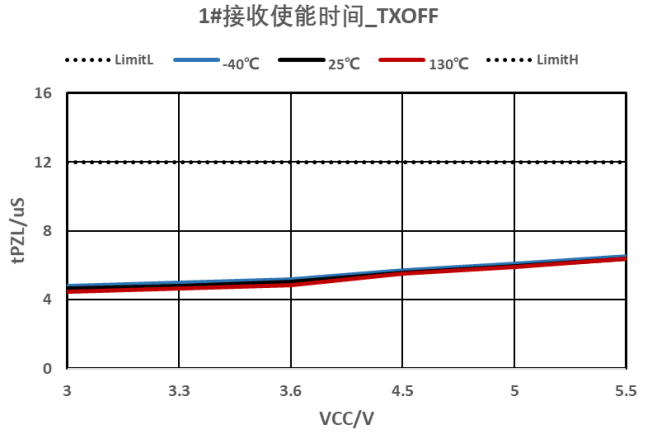


Figure 7-15 Receiver Enable Time vs. Supply Voltage: t_{PZL}

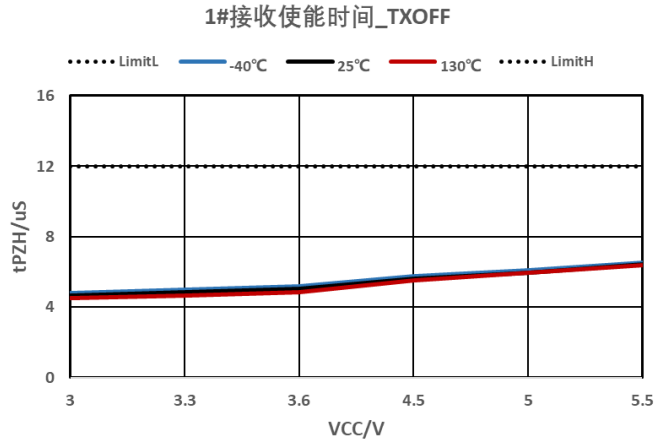


Figure 7-16 Receiver Enable Time vs. Supply Voltage: t_{PZH}

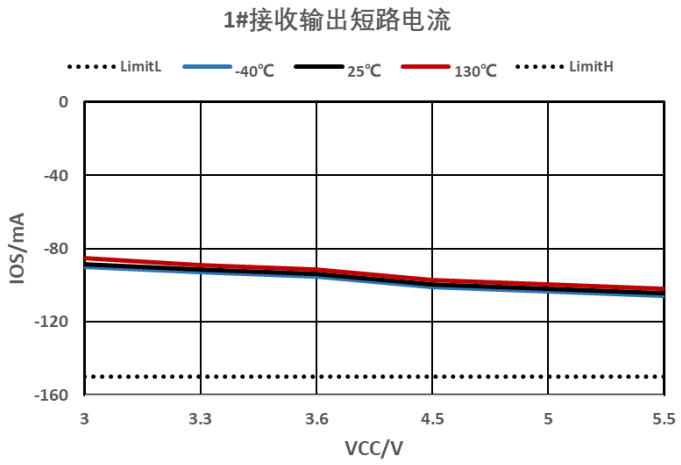


Figure 7-17 Receiver Output Short Current

8. Parameter Measurement Information

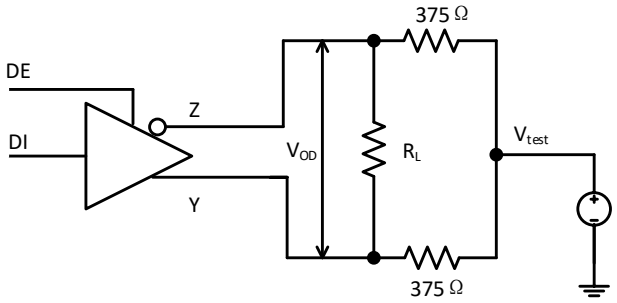


Figure8- 1. Driver Differential Output Voltage With Common-Mode Load

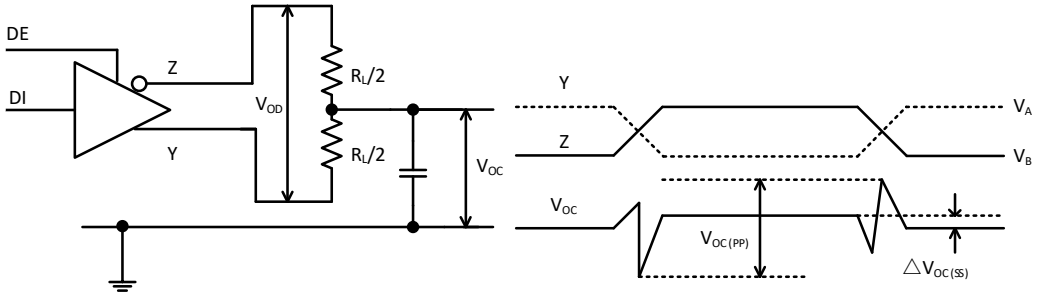


Figure8- 2. Driver Differential and Common-Mode Output With RS-485 Load

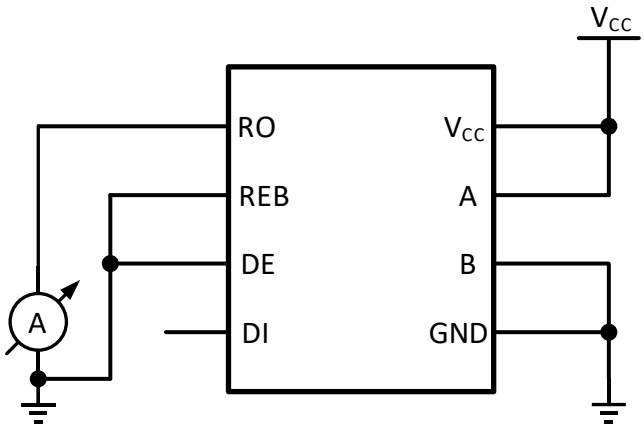


Figure8- 3.Receiver Output Short Current Measurement

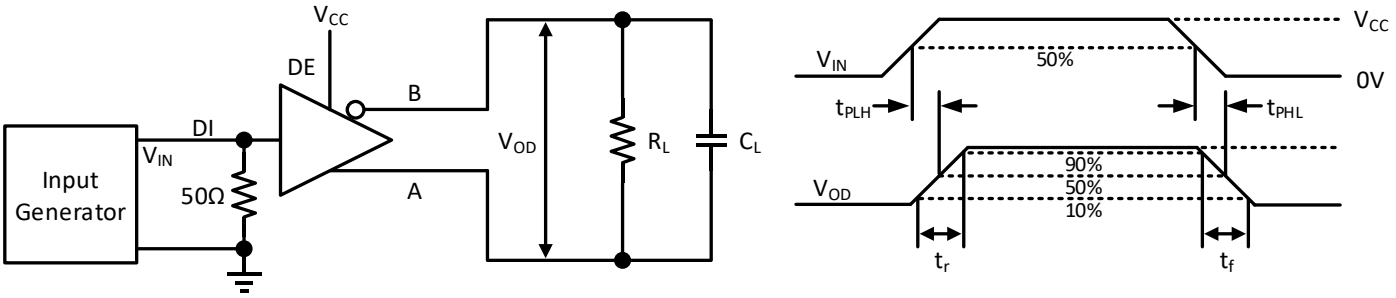


Figure8- 4.Driver Differential Output Rise and Fall Times and Propagation Delays

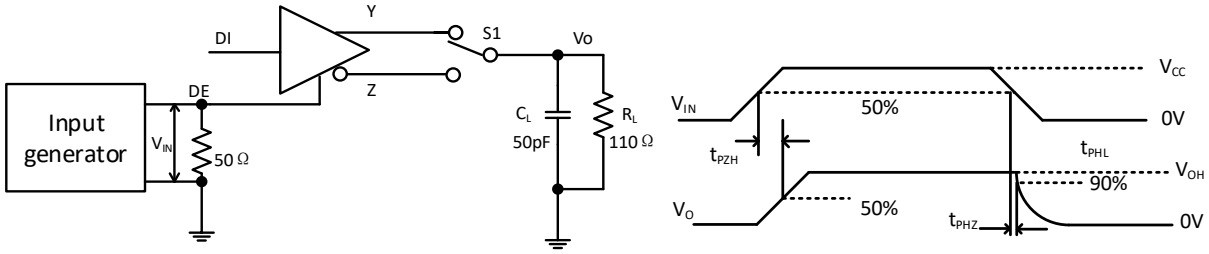


Figure8- 5. Driver Enable and Disable Times With Active High Output and Pull-Down Load

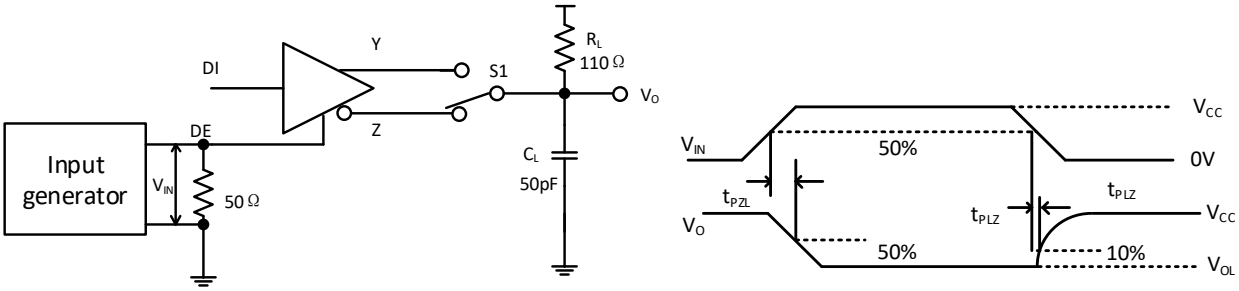


Figure8- 6. Driver Enable and Disable Times With Active Low Output and Pull-up Load

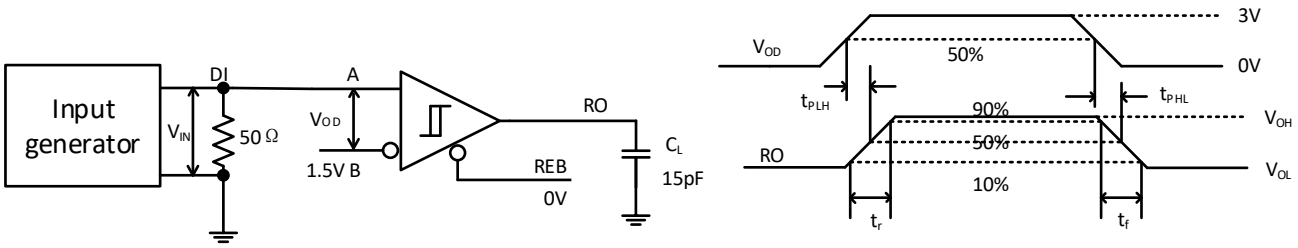


Figure8- 7. Receiver Output Rise and Fall Times and Propagation Delays

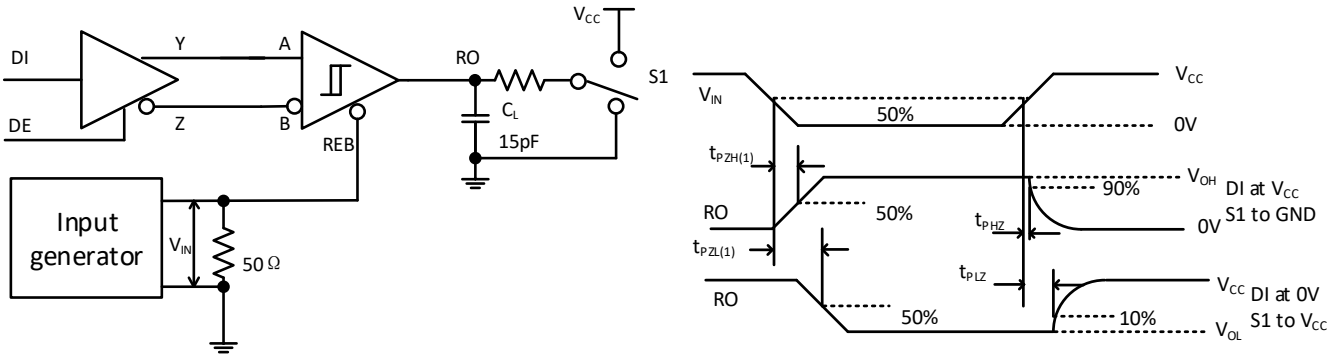


Figure8- 8. Receiver Enable/Disable Times With Driver Enabled

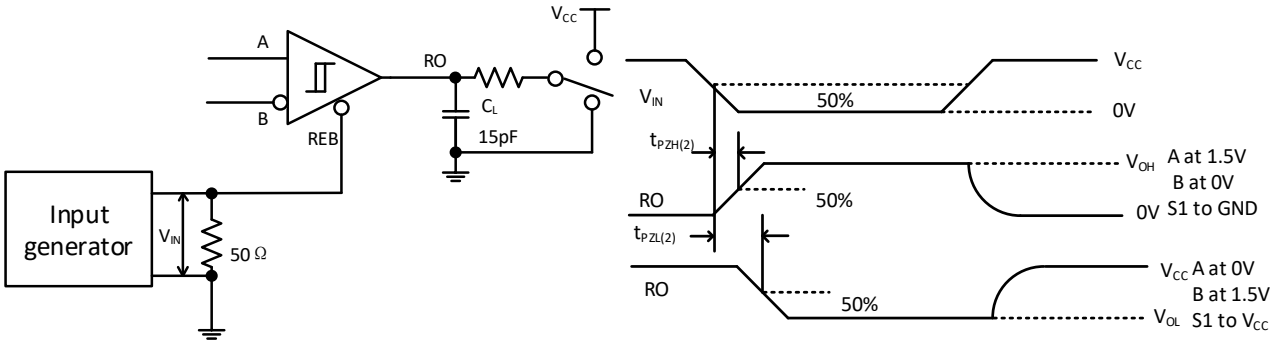


Figure8- 9. Receiver Enable Times With Driver Disabled

9. Detailed Description

9.1. Overview

The CS485xx family of devices are optimized for RS-485/RS-422 applications per the EIA/TIA-485 standard. These devices contain one differential driver and one differential receiver. The receiver allows up to 50 transceivers on a single bus. Driver Enable (DE) and Receiver Enable (REB) pins are included on these half-duplex transceivers. When disabled, the driver and receiver outputs are high impedance. In addition, the CS48505x features reduced slew-rate driver that minimize EMI and reduce reflections caused by improperly terminated cables, thus allowing error-free data transmission up to 500kbps. The driver slew-rate of the CS48520x is not limited, allowing them to transmit up to 20Mbps data rate.

To reduce system complexity and the need for external protection, the driver outputs/receiver inputs of the CS48505/CS48520 incorporate a high ESD protection circuit capable of protecting against up to ±20kV of ESD Human Body Model (HBM) and ±4kV Contact Discharge per IEC 61000-4-2. In addition, two mechanisms against excessive power dissipation caused by faults or bus contention. The first, over-current protection on the output stage, provides immediate protection against short circuits over the entire common-mode voltage range. The second, a thermal shutdown circuit, forces the driver outputs into a high-impedance state once the junction temperature of the devices exceed the thermal shutdown threshold T_{SD} (200°C, typ.). The shutdown condition is cleared when the junction temperature drops to 175°C.

9.2. Device Functional Modes

9.2.1. Driver

The CS485xx driver accepts a single-ended, logic-level input (DI) and transfers it to a differential RS-485/RS-422 level output on the A and B driver outputs. Set the driver enable input (DE) low to disable the driver. A and B are high impedance when the driver is disabled. The DI pin has an internal pull-up resistor to V_{CC}, thus, when left open while the driver is enabled, the noninverting output A turns high and inverting output B turns low. See Table 9-1 for details.

Table 9-1. CS485xx Driver Function Table

Input	Enable	Output		Function
DI	DE	A	B	
H	H	H	L	Drive bus high
L	H	L	H	Drive bus low
X	L	Z	Z	Driver disabled
X	OPEN	Z	Z	Driver disabled by default
OPEN	H	H	L	Drive bus high by default

Note:
L = Low level; H = High level; Z = high impedance; X = Don't care.

9.2.2. Fail-Safe Receiver

The CS485xx receiver accepts a differential, RS-485/RS-422 level input on the A and B inputs and transfers it to a single-ended, logic-level output (RO). Drive the receiver enable input (REB) low to enable the receiver. Drive REB high to disable the receiver. RO is high impedance when REB is high.

The CS485xx receiver includes a true fail-safe feature that ensures the receiver output (RO) is high when the receiver inputs are shorted or open, or when they are connected to a differentially terminated transmission line with all drivers disabled. If the differential receiver input voltage (V_A - V_B) is greater than or equal to V_{TH+} (-50mV, maximum), RO is logic high; if the input voltage (V_A - V_B) is less than the negative input threshold V_{TH-} (-200mV, minimum), the receiver output RO turns low. See Table 9-2 for more details.

Table 9-2. CS485xx Receiver Function Table

Differential Input	Enable	Output	Function
$V_{ID} = V_A - V_B$	REB	RO	
$V_{TH+} < V_{ID}$	L	H	High-level bus state
$V_{TH-} < V_{ID} < V_{TH+}$	L	Indeterminate	Indeterminate bus state
$V_{ID} < V_{TH-}$	L	L	Low-level bus state
X	H	Z	Receiver disabled
X	OPEN	Z	Receiver disabled by default
Open-circuit bus	L	H	Fail-safe high output
Short-circuit bus	L	H	Fail-safe high output
Idle (terminated) bus	L	H	Fail-safe high output

Note:
L = Low level; H = High level; Z = high impedance.

10. Application Information

The CS485xx family of half-duplex RS-485 transceivers commonly used for asynchronous data transmissions, the driver and receiver enable pins allow for the configuration of different operating modes. An RS-485 bus consists of multiple transceivers connecting in parallel to a bus cable. As seen in the following Figure 10-1 typical network application circuit, to minimize reflections, terminate the line at both ends with a termination resistor, R_T, whose value matches the characteristic impedance(Z_0) of the cable, and keep stub lengths off the main line as short as possible. This method, known as parallel termination, generally allows for higher data rates over longer cable length.

To ensure reliable operation at all data rates and supply voltages, each supply should be decoupled with at least 100nF ceramic capacitor located as close to the supply pins as possible. This helps to reduce supply voltage ripple present on the outputs of switched-mode power supplies and also helps to compensate for the resistance and inductance of the PCB power planes.

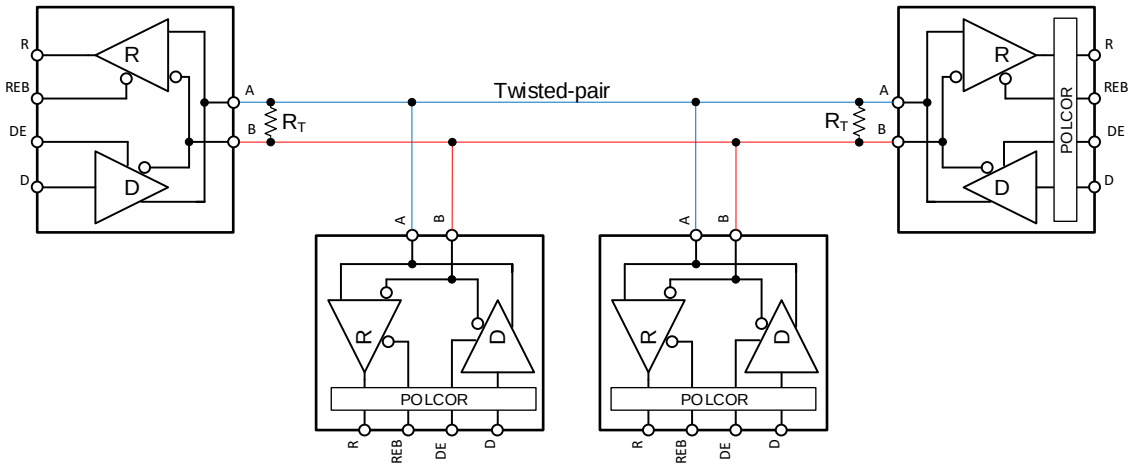
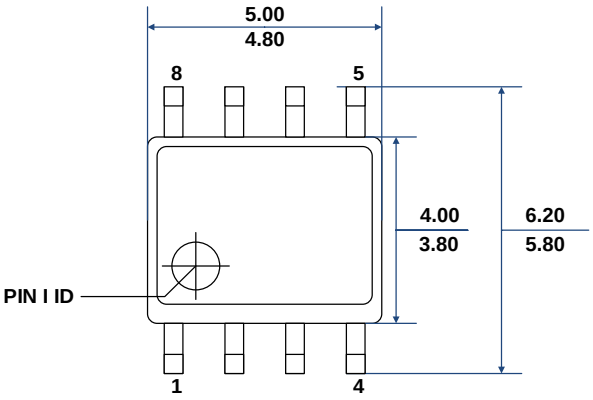


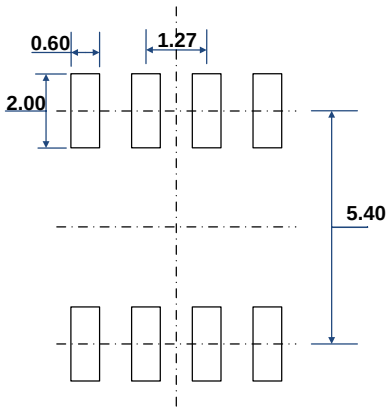
Figure 10-1. Typical RS-485 Network With CS485xx Half-Duplex Transceivers

11. Package Information

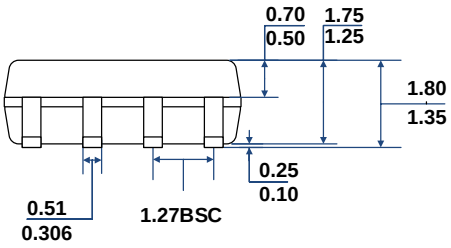
11.1. SOIC8 Package Outline



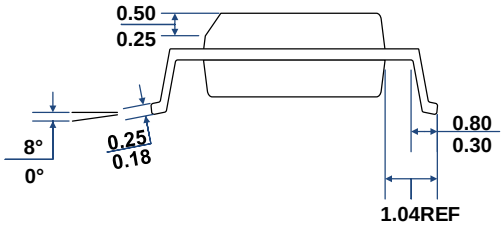
TOP VIEW



RECOMMENDED LAND PATTERN

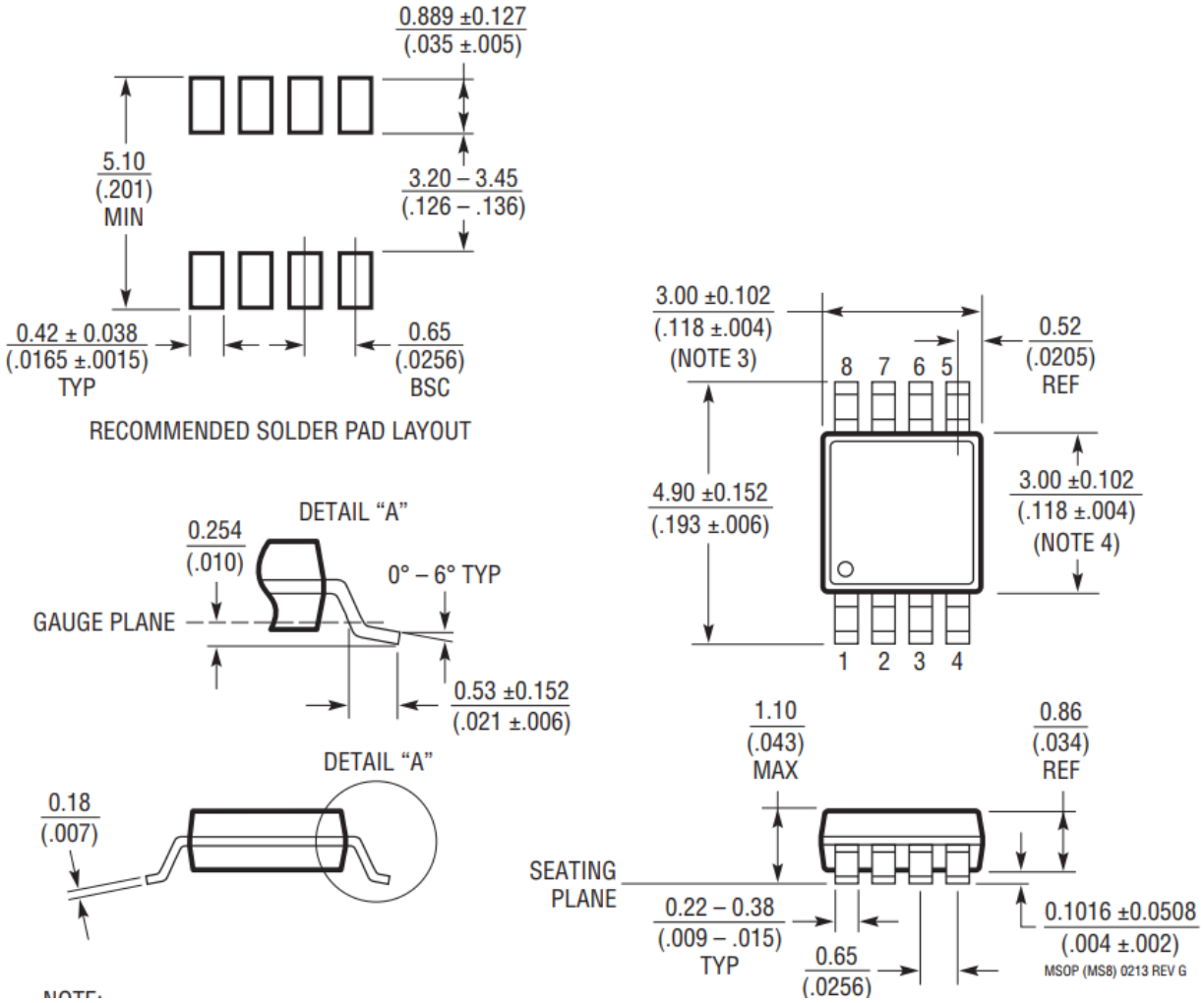


FRONT VIEW

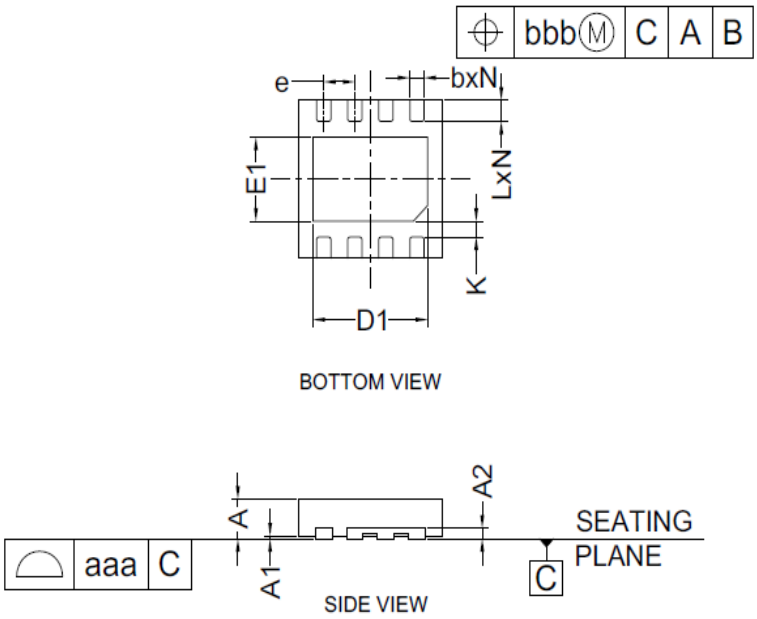


LEFT-SIDE VIEW

11.2. MSOP8 Package Outline



11.3. DFN8 Package Outline

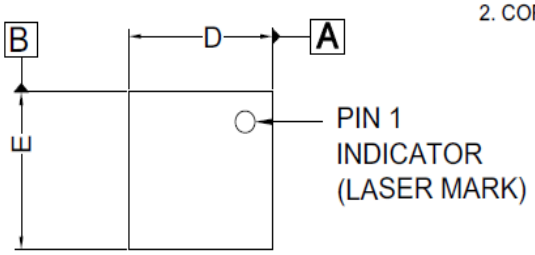


COMMON DIMENSIONS

(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	TYP	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A2		0.203	
b	0.30	0.35	0.40
D	2.90	3.00	3.10
D1	2.51	2.56	2.61
E	2.90	3.00	3.10
E1	1.55	1.60	1.65
e		0.65BSC	
L	0.35	0.40	0.45
N		8	
aaa		0.08	
bbb		0.10	

NOTES:
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS(ANGLES IN DEGREES).
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS THE TERMINALS.



TOP VIEW

12. Soldering Temperature (reflow) Profile

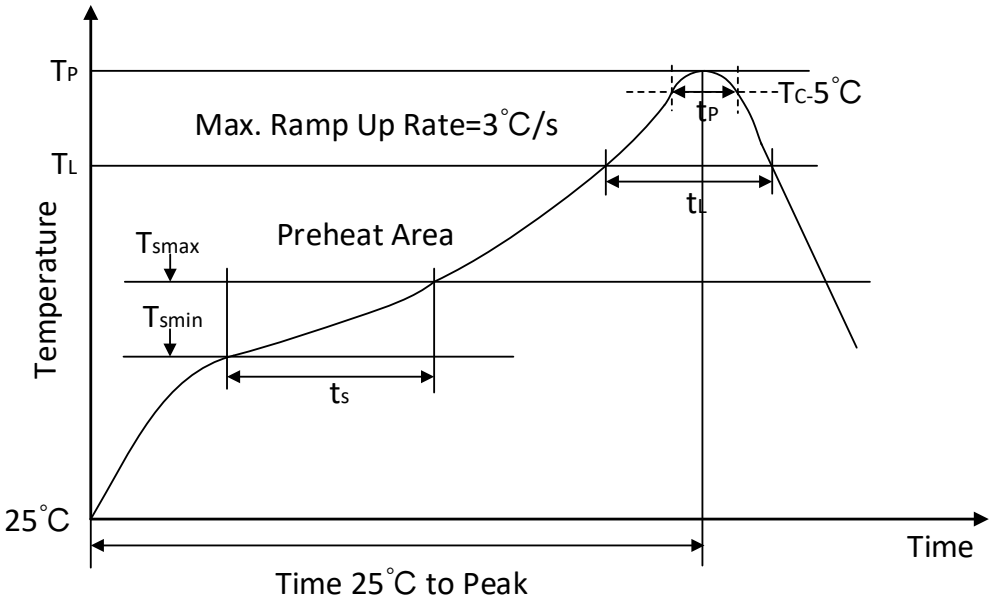


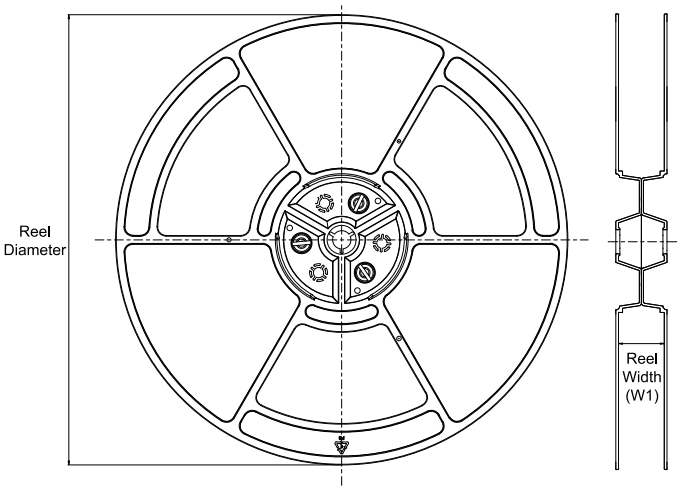
Figure 12- 1 Soldering Temperature (reflow) Profile

Table12- 1 Soldering Temperature Parameter

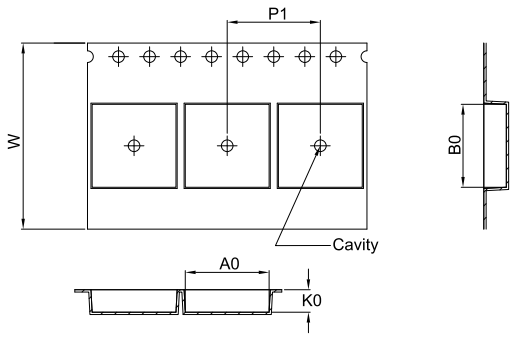
Profile Feature	Pb-Free Assembly
Average ramp-up rate(217 □ to Peak)	3℃/second max
Time of Preheat temp(from 150 □ to 200 □	60-120 second
Time to be maintained above 217 □	60-150 second
Peak temperature	260 +5/-0 □
Time within 5 □of actual peak temp	30 second
Ramp-down rate	6 ℃/second max.
Time from 25□ to peak temp	8 minutes max

13. Tape and Reel Information

REEL DIMENSIONS

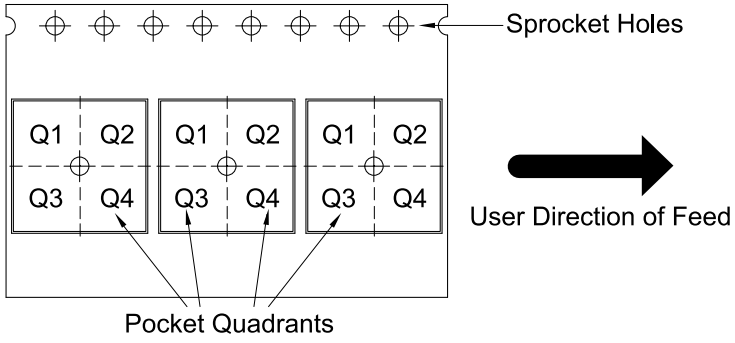


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CS48505S	SOIC8	S	8	2500	330	12.4	6.5	5.4	2.1	8.0	12.0	Q1
CS48520S	SOIC8	S	8	2500	330	12.4	6.5	5.4	2.1	8.0	12.0	Q1
CS48505M	MSOP8	M	8	5000	330	12.6	6.55	5.4	1.9	8.0	12.0	Q1
CS48520M	MSOP8	M	8	5000	330	12.6	6.55	5.4	1.9	8.0	12.0	Q1
CS48505D	DFN8	D	8	3000	180	12.4	3.3	3.3	1.1	8.0	12.0	Q1
CS48520D	DFN8	D	8	3000	180	12.4	3.3	3.3	1.1	8.0	12.0	Q1

14. Important statement

The above information is for reference only and used for helping Chipanalog customers with design, research and development. Chipanalog reserves the rights to change the above information due to technological innovation without advance notice.

All Chipanalog products pass ex-factory test. As for specific practical applications, customers need to be responsible for evaluating and determining whether the products are applicable or not by themselves. Chipanalog's authorization for customers to use the resources are only limited to development of the related applications of the Chipanalog products. In addition to this, the resources cannot be copied or shown, and Chipanalog is not responsible for any claims, compensations, costs, losses, liabilities and the like arising from the use of the resources.

Trademark information

Chipanalog Inc.® and Chipanalog® are registered trademarks of Chipanalog.

http://www.chipanalog.com