



AEC-Q100 Qualification Report

Product Series: CA-IF1044X-Q1

Report Version: V1.1

Reference Doc.: AEC-Q100-REV-H

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1. Overview

Reliability testing of microelectronic products is a risk mitigation process designed to ensure the service life of device in customer applications. Semiconductor wafer manufacturing process and package-level reliability can be assessed in a variety of ways and may include accelerated environmental test conditions. Chipanalog evaluates manufacturability of the device to verify a robust silicon and assembly flow to ensure continuity of supply to customers. Chipanalog qualifies new devices, significant changes, and product families based on AEC-Q100.

2. Part Number List

Package Type	Part Number
SOIC8 (S)	CA-IF1044S-Q1/CA-IF1044VS-Q1
DFN8 (D)	CA-IF1044D-Q1/CA-IF1044VD-Q1

Note: AECQ-100 provides the guideline for the use of generic data to accelerate and streamline the qualification process. Products sharing the same major product, process and materials elements may be categorized in a product qualification family.

3. Production Information

3.1. Wafer information

Fab site	DBH
Wafer	ARIES
Fab Process	18BCD

3.2. Package information

Assembly site	UNIMOS	JCET-D3
FT site	UNIMOS	JCET-D3
Package	SOIC8 (S)	DFN8(D)
Lead Frame	Cu	Cu
Bond wire	20um Au	20um Au
MSL level	MSL1	MSL1
Operation Temp.	Grade 1 (-40°C - 125°C)	Grade 1 (-40°C - 125°C)

4. Reliability Qualification Plan

Test Group A–Accelerated Environment Stress Tests					
Group	Item	Refer.	Test condition	QTY	Remark
A1	PC	J-STD-020 JESD22-A113	Test @ Rm, SMD only, Moisture Preconditioning Before THB/BHAST, AC/UHAST, TC, and PTC stress, MSL = 1, Peak Reflow Temp = 260°C	231 pcs*3 lots	
A2	BHAST	JESD22-A110	BHAST: 130°C, 85% RH, 96 hrs (Test @ Rm/Hot)	77 pcs*3 lots	
A3	UHAST	JESD22-A101	UHAST: 130°C, 85% RH, 96 hrs (Test @ Rm)	77 pcs*3 lots	
A4	TC	JESD22-A104	-65°C-150°C, 500 cycles (Test @ Hot)	77 pcs*3 lots	
A5	PTC	JESD22-A105	-40°C-125°C, 1000 cycles (Test @ Rm/Hot)	NA	Not Applicable
A6	HTSL	JESD22-A103	T _a = 150°C, 1000 hrs (Test @ Rm/Hot)	45 pcs*1 lot	
Test Group B–Accelerated Lifetime Simulation Tests					
Group	Item	Refer.	Test condition	QTY	Remark
B1	HTOL	JESD22-A108	T _a = 135°C, V _{cc1} = 40V, V _{cc2} = 5.5V, 1000 hrs (Test @ Rm/Cold/Hot)	77 pcs*3 lots	
B2	ELFR	AEC-Q100-008	T _a = 135°C, V _{cc1} = 40V, V _{cc2} = 5.5V, 48 hrs (Test @ Rm/Hot)	800 pcs*3 lots	
B3	EDR	AEC-Q100-005	Test @ Rm/Hot	NA	Not Applicable
Group C–Package Assembly Integrity Tests					
Group	Item	Refer.	Test condition	QTY	Remark
C1	WBS	AEC-Q100-001 AEC-Q003	Cpk > 1.67, Each bonder used, T0 samples	30 bonds from 5 pcs	
C1	WBS	AEC-Q100-001 AEC-Q003	0 fails, Each bonder used, post-TC samples	30 bonds from 5 pcs	
C2	WBP	MIL-STD883 AEC-Q003	Cpk > 1.67, Each bonder used T0	30 bonds from 5 pcs	
C2	WBP	MIL-STD883 AEC-Q003	0 fails, Each bonder used, post-TC samples	30 bonds from 5 pcs	
C3	SD	JESD22-B102 JSTD-002D	> 95% coverage, 8hr steam aging prior to testing	15 pcs*1 lot	
C4	PD	JESD22-B100 JESD22-B108 AEC-Q003	Cpk > 1.67	10 pcs*3 lots	
C5	SBS	AEC-Q100-010 AEC-Q003	Cpk > 1.67, 5 balls from min. of 10 devices	NA	Not Applicable

C6	LI	JESD22 B105	10 leads from each of 5 devices	NA	Not Applicable
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Test Group D-Die Fabrication Reliability Tests

Group	Item	Refer.	Test condition	QTY	Remark
D1	EM	JESD61	---	---	Done by Fab
D2	TDDDB	JESD35	---	---	Done by Fab
D3	HCI	JESD60 & 28	---	---	Done by Fab
D4	NBTI	JESD90	---	---	Done by Fab
D5	SM	JESD61, 87, & 202	---	---	Done by Fab

Group E-Electrical Verification Tests

Group	Item	Refer.	Test condition	QTY	Remark
E1	TEST	per datasheet	Pre and Post Stress Electrical Test	all	
E2	HBM	AEC Q100-002	$\pm 500V$, $\pm 1KV$, $\pm 2KV$, $\pm 6KV$ (Test @ Rm/Hot)	3 pcs*1 lot	
E3	CDM	AEC-Q100-011	$\pm 250V$, $\pm 500V$, $\pm 750V$, $\pm 2KV$ (Test @ Rm/Hot)	3 pcs*1 lot	
E4	LU	AEC-Q100-004	125°C, I-trigger $\pm 200mA$ (Test @ Rm/Hot)	6 pcs*1 lot	
E9	EMC	SAE J1752/3	Electromagnetic Compatibility (Radiated Emissions)	1 pcs*1 lot	

5. Reliability Test Results

Group	Items	Test Condition	QTY	Date Code	Result
Test Group A - Accelerated Environment Stress Tests(SOIC8)					
A1	PC	MSL 1	Min. MSL = 3	149AC01	Pass
				149AC02	Pass
				149AC03	Pass
A2	BHAST	130°C, 85%RH 96hrs. Vcc=5.5V	3*77pcs	149AC01	Pass
				149AC02	Pass
				149AC03	Pass
	DPA-BHAST	DPA after BHAST 96hrs	1*10pcs	149AC01	Pass
THB	85°C,85%RH 1000hrs, Vcc=5.5V	1*77pcs	149AC01	Pass	
DPA-THB	DPA after THB 1khrs	1*10pcs	149AC01	Pass	
A3	UHAST	130°C, 85%RH 96hrs.	3*77pcs	149AC01	Pass
				149AC02	Pass
				149AC03	Pass
A4	TC	-65°C-150°C, 500/1000cycles	3*77pcs	149AC01	Pass
				149AC02	Pass
				149AC03	Pass
	DPA-TCT	DPA after TCT500/1000cycles	1*10pcs	149AC01	Pass
SAT-TCT	SAT after TC1000cycles	3*77pcs	/	Pass	
A6	HTSL	Ta=150°C, 1000hrs/2000hrs	1*45pcs	149AC01	Pass
Test Group A - Accelerated Environment Stress Tests(DFN8)					
A1	PC	MSL 1	Min. MSL = 3	DJ2N1	Pass
				DJ2N2	Pass
				DJ2N3	Pass
A2	BHAST	130°C, 85%RH 96hrs. Vcc=5.5V	3*77pcs	DJ2N1	Pass
				DJ2N2	Pass
				DJ2N3	Pass
DPA-BHAST	DPA after BHAST 96hrs	1*10pcs	DJ2N1	Pass	
A3	UHAST	130°C, 85%RH 96hrs.	3*77pcs	DJ2N1	Pass
				DJ2N2	Pass
				DJ2N3	Pass
A4	TC	-65°C-150°C, 500/1000cycles	3*77pcs	DJ2N1	Pass
				DJ2N2	Pass
				DJ2N3	Pass
	DPA-TCT	DPA after TCT500/1000cycles	1*10pcs	DJ2N1	Pass
SAT-TCT	SAT after TC1000cycles	3*77pcs	All	Pass	
A6	HTSL	Ta=150°C, 1000hrs/2000hrs	1*45pcs	DJ2N1	Pass
Test Group B - Accelerated Lifetime Simulation Tests					
B1	HTOL	Ta=125°C, 1000hrs, Vcc=5.5V, TTL input, F=5Mbps.	3*77pcs	DUG12227A	Pass
				DUG12227B	Pass
				DUG12227C	Pass
HTOL-robust	Ta=125°C, 2000hrs, Vcc=5.5V, TTL input, F=5Mbps.	1*77pcs	DUG12227A	Pass	
B2	ELFR	ELFR: Ta=150°C, Vcc=5.5V, 24hrs TTL input, F=5Mbps.	3*800pcs	DUG12227A	Pass
				DUG12227B	Pass
				DUG12227C	Pass
Group C - Package Assembly Integrity Tests(SOIC8)					
C1	WBS	Wire Bond Shear Test: (Cpk > 1.67)	30wire from 5pcs	149AC01	Pass, CPK=2.56
C2	WBP	Wire Bond Pull: (Cpk > 1.67); Each bonder used	30wire from 5pcs	149AC01	Pass, CPK=6.04

C3	SD	Solderability: (>95% coverage) 8hr steam aging prior to testing	1*15pcs	149AC01	Pass
C4	PD	Physical Dimensions: (Cpk > 1.67)	3*10pcs	149AC01	Pass
				149AC02	Pass
				149AC03	Pass
Group C – Package Assembly Integrity Tests(DFN8)					
C1	WBS	Wire Bond Shear Test: (Cpk > 1.67)	30wire from 5pcs	DJ2N1	Pass, CPK=2.66
C2	WBP	Wire Bond Pull: (Cpk > 1.67); Each bonder used	30wire from 5pcs	DJ2N1	Pass, CPK=5.28
C3	SD	Solderability: (>95% coverage) 8hr steam aging prior to testing	1*15pcs	DJ2N1	Pass
C4	PD	Physical Dimensions: (Cpk > 1.67)	3*10pcs	DJ2N1	Pass
				DJ2N2	Pass
				DJ2N3	Pass
TEST GROUP D – Die Fabrication Reliability Tests					
D1	EM	Electromigration		The Die Fabrication Reliability Tests are carried out for every fabrication site. The data, test method, calculations and internal criterial is available to the customer upon request.	
D2	TDDB	Time Dependant Dielectric Breakdown			
D3	HCI	Hot Carrier Injection			
D4	NBTI	Negative Bias Temperature Instability			
D5	SM	Stress Migration			
Group E- Electrical Verification					
E1	TEST	Pre and Post Stress Electrical Test:	all	all	Pass
E2	HBM	HBM: 500V,1KV,2KV,6KV (Test @ Rm/Hot);	3pcs/voltage level	DUG02152E	Pass 6KV class 3A
E3	CDM	CDM: 250V,500V,750V,1KV,2KV(Test @ Rm/Hot);	3pcs/voltage level	DUG02152E	Pass 2KV class C6
E4	LU	Latch-Up: (Test @ Rm/Hot)	1*6pcs	DUG02152E	Pass, class II A
E9	EMC	Electromagnetic Compatibility (Radiated Emissions)	1*1pcs	DUG02152E	Refer attachment 1

Note: Group A&C of SOIC8 use 3 lots general data from CA-IF1042VS-Q1.

6. MTBF&FIT

Supporting Data (Ea = 0.7 eV, Confidence Level = 60%)							MTBF (hrs)	FIT
Test Temp.	Test Voltage	Duration	QTY	Fail QTY	Operation Temp.	Operation Voltage	9.43E+07	10.60
125°C	5.5V	1000 hrs	231	0	55°C	5V		
150°C	5.5V	24 hrs	2400	0	55°C	5V		

Note: The FIT data is generated based on Arrhenius model and voltage acceleration model.

7. Conclusion

CA-IF1044X-Q1 series products are qualified by AEC-Q100 standard.

Disclaimer

This information is provided to assist customers in design and development. It could change for technology innovation without notice.

The devices are shipped after passing final test. Customers are responsible to conduct sufficient engineering and additional qualification testing to determine whether a device is suitable for use in their applications.

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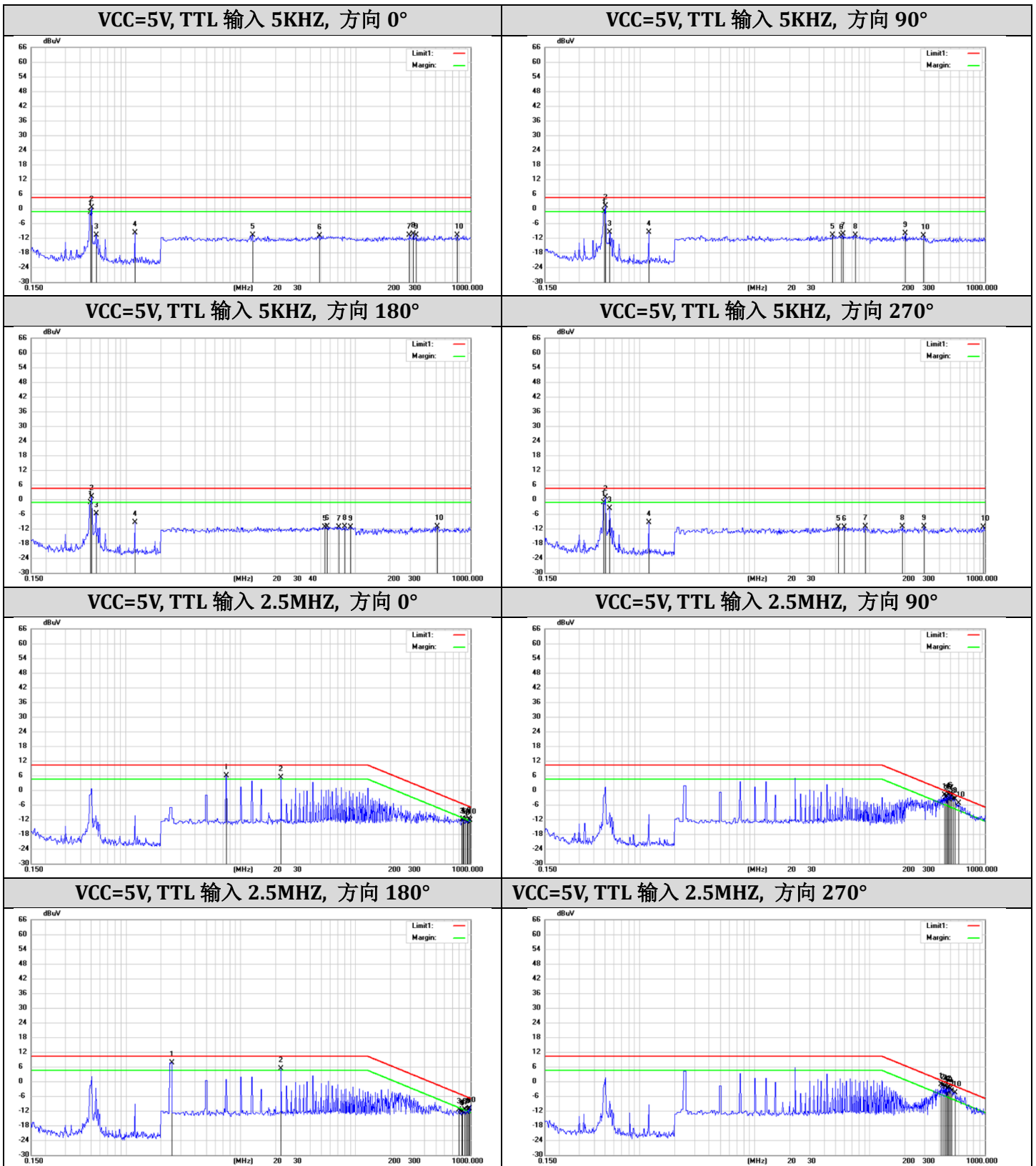
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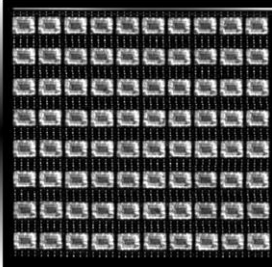


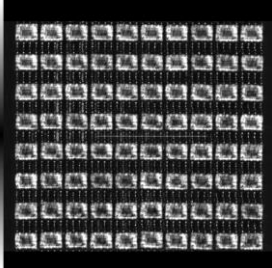
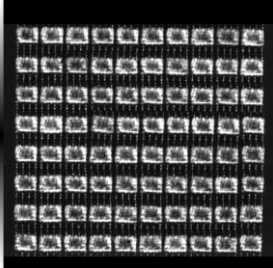
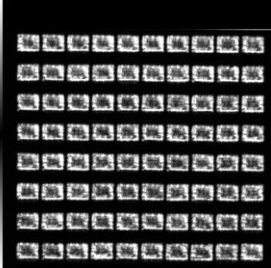
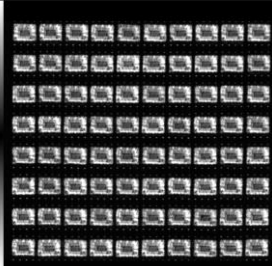


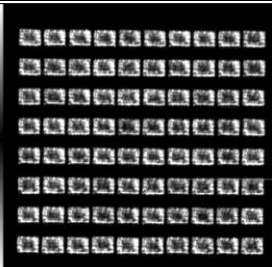
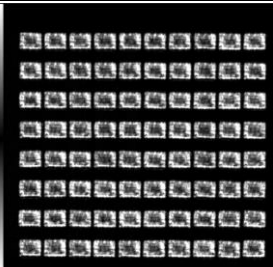
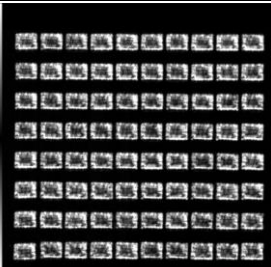
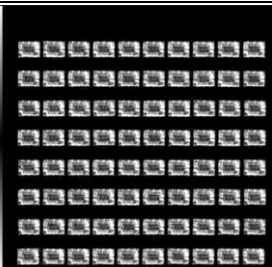
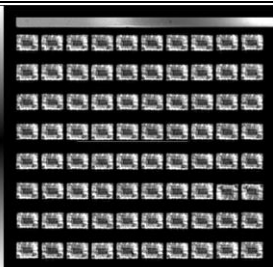
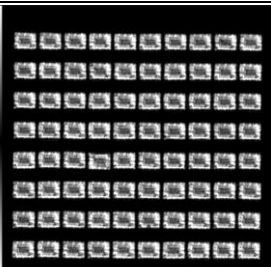
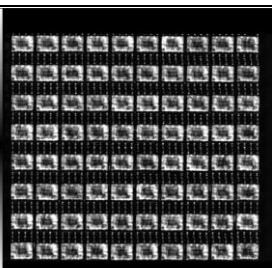
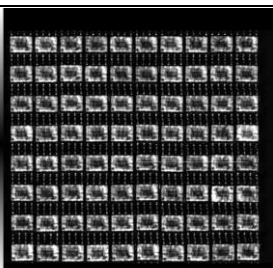
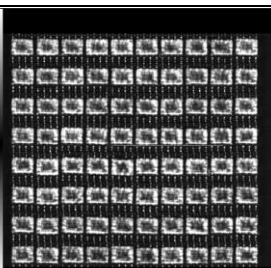
Revision History

Revision	Change Log	Date
V1.0	Initial	Jan. 2023
V1.1	Update robust test result: 1.1lot HTOL 2Khrs pass; 2.3lot TCT 1000cyc SAT&DPA*FT pass; 3.BHAST 96hrs DPA pass; 4.1lot HTSL 2khrs pass.	Feb. 2023

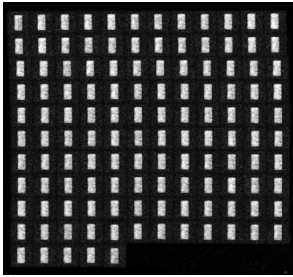
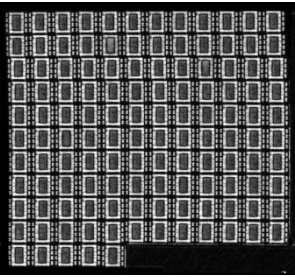
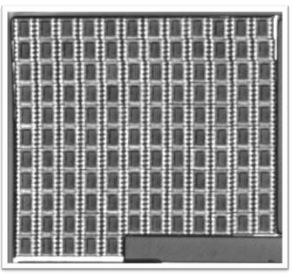
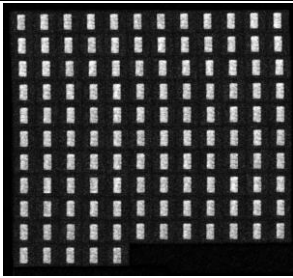
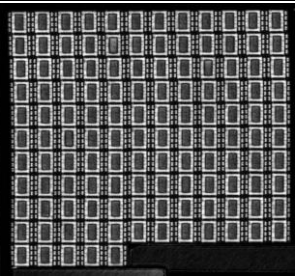
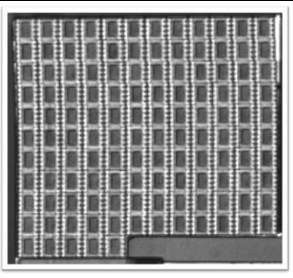
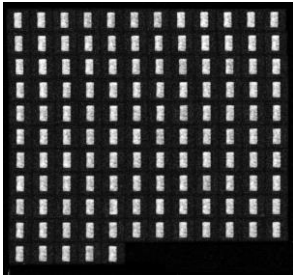
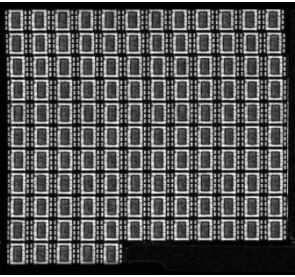
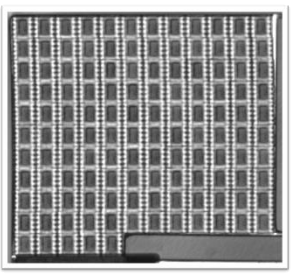
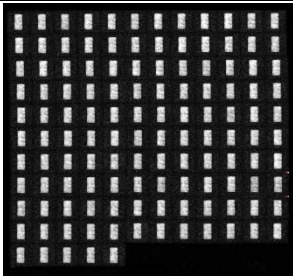
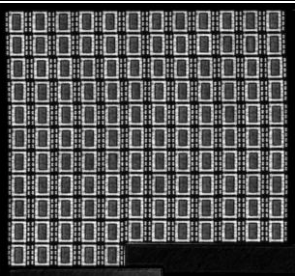
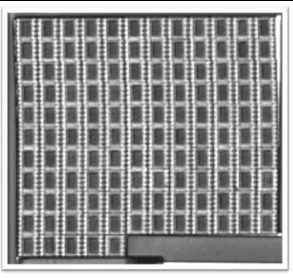
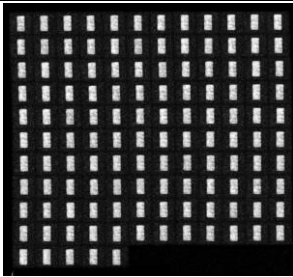
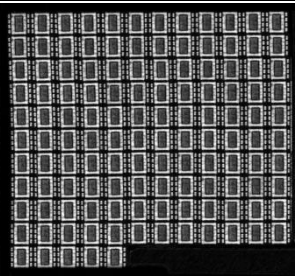
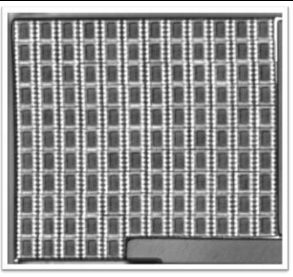
Appendix 1: EMC Test Results



Appendix 2: SAT Test Results (SOP8)

<p>Lot 1 pre-MSL</p>					
<p>Lot 1 post-MSL</p>					
<p>Lot 2 pre-MSL</p>					
<p>Lot 2 post-MSL</p>					
<p>Lot 3 pre-MSL</p>					
<p>Lot 3 post-MSL</p>					

Appendix 3: SAT Test Results (DFN8)

<p>Lot 1 pre-MSL</p>					
<p>Lot 1 post-MSL</p>					
<p>Lot 2 pre-MSL</p>					
<p>Lot 2 post-MSL</p>					
<p>Lot 3 post-MSL</p>					
<p>Lot 3 pre-MSL</p>		