# Reliability Test Report

Product Name: CA-IS36XX&CA-IS306X&CA-IS309X
Report Version: V1.2

# Contents

# 1. Overview

Reliability testing of microelectronic products is a risk mitigation process designed to ensure the service life of device in customer applications. Semiconductor wafer manufacturing process and package-level reliability can be assessed in a variety of ways and may include accelerated environmental test conditions. Chipanalog evaluates manufacturability of the device to verify a robust silicon and assembly flow to ensure continuity of supply to customers. Chipanalog qualifies new devices, significant changes, and product families based on JEDEC JESD47.

CA-IS36XX&CA-IS306X&CA-IS309X series chips are packaged with the same wafer. The differences between part numbers are the package and bonding diagram. The data shown is representative of the material sets, processes, and manufacturing sites used by the device family.

# 2. Part Number List

| **Package Type** | **Part Number** |
|---|---|
| SOIC16-WB(W) | CA-IS3640HW/CA-IS3641HW/CA-IS3642HW/CA-IS3643HW/CA-IS3644HW<br>CA-IS3640LW/CA-IS3641LW/CA-IS3642LW/CA-IS3643LW/CA-IS3644LW<br>CA-IS3640HVW/CA-IS3641HVW/CA-IS3642HVW/CA-IS3643HVW/CA-IS3644HVW<br>CA-IS3640LVW/CA-IS3641LVW/CA-IS3642LVW/CA-IS3643LVW/CA-IS3644LVW<br>CA-IS3621LW/CA-IS3620LW/CA-IS3621LVW<br>CA-IS3092W/CA-IS3092VW/CA-IS3098W/CA-IS3098VW<br>CA-IS3062W/CA-IS3062VW |

**Note:** JEDEC specification is designed to also qualify a family of similar components utilizing the same fabrication process, design rules, and similar circuits. The family qualification may also be applied to a package family where the construction is the same and only the size and number of leads differs.

# 3. Product Information

## 3.1. Wafer Information

| **Wafer ID** | SHENGFO | SATURN | EUROPA |
|---|---|---|---|
| **Die Tech** | BCDXXX | BCDXXX | BCDXXX |

## 3.2. Package Information

| | |
|---|---|
| **Assembly site** | UNIMOS |
| **FT site** | UNIMOS |
| **Package** | SOIC16-WB(W) |
| **Lead frame** | Cu |
| **Bond wire** | 25um Au |
| **MSL level** | MSL3 |

# 4. Reliability Qualification Plan

## 4.1. Device Qualification Test Requirements

| **Stress** | **Ref.** | **Abbv.** | **Conditions** | **Duration /Accept** |
|---|---|---|---|---|
| Electrical Parameter Assessment | JESD86 | ED | Per Datasheet | Per Datasheet |
| High Temperature Operating Life | JESD22-A108,<br>JESD85 | HTOL | $T_J \geq 125°C$<br>$V_{CC} \geq V_{CC}$ max | 1000 hrs/0 Fail |
| Human Body Model ESD | JS-001 | ESD-HBM | $T_A = 25°C$ | Classification |
| Charged Device Model ESD | JS-002 | ESD-CDM | $T_A = 25°C$ | Classification |
| Latch-Up | JESD78 | LU | Class I or Class II | 0 Fail |

## 4.2. Nonhermetic Package Qualification Test Requirements

| **Stress** | **Ref.** | **Abbv.** | **Conditions** | **Duration /Accept** |
|---|---|---|---|---|
| MSL Preconditioning | JESD22-A113 | PC | Per appropriate MSL level per J-STD-020 | Electrical Test (optional) |
| High Temperature Storage | JESD22-A103 & A113 | HTSL | 150°C, 1000 hrs | 1000 hrs/0 Fail |
| Temperature Humidity Bias | JESD22-A101 | THB | 85°C, 85% RH, $V_{CC}$ max | 1000 hrs/0 Fail |
| Highly Accelerated Temperature and Humidity Stress | JESD22-A110 | HAST | 130°C/110°C, 85% RH, $V_{CC}$ max | 96/264 hrs/0 Fail |
| Temperature Cycling | JESD22-A104 | TC | -65°C to +150°C | 500 cycles/0 Fail |
| Unbiased Temperature/Humidity | JESD22-A102 | AC | 121°C/100% RH | 96 hrs/0 Fail |
| Bond Pull Strength | M2011 | BPS | Characterization,<br>Pre Encapsulation | Ppk≥1.66<br>or Cpk≥1.33 |
| Bond Shear | JESD22-B116 | BS | Characterization,<br>Pre Encapsulation | Ppk≥1.66<br>or Cpk≥1.33 |
| Solderability | M2003<br>JESD22-B102 | SD | Characterization | 0 Fail |

**Note**: Either HAST or THB may be chosen.

# 5. Reliability Test Results

## 5.1. Device Reliability Test Results

| Stress | Condition | Duration | Sample Size | Result | Classification |
|---|---|---|---|---|---|
| ED | Per Datasheet | / | 10*3 lots | Pass | / |
| HTOL | $T_A$ = 125℃,<br>$V_{CC}$ = 5.5V | 1000 hrs | 77*3 lots | Pass | / |
| ESD-HBM | $T_A$ = 25℃ | / | 3*1 lot | Pass | Class 3A |
| ESD-CDM | $T_A$ = 25℃ | / | 3*1 lot | Pass | Class C3 |
| LU | $T_A$ = 25℃ | / | 3*1 lot | Pass | Class I A |

## 5.2. Package Reliability Test Results

| **Package Type: SOIC16-WB(W)** | | | | |
|---|---|---|---|---|
| **Stress** | **Condition** | **Duration** | **Sample size** | **Result** |
| PC | MSL 3 | / | 231*3 lots | Pass |
| HTSL | $T_A$ = 150℃ | 1000 hrs | 45*1 lot | Pass |
| HAST | 130℃/85% RH | 96 hrs | 77*3 lots | Pass |
| TC | -65°C to +150°C | 500 cycles | 77*3 lots | Pass |
| AC | 121℃/100% RH | 96 hrs | 77*3 lots | Pass |
| BPS | M2011 | / | 30 bonds/5 ea. | Pass |
| BS | JESD22-B116 | / | 30 bonds/5 ea. | Pass |
| SD | Steam aging 8hrs, 245℃ dipping | / | 22 leads*1 lot | Pass |

# 6. Conclusion

CA-IS36XX&CA-IS306X&CA-IS309X series products are qualified with JEDEC standards.

## Disclaimer

This information is provided to assist customers in design and development. It could change for technology innovation without notice.

The devices are shipped after passing final test. Customers are responsible to conduct sufficient engineering and additional qualification testing to determine whether a device is suitable for use in their applications.

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## Revision History

| **Revision** | **Change Log** | **Date** |
|---|---|---|
| V1.0 | Initial release | Mar, 2021 |
| V1.1 | 1. Wafer version change<br>2. OSAT site change | Aug, 2022 |
| V 1.2 | Include more part numbers from the product family:<br>CA-IS3640HVW/CA-IS3641HVW/CA-IS3642HVW<br>CA-IS3643HVW/CA-IS3644HVW CA-IS3640LVW<br>CA-IS3641LVW/CA-IS3642LVW/CA-IS3643LVW<br>CA-IS3644LVW/CA-IS3620LW/CA-IS3621LVW<br>CA-IS3062VW/CA-IS3092VW/CA-IS3098VW | Jul, 2023 |