Reliability Test Report

Product Name: CS485XX

Report Version: V1.0

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1. Overview

Reliability testing of microelectronic products is a risk mitigation process designed to ensure the service life of device in customer applications. Semiconductor wafer manufacturing process and package-level reliability can be assessed in a variety of ways and may include accelerated environmental test conditions. Chipanalog evaluates manufacturability of the device to verify a robust silicon and assembly flow to ensure continuity of supply to customers. Chipanalog qualifies new devices, significant changes, and product families based on JEDEC JESD47. CS485XX series chips are packaged with the same wafer. The differences between part numbers are the package and bonding diagram. The data shown is representative of the material sets, processes, and manufacturing sites used by the device family.

2. Part Number List

Package Type	**Part Number**
SOIC8(S)	CS485S/CS48505S/CS48520S
MSOP8(M)	CS485M/CS48505M/CS48520M
DFN8(D)	CS48505D/CS48520D

Note: JEDEC specification is designed to also qualify a family of similar components utilizing the same fabrication process, design rules, and similar circuits. The family qualification may also be applied to a package family where the construction is the same and only the size and number of leads differs.

3. Product Information

3.1. Wafer Information

Wafer ID	EUROPA
Die Tech	BCDXXX

3.2. Package Information

Assembly site	SiMAT/JCET	JCET	SiMAT
FT site	SiMAT/JCET	JCET	SiMAT
Package	SOIC8	MSOP8	DFN8
Lead frame	Cu	Cu	Cu
Bond wire	20 um AuPdCu	20 um AuPdCu	20 um AuPdCu
MSL level	3	3	3

4. Reliability Qualification Plan

4.1. Device Qualification Test Requirements

Stress	Ref.	Abbv.	Conditions	Duration /Accept
Electrical Parameter Assessment	JESD86	ED	Per Datasheet	Per Datasheet
High Temperature Operating Life	JESD22-A108, JESD85	HTOL	$T_J \geq 125°C$ $V_{CC} \geq$ Vcc max	1000 hrs/0 Fail
Human Body Model ESD	JS-001	ESD-HBM	$T_A = 25°C$	Classification
Charged Device Model ESD	JS-002	ESD-CDM	$T_A = 25°C$	Classification
Latch-Up	JESD78	LU	Class I or Class II	0 Fail

4.2. Non-hermetic Package Qualification Test Requirements

Stress	Ref.	Abbv.	Conditions	Duration /Accept
MSL Preconditioning	JESD22-A113	PC	Per appropriate MSL level per J-STD-020	Electrical Test (optional)
High Temperature Storage	JESD22-A103 & A113	HTSL	150°C, 1000 hrs	1000 hrs/0 Fail
Temperature Humidity Bias	JESD22-A101	THB	85°C, 85% RH, V_{CC} max	1000 hrs/0 Fail
Highly Accelerated Temperature and Humidity Stress	JESD22-A110	HAST	130°C/110°C, 85% RH, V_{CC} max	96/264 hrs/0 Fail
Temperature Cycling	JESD22-A104	TC	-65°C to +150°C	500 cycles/0 Fail
Unbiased Temperature/Humidity	JESD22-A102	AC	121°C/100% RH	96 hrs/0 Fail
Bond Pull Strength	M2011	BPS	Characterization, Pre Encapsulation	Ppk≥1.66 or Cpk≥1.33
Bond Shear	JESD22-B116	BS	Characterization, Pre Encapsulation	Ppk≥1.66 or Cpk≥1.33
Solderability	M2003 JESD22-B102	SD	Characterization	0 Fail

Note: Either HAST or THB may be chosen.

5. Reliability Test Results

5.1. Device Reliability Test Results

Stress	Condition	Duration	Sample Size	Result	Classification
ED	Per Datasheet	/	5*3 lots	Pass	/
HTOL	T_A =125℃, V_{CC} =5.5V	1000 hrs	77*1 lot	Pass	/
ESD-HBM	T_A = 25℃	/	3*1 lot	Pass	Class 3A
ESD-CDM	T_A = 25℃	/	3*1 lot	Pass	Class C3
LU	T_A = 25℃	/	3*1 lot	Pass	Class I A

5.2. Package Reliability Test Results

Package Type: SOIC8					
Stress	Condition	Duration	Sample size	Result	
				SiMAT	JCET
PC	MSL 3	/	231*1 lot	Pass	Pass
HTSL	T_A = 150℃	1000 hrs	77*1 lot	Pass	Pass
HAST	130℃/85% RH	96 hrs	77*1 lot	Pass	Pass
TC	-65°C to +150°C	500 cycle	77*1 lot	Pass	Pass
AC	121℃/100% RH	96 hrs	77*1 lot	Pass	Pass
SBS	M2011	/	30 bonds*5 ea.	Pass	Pass
BPS	JESD22-B116	/	30 bonds*5 ea.	Pass	Pass
SD	Steam aging 8hrs, 245℃ dipping	/	22 leads*1 lot	Pass	Pass

Package Type: MSOP8				
Stress	Condition	Duration	Sample size	Result-JCET
PC	MSL 3	/	231*1 lot	Pass
HTSL	T_A = 150℃	1000 hrs	77*1 lot	Pass
HAST	130℃/85% RH	96 hrs	77*1 lot	Pass
TC	-65°C to +150°C	500 cycle	77*1 lot	Pass
AC	121℃/100% RH	96 hrs	77*1 lot	Pass
SBS	M2011	/	30 bonds*5 ea.	Pass
BPS	JESD22-B116	/	30 bonds*5 ea.	Pass
SD	Steam aging 8hrs, 245℃ dipping	/	22 leads*1 lot	Pass

Package Type: DFN8				
Stress	**Condition**	**Duration**	**Sample size**	**Result-SiMAT**
PC	MSL 3	/	231*1 lot	Pass
HTSL	T_A = 150℃	1000 hrs	77*1 lot	Pass
HAST	130℃/85% RH	96 hrs	77*1 lot	Pass
TC	-65°C to +150°C	500 cycle	77*1 lot	Pass
AC	121℃/100% RH	96 hrs	77*1 lot	Pass
SBS	M2011	/	30 bonds*5 ea.	Pass
BPS	JESD22-B116	/	30 bonds*5 ea.	Pass
SD	Steam aging 8hrs, 245℃ dipping	/	22 leads*1 lot	Pass

6. Conclusion

CS485XX series products are qualified with industry standards test methodologies performed to the intent of Joint Electron Devices Engineering Council(JEDEC).

Disclaimer

This information is provided to assist customers in design and development. It could change for technology innovation without notice.

The devices are shipped after passing final test. Customers are responsible to conduct sufficient engineering and additional qualification testing to determine whether a device is suitable for use in their applications.

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Revision History

Revision	Change Log	Date
V1.0	Initial release	Aug. 2022