



AEC-Q100 Reliability Qual Report

Product Series: CA-IF1021X-Q1

Report Version: V1.1

Reference Doc.: AEC-Q100-REV-H

Qualification Lab: Chinaisti (Shanghai) Testing Technology Co., LT

Catalogue

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1 Summary

Chipanalog product quality and reliability test is a risk mitigation process designed to ensure the lifetime of device in customer application. There are a variety of methods for evaluating semiconductor wafer fabrication process and package-level reliability, which may include accelerated environmental test conditions followed by reduction to actual use conditions. The manufacturability assessment of chips includes verifying a robust assembly process, continuity of product production, and ensuring availability. According to the AEC-Q100 standards and procedures, the product evaluation of Chipanalog conforms to industry standard test methods.

2 Product Series List

| Package | Part NO. |
|----------|---------------|
| SOIC8(S) | CA-IF1021S-Q1 |
| DFN8(D) | CA-IF1021D-Q1 |

Note: Based on AEC-Q100 Qualification family rule, the family qualification may be applied to similar components with the same fabrication process, design rules, and similar circuits.

3 Production Information

3.1 Fab information

| | |
|------------------|--------|
| Fab site | DBH |
| Wafer ID | LEO |
| Die Tech. | BCDXXX |

3.2 Package information

| | | |
|------------------------|-------------------------|-------------------------|
| Assembly site | UNIMOS | JCET-D3 |
| FT site | UNIMOS | JCET-D3 |
| Package | SOIC8 (S) | DFN8(D) |
| Lead Frame | Cu | Cu |
| Bond wire | 20um Au | 20um Au |
| MSL level | MSL1 | MSL1 |
| Operation Temp. | Grade 1 (-40°C - 125°C) | Grade 1 (-40°C - 125°C) |

4 Reliability Qualification Plan

| Group | Item | Refer. | Test condition | QTY | Remark |
|---|-------------|---|---|------------------|---|
| Test Group A – Accelerated Environment Stress Tests | | | | | |
| A1 | PC | J-STD-020 JESD22-A113 | Preconditioning: (Test @ Rm) SMD only; Moisture Preconditioning for THB/HAST, AC/UHST, TC, &PTC; Peak Reflow Temp =260°C | Min. MSL = 3 | Use 3lots CA-IF1042S- Q1/CA- IF1044VD-Q1 as generic data |
| A2 | THB/BHAST | JESD22-A101 JESD22-A110 | THB: 85°C, 85%RH 1000hrs. (Test @ Rm/Hot) BHAST: 130°C, 85%RH 96hrs. (Test @ Rm/Hot) | 1*77pcs | |
| A3 | AC/TH/UHAST | JESD22-A102 JESD22-A118 JESD22-A101 | AC: 121°C, 100%RH 96hrs. (Test @ Rm) TH: 85°C, 85%RH 1000hrs. (Test @ Rm) UHAST: 130°C, 85%RH 96hrs. (Test @ Rm) | 1*77pcs | |
| A4 | TC | JESD22-A104 | TC: -65°C-150°C, 500cycles (Test @Rm/ Hot) | 1*77pcs | |
| A5 | PTC | JESD22-A105 | PTC: -65°C-125°C, 1000cycles (Test @ Rm/Hot) | NA | Not Applicable |
| A6 | HTSL | JESD22-A103 | HTSL: Ta=150°C, 1000hrs (Test @ Rm/Hot) | 1*45pcs | |
| Test Group B – Accelerated Lifetime Simulation Tests | | | | | |
| B1 | HTOL | JESD22-A108 | HTOL: Ta=125°C, Vcc=5V, 1000hrs (Test @ Rm/Cold/Hot) | 3*77pcs | |
| B2 | ELFR | AEC-Q100-008 | ELFR: Ta=125°C, Vcc=5V, 48hrs (Test @ Rm/Hot) | 3*800pcs | |
| B3 | EDR | AEC-Q100-005 | EDR: (Test @ Rm/Hot) | NA | Not Applicable |
| Group C – Package Assembly Integrity Tests | | | | | |
| C1 | WBS | AEC-Q100-001 AEC-Q003 | Wire Bond Shear Test: (Cpk > 1.67) | 30wire from 5pcs | Use 3lots CA- IF1042S- Q1/CA- IF1044VD-Q1 as generic data |
| C2 | WBP | MIL-STD883 AEC-Q003 | Wire Bond Pull: (Cpk > 1.67); Each bonder used | 30wire from 5pcs | |
| C3 | SD | JESD22-B102 JSTD-002D | Solderability: (>95% coverage) 8hr steam aging prior to testing | 1*15pcs | |
| C4 | PD | JESD22-B100 JESD22-B108 AEC-Q003 | Physical Dimensions: (Cpk > 1.67) | 3*10pcs | |
| C5 | SBS | AEC-Q100-010 AEC-Q003 | Solder Ball Shear: (Cpk > 1.67); 5 balls from min. of 10 devices | NA | Not Applicable |
| C6 | LI | JESD22 B105 | Lead Integrity: (No lead cracking or breaking); Through-hole only; 10 leads from each of 5 devices | NA | Not Applicable |

| Group | Item | Refer. | Test condition | QTY | Remark |
|---|------|-------------------|--|--------------------|-----------------|
| Test Group D - Die Fabrication Reliability Tests | | | | | |
| D1 | EM | JESD61 | Electromigration | | FAB TEST |
| D2 | TDDB | JESD35 | Time Dependent Dielectric Breakdown | | FAB TEST |
| D3 | HCI | JESD60 & 28 | Hot Carrier Injection | | FAB TEST |
| D4 | NBTI | JESD90 | Negative Bias Temperature Instability | | FAB TEST |
| D5 | SM | JESD61, 87, & 202 | Stress Migration | | FAB TEST |
| Group E- Electrical Verification | | | | | |
| E1 | TEST | per datasheet | Pre and Post Stress Electrical Test: | all | |
| E2 | HBM | AEC Q100-002 | HBM: 500V,1KV,2KV(Test @ Rm/Hot); | 3pcs/voltage level | |
| E3 | CDM | AEC-Q100-011 | CDM: 250V,500V,750V,1KV,2KV(Test @ Rm/Hot); | 3pcs/voltage level | |
| E4 | LU | AEC-Q100-004 | Latch-Up: (Test @ Rm/Hot) | 1*6pcs | |
| E9 | EMC | SAE J1752/3 | Electromagnetic Compatibility (Radiated Emissions) | 1*1pcs | |

5 Reliability Test Report

| Group | Item | Test Condition | QTY | Lot NO. | Result |
|---|--------|---|---|-----------|--------------------|
| Test Group A – Accelerated Environment Stress Tests | | | | | |
| A1 | PC | MSL 1 | Min. MSL = 3 | DUJ02217B | Pass |
| A2 | BHAST | 130°C, 85%RH 96hrs. Vcc=5.5V | 3*77pcs | DUJ02217B | Pass |
| A3 | UHAST | 130°C, 85%RH 96hrs. | 3*77pcs | DUJ02217B | Pass |
| A4 | TC | -65°C-150°C, 500cycles | 3*77pcs | DUJ02217B | Pass |
| | DPA-TC | DPA post TC 500cycle | 1*10pcs | DUJ02217B | Pass |
| A6 | HTSL | Ta=150°C, 1000hrs | 1*45pcs | DUJ02217B | Pass |
| Test Group B – Accelerated Lifetime Simulation Tests | | | | | |
| B1 | HTOL | Ta=150°C, 1000hrs, Vcc=5.5V, Vbat=27V, TTL signal input, F=5Mbps. | 3*77pcs | DUJ02217A | Pass |
| | | | | DUJ02217B | Pass |
| | | | | DUJ02224M | Pass |
| B2 | ELFR | Ta=150°C, 24hrs, Vcc=5.5V, Vbat=27V, TTL signal input, F=5Mbps. | 3*800pcs | DUJ02217A | Pass |
| | | | | DUJ02217B | Pass |
| | | | | DUJ02224M | Pass |
| Group C – Package Assembly Integrity Tests | | | | | |
| C1 | WBS | Wire Bond Shear Test: (Cpk > 1.67) | 30wire from 5pcs | 149AC01 | Pass, CPK=2.56 |
| C2 | WBP | Wire Bond Pull: (Cpk > 1.67); Each bonder used | 30wire from 5pcs | 149AC01 | Pass, CPK=6.04 |
| C3 | SD | Solderability: (>95% coverage) 8hr steam aging prior to testing | 1*15pcs | 149AC01 | Pass |
| C4 | PD | Physical Dimensions: (Cpk > 1.67) | 3*10pcs | 149AC01 | Pass |
| | | | | 149AC02 | Pass |
| | | | | 149AC03 | Pass |
| TEST GROUP D – Die Fabrication Reliability Tests | | | | | |
| D1 | EM | Electromigration | The Die Fabrication Reliability Tests are carried out for every fabrication site. The data, test method, calculations and internal criterial is available to the customer upon request. | | |
| D2 | TDDDB | Time Dependant Dielectric Breakdown | | | |
| D3 | HCI | Hot Carrier Injection | | | |
| D4 | NBTI | Negative Bias Temperature Instability | | | |
| D5 | SM | Stress Migration | | | |
| Group E- Electrical Verification | | | | | |
| E1 | TEST | Pre and Post Stress Electrical Test: | all | all | Pass |
| E2 | HBM | HBM: 500V,1KV,2KV (Test @ Rm/Hot); | 3pcs/voltage level | DUJ02217B | Pass 2KV class 2 |
| E3 | CDM | CDM: 250V,500V,750V,1KV,2KV(Test @ Rm/Hot); | 3pcs/voltage level | DUJ02217B | Pass 2KV class C6 |
| E4 | LU | Latch-Up: (Test @ Rm/Hot) | 1*6pcs | DUJ02217B | Pass, class II A |
| E9 | EMC | Electromagnetic Compatibility (Radiated Emissions) | 1*1pcs | DUJ02217B | Refer to Appendix1 |

注: Group A&C use CA-IF1042S-Q1 and CA-IF1044VD-Q1 result as generic data.

6 MTBF&FIT

| Supporting Data | | | | | | | | | MTBF (Hrs.) | FIT |
|-----------------|-----------------|----------|------|-------------|-------------------|----------------------|-----------------------|---------------------|----------------|------|
| Test Temp. | Test Voltage | Duration | QTY | Fail QTY | Operation Temp | Operation Voltage | Active energy (eV) | Confidence level | | |
| 150°C | 5.5V/27V | 7.39 | 231 | 0 | 55°C | 5V/27V | 0.7 | 60% | 1.35E+08 | 7.39 |
| 150°C | 5.5V/27V | 24hrs | 2400 | 0 | 55°C | 5V/27V | 0.7 | 60% | | |

7 Conclusion

All above test items conform to AEC-Q100 standard and test execute by 3rd Lab Chinaisti (Shanghai) Testing Technology Co., LT. CA-IF1021X-Q1 series products meet all test requirements, and all reliability test results are acceptable.

Statement

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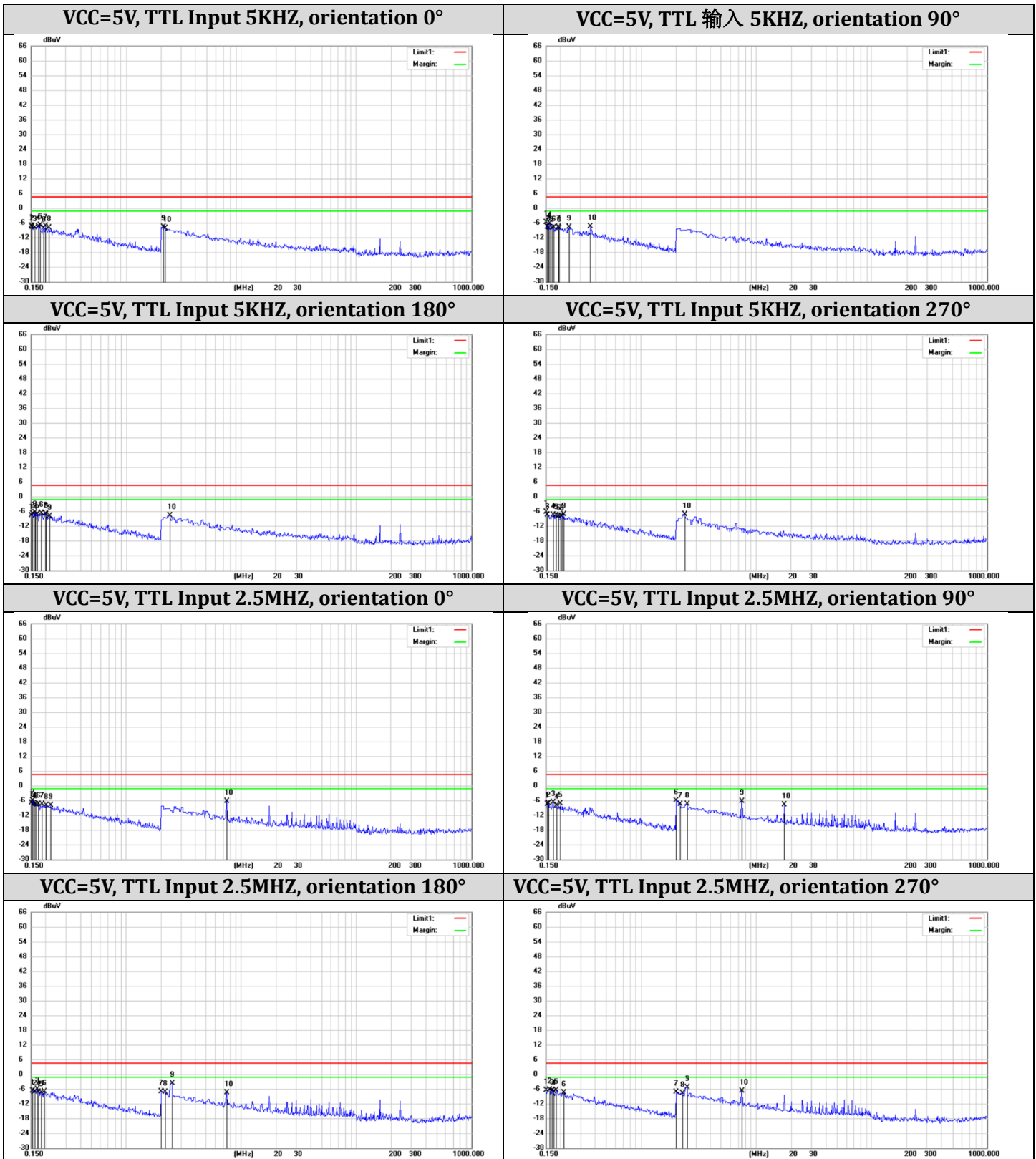
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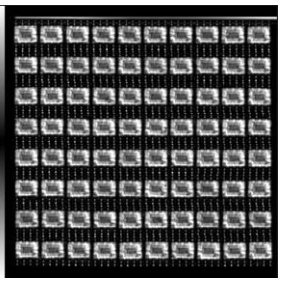
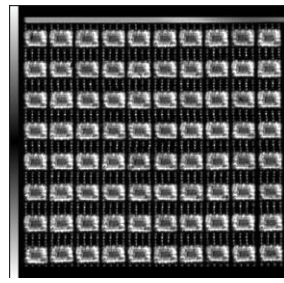
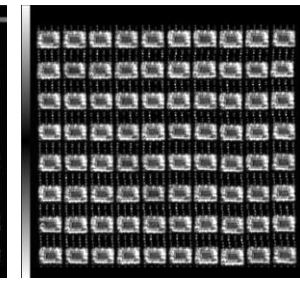
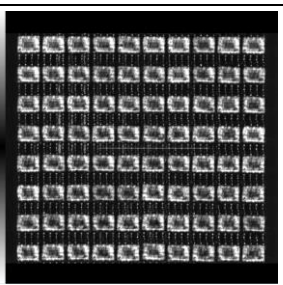
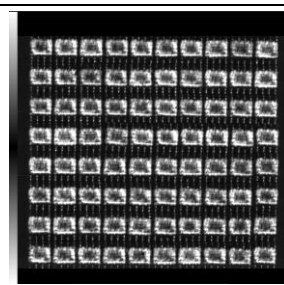
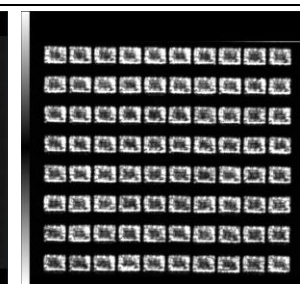
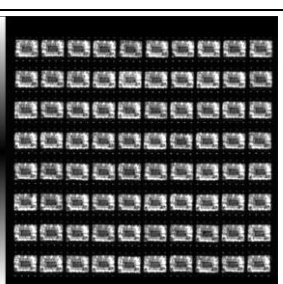
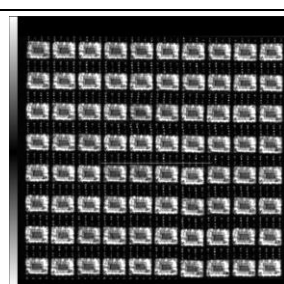
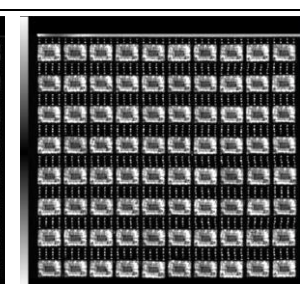
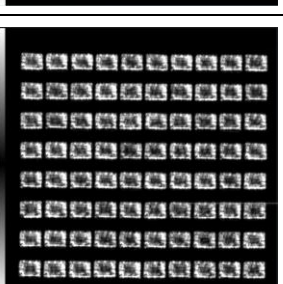
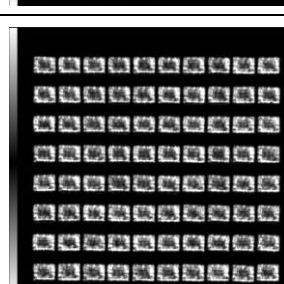
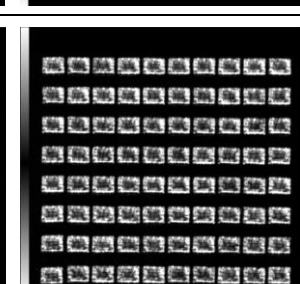
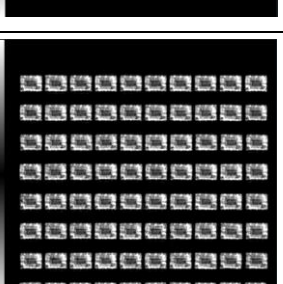
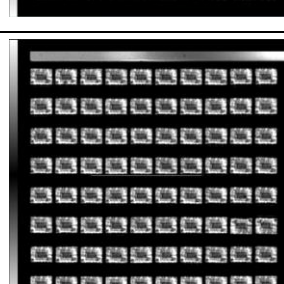
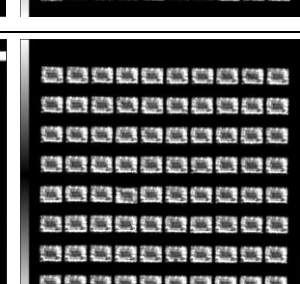
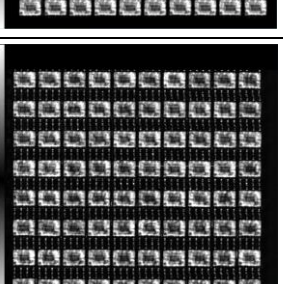
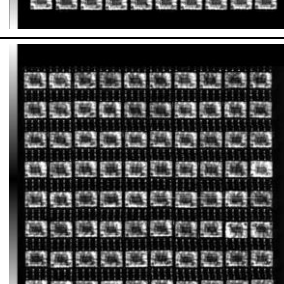
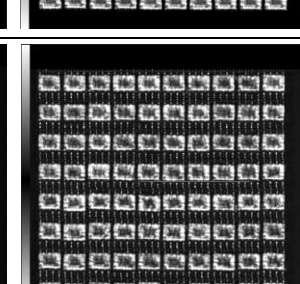
Version History

| Version | Change reason | Release Date |
|---------|------------------------------|--------------|
| Draft | Draft | Aug. 2022 |
| V1.0 | Formal version release | Nov. 2022 |
| V1.1 | Add DFN8 package qual result | Jan. 2023 |

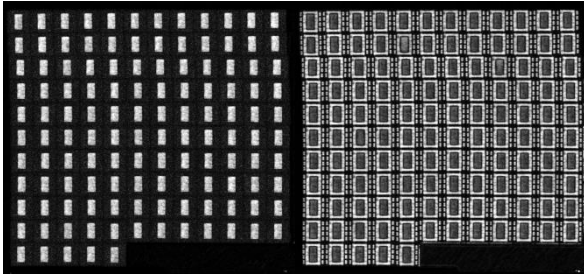
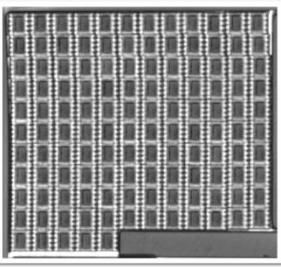
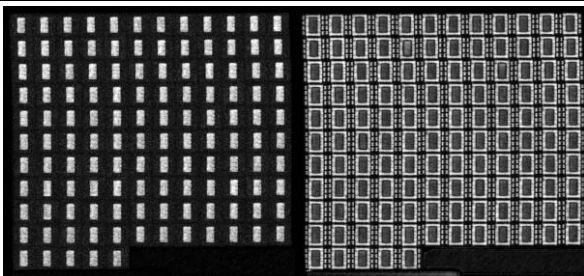
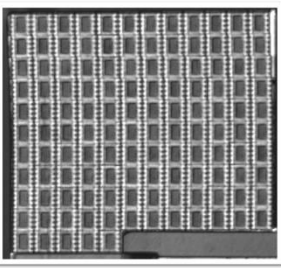
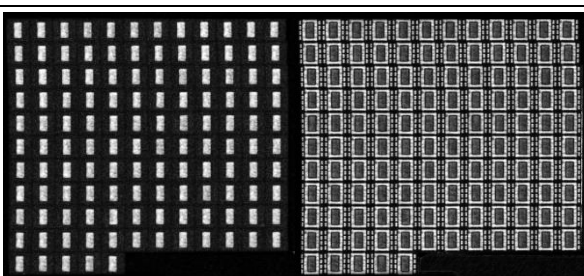
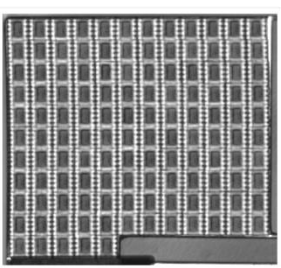
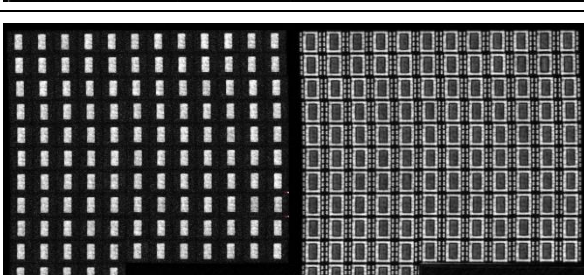
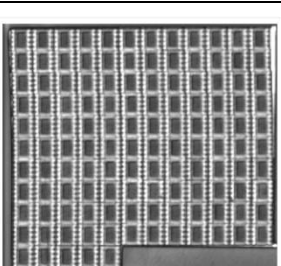
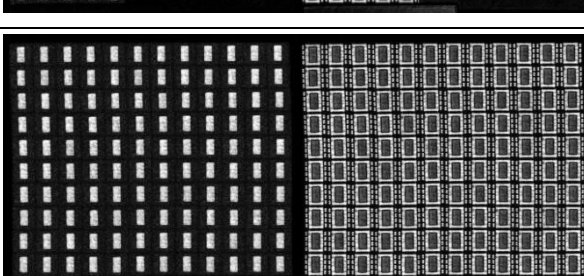
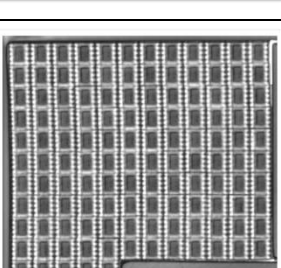
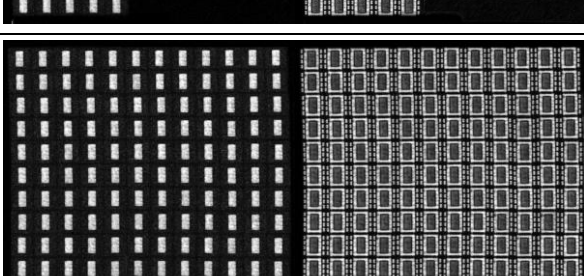
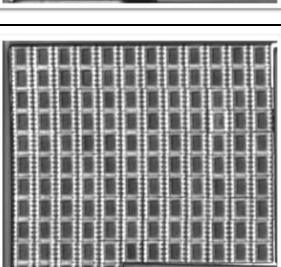
Appendix1 : EMC Test Result



Appendix2 : SAT result before and post MSL1(SOIC8)

| | | | | | |
|----------------------------------|--|---|--|---|--|
| <p>Lot 1 pre-MSL</p> | |  |  |  | |
| <p>Lot 1 post-MSL</p> | |  |  |  | |
| <p>Lot 2 pre-MSL</p> | |  |  |  | |
| <p>Lot 2 post-MSL</p> | |  |  |  | |
| <p>Lot 3 pre-MSL</p> | |  |  |  | |
| <p>Lot 3 post-MSL</p> | |  |  |  | |

Appendix3 : SAT result before and post MSL1(DFN8)

| | | |
|----------------------------------|--|---|
| <p>Lot 1 pre-MSL</p> |  |  |
| <p>Lot 1 post-MSL</p> |  |  |
| <p>Lot 2 pre-MSL</p> |  |  |
| <p>Lot 2 post-MSL</p> |  |  |
| <p>Lot 3 pre-MSL</p> |  |  |
| <p>Lot 3 post-MSL</p> |  |  |