



Reliability Qual Report

Product Series: CA-IS12XX & CA-IS13XX

Report Version: A2

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1 Summary

Chipanalog product quality and reliability test is a risk mitigation process designed to ensure the lifetime of device in customer application. There are a variety of methods for evaluating semiconductor wafer fabrication process and package-level reliability, which may include accelerated environmental test conditions followed by reduction to actual use conditions. The manufacturability assessment of chips includes verifying a robust assembly process, continuity of product production, and ensuring availability. According to the Joint Electronic Devices Engineering Committee (JEDEC) standards and procedures, the product evaluation of Chipanalog conforms to industry standard test methods.

2 Product Series List

Product Series		CA-IS12XX & CA-IS13XX
Package and Part NO.	DUB 8 (U)	CA-IS1200U
	SOIC8-WB (G)	CA-IS1200G/CA-IS1300G25G/CA-IS1300B25G/CA-IS1306M25G
	SOIC16-WB (W)	CA-IS1204W/CA-IS1306AM25W/CA-IS1305AM25W

Note:

Based on JEDEC Qualification family rule, the family qualification may be applied to similar components with the same fabrication process, design rules, and similar circuits. The same package structure, allowing different sizes and pin counts, with the same BOM, can be used as the same series group.

3 Product Information

3.1 Fab Information

Wafer ID	ZHUQUE	FUXI
Wafer Supplier	SMIC	SMIC
Wafer Process	BCDXXX	BCDXXX

3.2 Package Information

Assembly Site	SiMAT	SiMAT	SiMAT
FT Test Site	SiMAT	SiMAT	SiMAT
Package	DUB 8(U)	SOIC8-WB(G)	SOIC16-WB(W)
Lead Frame	Cu	Cu	Cu
Bond wire	20um Au	20um Au	20um Au
MSL Level	MSL3	MSL3	MSL3

4 Product Reliability Qualification Requirement

4.1 Device Reliability Test Requirement

Stress Test	Ref.	Abbv.	Conditions	Duration /Accept
Electrical Parameter Assessment	JESD86	ED	Per Datasheet	Per Datasheet
High Temperature Operating Life	JESD22-A108, JESD85	HTOL	TJ ≥ 125 °C Vcc ≥ Vcc max	1000 hrs/ 0 Fail
Human Body Model ESD	JS-001	ESD-HBM	TA = 25 °C	Classification
Charged Device Model ESD	JS-002	ESD-CDM	TA = 25 °C	Classification
Latch-Up	JESD7809	LU	Class I or Class II	0 Fail

4.2 Package Reliability Test Requirement

Stress Test	Ref.	Abbv.	Conditions	Duration /Accept
MSL	JESD22 - A113	PC	Per appropriate MSL level per J-STD-020	Electrical Test (optional)
High Temperature Storage	JESD22-A103 & A113	HTSL	150 °C, 1000hrs	1000 hrs / 0 Fail
Temperature Humidity Bias	JESD22-A101	THB	85 °C, 85 % RH, Vcc max	1000 hrs / 0 Fail
Highly Accelerated Temperature and Humidity Stress	JESD22-A110	HAST	130 °C / 110 °C, 85 % RH, Vcc max	96/264 hrs/ 0 Fail
Temperature Cycling	JESD22-A104	TCT	- 65 °C to +150 °C	500 cycles / 0 Fail
Unbiased Temperature/Humidity	JESD22-A102	AC	121 °C / 100% RH	96 hrs / 0 Fail
Bond Pull Strength	M2011	BPS	Characterization, Pre Encapsulation	Ppk≥1.66 or Cpk≥1.33
Bond Shear	JESD22-B116	BS	Characterization, Pre Encapsulation	Ppk≥1.66 or Cpk≥1.33
Solderability	M2003 JESD22-B102	SD	Characterization	0 Fail

Note: Either HAST or THB may be chosen.

5 Product Reliability Qualification Result

5.1 Device Reliability Test Result

Stress Test	Condition	Duration	Sample size	Result	Classification	Remark
ED	Per Datasheet	/	5*3lots	Pass	/	
HTOL	Ta=125°C, Vcc=5.5V	1000hrs	77*1lot	Pass	/	
ESD-HBM	Ta=25°C	/	3*1lot	Pass	Class 3A	DUB8
ESD-CDM	Ta=25°C	/	3*1lot	Pass	Class C3	DUB8
LU	Ta=25°C	/	3*1lot	Pass	Class I	DUB8
ESD-HBM	Ta=25°C	/	3*1lot	Pass	Class 3A	SOIC8-WB
ESD-CDM	Ta=25°C	/	3*1lot	Pass	Class C3	SOIC8-WB
LU	Ta=25°C	/	3*1lot	Pass	Class I	SOIC8-WB
ESD-HBM	Ta=25°C	/	3*1lot	Pass	Class 3A	SOIC16-WB
ESD-CDM	Ta=25°C	/	3*1lot	Pass	Class C3	SOIC16-WB
LU	Ta=25°C	/	3*1lot	Pass	Class I	SOIC16-WB

5.2 DUB 8 Package Reliability Test Result

Stress Test	Condition	Duration	Sample size	Result
PC	MSL 3	/	231*3lot	Pass
HTSL	Ta=150°C	1000hrs	45*1lot	Pass
HAST	130°C/100%RH/Vcc=5.5V	96hrs	77*3lot	Pass
TCT	-65°C to +150°C	500cycle	77*3lot	Pass
AC	121°C/100%RH	96hrs	77*3lot	Pass
SBS	M2011	/	30wire*5ea	Pass
BPS	JESD22-B116	/	30wire*5ea	Pass
SD	Steam aging 8hrs, 245°C dipping	/	22*1lot	Pass

5.3 SOIC8-WB Package Reliability Test Result

Stress Test	Condition	Duration	Sample size	Result
PC	MSL 3	/	231*3lot	Pass
HTSL	Ta=150°C	1000hrs	45*1lot	Pass
HAST	130°C/100%RH/Vcc=5.5V	96hrs	77*3lot	Pass
TCT	-65°C to +150°C	500cycle	77*3lot	Pass
AC	121°C/100%RH	96hrs	77*3lot	Pass
SBS	M2011	/	30wire*5ea	Pass
BPS	JESD22-B116	/	30wire*5ea	Pass
SD	Steam aging 8hrs, 245°C dipping	/	22*1lot	Pass

5.4 SOIC8-WB Package Reliability Test Result

Stress Test	Condition	Duration	Sample size	Result
PC	MSL 3	/	231*3lot	Pass
HTSL	Ta=150°C	1000hrs	45*1lot	Pass
HAST	130°C/100%RH/Vcc=5.5V	96hrs	77*3lot	Pass
TCT	-65°C to +150°C	500cycle	77*3lot	Pass
AC	121°C/100%RH	96hrs	77*3lot	Pass
SBS	M2011	/	30wire*5ea	Pass
BPS	JESD22-B116	/	30wire*5ea	Pass
SD	Steam aging 8hrs, 245°C dipping	/	22*1lot	Pass

6 Conclusion

All above test items conform to JEDEC standard and CA-IS12XX and CA-IS13XX series products meet all test requirements. All reliability test of CA-IS12XX and CA-IS13XX is acceptable.

Statement

The above information is for reference only and used to support better design and development of Chipanalog's customer. Chipanalog reserves the right to change the above information due to technical innovation without prior notice.

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Version History

Version	Change Reason	Release Date
A1	Initial	Mar. 2022
A2	1. Add SOIC8-WB and SOIC16-WB part NO.; 2. Add SOIC8-WB and SOIC16-WB reliability test result.	Jun. 2022