CA-IS2631HA High-performance, 2.5kV$_{RMS}$ Reinforced Digital Isolators with Integrated high-efficiency, Low-emissions DC-DC Converter

1 Features

- **Integrated High-efficiency DC-DC Converter withon-chip Transformer**
  - Regulated output options: 3.3 V or 5.0 V
  - Up to 500mW output power
  - Soft-start to limit inrush current and overshoot
  - Overload and short-circuit protection
  - Thermal shutdown
  - Low emissions
- **Robust Galvanic Isolation of Digital Signals**
  - High lifetime: > 40 years
  - Withstands 2.5kV$_{RMS}$ for 60s
  - ±150 kV/μs typical CMTI
  - Schmitt trigger inputs
- **Interfaces Directly with Most Micros and FPGAs**
  - Data rate: DC to 50Mbps
  - 3V to 5.5V single supply operation (VDDP)
  - 2.5V to 5.5V Individual logic supply input (VDDL)
  - Default output *High* (VO1, VO3) and *Low* (VO2)
- **Low propagation delay (25ns, typical)**
- **No Start-Up Initialization Required**
- **Small Package to Save PCB Area**
  - LGA16 (4.65mm × 5.2mm)
- **Wide operating temperature range: -40°C to 125°C**
- **Safety Regulatory Approvals (Pending)**
  - VDE 0884-11 Reinforced Isolation
  - UL According to UL1577

2 Applications

- Industrial automation systems
- Motor control
- Medical equipment
- Power instruments and equipment
- Low pressure energy storage

3 General Description

The CA-IS2631HA integrated signal and power isolation device simplifies system design and reduces board area. This device is high-performance, triple-channel, unidirectional digital isolators with up to 2.5kV$_{RMS}$ isolation rating and ultra-fast data rate. The integrated isolated DC-DC converter provides up to 500mW of isolated power and different output voltage configurations. Each isolation channel has a logic input and output buffer separated by capacitive silicon dioxide (SiO_2) insulation barrier, the integrated Schmitt trigger on each input provide excellent noise immunity. With these advanced features, the CA-IS2631HA digital isolator offers high electromagnetic immunity and low emissions while isolating different ground domains and block high-voltage/high-current transients from sensitive or human interface circuitry.

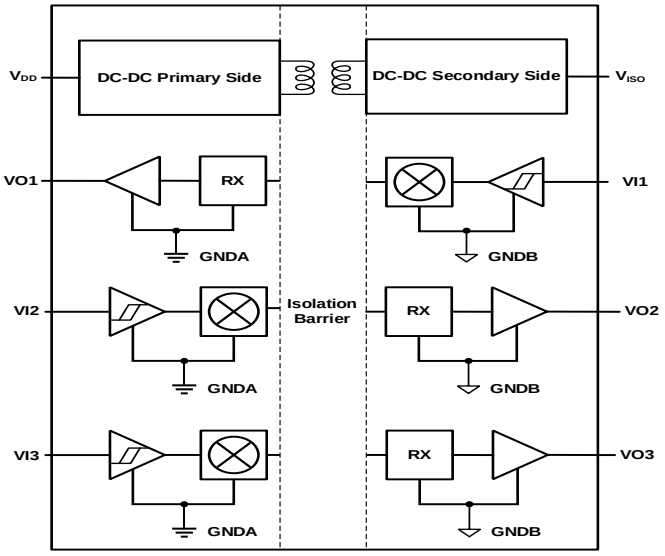
The CA-IS2631HA has 2 forward and 1 reverse-direction channels. It comes with enable control pin which can be used to put the driver output in high-impedance for the multi-master driving applications. The CA-IS2631HA also features different default outputs. When the input is either not powered or is open-circuit, the default output is high for driver output VO1/VO3 and low for driver output VO2.

The CA-IS2631HA is specified over the -40°C to +125°C operating temperature range and is available in LGA16 small package.

Device Information

PART NUMBER	PACKAGE	BODY SIZE(NOM)
CA-IS2631HA	LGA16	4.65mm × 5.2mm

Simplified Functional Diagram



4 Ordering Information

Table 4-1. Ordering Information

Ordering Part Number	Number of Inputs Primary-side (Side A)	Number of Inputs Secondary side (Side B)	Default Output	Isolation Rating (kV)	Package
CA-IS2631HA	2	1	VO1, VO3: high VO2: low	2.5	LGA16

Table of Contents

5 Revision History

Revision Number	Description	Page Changed
Version 1.00	N/A	N/A

6 Pin Configuration and Functions

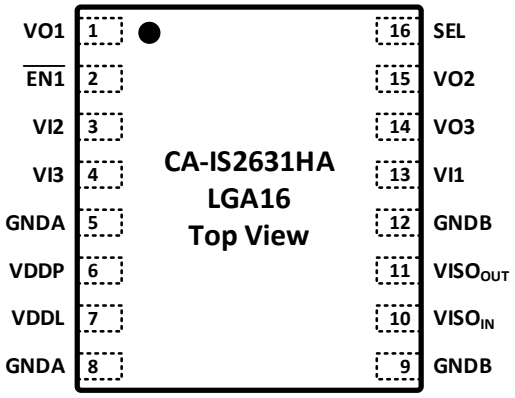


Figure 6-1. CA-IS2631HA pin configuration

Table 6-1. CA-IS2631HA Pin Description and Functions

Name	CA-IS2631HA Pin #	Type	Description
VO1	1	Logic output	Digital output 1 on primary-side (side A), VO1 is the logic output for the VI1 input on secondary side (side B), default output high.
$\overline{EN1}$	2	Logic input	Enable control input for driver output VO1 on side A, active low. Drive $\overline{EN1}$ high to put VO1 in high-impedance; Connect $\overline{EN1}$ to GNDA if not used. See Table 9-3 for more details.
VI2	3	Logic input	Digital input 2 on side A, corresponds to logic output 2 on secondary side (side B).
VI3	4	Logic input	Digital input 3 on side A, corresponds to logic output 3 on secondary side (side B).
GNDA	5, 8	Ground	Ground reference for side A.
VDDP	6	Supply	Power supply input for side A. Bypass to GNDA with 10μF||0.1μF capacitors. The capacitor should be placed as close as possible to this pin.
VDDL	7	Supply	Logic-supply input. V_{DDL} is the logic supply voltage for side-A input/output. Bypass to GNDA with a 1μF capacitor.
GNDB	9, 12	Ground	Ground reference for side B.
$VISO_{IN}$	10	Output voltage	Power supply input for secondary side. Connect this pin to $VISO_{OUT}$ externally on PCB. Bypass $VISO_{IN}$ to GNDB with a 1μF ceramic capacitor as close as possible to $VISO_{IN}$ pin.
$VISO_{OUT}$	11	Output voltage	Output of the isolated DC-DC converter. Bypass to GNDB with 10μF||0.1μF capacitors. The capacitor should be placed as close as possible to this pin.
VI1	13	Logic input	Digital input 1 on side B, corresponds to logic output 2 on side A.
VO3	14	Logic output	Digital output 3 on side B, VO3 is the logic output for the VI3 input on side A, default output high.
VO2	15	Logic output	Digital output 2 on side B, VO2 is the logic output for the VI2 input on side A, default output low.
SEL	16	Logic input	$VISO_{OUT}$ output selection pin, $VISO_{OUT}$ = 5 V, when SEL is connected to $VISO_{IN}$. $VISO_{OUT}$ = 3.3 V, when SEL is connected to GNDB. Don't leave this pin float, see Table 9-2 for more detail.

7 Specifications

7.1 Absolute Maximum Ratings[1, 2]

		MIN	MAX	UNIT
VDDP, VDDL	Supply voltage	-0.5	6.0	V
$VISO_{OUT}$, $VISO_{IN}$	Isolated supply voltage	-0.5	6.0	V
V_{IN}	Voltage at VIx, SEL pins	-0.5	V_{DDI} + 0.5[3]	V
I_O	Output current	-20	20	mA
T_J	Junction temperature		150	°C
T_{STG}	Storage temperature	-65	150	°C

Notes:

1. The stresses listed under "Absolute Maximum Ratings" are stress ratings only, not for functional operation condition. Exposure to absolute maximum rating conditions for extended periods may cause permanent damage to the device.
2. All voltage values are with respect to the local ground terminal (GNDA or GNDB) and are peak voltage values.
3. Maximum voltage must not be exceed 6 V, V_{DDI} is the voltage on the same side as the pin.

7.2 ESD Ratings

		VALUE	UNIT
V_{ESD} Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1]	±4000	V
	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[2]	±2000	

7.3 Recommended Operating Conditions

PARAMETER		MIN	TYP	MAX	UNIT
VDDP	Primary side supply Voltage	3		5.5	V
VDDL	Logic supply	2.5		5.5	V
I_{OH}	Low-level Output Current	–4			mA
I_{OL}	Low-level Output Current			4	mA
DR	Data Rate	0		50	Mbps
T_A	Ambient Temperature	–40	25	125	°C

7.4 Thermal Information

THERMAL METRIC		LGA16	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	TBD	°C/W

7.5 Power Rating

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_D	Maximum Power Dissipation	VDDP = VDDL = 5.5V, $VISO_{OUT}$ = 5V, I_{ISO} = 100mA, all the input signal is 50Mbps with 50% duty circle square and C_L = 15pF.			1	W

7.6 Insulation Specifications

PARAMETR		TEST CONDITIONS	VALUE A	UNIT
CLR	External clearance	Shortest terminal-to-terminal distance through air	3.45	mm
CPG	External creepage	Shortest terminal-to-terminal distance across the package surface	3.45	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	18	µm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	>400	V
	Material group	According to IEC 60664-1	II	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 300 V_{RMS}	I-IV	
		Rated mains voltage ≤ 400 V_{RMS}	I-IV	
		Rated mains voltage ≤ 600 V_{RMS}	I-III	
DIN V VDE V 0884-11:2017-01[1]				
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	566	V_{PK}
V_{IOWM}	Maximum working isolation voltage	AC voltage; Time dependent dielectric breakdown (TDDB) Test	400	V_{RMS}
		DC voltage	566	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t = 60 s (qualification); $V_{TEST} = 1.2 \times V_{IOTM}$, t= 1 s (100% production)	3535	V_{PK}
V_{IOSM}	Maximum surge isolation voltage[2]	Test method per IEC 60065, 1.2/50 µs waveform, $V_{TEST} = 1.6 \times V_{IOSM}$ (qualification)	5000	V_{PK}
q_{pd}	Apparent charge[3]	Method a, after input/output safety test subgroup 2/3, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)} = 1.2 \times V_{IORM}$, t_m = 10 s	≤5	pC
		Method a, after environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)} = 1.6 \times V_{IORM}$, t_m = 10 s	≤5	
		Method b1, at routine test (100% production) and preconditioning (type test) $V_{ini} = 1.2 \times V_{IOTM}$, t_{ini} = 1 s; $V_{pd(m)} = 1.875 \times V_{IORM}$, t_m = 1 s	≤5	
C_{IO}	Barrier capacitance, input to output[4]	V_{IO} = 0.4 × sin (2πft), f = 1 MHz	~3	pF
R_{IO}	Isolation resistance	V_{IO} = 500 V, T_A = 25°C	$>10^{12}$	Ω
		V_{IO} = 500 V, 100°C ≤ T_A ≤ 125°C	$>10^{11}$	
		V_{IO} = 500 V at T_S = 150°C	$>10^{9}$	
	Pollution degree		2	
UL[2]				
$V_{ISO(max)}$	Maximum withstanding isolation voltage	$V_{TEST} = V_{ISO}$, t = 60 s (qualification), $V_{TEST} = 1.2 \times V_{ISO}$, t = 1 s (100% production)	2500	V_{RMS}

Notes:

1. This coupler is suitable for “safe electrical insulation” only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
2. Devices are immersed in oil during surge characterization test.
3. The characterization charge is discharging charge (pd) caused by partial discharge.
4. Capacitance and resistance are measured with all pins on field-side and logic-side tied together.

7.7 Safety-Related Certifications

VDE	UL
Certified according to DIN V VDE V 0884-11:2017-01 Basic insulation: Maximum transient isolation voltage: 3535V_{pk} Maximum repetitive peak isolation voltage: 566V_{pk} Maximum surge isolation voltage: 5000V_{pk}	Certified according to UL 1577 Component Recognition Program LGA16: 2500 V_{RMS};
Certificate number: pending	Certificate number: pending

7.8 Electrical Characteristics

VDDP = VDDL, $VISO_{OUT}$ = $VISO_{IN}$, T_A = -40 to 125°C, (over recommended operating conditions, unless otherwise specified).

Parameters		Test Conditions	Min	Typ	Max	Unit
$VDDP_{(UVLO+)}$	V_{DDP} undervoltage threshold when supply voltage is rising		2.5	2.7	2.9	V
$VDDP_{(UVLO-)}$	V_{DDP} undervoltage threshold when supply voltage is falling		2.1	2.3	2.5	V
$V_{HYS(UVLO)}$	V_{DDP} undervoltage threshold hysteresis			0.4		V
$VDDL_{(UVLO+)}$	V_{DDL} undervoltage threshold when supply voltage is rising		2.05	2.25	2.45	V
$VDDL_{(UVLO-)}$	V_{DDL} undervoltage threshold when supply voltage is falling		1.9	2.1	2.3	V
$V_{HYS(UVLO)}$	V_{DDL} undervoltage threshold hysteresis			0.15		V
V_{IH}	Input high voltage		0.7 × V_{DDI}[1]			V
V_{IL}	Input low voltage				0.3 × V_{DDI}[1]	V
V_{HYS}	Input hysteresis			0.1 × V_{DDI}[1]		V
I_{IH}	High-level input leakage current	V_{IH} = V_{DDI}[1] @ VIx or SEL			20	μA
I_{IL}	Low-level input leakage current	V_{IL} = 0V @ VIx or SEL	–20			μA
V_{OH}	High-level output voltage	I_{OH}=-4mA, See Figure 8-1	V_{DDO}[1] – 0.4	V_{DDO}[1] – 0.2		V
V_{OL}	Low-level output voltage	I_{OL}=4mA, See Figure 8-1		0.2	0.4	V
CMTI	Common-mode transient immunity	V_I = V_{DDI}[1] or 0V, V_{CM}=1000V, see Figure 8-2	100	150		kV/μs

Note:
V_{DDI} = input side supply; V_{DDO} = output side supply.

7.9 Power Supply Characteristics

7.9.1 5V Input, 5V Output

VDDP = VDDL, $VISO_{OUT}$ = $VISO_{IN}$, T_A = -40 to 125°C, (over recommended operating conditions, unless otherwise specified).

Parameters		Test Conditions	Min.	Typ.	Max.	Unit
$VISO_{OUT}$	Isolated supply voltage	I_{ISO} = 0 to 80mA	4.67	5.07	5.43	V
I_{ISO}	Maximum load current[1]	Data-rate of each channel: DR<1Mbps	80	100		mA
$VISO_{(LINE)}$	DC line regulation	I_{ISO}=40mA, V_{DD}=4.5V to 5.5V		2		mV/V
$VISO_{(LOAD)}$	DC load regulation	I_{ISO}=0 to 80mA		0.4		%
EFF	Efficiency@maximum load current	I_{ISO} = 80mA，C_{LOAD} = 0.1μF || 10μF；V_I = 0V		51		%
I_{SCC_SC}	VISO supply current	VISO shorted to GNDB		50	75	mA
$VISO_{(RIP)}$	Output ripple on isolated supply(pk-pk)			60		mV
I_{DD}	Supply current	No load, V_I = 0V		10	15	mA
		No load, V_I = V_{DDI}[2]		8	12	
		Apply 1MHz, 50% duty cycle square wave at each input, C_L = 15pF, no external load.		9	14	
		Apply 10MHz, 50% duty cycle square wave at each input, C_L = 15pF, no external load.		11	18	
		Apply 50MHz, 50% duty cycle square wave at each input, C_L = 15pF, no external load.		20	30	

Notes:
1. The maximum VISO output current will be decreased with the data rate increased ta each isolation channel. Also, the available output current will be reduced when T_A > 85˚C.
2. V_{DDI} = input side supply.

7.9.2 5V Input, 3.3V Output

VDDP = VDDL, $VISO_{OUT}$ = $VISO_{IN}$, T_A = -40 to 125°C, (over recommended operating conditions, unless otherwise specified).

Parameters		Test Conditions	Min.	Typ.	Max.	Unit
VISO	Isolated supply voltage	I_{ISO} = 0 to 100mA	3.09	3.34	3.59	V
I_{ISO}	Maximum load current[1]	Data-rate of each channel: DR<1Mbps	100	120		mA
$VISO_{(LINE)}$	DC line regulation	I_{ISO}=50mA, V_{DD}=4.5V to 5.5V		2		mV/V
$VISO_{(LOAD)}$	DC load regulation	I_{ISO}=0 to 100mA		0.8		%
EFF	Efficiency@maximum load current	I_{ISO} = 100mA， C_{LOAD} = 0.1μF || 10μF；V_I = 0V		41		%
I_{SCC_SC}	VISO supply current	VISO shorted to GNDB		50	75	mA
$VISO_{(RIP)}$	Output ripple on isolated supply(pk-pk)			50		mV
I_{DD}	Supply current	No load, V_I = 0V		9	14	mA
		No load, V_I = V_{DDI}[2]		7	11	
		Apply 1MHz, 50% duty cycle square wave at each input, C_L = 15pF, no external load.		8	12	
		Apply 10MHz, 50% duty cycle square wave at each input, C_L = 15pF, no external load.		10	15	
		Apply 50MHz, 50% duty cycle square wave at each input, C_L = 15pF, no external load.		15	23	

Notes:
1. The maximum $VISO_{OUT}$ output current will be decreased with the data rate increased ta each isolation channel. Also, the available output current will be reduced when T_A > 85˚C.
2. V_{DDI} = input side supply.

7.9.3 3.3V Input, 3.3V Output

VDDP = VDDL, $VISO_{OUT}$ = $VISO_{IN}$, T_A = -40 to 125°C, (over recommended operating conditions, unless otherwise specified).

Parameters		Test Conditions	Min.	Typ.	Max.	Unit
VISO	Isolated supply voltage	I_{ISO} = 0 to 40mA	3.09	3.34	3.59	V
I_{ISO}	Maximum load current[1]	Data-rate of each channel: DR<1Mbps	40	60		mA
$VISO_{(LINE)}$	DC line regulation	I_{ISO}= 20mA, V_{DD}=3.0V to 3.6V		2		mV/V
$VISO_{(LOAD)}$	DC load regulation	I_{ISO}=0 to 40mA		1		%
EFF	Efficiency@maximum load current	I_{ISO} = 50mA， C_{LOAD} = 0.1μF || 10μF；V_I = 0V		47		%
I_{SCC_SC}	VISO supply current	VISO shorted to GNDB		36	54	mA
$VISO_{(RIP)}$	Output ripple on isolated supply(pk-pk)			45		mV
I_{DD}	Supply current	No load, V_I = 0V		10	15	mA
		No load, V_I = V_{DDI}[2]		8	12	
		Apply 1MHz, 50% duty cycle square wave at each input, C_L = 15pF, no external load.		9	14	
		Apply 10MHz, 50% duty cycle square wave at each input, C_L = 15pF, no external load.		10	15	
		Apply 50MHz, 50% duty cycle square wave at each input, C_L = 15pF, no external load.		17	24	

Notes:
1. The maximum $VISO_{OUT}$ output current will be decreased with the data rate increased ta each isolation channel. Also, the available output current will be reduced when T_A > 85˚C.
2. V_{DDI} = input side supply.

7.10 Timing Characteristics

7.10.1 5V Input, 5V Output

VDDP = VDDL, $VISO_{OUT}$ = $VISO_{IN}$, T_A = -40 to 125°C, (over recommended operating conditions, unless otherwise specified).

Parameters		Test Conditions	Min	Typ.	Max	Unit
DR	Data rate		0		50	Mbps
t_{PLH}, t_{PHL}	Propagation Delay Time	See Figure 8-1		25	40	ns
PWD	Pulse Width Distortion $\lvert t_{PLH} - t_{PHL} \rvert$			3	10	ns
t_{sk}	Channel-to-channel Output Skew Time[1]			3	8	ns
t_r	Output Signal Rise Time	See Figure 8-1		1.6	4.0	ns
t_f	Output Signal Fall Time			1.6	4.0	ns

Note:

1. t_{sk} is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.

7.10.2 5V Input, 3.3V Output

VDDP = VDDL, $VISO_{OUT}$ = $VISO_{IN}$, T_A = -40 to 125°C, (over recommended operating conditions, unless otherwise specified).

Parameters		Test Conditions	Min	Typ.	Max	Unit
DR	Data rate		0		50	Mbps
t_{PLH}, t_{PHL}	Propagation Delay Time	See Figure 8-1		25	40	ns
PWD	Pulse Width Distortion $\lvert t_{PLH} - t_{PHL} \rvert$			3	10	ns
t_{sk}	Channel-to-channel Output Skew Time[1]			3	8	ns
t_r	Output Signal Rise Time	See Figure 8-1		1.6	4.0	ns
t_f	Output Signal Fall Time			1.6	4.0	ns

Note:

1. t_{sk} is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.

7.10.3 3.3V Input, 3.3V Output

VDDP = VDDL, $VISO_{OUT}$ = $VISO_{IN}$, T_A = -40 to 125°C, (over recommended operating conditions, unless otherwise specified).

Parameters		Test Conditions	Min	Typ.	Max	Unit
DR	Data rate		0		50	Mbps
t_{PLH}, t_{PHL}	Propagation Delay Time	See Figure 8-1		25	40	ns
PWD	Pulse Width Distortion $\lvert t_{PLH} - t_{PHL} \rvert$			3	10	ns
t_{sk}	Channel-to-channel Output Skew Time[1]			3	8	ns
t_r	Output Signal Rise Time	See Figure 8-1		1.6	4.0	ns
t_f	Output Signal Fall Time			1.6	4.0	ns

Note:

1. t_{sk} is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.

7.11

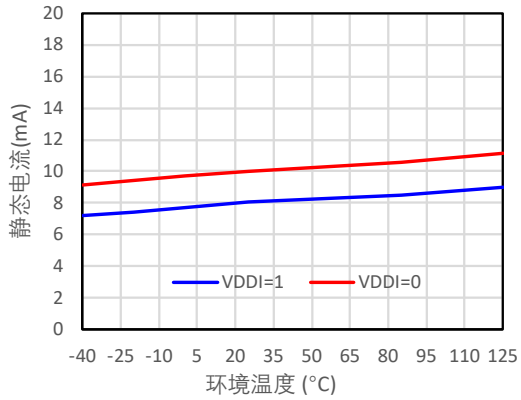


Figure 8.11-1
V_{DD} quiescent current, all input connected to logic HIGH or logic LOW
VDDP = 5V， $VISO_{OUT}$ = 5V

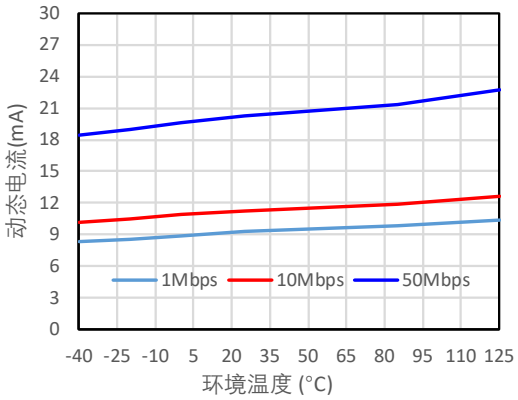


Figure 8.11-2
V_{DD} supply current for the CA-IS2631HA at different data rate
VDDP = 5V， $VISO_{OUT}$ = 5V

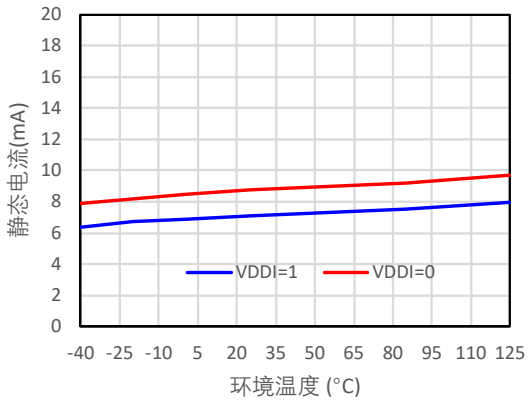


Figure 8.11-3
V_{DD} quiescent current, all input connected to logic HIGH or logic LOW
VDDP = 5V， $VISO_{OUT}$ = 3.3V

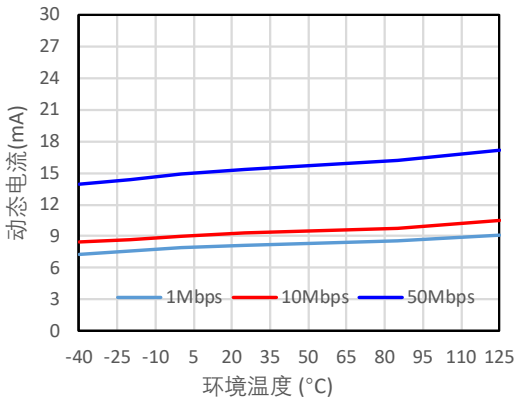


Figure 8.11-4
V_{DD} supply current for the CA-IS2631HA at different data rate
VDDP = 5V， $VISO_{OUT}$ = 3.3V

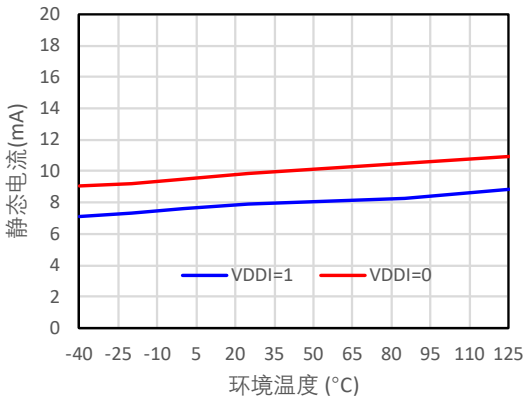


Figure 8.11-5
V_{DD} quiescent current, all input connected to logic HIGH or logic LOW
VDDP = 3.3V， $VISO_{OUT}$ = 3.3V

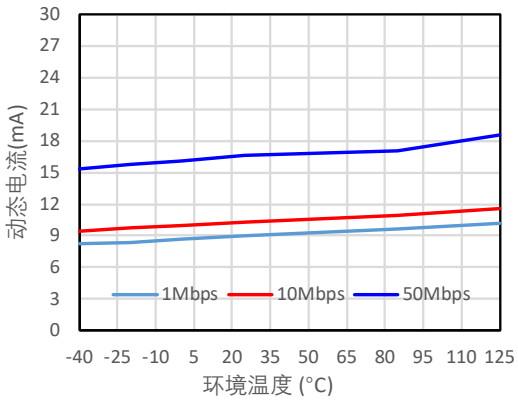


Figure 8.11-6
V_{DD} supply current for the CA-IS2631HA at different data rate
VDDP = 3.3V， $VISO_{OUT}$ = 3.3V

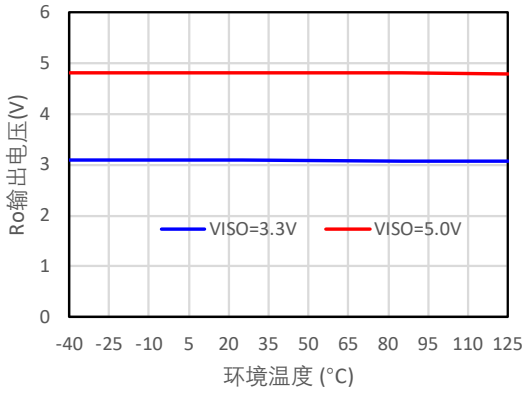


Figure 8.11-7
R_O = High, pull-down current = 4mA

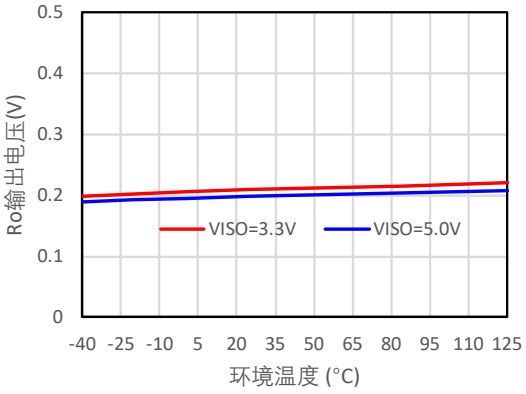


Figure 8.11-8
R_O = Low， pull-up current = 4mA

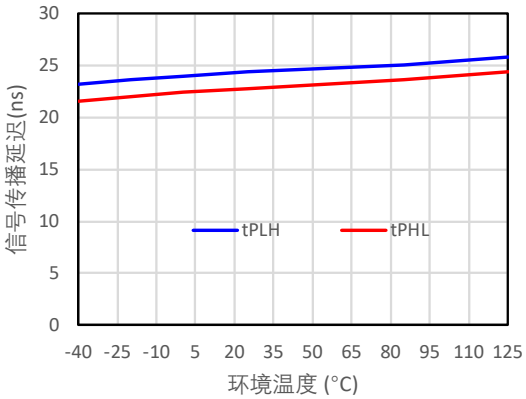


Figure 8.11-9
Propagation delay time vs. temperature, V_{DD} = 5V， V_{ISO} = 5V

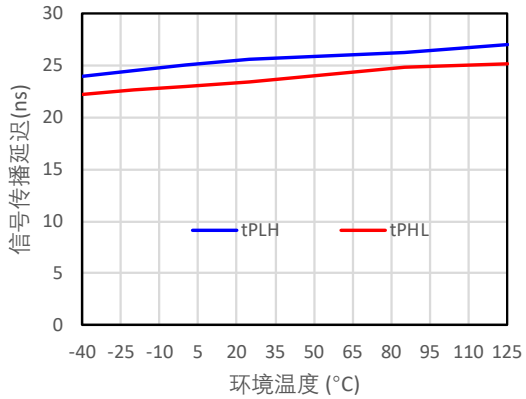


Figure 8.11-10
Propagation delay time vs. temperature, V_{DD} = 3.3V， V_{ISO} = 3.3V

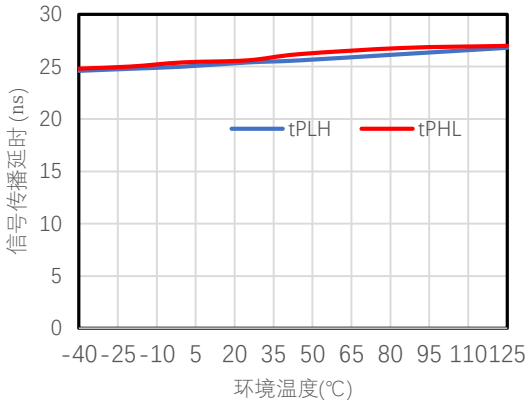


Figure 8.11-11
Propagation delay time vs. temperature, V_{DD} = 5V， V_{ISO} = 3.3V

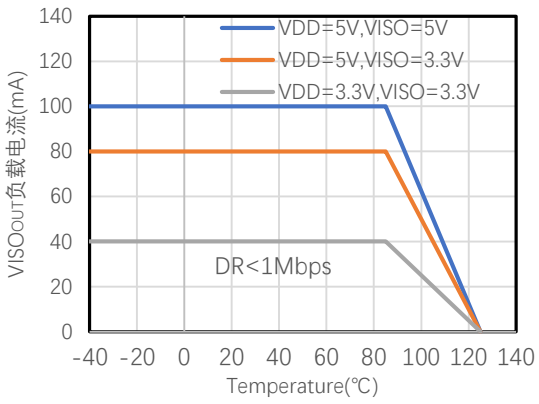


Figure 8.11-11
Maximum output current from V_{ISO} vs. temperature
DR < 1Mbps

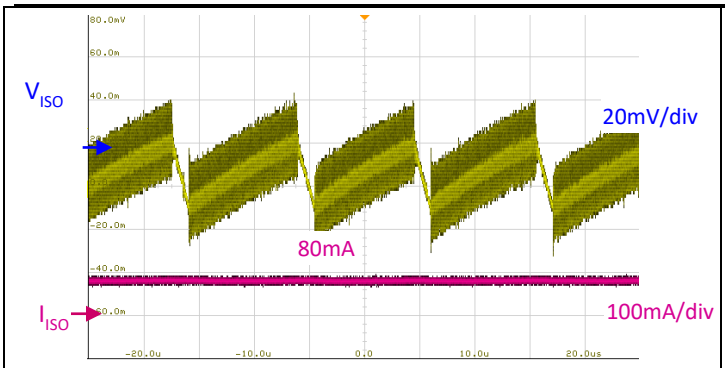


Figure 8.11-12
VDD= 5V, $VISO_{OUT}$ = 5V, R_L = NC between A and B
V_{ISO} ripple voltage@ 80mA load current: 66mV

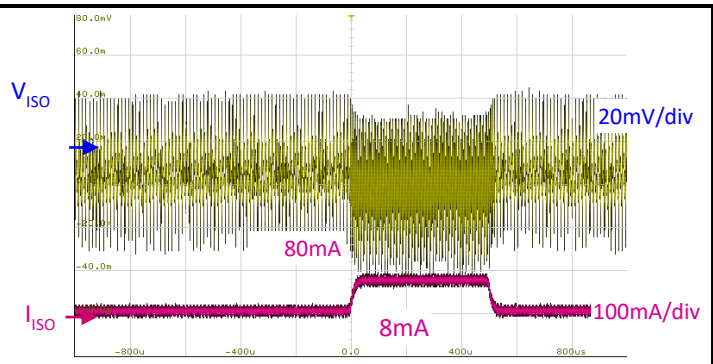


Figure 8.11-13
VDD = 5V, $VISO_{OUT}$ = 5V, R_L = NC between A and B
8 mA to 80mA load transient response;
V_{ISO} ripple voltage (pick to pick): 80mV

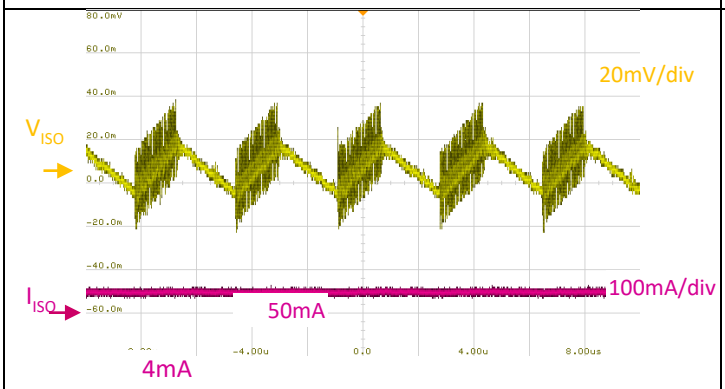


Figure 8.11-14
VDD= 5V, $VISO_{OUT}$ = 3.3V, R_L = NC between A and B
V_{ISO} ripple voltage@ 50mA load current: 55mV

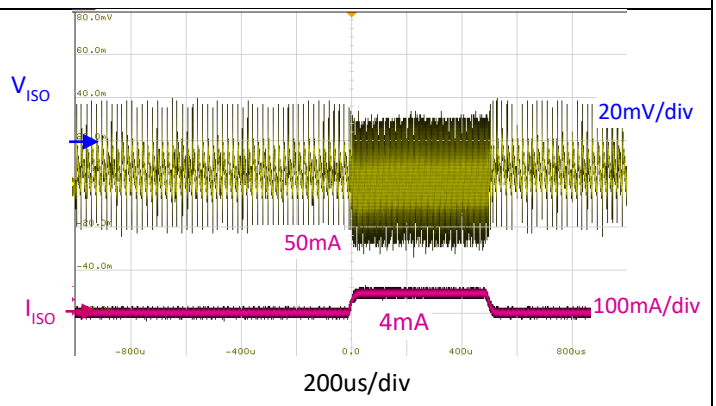


Figure 8.11-15
VDD = 5V, $VISO_{OUT}$ = 3.3V, R_L = NC between A and B
4 mA to 50mA load transient response;
V_{ISO} ripple voltage (pick to pick): 70mV

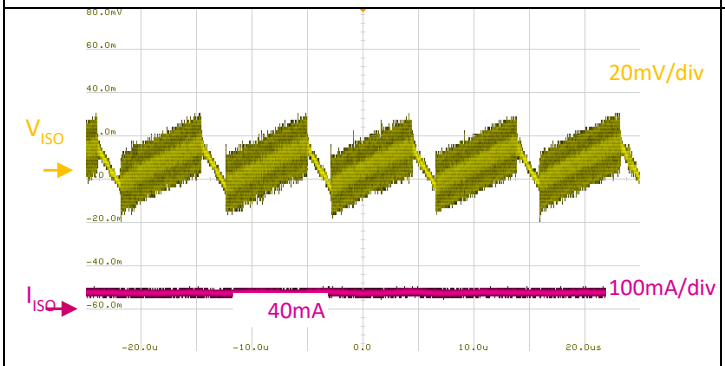


Figure 8.11-17
VDD= 3.3V, $VISO_{OUT}$ = 3.3V, R_L = NC between A and B
V_{ISO} ripple voltage@ 40mA load current: 45mV

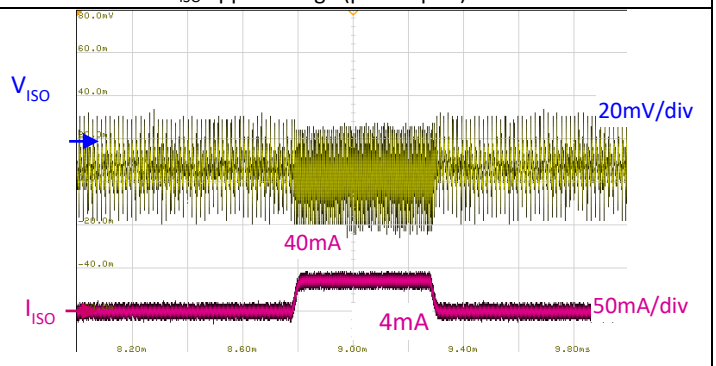


Figure 8.11-18
VDD = 3.3V, $VISO_{OUT}$ = 3.3V, R_L = NC between A and B
4 mA to 40mA load transient response;
V_{ISO} ripple voltage (pick to pick): 50mV

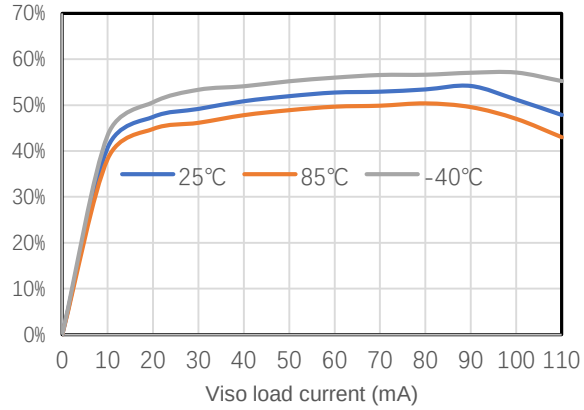


Figure 8.11-16
Efficiency vs. load current (I_{ISO}) at different ambient temperature,
V_{DD} = 5V， V_{ISO} = 5V

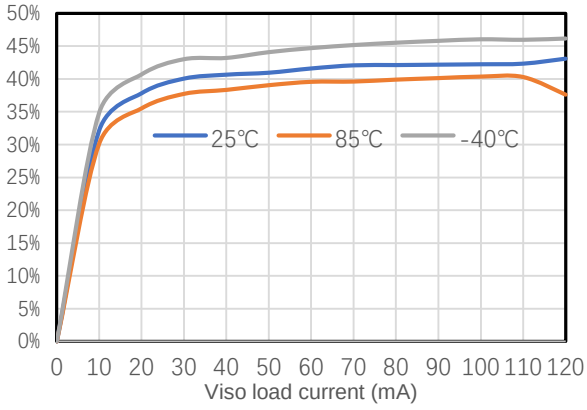


Figure 8.11-20
Efficiency vs. load current (I_{ISO}) at different ambient temperature,
V_{DD} = 5V， V_{ISO} = 3.3V

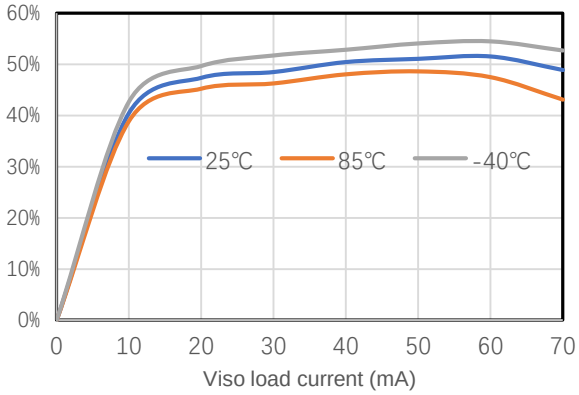
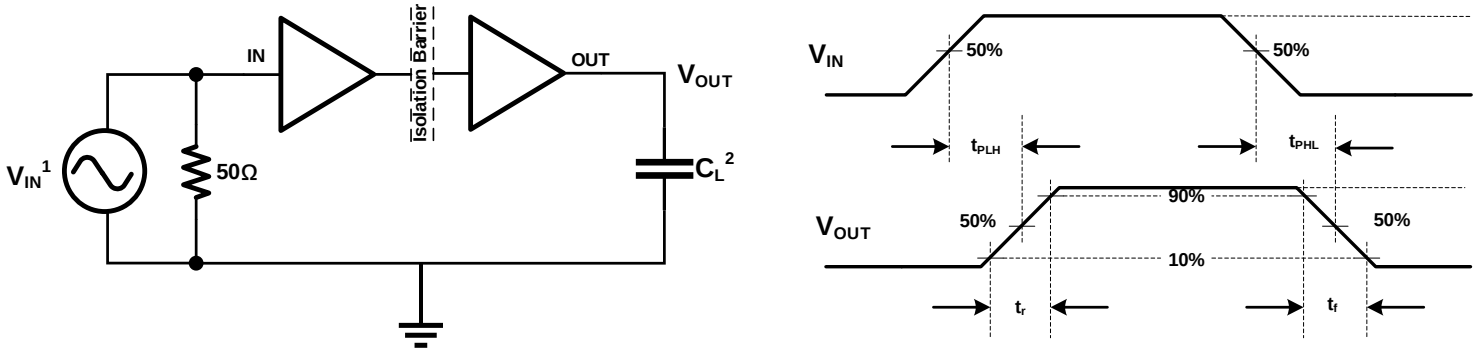


Figure 8.11-21
Efficiency vs. load current (I_{ISO}) at different ambient temperature,
V_{DD} = 3.3V， V_{ISO} = 3.3V

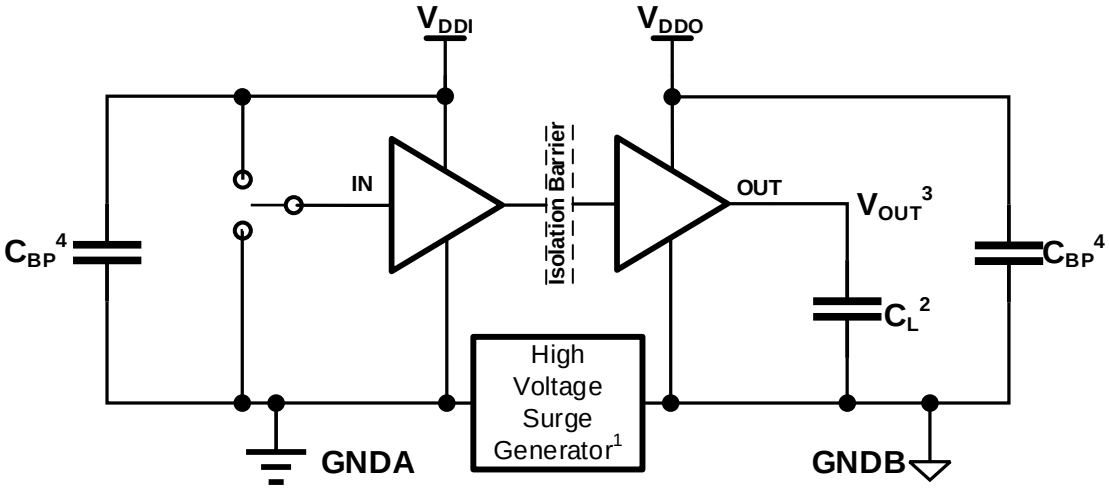
8 Parameter Measurement Information



Notes:

1. A square wave generator provide V_{IN} input signal with characteristics of frequency ≤100kHz, 50% duty cycle, tr≤3ns, t_f≤3ns, Zout = 50Ω. At the input, 50 Ω resistor is required to terminate input generator signal. It is not needed in actual application.
2. C_L = 15pF, includes external circuit (instrumentation and fixture etc.) capacitance. Since the load capacitance influence the output rising time, it's a key factor in the timing characteristic measurement.

Figure 8-1. Timing Characteristics Test Circuit and Voltage Waveforms



Notes:

1. The High Voltage Surge Generator generates repetitive high voltage surges with > 1.5kV amplitude, rise time <10ns and fall time <10ns, to reach common-mode transient noise with > 150kV/μs slew rate.
2. C_L = 15pF and includes external circuit (instrumentation and fixture etc.) capacitance.
3. Pass-fail criteria: the output must remain stable.
4. C_{BP} (0.1 ~ 1uF) is bypass capacitance.

Figure 8-2. Common-Mode Transient Immunity Test Circuit

9 Detailed Description

9.1 Overview

The CA-IS2631HA device integrates most of the components needed for digital isolation application, a high-efficiency, low-emissions isolated DC-DC converter with internal transformer and high-speed isolated data channels, into a single compact LGA16 package. This results an efficient and compact fully integrated solution that complies with EMI requirements and makes system level design as easy as possible.

The CA-IS2631HA device offers triple-channel digital galvanic isolators using Chipanalog's full differential capacitive isolation technology. This device has an ON-OFF keying (OOK) modulation scheme to transfer digital signals across the SiO_2 based isolation barrier between circuits with different power domains. The transmitter sends a high frequency carrier across the barrier to represent one digital state and sends no signal to represent the another digital state. The receiver demodulates the signal and recovery input signal at output through a buffer stage. With this OOK architecture, the CA-IS2631HA device builds a robust data transmission path between different power domains, without any special start-up initialization requirements. This digital isolator also incorporate advanced full differential techniques to maximize the CMTI performance and minimize the radiated emissions due to the high frequency carrier and I/O buffer switching.

The internal DC-DC converter uses switched mode operation and proprietary PWM feedback circuit techniques to provide high efficiency and low radiated emissions. Undervoltage lockout (UVLO) with hysteresis is integrated on the VDDP and VDDL supplies which ensures robust system performance under noisy conditions. An integrated soft-start mechanism ensures controlled inrush current and avoids any overshoot on the output during power-up.

9.2 Functional Block Diagram

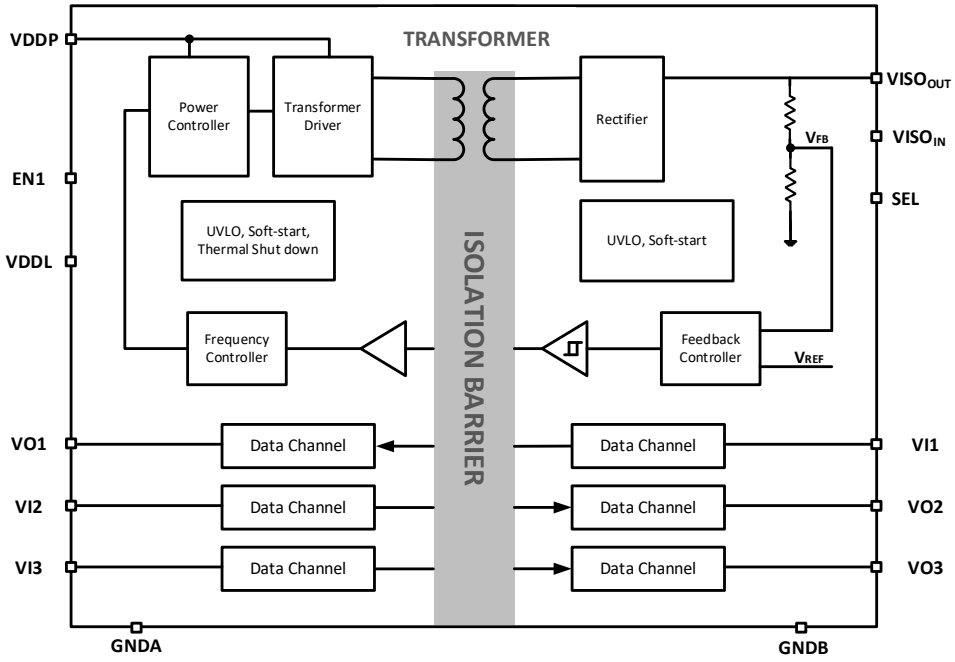


Figure 9-1. Functional Block Diagram of CA-IS2631HA

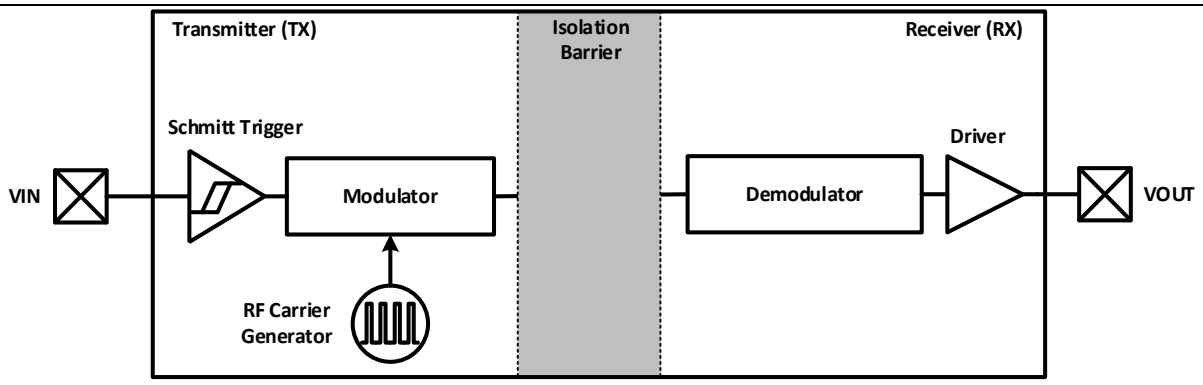


Figure 9-2. Functional Block Diagram of a Single Channel

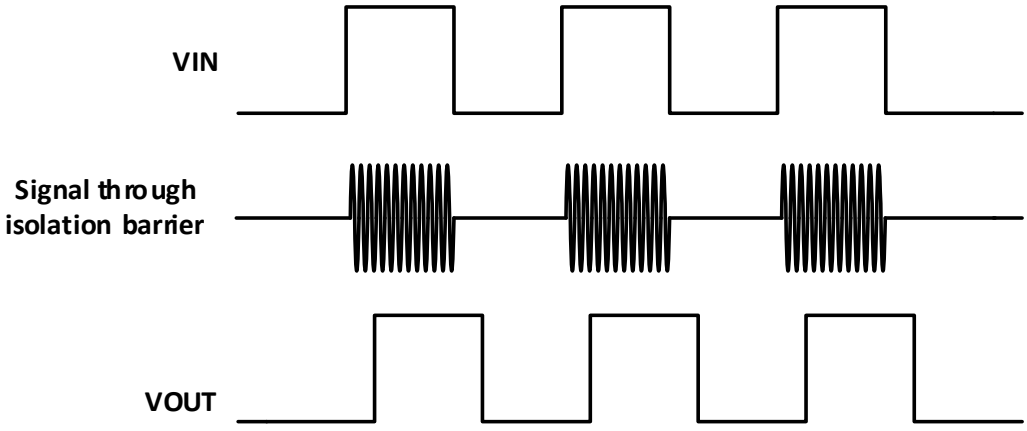


Figure 9-3. Operation Waveforms of a Single Channel

9.3 Undervoltage Lockout

The CA-IS2631HA has undervoltage detection on both VDDP and VDDL supply terminals, that place the driver outputs to high-impedance once an undervoltage condition is detected at VDDP or VDDL . See Table 9-1 for more detail.

Table 9-1. CA-IS2631HA driver output @ different power supplu status

VDDP	VDDL	Output on Primary-side (side A)	$VISO_{OUT}$	Output on Secondary side (side B)
PD	PD	High Impedance	No Output	High Impedance
PD	PU	Normal operation	No Output	High Impedance
PU	PD	High Impedance	No Output	High Impedance
PU	PU	Normal operation	Normal Output	Normal operation

Notes:
1. X = don't care.
2. PU = power up (PU = VDDP ≥ $VDDP_{(UVLO+)}$ and VDDL ≥ $VDDL_{(UVLO+)}$; PD = power down (VDDP < $VDDP_{(UVLO-)}$ and VDDL < $VDDL_{(UVLO-)}$.

9.4 Thermal shutdown

If the junction temperature of the CA-IS2631HA device exceeds the thermal shutdown threshold $T_{J(shutdown)}$ (180°C, typ.),output Voltage $VISO_{OUT}$ shutdown. The shutdown condition is cleared when the junction temperature drops to normal operation temperature range (< 160°C, typ.) of the device.

9.5 Isolated Supply Output

The integrated isolated DC-DC converter based on PWM control structure provides up to 500mW of isolated power and different output voltage configurations. The VDDP supply is provided to the primary of power controller that switches the power stage connected to the integrated high-Q transformer. The output voltage $VISO_{OUT}$ is monitored and a PWM signal based on feedback information is conveyed to the supply primary side through a dedicated isolation channel, the PWM duty cycle of the primary switching stage is adjusted accordingly. Power is transferred to the secondary side of transformer, internal rectified and regulated to either 3.3 V or 5 V, depending on the SEL pin status, see Table 9-2 for the supply configurations of CA-IS2631HA device. Note that the value of I_{ISO} in Electrical Characteristics is the typical output current at +25°C. With the increase of temperature, especially when the temperature exceeds +85°C, the maximum load current will be decreased.

Table 9-2. Supply Configuration[1]

Supply Voltage VDDP (V)	SEL[2]	$VISO_{OUT}$、$VISO_{IN}$ (V)
4.5~5.5	Shorted to $VISO_{IN}$	5
4.5~5.5	Shorted to GNDB	3.3
3.0~3.6	Shorted to GNDB	3.3

Notes:

1. VDDP = 3.3 V, SEL shorted to $VISO_{OUT}$ (essentially V_{ISO} = 5 V) is not recommended.
2. The SEL pin has a weak pull-down internally. However, for V_{ISO} = 3.3 V, the SEL pin should be connected to the GNDB externally, especially in the noisy system.
3. Connect SEL pin to a fixed state (GNDB or $VISO_{IN}$) before the device power up. Do not change SEL pin state during power on.

10 Application and Implementation

10.1 Typical Application Circuit

The CA-IS2631HA isolation IC provides complete galvanic isolation between two power domains, protecting circuits from high common-mode transients and faults, eliminating ground loops. In many applications, digital isolators are replacing optocouplers because they can reduce the power requirements and take up less board space while offering the same isolation capability. Unlike optocouplers, which require external components to improve performance, provide bias, or limit current, the CA-IS2631HA device integrated both signal and power isolation, only require few external bypass capacitors to operate, and save an external isolated power supply on the secondary side (side B), help designers to simplify system-level design and reduces board area. Small size and high integration make this device ideal for applications that have limited board space and desire more integration. Figure 10-1 shows typical operating circuit of the CA-IS2631HA.

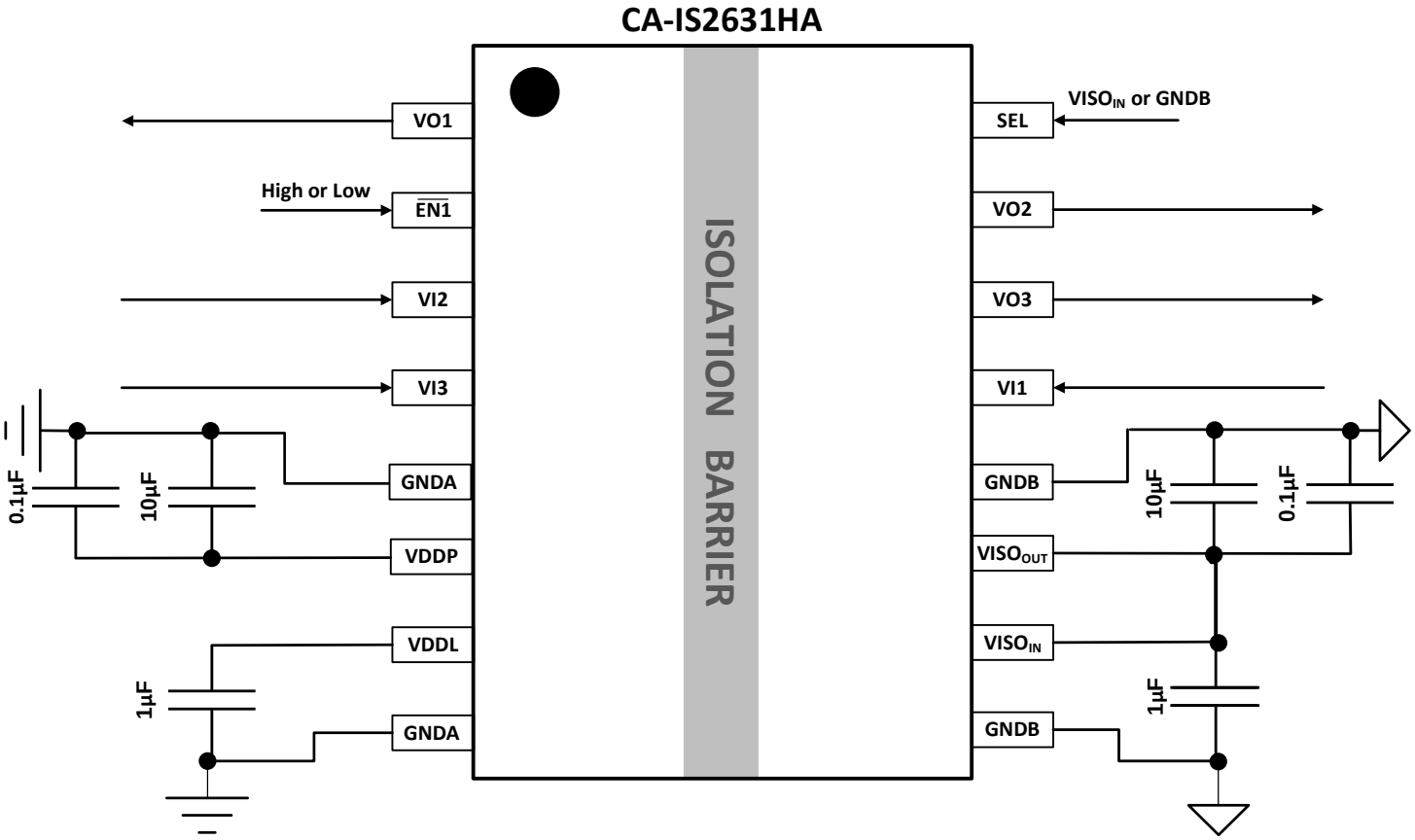


Figure 10-1. Typical Application Circuit of CA-IS2631HA

10.2 PCB Layout Guidelines

Careful PCB layout is critical to achieve clean and stable data transmission. It is recommended to design an isolation channel underneath the isolator that is free from ground and signal planes. Any galvanic or metallic connection between the primary side and secondary side will defeat the isolation. To make sure device operation is reliable at all data rates and supply voltages, the minimum 10μF decoupling capacitors between VDDP and GNDA, between $VISO_{OUT}$ and GNDB are recommended. A 0.1μF low-ESR, low-ESL decoupling capacitor in parallel with the bulk capacitor is also recommended for each power supply to filter out high frequency noise. The 0.1μF capacitor should be placed as close as possible to the supply pin.

For the individual logic supply input VDDL and secondary side supply input $VISO_{IN}$, we recommend to use a 1μF ceramic capacitors with X5R or X7R between VDDL pin and GNDA, between $VISO_{IN}$ and GNDB . Place the bypass capacitors, and the CA-IS2631HA IC on the same PCB layer. Place decoupling capacitors as close as possible to the device supply pins, see Figure 10-2 recommended components placement for the PCB layout. The paths must be wide and short to minimize inductance, also any via holes must be avoided on these paths.

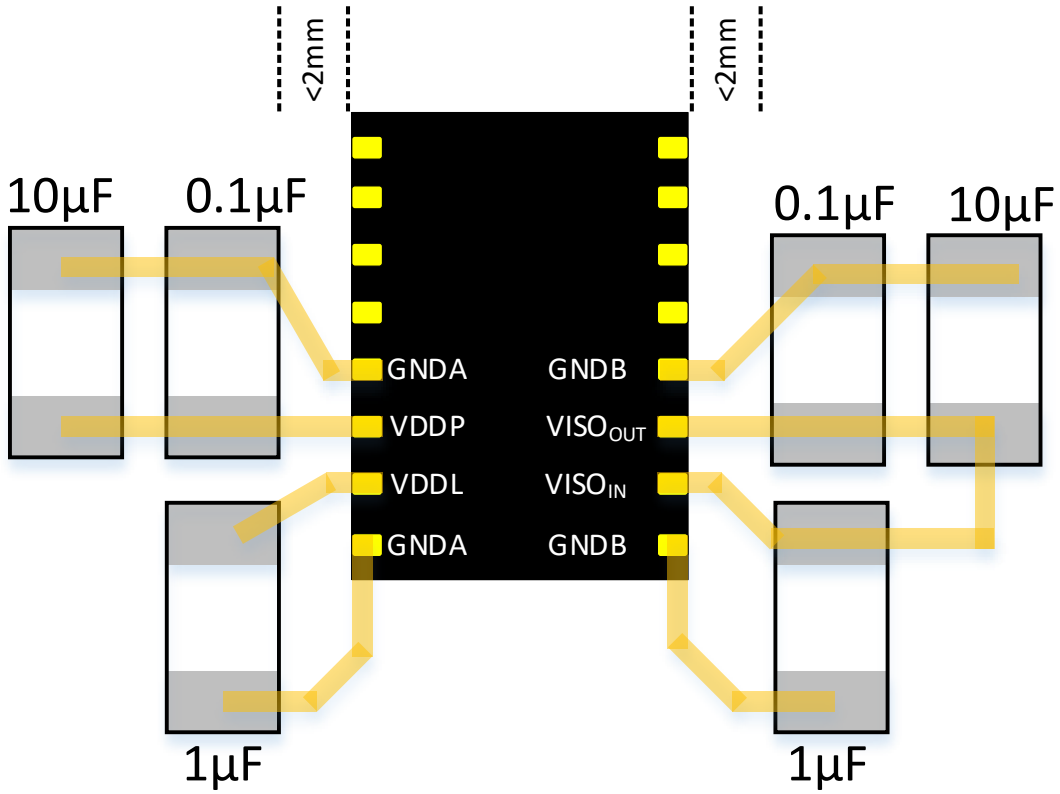
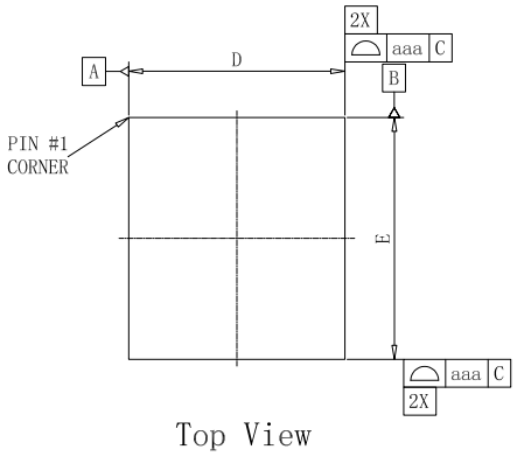
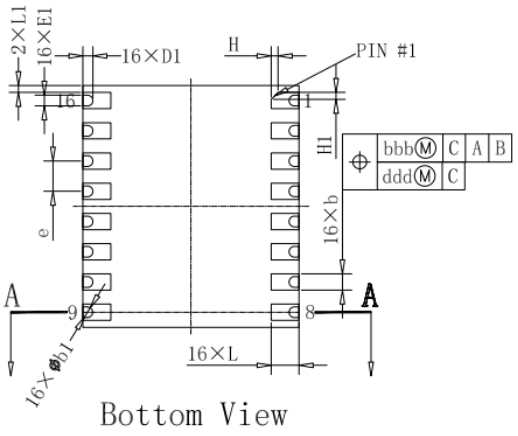


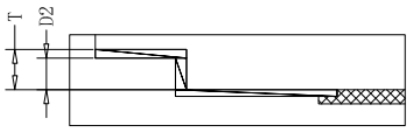
Figure 10-2. Recommended PCB layout for CA-IS2631HA Power Supply

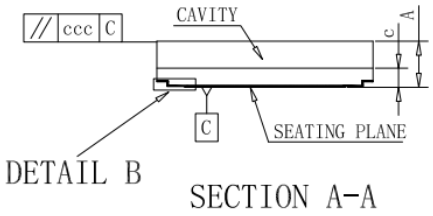
11 Package Information

LGA16 Package Outline









symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.890	0.990	1.090	0.035	0.039	0.043
c	0.370	0.410	0.450	0.015	0.016	0.018
D	4.550	4.650	4.750	0.179	0.183	0.187
E	5.100	5.200	5.300	0.201	0.205	0.209
D1	0.185	0.215	0.245	0.007	0.008	0.010
E1	0.200	0.230	0.260	0.008	0.009	0.010
D2	0.060	0.085	0.110	0.002	0.003	0.004
H	---	0.150	---	---	0.006	---
H1	---	0.150	---	---	0.006	---
L	0.500	0.600	0.700	0.020	0.024	0.028
L1	0.075	0.150	0.225	0.003	0.006	0.009
e	---	0.650	---	---	0.026	---
b	0.300	0.350	0.400	0.012	0.014	0.016
b1	0.200	0.230	0.260	0.008	0.009	0.010
T	0.083	---	---	0.003	---	---
aaa	0.100			0.004		
bbb	0.150			0.006		
ccc	0.100			0.004		
ddd	0.080			0.003		

Note:

1. All dimensions are in millimeters, angles are in degrees.

12 Soldering Temperature (reflow) Profile

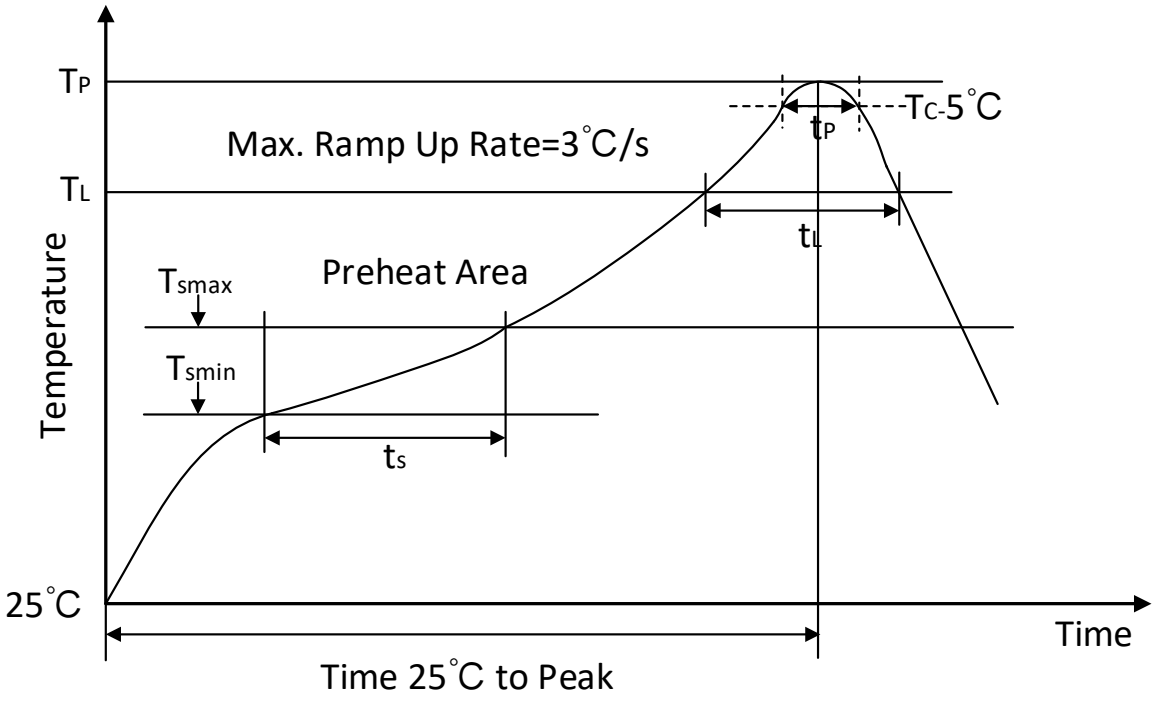


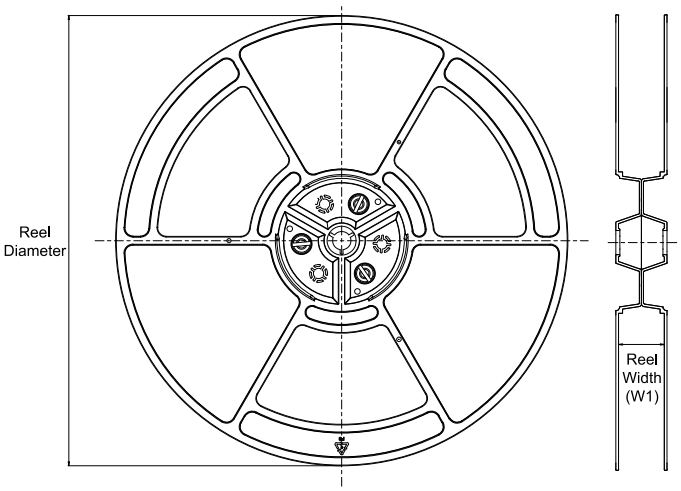
Figure 12-1. Soldering Temperature (reflow) Profile

Table 12-1. Soldering Temperature Parameter

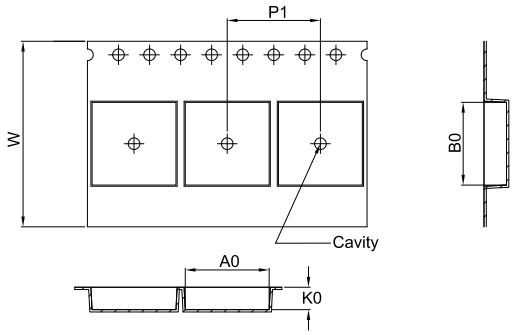
Profile Feature	**Pb-Free Assembly**
Average ramp-up rate(217 ℃ to Peak)	3℃/second max
Time of Preheat temp(from 150 ℃ to 200 ℃	60-120 second
Time to be maintained above 217 ℃	60-150 second
Peak temperature	260 +5/-0 ℃
Time within 5℃of actual peak temp	30 second
Ramp-down rate	6 ℃/second max.
Time from 25℃ to peak temp	8 minutes max

13 Tape and Reel Information

REEL DIMENSIONS

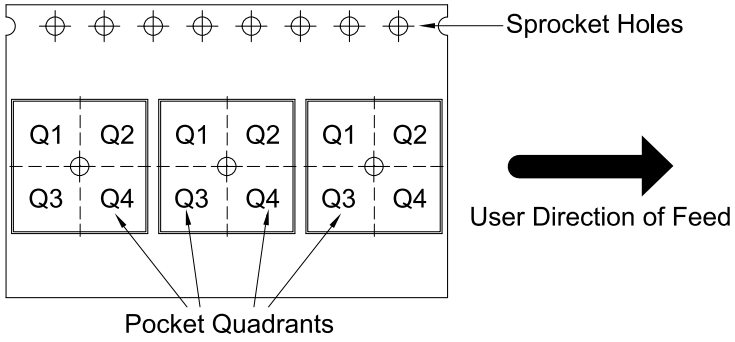


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CA-IS2631HA	LGA16 4.65x5.2	A	16	3000	330	12.4	4.95	5.50	1.29	8.0	12.0	Q1

14 Important Statement

The above information is for reference only and intended to help Chipanalog customers with design, research and development. Chipanalog reserves the rights to change the above information due to technological innovation without advance notice.

All Chipanalog products pass ex-factory test. As for specific practical applications, customers need to be responsible for evaluating and determining whether the products are applicable or not by themselves. Chipanalog's authorization for customers to use the resources are only limited to development of the related applications of the Chipanalog products. In addition to this, the resources cannot be copied or shown, and Chipanalog is not responsible for any claims, compensations, costs, losses, liabilities and the like arising from the use of the resources.

Trademark information

Chipanalog Inc.® and Chipanalog® are registered trademarks of Chipanalog.