AEC-Q100 Qualification Report

Product Series：CA-IS372X-Q1&CA-IS371X-Q1

Report Version：V1.1

Reference Doc.：AEC-Q100-REV-H

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1. Overview

Reliability testing of microelectronic products is a risk mitigation process designed to ensure the service life of device in customer applications. Semiconductor wafer manufacturing process and package-level reliability can be assessed in a variety of ways and may include accelerated environmental test conditions. Chipanalog evaluates manufacturability of the device to verify a robust silicon and assembly flow to ensure continuity of supply to customers. Chipanalog qualifies new devices, significant changes, and product families based on AEC-Q100.

2. Part Number List

Package Type	Part Number
SOIC8-NB(S)	CA-IS3722HS-Q1/CA-IS3722LS-Q1/CA-IS3721HS-Q1/CA-IS3721LS-Q1/CA-IS3720HS-Q1/CA-IS3720LS-Q1/CA-IS3710HS-Q1/CA-IS3710LS-Q1
SOIC8-WB(G)	CA-IS3722HG-Q1/CA-IS3722LG-Q1/CA-IS3720HG-Q1/CA-IS3720LG-Q1

Note：AECQ-100 provides the guideline for the use of generic data to accelerate and streamline the qualification process. Products sharing the same major product, process and materials elements may be categorized in a product qualification family.

3. Production Information

3.1. Wafer information

Fab site	SMIC
Wafer	QINGLONG
Fab Process	18BCDX

3.2. Package information

Assembly site	JCET	JCET
FT site	JCET	JCET
Package	SOIC8(S)	SOIC8(G)
Lead Frame	Cu	Cu
Bond wire	20um Au	20um Au
MSL level	MSL3	MSL3
Operation Temp.	Grade 1(-40°C - 125°C)	Grade 1(-40°C - 125°C)

4. Reliability Qualification Plan

Test Group A–Accelerated Environment Stress Tests					
Group	**Item**	**Refer.**	**Test condition**	**QTY**	**Remark**
A1	PC	J-STD-020 JESD22-A113	Test @ Rm, SMD only, Moisture Preconditioning Before THB/BHAST, AC/UHAST, TC, and PTC stress, Min. MSL = 3, Peak Reflow Temp = 260°C	231 pcs*3 lots	
A2	BHAST	JESD22-A110	V_{cc} = 5.5V, 130°C, 85% RH, 96 hrs (Test @ Rm/Hot)	77 pcs*3 lots	
A3	UHAST	JESD22-A101	130°C, 85% RH, 96 hrs (Test @ Rm)	77 pcs*3 lots	
A4	TC	JESD22-A104	-65°C-150°C, 500 cycles (Test @ Hot)	77 pcs*3 lots	
A5	PTC	JESD22-A105	-40°C-125°C, 1000 cycles (Test @ Rm/Hot)	45 pcs*1 lot	NA
A6	HTSL	JESD22-A103	T_a = 150°C, 1000 hrs (Test @ Rm/Hot)	45 pcs*1 lot	
Test Group B–Accelerated Lifetime Simulation Tests					
Group	**Item**	**Refer.**	**Test condition**	**QTY**	**Remark**
B1	HTOL	JESD22-A108	T_a = 135°C, V_{cc} = 5.5V, 1000 hrs (Test @ Rm/Cold/Hot)	77 pcs*3 lots	
B2	ELFR	AEC-Q100-008	T_a = 125°C, V_{cc} = 5 V, 48 hrs (Test @ Rm/Hot)	800 pcs*3 lots	QBS CA-IS3741HW-Q1
B3	EDR	AEC-Q100-005	Test @ Rm/Hot	77 pcs*3 lots	NA
Group C–Package Assembly Integrity Tests					
Group	**Item**	**Refer.**	**Test condition**	**QTY**	**Remark**
C1	WBS	AEC-Q100-001 AEC-Q003	Cpk > 1.67, Each bonder used T0 samples	30 bonds from 5 pcs	
C2	WBP	MIL-STD883 AEC-Q003	Cpk > 1.67, Each bonder used T0	30 bonds from 5 pcs	
C2	WBP	MIL-STD883 AEC-Q003	0 fails, post-TC samples	30 bonds from 5 pcs	
C3	SD	JESD22-B102 JSTD-002D	> 95% coverage, 8hr steam aging prior to testing	15 pcs*1 lot	
C4	PD	JESD22-B100 JESD22-B108 AEC-Q003	Cpk > 1.67	10 pcs*3 lots	
C5	SBS	AEC-Q100-010 AEC-Q003	Cpk > 1.67, 5 balls from min. of 10 devices	10pcs*3 lots	NA
C6	LI	JESD22 B105	10 leads from each of 5 devices	5pcs*1 lot	NA

Test Group D–Die Fabrication Reliability Tests					
Group	**Item**	**Refer.**	**Test condition**	**QTY**	**Remark**
D1	EM	JESD61	---	---	Done by Fab
D2	TDDB	JESD35	---	---	Done by Fab
D3	HCI	JESD60 & 28	---	---	Done by Fab
D4	NBTI	JESD90	---	---	Done by Fab
D5	SM	JESD61, 87, & 202	---	---	Done by Fab
Group E-Electrical Verification Tests					
Group	**Item**	**Refer.**	**Test condition**	**QTY**	**Remark**
E1	TEST	per datasheet	Pre and Post Stress Electrical Test	all	
E2	HBM	AEC Q100-002	±500V, ±1KV, ±2KV, ±6KV (Test @ Rm/Hot)	3 pcs/voltage level	
E3	CDM	AEC-Q100-011	±250V, ±500V, ±750V, ±2KV (Test @ Rm/Hot)	3 pcs/voltage level	
E4	LU	AEC-Q100-004	Test @ Rm/Hot	6 pcs*1 lot	
E9	EMC	SAE J1752/3	Electromagnetic Compatibility (Radiated Emissions)	1 pcs*1 lot	
E10	SC	AEC-Q100-012	/	10 pcs*3 lots	NA
E11	SER	JESD89-1/-2/-3	/	3 pcs *1 lot	NA
E12	LF	AEC-Q005	/	2 pcs*3 lots	NA

Note：Group E5, E6, E7 and Group F are not reliability related items.

5. Reliability Test Results

Test Group A–Accelerated Environment Stress Test(SOIC8-NB)					
Group	**Item**	**Test Condition**	**QTY**	**Lot NO.**	**Result**
A1	PC	Test @ Rm, SMD only, Moisture Preconditioning before BHAST, UHAST, TC stress, MSL = 3, Peak Reflow Temp = 260°C	240 pcs*3 lots	SJE22242E	Pass
				SJE22244E	Pass
				SJE22229E	Pass
A2	BHAST	130°C, 85% RH, 96 hrs, V_{cc} = 5.5 V	80 pcs*3 lots	SJE22242E	Pass
				SJE22244E	Pass
				SJE22229E	Pass
A3	UHAST	130°C, 85% RH, 96 hrs	80 pcs*3 lots	SJE22242E	Pass
				SJE22244E	Pass
				SJE22229E	Pass
A4	TC	-65°C-150°C, 500 cycles	80 pcs*3 lots	SJE22242E	Pass
				SJE22244E	Pass
				SJE22229E	Pass
A6	HTSL	T_a = 150°C, 1000 hrs	45 pcs*1 lot	SJE22242E	Pass
Test Group A–Accelerated Environment Stress Test(SOIC8-WB)					
Group	**Item**	**Test Condition**	**QTY**	**Lot NO.**	**Result**
A1	PC	Test @ Rm, SMD only, Moisture Preconditioning before BHAST, UHAST, TC stress, MSL = 3, Peak Reflow Temp = 260°C	240 pcs*3 lots	2333A	Pass
				2334A	Pass
				2335A	Pass
A2	BHAST	130°C, 85% RH, 96 hrs, V_{cc} = 5.5 V	80 pcs*3 lots	2333A	Pass
				2334A	Pass
				2335A	Pass
A3	UHAST	130°C, 85% RH, 96 hrs	80 pcs*3 lots	2333A	Pass
				2334A	Pass
				2335A	Pass
A4	TC	-65°C-150°C, 500 cycles	80 pcs*3 lots	2333A	Pass
				2334A	Pass
				2335A	Pass
A6	HTSL	T_a = 150°C, 1000 hrs	45 pcs*1 lot	2333A	Pass
Test Group B–Accelerated Lifetime Simulation Tests					
Group	**Item**	**Test Condition**	**QTY**	**Lot NO.**	**Result**
B1	HTOL	T_a = 135°C, 1000 hrs, V_{cc} = 5.5 V, TTL input, F = 10 kHz	80 pcs*3 lots	SJE22242E	Pass
				SJE22244E	Pass
				SJE22229E	Pass

B2	ELFR	T_a = 125°C, V_{cc} = 5 V, 48 hrs	800 pcs*3 lots	NA	QBS CA-IS3741HW-Q1
				NA	QBS CA-IS3741HW-Q1
				NA	QBS CA-IS3741HW-Q1
Group C–Package Assembly Integrity Tests(SOIC8-NB)					
Group	**Item**	**Test Condition**	**QTY**	**Lot NO.**	**Result**
C1	WBS	Cpk > 1.67， Each bonder used T0 samples	30 bonds from 5 pcs	SJE22242E	Cpk = 1.780
C2	WBP	Cpk > 1.67, each bonder used T0	30 bonds from 5 pcs	SJE22242E	Cpk = 1.827
C2	WBP	0 fails, Each bonder used, post-TC samples	30 bonds from 5 pcs	SJE22242E	Cpk = 1.900
C3	SD	>95% coverage, 8 hrs steam aging prior to testing	15 pcs*1 lot	SJE22242E	Pass
C4	PD	Cpk > 1.67	10 pcs*3 lots	SJE22242E	Pass
				SJE22244E	Pass
				SJE22229E	Pass
Group C–Package Assembly Integrity Tests(SOIC8-WB)					
Group	**Item**	**Test Condition**	**QTY**	**Lot NO.**	**Result**
C1	WBS	Cpk > 1.67， Each bonder used T0 samples	30 bonds from 5 pcs	2333A	Cpk = 2.20
C2	WBP	Cpk > 1.67, each bonder used T0	30 bonds from 5 pcs	2333A	Cpk = 2.28
C2	WBP	0 fails, Each bonder used, post-TC samples	30 bonds from 5 pcs	2333A	Cpk = 2.183
C3	SD	>95% coverage, 8 hrs steam aging prior to testing	15 pcs*1 lot	2333A	Pass
C4	PD	Cpk > 1.67	10 pcs*3 lots	2333A	Pass
				2334A	Pass
				2335A	Pass
TEST GROUP D–Die Fabrication Reliability Tests					
Group	**Item**	**Test Condition**	**ADDITIONAL REQUIREMENTS**		
D1	EM	---	The Die Fabrication Reliability Tests are carried out by every fabrication site. The data, test method, calculations and internal criteria are available to the customer upon request.		
D2	TDDB	---			
D3	HCI	---			
D4	NBTI	---			
D5	SM	---			

Group E-Electrical Verification Tests					
Group	**Item**	**Test Condition**	**QTY**	**Lot NO.**	**Result**
E1	TEST	Pre and Post Stress Electrical Test	all	SJE22242E SJE22244E SJE22229E	Pass
E2	HBM	±500V, ±1KV, ±2KV, ±6KV (Test @ Rm/Hot)	3 pcs/voltage level	SJE22244E	C3A
E3	CDM	±250V, ±500V, ±750V, ±2KV (Test @ Rm/Hot)	3 pcs/voltage level	SJE22244E	C3
E4	LU	Test @ Rm/Hot	6 pcs*1 lot	SJE22244E	Class II A
E9	EMC	Electromagnetic Compatibility (Radiated Emissions)	1 pcs*1 lot	SJE22244E	Pass

6. MTTF&FIT

Supporting Data (Ea = 0.7 eV, Confidence Level = 60%)							MTTF (hrs)	FIT
Test Temp.	**Test Voltage**	**Duration**	**QTY**	**Fail QTY**	**Operation Temp.**	**Operation Voltage**	3.03E+08	3.29
135°C	5.5 V	1000 hrs	240	0	55°C	3.3 V		

7. Conclusion

CA-IS372X-Q1&CA-IS371X-Q1 series products are qualified by AEC-Q100 standard.

Disclaimer

This information is provided to assist customers in design and development. It could change for technology innovation without notice.

The devices are shipped after passing final test. Customers are responsible to conduct sufficient engineering and additional qualification testing to determine whether a device is suitable for use in their applications.

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Revision History

Revision	Change Log	Date
V1.0	Initial release	Apr. 2023
V1.1	Update reliability data of SOIC8-WB package	Jan. 2024

Appendix 1: EMC Test Results

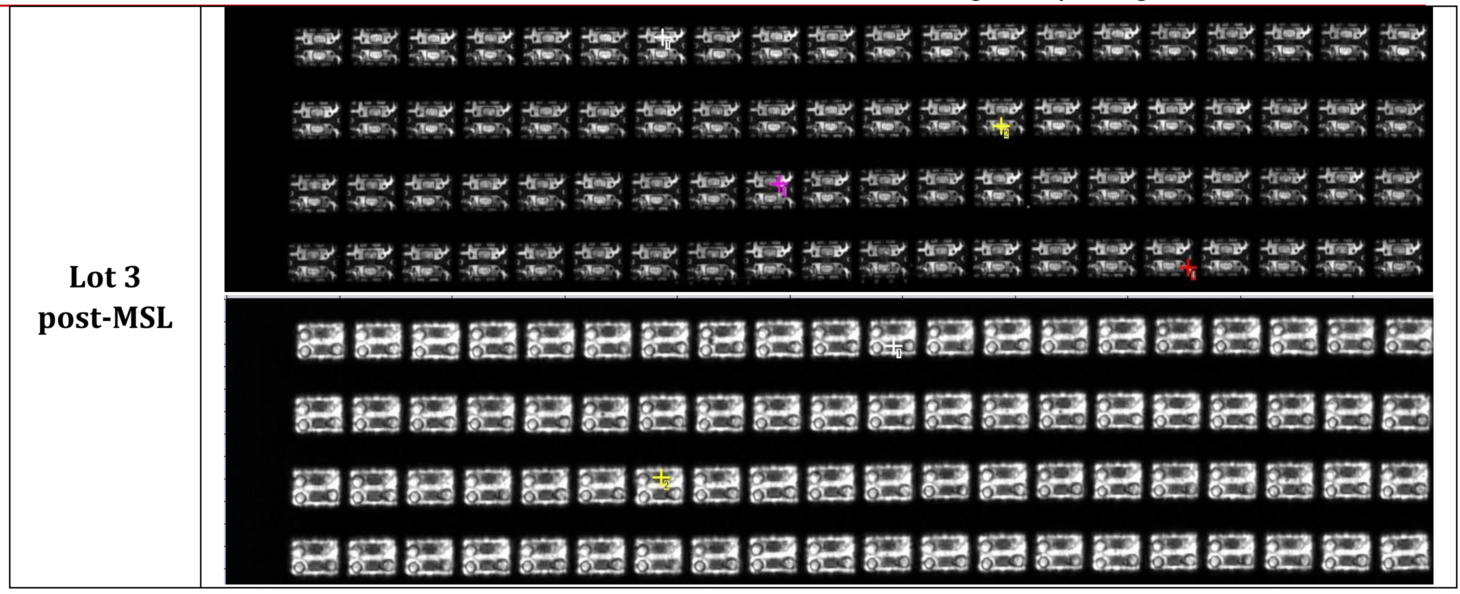
VCC=5V, TTL Input 1 MHz, orientation 0°	VCC=5V, TTL Input 1 MHz, orientation 90°
VCC=5V, TTL Input 1 MHz, orientation 180°	**VCC=5V, TTL Input 1 MHz, orientation 270°**
VCC=5V, TTL Input 10 MHz, orientation 0°	**VCC=5V, TTL Input 10 MHz, orientation 90°**
VCC=5V, TTL Input 10 MHz, orientation 180°	**VCC=5V, TTL Input 10 MHz, orientation 270°**

Appendix 2: SAT Test Results

1. SOIC8-NB Package

Lot 1 pre-MSL	
Lot 1 post-MSL	

Lot 2 pre-MSL	
Lot 2 post-MSL	
Lot 3 pre-MSL	

Lot 3 post-MSL	

2. SOIC8-WB Package

Lot 1 pre-MSL	

Lot 1 post-MSL	
Lot 2 pre-MSL	

Lot 2 post-MSL	
Lot 3 pre-MSL	

Lot 3 post-MSL	