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Final

Test Report

P22_0213_007_Chipanalog_LINiso7_CA-IF1021_Report00

Date of Approval: 2022-Aug-22

Device Under Test		**Customer**	
Device Name	CA-IF1021S-Q1 CA-IF1021D-Q1	Order No.	P22_0213
Manufacturer	Shanghai Chipanalog Microelectronics Co., Ltd.	Name	Shanghai Chipanalog Microelectronics Co., Ltd.
Type / Version	CA-IF1021S-Q1	Address	2F, Block C,GaoJing Road,Qingpu District Shanghai, 201601 P.R. China
Sample marking	1021S-Q1 84540 03 DUJ022170		

Number of Pages	50
Test Period	from ww28/2022 until ww28/2022
Test Method / Test Requirement	LIN Conformance Test Specification
Performed Tests and References	1 LIN OSI Layer 1 – Physical Layer ISO 17987-7:2016 Road vehicles – Local Interconnect Network (LIN) – Part 7: Electrical Physical Layer (EPL) conformance test specification – EPL 12 V LIN devices with RX and TX access
Conformance Test Results	The Test Results refer to the delivered device.
1 ISO LIN conformance tests -Physical Layer-*	**Pass**

* DAkkS accredited according to DIN EN ISO/IEC 17025:2018. The accreditation is only valid for the scope of accreditation listed in the annex to certificate D-PL-18596-01-00.

For detailed information see chapter Test List at the following pages.

Approved by	Test performed by
L. Kukla, Project Manager	J. Eversmeier, Test Engineer

Table of Content

Revision History

Old revision	New revision	Amendment Description	Editor
–	00	Final version	LK

1 Device Under Test (detailed)

General	
Date of Sample Arrival	27.06.2022
Manufacturer	Shanghai Chipanalog Microelectronics Co., Ltd.
Sample Marking	1021S-Q1 84540 03 DUJ022170
Test performed with DUT no.	#1

Device Specification (all information provided by the customer)	
Device Name	CA-IF1021S-Q1 / CA-IF1021D-Q1
Type / Version	CA-IF1021S-Q1
Design step	-
HW-Version	-
SW-Version	-

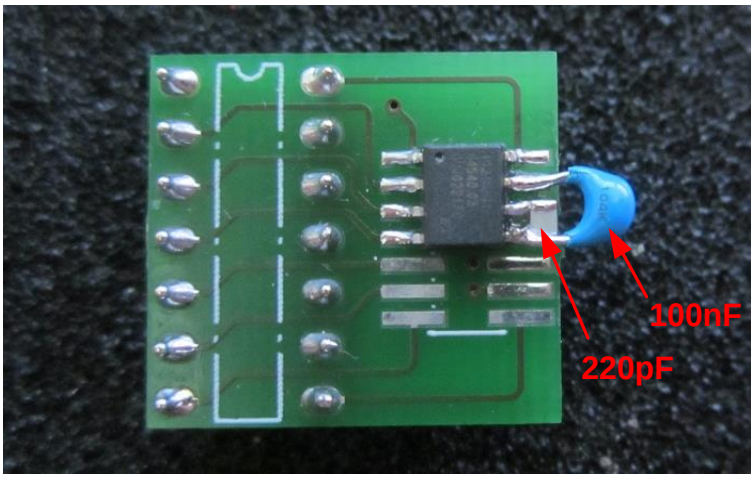
Documentation (all information provided by the customer)	
Hardware manual	-
User manual / datasheet	CA-IF1021-Q1_datasheet_Version1.01_en_20220629.pdf *(Version 1.01, 2022/06/29)*

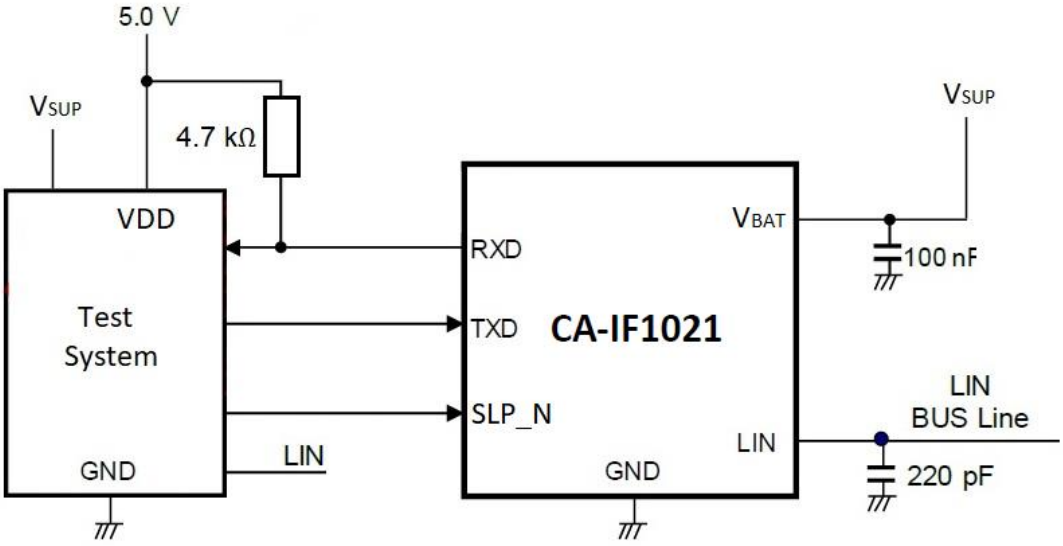
Device Classification	
According to	A

Software Specification	
IDE	-
Compiler	-
Device	-

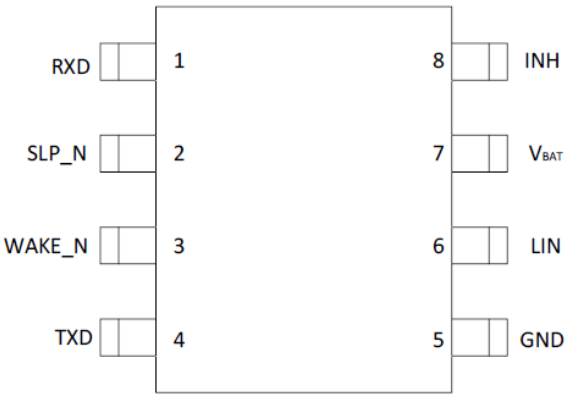
Supplement	
Node Capability File	-
Connection plan	P22_0213_001_Connection_Plan00.pdf

2 Setup for Device Under Test





Pin Configuration and Functions



SOIC8 Package

No.	Function	Description
1	RXD	Data receive output. Open-drain output requires an external pull-up resistor. The RXD reads back information from the LIN bus in normal operation mode and indicates a wake-up event in standby mode, RXD is low if a wake event occurred.
2	SLP_N	Enable input with integrated pull-down resistor to GND. A logic high on SLP_N pin puts the transceiver in normal operating mode. A logic low on SLP_N pin to select the sleep mode.
3	WAKE_N	Active-low local wake-up input. Pull WAKE low to generate a local wake-up event.
4	TXD	Transmit data input. TXD is a CMOS/TTL compatible input from microcontroller with an internal pulled down resistor to GND. Set this pin to “low” to drive a dominant stat on LIN Bus. In standby mode, TXD indicates the wake-up source as an output. Active low after a wake-up event.
5	GND	Ground
6	LIN	LIN bus input/output; external capacitance with 220pF added between LIN and ground.
7	V_{BAT}	Battery voltage input. Bypass V_{BAT} to ground with at least 0.1µF ceramic capacitor as close as possible to the device
8	INH	Inhibit Output. INH can be used to control one or more external voltage regulators and microcontroller. Active high after a wake-up event.

Interface voltage is set to 5.0 V for all tests.

3 Test Equipment

The following test equipment and test system have been used.

No.	Component	Manufacturer	Version / Type	ID
Test System 2				
C&S Hardware				
ISO17987-7				
1	LIN-Power switch Board	C&S	Rev 2.1	CS140214
2	LIN-Stimulation Board	C&S	Rev 2.2	CS140210
3	LIN-GND-shift Board	C&S	Rev 1.3	CSHW_000075
4	LIN-IUT Board	C&S	Rev 2.1	CS140211
5	LIN-Adapter Board	C&S	Rev 2.2	CS140212
6	LIN-Adapter Board	C&S	Rev 2.2	CSHW_000073
7	LIN-Adapter Board	C&S	Rev 1.1	CSHW_000040
8	LIN-Adapter Board	C&S	Rev 1.1	CSHW_000099
9	LIN Stimuli Board	C&S	Rev.1.2	CSHW_000010
10	LIN IUT Board	C&S	Rev 2.1	CSHW_000193
LIN ext. Duty Cycle Test				
11	Duty Cycle Board	C&S	Rev 1.0	CSHW_000212
Test System Hardware				
12	Power Supply	Hameg	HM 8142	CS140142
13	Power Supply	Hameg	HM 8142	700013
14	Power Supply	Hameg	HM 8142	CS140220
15	Oscilloscope	Agilent	54622D	700035
16	Oscilloscope	Tektronix	MSO54	CS140701
17	Function/ Waveform generator	Hewlett Packard	33120A	700007
18	Function/ Waveform generator	Hewlett Packard	33120A	700043
19	Data Acquisition /Switch Unit	Agilent	34970A	700062
20	Data Acquisition /Switch Unit	Agilent	34970A	CS140146
21	20-Channel-Multiplexer Module (2/4 Wire)	Agilent	34901A	700096
22	20-Channel-Multiplexer Module (2/4 Wire)	Agilent	34901A	700095
23	20-Channel Actuator Module	Agilent	34903A	CS140145
Software				
24	LIN_PL_Supervisor	C&S	1.0.5.0, Build 5	

4 Technical Correspondence

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5 Test List

5.1 Dynamic Tests

Following test case numeration relates on the corresponding test specification.

No.	Description		Result	Comment
5.2.2	**[EPL-CT 1] Operating Voltage Range**			
	[EPL-CT 1].1 V_{IUT} range: [V_{SUP} / V_{BAT}] = [7V to 18V] / [8V to 18V]		Pass	RX shows the 10kHz Signal, The maximum deviation is less or equal than 10%
	[EPL-CT 1].1 VIUT range: [VSUP / VBAT] = [18 to 7V] / [18V to 8V]		Pass	RX shows the 10kHz Signal, The maximum deviation is less or equal 10%
5.2.3	**Threshold Voltages**			
5.2.3.2	**[EPL-CT 2] IUT as Receiver: V_{SUP} @ V_{BUS_DOM} (down)**			
	[EPL-CT 2].1 V_{SUP} = 7V	Signal Range [18V to 4.2V]	Pass	RX is recessive
		Signal Range [2.8V to -1.05V]		RX is dominant
	[EPL-CT 2].2 V_{SUP} = 14V	Signal Range [18V to 8.4V]	Pass	RX is recessive
		Signal Range [5.6V to -2.1V]		RX is dominant
	[EPL-CT 2].3 V_{SUP} = 18V	Signal Range [20.7V to 10.8V]	Pass	RX is recessive
		Signal Range [7.2V to -2.7V]		RX is dominant
5.2.3.3	**IUT as Receiver: V_{SUP} @ V_{BUS_REC} (up)**			
	[EPL-CT 3].1 V_{SUP} = 7V	Signal Range [-1.05V to 2.8V]	Pass	RX is dominant
		Signal Range [4.2V to 18V]		RX is recessive
	[EPL-CT 3].2 V_{SUP} = 14V	Signal Range [-2.1V to 5.6V]	Pass	RX is dominant
		Signal Range [8.4V to 18V]		RX is recessive

No.	Description		Result	Comment
	[EPL-CT 3].3 V_{SUP} = 18V	Signal Range [-2.7V…7.2V]	Pass	RX is dominant
		Signal Range [10.8V…20.7V]		RX is recessive
5.2.3.4	**[EPL-CT 4] IUT as Receiver: V_{SUP} @ V_{BUS}**			
	[EPL-CT 4].1 V_{SUP} = 7V	Signal Range [-1.05V…8.05V] up	Pass	V_{BUS_CNT} is in range of [0.475…0.525]*V_{SUP}, V_{HYS} is less than 0.175* V_{SUP}.
		Signal Range [8.05V…-1.05V] down		
	[EPL-CT 4].2 V_{SUP} = 14V	Signal Range [-2.1V…16.1V] up	Pass	V_{BUS_CNT} is in range of [0.475…0.525]*V_{SUP}, V_{HYS} is less than 0.175* V_{SUP}.
		Signal Range [16.1V…-2.1V] down		
	[EPL-CT 4].3 V_{SUP} = 18V	Signal Range [-2.7V…20.7V] up	Pass	V_{BUS_CNT} is in range of [0.475…0.525]*V_{SUP}, V_{HYS} is less than 0.175* V_{SUP}.
		Signal Range [20.7V…-2.7V] down		
5.2.4	**[EPL-CT 5] Variation of $V_{SUP\_NON\_OP} \in$ [- 0.3V ... 7.0V]; [18V … 40V]**			
	[EPL-CT 5].1 Class B device as master V_{IUT} = [-0.3V…8V], [18V…40V]		Not applicable	IUT is a Class A device
	[EPL-CT 5].2 Class B device as slave V_{BAT} = [-0.3V…8V], [18V…40V]		Not applicable	IUT is a Class A device
	[EPL-CT 5].3 Class A device V_{SUP} = [-0.3V…7V], [18V…40V]		Pass	No dominant state occurs, the IUT is not destroyed, the recessive voltage afterwards is less or equal +/-5%
5.2.5	**I_{BUS} Under Several Conditions**			
5.2.5.1	**[EPL-CT 6] I_{BUS_LIM} @ dominant state (driver on)**			
	[EPL-CT 6].1 V_{IUT}: [V_{SUP} / V_{BAT}] = 18V; R_{MEAS} = 440 Ω		Pass	LIN shows the rectangular signal, the dominant state bus level is lower than TH_DOM=4.518V for transceiver
5.2.5.2	**[EPL-CT 7] $I_{BUS\_PAS\_dom}$: IUT in recessive state: V_{BUS} = 0 V**			
	[EPL-CT 7].1 V_{IUT}: [V_{SUP} / V_{BAT}] = 12V; R_{MEAS} = 499 Ω		Pass	The maximum voltage drop is higher than -500mV.

No.	Description	Result	Comment
5.2.5.3	**[EPL-CT 8] $I_{BUS\_PAS\_rec}$: IUT in recessive state: V_{SUP} = 7V with variation of VBUS ∈ [8V to 18V]**		
	[EPL-CT 8].1 V_{IUT}: [V_{SUP} / V_{BAT}] = 7V / 8V; R_{MEAS} = 1000 Ω	Pass	The maximum voltage drop is less or equal than 20mV.
5.2.6	**Slope Control**		
5.2.6.2	**[EPL-CT 9] Measuring the duty cycle @ 10.417 kbit/s – IUT as transmitter**		
	[EPL-CT 9].1 V_{IUT} = 7V/8V; V_{PS2}=6.0V; Bus Load = 1nF, 1kΩ	Pass	The measured duty cycle D3 is greater or equal than 0.417.
	[EPL-CT 9].2 V_{IUT} = 7V/8V; V_{PS2}=6.6V; Bus Load = 1nF, 1kΩ	Pass	The measured duty cycle D3 is greater or equal than 0.417.
	[EPL-CT 9].3 V_{IUT} = 7V/8V; V_{PS2}=6.0V; Bus Load = 6.8nF, 660Ω	Pass	The measured duty cycle D3 is greater or equal than 0.417.
	[EPL-CT 9].4 V_{IUT} = 7V/8V; V_{PS2}=6.6V; Bus Load = 6.8nF, 660Ω	Pass	The measured duty cycle D3 is greater or equal than 0.417.
	[EPL-CT 9].5 V_{IUT} = 7V/8V; V_{PS2}=6.0V; Bus Load = 10nF, 500Ω	Pass	The measured duty cycle D3 is greater or equal than 0.417.
	[EPL-CT 9].6 V_{IUT} = 7V/8V; V_{PS2}=6.6V; Bus Load = 10nF, 500Ω	Pass	The measured duty cycle D3 is greater or equal than 0.417.
	[EPL-CT 9].7 V_{IUT} = 7.6V/8.6V; V_{PS2}=6.6V; Bus Load = 1nF, 1kΩ	Pass	The measured duty cycle D3 is greater or equal than 0.417, the measured duty cycle D4 is less or equal than 0.590.
	[EPL-CT 9].8 V_{IUT} = 7.6V/8.6V; V_{PS2}=7.2V; Bus Load = 1nF, 1kΩ	Pass	The measured duty cycle D3 is greater or equal than 0.417, the measured duty cycle D4 is less or equal than 0.590.
	[EPL-CT 9].9 V_{IUT} = 7.6V/8.6V; V_{PS2}=6.6V; Bus Load = 6.8nF, 660Ω	Pass	The measured duty cycle D3 is greater or equal than 0.417, the measured duty cycle D4 is less or equal than 0.590.

No.	Description	Result	Comment
	[EPL-CT 9].10 V_{IUT} = 7.6V/8.6V; V_{PS2}=7.2V; Bus Load = 6.8nF, 660Ω	Pass	The measured duty cycle D3 is greater or equal than 0.417, the measured duty cycle D4 is less or equal than 0.590.
	[EPL-CT 9].11 V_{IUT} = 7.6V/8.6V; V_{PS2}=6.6V; Bus Load = 10nF, 500Ω	Pass	The measured duty cycle D3 is greater or equal than 0.417, the measured duty cycle D4 is less or equal than 0.590.
	[EPL-CT 9].12 V_{IUT} = 7.6V/8.6V; V_{PS2}=7.2V; Bus Load = 10nF, 500Ω	Pass	The measured duty cycle D3 is greater or equal than 0.417, the measured duty cycle D4 is less or equal than 0.590.
	[EPL-CT 9].13 V_{IUT} = 18V/18.6V; V_{PS2}=17V; Bus Load = 1nF, 1kΩ	Pass	The measured duty cycle D3 is greater or equal than 0.417, the measured duty cycle D4 is less or equal than 0.590.
	[EPL-CT 9].14 V_{IUT} = 18V/18.6V; V_{PS2}=17.6V; Bus Load = 1nF, 1kΩ	Pass	The measured duty cycle D3 is greater or equal than 0.417, the measured duty cycle D4 is less or equal than 0.590.
	[EPL-CT 9].15 V_{IUT} = 18V/18.6V; V_{PS2}=17V; Bus Load = 6.8nF, 660Ω	Pass	The measured duty cycle D3 is greater or equal than 0.417, the measured duty cycle D4 is less or equal than 0.590.
	[EPL-CT 9].16 V_{IUT} = 18V/18.6V; V_{PS2}=17.6V; Bus Load = 6.8nF, 660Ω	Pass	The measured duty cycle D3 is greater or equal than 0.417, the measured duty cycle D4 is less or equal than 0.590.
	[EPL-CT 9].17 V_{IUT} = 18V/18.6V; V_{PS2}=17V; Bus Load = 10nF, 500Ω	Pass	The measured duty cycle D3 is greater or equal than 0.417, the measured duty cycle D4 is less or equal than 0.590.

No.	Description	Result	Comment
	[EPL-CT 9].18 V_{IUT} = 18V/18.6V; V_{PS2}=17.6V; Bus Load = 10nF, 500Ω	Pass	The measured duty cycle D3 is greater or equal than 0.417, the measured duty cycle D4 is less or equal than 0.590.
5.2.6.3	**[EPL-CT 10] Measuring the duty cycle @ 20.0 kbit/s – IUT as transmitter**		
	[EPL-CT 10].1 V_{IUT} = 7V/8V; V_{PS2}=6.0V; Bus Load = 1nF, 1kΩ	Pass	The measured duty cycle D1 is greater or equal than 0.396.
	[EPL-CT 10].2 V_{IUT} = 7V/8V; V_{PS2}=6.6V; Bus Load = 1nF, 1kΩ	Pass	The measured duty cycle D1 is greater or equal than 0.396.
	[EPL-CT 10].3 V_{IUT} = 7V/8V; V_{PS2}=6.0V; Bus Load = 6.8nF, 660Ω	Pass	The measured duty cycle D1 is greater or equal than 0.396.
	[EPL-CT 10].4 V_{IUT} = 7V/8V; V_{PS2}=6.6V; Bus Load = 6.8nF, 660Ω	Pass	The measured duty cycle D1 is greater or equal than 0.396.
	[EPL-CT 10].5 V_{IUT} = 7V/8V; V_{PS2}=6.0V; Bus Load = 10nF, 500Ω	Pass	The measured duty cycle D1 is greater or equal than 0.396.
	[EPL-CT 10].6 V_{IUT} = 7V/8V; V_{PS2}=6.6V; Bus Load = 10nF, 500Ω	Pass	The measured duty cycle D1 is greater or equal than 0.396.
	[EPL-CT 10].7 V_{IUT} = 7.6V/8.6V; V_{PS2}=6.6V; Bus Load = 1nF, 1kΩ	Pass	The measured duty cycle D1 must be greater or equal than 0.396, the measured duty cycle D2 is less or equal 0.581.
	[EPL-CT 10].8 V_{IUT} = 7.6V/8.6V; V_{PS2}=7.2V; Bus Load = 1nF, 1kΩ	Pass	The measured duty cycle D1 must be greater or equal than 0.396, the measured duty cycle D2 is less or equal 0.581.
	[EPL-CT 10].9 V_{IUT} = 7.6V/8.6V; V_{PS2}=6.6V; Bus Load = 6.8nF, 660Ω	Pass	The measured duty cycle D1 must be greater or equal than 0.396, the measured duty cycle D2 is less or equal 0.581.

No.	Description	Result	Comment
	[EPL-CT 10].10 V_{IUT} = 7.6V/8.6V; V_{PS2}=7.2V; Bus Load = 6.8nF, 660Ω	Pass	The measured duty cycle D1 must be greater or equal than 0.396, the measured duty cycle D2 is less or equal 0.581.
	[EPL-CT 10].11 V_{IUT} = 7.6V/8.6V; V_{PS2}=6.6V; Bus Load = 10nF, 500Ω	Pass	The measured duty cycle D1 must be greater or equal than 0.396, the measured duty cycle D2 is less or equal 0.581.
	[EPL-CT 10].12 V_{IUT} = 7.6V/8.6V; V_{PS2}=7.2V; Bus Load = 10nF, 500Ω	Pass	The measured duty cycle D1 must be greater or equal than 0.396, the measured duty cycle D2 is less or equal 0.581.
	[EPL-CT 10].13 V_{IUT} = 18V/18.6V; V_{PS2}=17V; Bus Load = 1nF, 1kΩ	Pass	The measured duty cycle D1 must be greater or equal than 0.396, the measured duty cycle D2 is less or equal 0.581.
	[EPL-CT 10].14 V_{IUT} = 18V/18.6V; V_{PS2}=17.6V; Bus Load = 1nF, 1kΩ	Pass	The measured duty cycle D1 must be greater or equal than 0.396, the measured duty cycle D2 is less or equal 0.581.
	[EPL-CT 10].15 V_{IUT} = 18V/18.6V; V_{PS2}=17V; Bus Load = 6.8nF, 660Ω	Pass	The measured duty cycle D1 must be greater or equal than 0.396, the measured duty cycle D2 is less or equal 0.581.
	[EPL-CT 10].16 V_{IUT} = 18V/18.6V; V_{PS2}=17.6V; Bus Load = 6.8nF, 660Ω	Pass	The measured duty cycle D1 must be greater or equal than 0.396, the measured duty cycle D2 is less or equal 0.581.
	[EPL-CT 10].17 V_{IUT} = 18V/18.6V; V_{PS2}=17V; Bus Load = 10nF, 500Ω	Pass	The measured duty cycle D1 must be greater or equal than 0.396, the measured duty cycle D2 is less or equal 0.581.

No.	Description	Result	Comment
	[EPL-CT 10].18 V_{IUT} = 18V/18.6V; V_{PS2}=17.6V; Bus Load = 10nF, 500Ω	Pass	The measured duty cycle D1 must be greater or equal than 0.396, the measured duty cycle D2 is less or equal 0.581.
5.2.7	**Propagation Delay**		
5.2.7.2	**[EPL-CT 11] Propagation delay of the receiver**		
	[EPL-CT 11].1 V_{SUP} = 7.0V; RXD Load = 20pF / 2.4kΩ (for “open drain” transceiver only)	Pass	t_{rx_pd} is less than 6µs, t_{rx_sym} is in range +/- 2µs.
	[EPL-CT 11].2 V_{SUP} = 14V; RXD Load = 20pF / 2.4kΩ (for “open drain” transceiver only)	Pass	t_{rx_pd} is less than 6µs, t_{rx_sym} is in range +/- 2µs.
	[EPL-CT 11].3 V_{SUP} = 18V; RXD Load = 20pF / 2.4kΩ (for “open drain” transceiver only)	Pass	t_{rx_pd} is less than 6µs, t_{rx_sym} is in range +/- 2µs.
5.2.8	**Supply Voltage Offset**		
5.2.8.2	**GND / VBAT Shift Test – Dynamic**		
5.2.8.3	[EPL-CT 12] GND Shift Test – Dynamic – IUT as Class A Device	Pass	The duty cycle of RXD2 is in range D1 – 2µs ... D2 + 2µs.
5.2.8.4	[EPL-CT 13] GND Shift Test – Dynamic – IUT as Class A Device	Pass	The duty cycle of RXD2 is in range D1 – 2µs ... D2 + 2µs.
5.2.8.5	[EPL-CT 14] VBAT Shift Test – Dynamic – IUT as Class A Device	Pass	The duty cycle of RXD2 is in range D1 – 2µs ... D2 + 2µs.
5.2.8.6	[EPL-CT 15] VBAT Shift Test – Dynamic – IUT as Class A Device	Pass	The duty cycle of RXD2 is in range D1 – 2µs ... D2 + 2µs.
5.2.8.7	[EPL-CT 16] GND Shift Test – Dynamic – IUT as Class B Device	Not applicable	IUT is a Class A device
5.2.8.8	[EPL-CT 17] GND Shift Test – Dynamic – IUT as Class B Device	Not applicable	IUT is a Class A device
5.2.8.9	[EPL-CT 18] VBAT Shift Test – Dynamic – IUT as Class B Device	Not applicable	IUT is a Class A device
5.2.8.10	[EPL-CT 19] VBAT Shift Test – Dynamic – IUT as Class B Device	Not applicable	IUT is a Class A device
5.2.9	**Failure**		

No.	Description	Result	Comment
5.2.9.2	[EPL-CT 20] Loss of Battery	Pass	No parasitic current path is formed between the bus line and the DUT.
5.2.9.3	[EPL-CT 21] Loss of GND	Pass	No parasitic current path is formed between the bus line and the DUT.
5.2.10	**[EPL-CT 22] Verifying internal capacitance and dynamic interference – IUT as Slave**		
	[EPL-CT 22].1 Normal power supply	Pass	C_{SLAVE} is less or equal than 250pF: $T_{INT} \leq T_{REF}$ The IUT does not interfere with the dynamic stimulus
	[EPL-CT 22].2 IUT loss of GND	Pass	C_{SLAVE} is less or equal than 250pF: $T_{INT} \leq T_{REF}$ The IUT does not interfere with the dynamic stimulus
	[EPL-CT 22].3 IUT loss of V_{SUP}	Pass	C_{SLAVE} is less or equal than 250pF: $T_{INT} \leq T_{REF}$ The IUT does not interfere with the dynamic stimulus
5.3	**Operation Mode Termination**		
5.3.2	[EPL–CT 23] Measuring internal resistor – IUT as slave	Pass	R_{INT} value is included in the range [20 kΩ; 60 kΩ]
5.3.3	[EPL–CT 24] Measuring internal resistor – IUT as master	Not applicable	IUT as Slave

5.2 Static Tests

The motivation of static test cases is to check the availability and the boundaries in the datasheet of the IUT. For all integrated circuits, every related parameter in Table 41 shall be part of the datasheet and fulfil the specified boundaries in terms of physical worst case condition. Datasheet parameter names may deviate from the names in Table 41, but in this case, a cross-reference list (datasheet versus Table 41) shall be provided for this test. Parameter conditions may deviate from the conditions in Table 41, if the datasheet conditions are according to the physical worst case context in Table 41 at least.

If one parameter does not pass this test, the result of the whole conformance test is “Failed”. See ISO 17987–4:2016, Table 10 and Table 20.

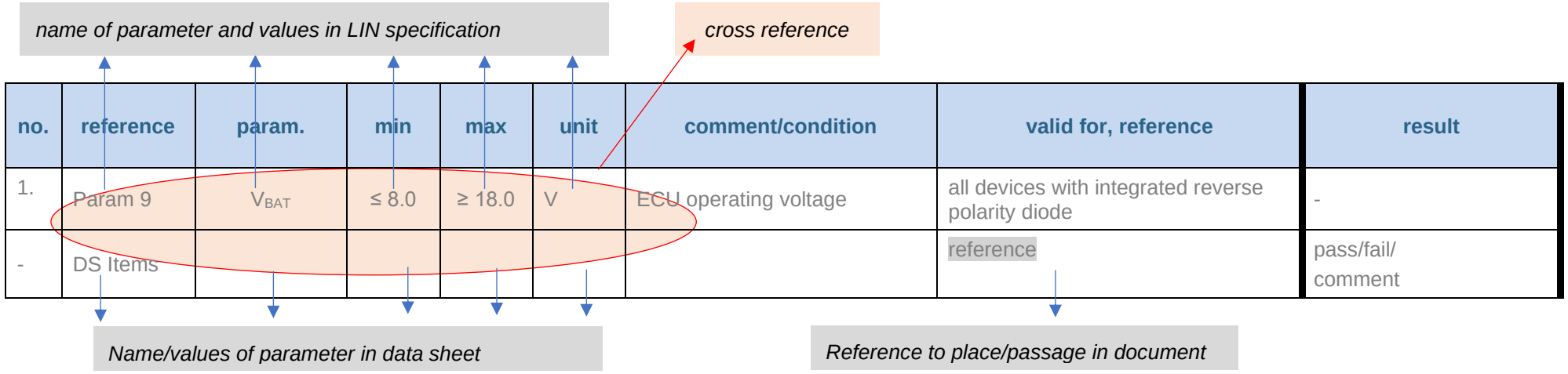
Table 41 defines the test system “LIN static test parameters for datasheets of integrated circuits”.

And in general, ISO 17987–4:2016, **1 Scope**: “All parameters in this specification are defined for the ambient temperature range from -40°C to 125°C”.

Used data sheets: **CA-IF1021-Q1_datasheet_Version1.01_en_20220629.pdf** *(Version 1.01, 2022/06/29)* (reference indicated with ‘Ref 1’)

Temperature range: Over recommended operating conditions, TJ = –40°C to 150°C (unless otherwise noted) (Ref 1; 7.5 Electrical Characteristics)

Notes to the following table:



no.	reference	param.	min	max	unit	comment/condition	valid for, reference	result
1.	Param 9	V_{BAT}	≤ 8.0	≥ 18.0	V	ECU operating voltage	all devices with integrated reverse polarity diode	-
-	DS Items						reference	pass/fail/ comment

no.	reference	parameter	min	max	unit	comment/condition	valid for, reference	result
1.	Param 9	V_{BAT} [a]	≤ 8.0	≥ 18.0	V	ECU operating voltage range	All devices with integrated reverse polarity diode	-
-								Not applicable No diode
2.	Param 10	V_{SUP} [b]	≤ 7.0	≥ 18.0	V	Supply voltage range	All devices without integrated reverse polarity diode	-
-		V_{BAT}	5.5	27	V	Battery voltage range	Ref 1; 7.3. Recommended Operating Conditions	Pass
3.	Param 11	$V_{SUP\_NON\_OP}$	≤ -0.3	≥ 40.0	V	Voltage range within which the device is not destroyed; no guarantee of correct operation.	All devices	-
-		V_{BAT}	-0.3	58	V	Supply voltage range	Ref 1; 7.1. Absolute Maximum Ratings	Pass
4.	Param 82	$V_{BUS\_MAX\_RATINGS}$	≤ -27.0	≥ 40.0	V	The part should not suffer any damage	All devices	-
-		V_{LIN}	-58	58	V	LIN bus voltage range	Ref 1; 7.1. Absolute Maximum Ratings	Pass
5.	Param 12	I_{BUS_LIM} [c]	≥ 40	≤ 200	mA	Current limitation for driver dominant state driver on $V_{BUS} = V_{BAT\_max}$ [d]	All devices with integrated LIN transmitter	-
-		I_{BUS_LIM}	40	100	mA	Driver output current limitation @dominant	Ref 1; 7.5.8 LIN	Pass

no.	reference	parameter	min	max	unit	comment/condition	valid for, reference	result
6.	Param 13	$I_{BUS\_PAS\_dom}$	≥ -1	-	mA	Input leakage current at the Receiver incl. slave pull–up resistor as specified in Param 71 driver off V_{BUS} = 0V V_{BAT}= 12V	All devices with integrated slave pull–up resistor	-
-		$I_{BUS\_PAS\_dom}$	-600		µA	Receiver input leakage current@ dominant Normal mode; V_{TXD} = 5V; V_{LIN} = 0V; V_{BAT} = 12V	Ref 1; 7.5.8 LIN	Pass
7.	Param 14	$I_{BUS\_PAS\_rec}$	-	≤ 20	µA	driver off 8V<V_{BAT}<18V 8V<V_{BUS}<18V V_{BUS} ≥ V_{BAT}	All devices	-
-		$I_{BUS\_PAS\_rec}$		20	µA	Receiver input leakage current@ recessive V_{TXD}=5V; V_{LIN}=27V; V_{BAT}=5.5V	Ref 1; 7.5.8 LIN	Pass
8.	Param 15	$I_{BUS\_NO\_GND}$	≥ -1	≤ 1	mA	Control unit disconnected from ground GND_{Device} = V_{SUP} 0V<V_{BUS}<18V V_{BAT} = 12V Loss of local ground shall not affect communication in the residual network.	All devices	-
-		$I_{BUS\_NO\_GND}$	-750	10	µA	Bus current @ loss ground V_{BAT}=27V; V_{LIN}= 0V	Ref 1; 7.5.8 LIN	Pass

no.	reference	parameter	min	max	unit	comment/condition	valid for, reference	result
9.	Param 16	$I_{BUS\_NO\_BAT}$	-	≤ 100	µA	V_{BAT} disconnected V_{SUP} = GND $0<V_{BUS}<18V$ Node shall sustain the current that can flow under this condition. Bus shall remain operational under this condition.	All devices	-
-		$I_{BUS\_NO\_BAT}$		10	µA	Bus current @ loss battery V_{BAT}=0V; V_{LIN}= 27V	Ref 1; 7.5.8 LIN	Pass
10.	Param 17	V_{BUS_dom}	-	≥ 0.4	V_{SUP}	Receiver dominant state	All devices with integrated LIN receiver	-
-		V_{BUSdom}		$0.4V_{BAT}$	V	LIN receiver dominant state	Ref 1; 7.5.8 LIN	Pass
11.	Param 18	V_{BUS_rec}	≤ 0.6	-	V_{SUP}	Receiver recessive state	All devices with integrated LIN receiver	-
-		V_{BUSrec}	$0.6V_{BAT}$		V	LIN receiver recessive state	Ref 1; 7.5.8 LIN	Pass
12.	Param 19	V_{BUS_CNT}	≥ 0.475	≤ 0.525	V_{SUP}	$V_{BUS\_CNT} = (V_{th\_dom}+V_{th\_rec})/2$ [e]	All devices with integrated LIN receiver	-
-		V_{BUS_CNT}	0.45 V_{BAT}	0.55 V_{BAT}	V	LIN receiver center threshold $V_{BUS\_CNT} = (V_{BUSdom} + V_{BUSrec})/2$	Ref 1; 7.5.8 LIN	Pass
13.	Param 20	V_{HYS}	-	≤ 0.175	V_{SUP}	$V_{HYS} = V_{th\_rec}-V_{th\_dom}$	All devices with integrated LIN receiver	-
-		V_{HYS}		0.175 V_{BAT}	V	LIN receiver hysteresis voltage $V_{HYS} = V_{BUSrec} - V_{BUSdom}$	Ref 1; 7.5.8 LIN	Pass

no.	reference	parameter	min	max	unit	comment/condition	valid for, reference	result
14.	Param 27	D1	≥ 0.396	-	-	$TH_{Rec(max)}$ = 0.744 x V_{SUP}; $TH_{Dom(max)}$ = 0.581 x V_{SUP}; V_{SUP} = 7.0V...18V; t_{BIT} = 50µs; D1 = $t_{Bus\_rec(min)}$ / (2 x t_{BIT})	All devices with integrated LIN transmitter D1 valid for 20 kbit/s	-
-		δ1	0.396			Duty cycle 1 $V_{th(rec)(max)}$=0.744xV_{BAT}; $V_{th(dom)(max)}$=0.581xV_{BAT}; t_{bit}=50µs; V_{BAT}=7V~18V	Ref 1; 7.5.10. Duty cycle	Pass
15.	Param 28	D2	-	≤ 0.581		$TH_{Rec(min)}$ = 0.422 x V_{SUP}; $TH_{Dom(min)}$ = 0.284 x V_{SUP}; V_{SUP} = 7.6V…18V; t_{BIT} = 50µs; D2 = $t_{Bus\_rec(max)}$ / (2 x t_{Bit})	all devices with integrated LIN transmitter D2 valid for 20kBaud	-
-		δ2		0.581		Duty cycle 2 $V_{th(rec)(min)}$=0.422xV_{BAT}; $V_{th(dom)(min)}$=0.284xV_{BAT}; t_{bit}=50µs; V_{BAT}=7.6V~18V	Ref 1; 7.5.10. Duty cycle	Pass
16.	Param 29	D3	≥ 0.417	-		$TH_{Rec(max)}$ = 0.778 x V_{SUP}; $TH_{Dom(max)}$ = 0.616 x V_{SUP}; V_{SUP} = 7.0V...18V; t_{BIT} = 96µs; D3 = $t_{Bus\_rec(min)}$ / (2 x t_{BIT})	All devices with integrated LIN transmitter D3 valid for 10,417 kbit/s	-
-		δ3	0.417			Duty cycle 3 $V_{th(rec)(max)}$=0.778xV_{BAT}; $V_{th(dom)(max)}$=0.616xV_{BAT}; t_{bit}=96µs; V_{BAT}=7V~18V	Ref 1; 7.5.10. Duty cycle	Pass
17.	Param 30	D4	-	≤ 0.590		$TH_{Rec(min)}$ = 0.389 x V_{SUP}; $TH_{Dom(min)}$ = 0.251 x V_{SUP}; V_{SUP} = 7.6V...18V; t_{BIT} = 96µs; D4 = $t_{Bus\_rec(max)}$ / (2 x t_{BIT})	All devices with integrated LIN transmitter D4 valid for 10,417 kbit/s	-

no.	reference	parameter	min	max	unit	comment/condition	valid for, reference	result
-		δ4		0.590		Duty cycle 4 Vth(rec)(min)=0.389xVBAT; Vth(dom)(min)=0.251xVBAT; tbit=96µs; VBAT=7.6V~18V	Ref 1; 7.5.10. Duty cycle	Pass
18.	Param 31	t_{rx_pd}	-	≤ 6	µs	Propagation delay of receiver	All devices with integrated LIN receiver	-
-		$t_{P(RX)}$		6	µs	RXD propagation delay, Rise and fall	Ref 1; 7.5.11. Switching Characteristics	Pass
19.	Param 32	t_{rx_sym}	≥ -2	≤ 2	µs	Symmetry of receiver propagation delay rising edge with respect to falling edge	All devices with integrated LIN receiver	-
-		$t_{P(RX)sym}$	-2	2	µs	RXD propagation delay symmetry	Ref 1; 7.5.11. Switching Characteristics	Pass
20.	Param 26	R_{SLAVE}	≥ 20	≤ 60	kΩ	The serial diode is mandatory.	All devices with integrated slave pull–up resistor	-
-		R_{slave}	20	47	kΩ	Slave resistance Resistance between LIN and V_{BAT}; V_{LIN} = 0V; V_{BAT} = 12V	Ref 1; 7.5.8 LIN	Pass
21.	Param 25	R_{MASTER}	≥ 900	≤ 1100	Ω	The serial diode is mandatory. Only for valid for transceiver with integrated master pull–up resistor	All devices with integrated master pull–up resistor	-
-								Not applicable No master
22.	Param 37	C_{SLAVE}	-	≤ 250	pF	Capacitance of slave node	All LIN slave devices	-

no.	reference	parameter	min	max	unit	comment/condition	valid for, reference	result
-								Not applicable No slave
23.	6.3.7.1 General	LIN device states changes	-	-	-	All LIN device state changes on conditional events (e.g. temperature shut–down) shall be specified in the LIN device data sheet.	All devices	-
-		$T_{jsd(sd)}$	160	200	°C	Thermal shutdown temperature	Ref 1; 7.5.9. Thermal Shutdown	Pass
-		$t_{to(dom)TXD}$	27	90	ms	TXD-dominant timeout V_{TXD} = 0V	Ref 1; 7.5.11. Switching Characteristics	Pass
24.		LIN transceiver input capacitance	-	-	-	A maximum LIN transceiver input capacitance shall be specified in the LIN device data sheet. Please consider the data sheet limits (e.g. voltage, temperature).	All devices	-
-		C_{LIN}		30	pF	Capacitance on LIN pin	Ref 1; 7.5.8 LIN	Pass

[a] V_{BAT} denotes the supply voltage at the connector of the control unit and may be different from the internal supply V_{SUP} for electronic components (see ISO 17987-4 subclause 5.3.2).
[b] V_{SUP} denotes the supply voltage at the transceiver inside the control unit and may be different from the external supply V_{BAT} for control units (see ISO 17987-4 subclause 5.3.2).
[c] I_{BUS}: Current flowing into the node.
[d] A transceiver shall be capable to sink at least 40mA. The maximum current flowing into the node shall not exceed 200 mA under DC conditions to avoid possible damage.
[e] V_{th_dom}: receiver threshold of the recessive to dominant LIN bus edge. $V_{th\_rec:}$ receiver threshold of the dominant to recessive LIN bus edge.

6 Test Protocol Dynamic Tests

Following test case numeration and cross references relates on the corresponding test specification.

5.2 Operational conditions – Calibration

5.2.2 [EPL–CT 1] Operating voltage range

This test shall ensure the correct operation in the valid supply voltage ranges, by correct reception of dominant bits. The IUT is therefore supplied with an increasing/decreasing voltage ramp.

[EPL–CT 1].1 [7.0 V to 18 V]

Comment	Test Result
Observed minimal Duty Cycle	50.00%
Observed maximal Duty Cycle	50.10%
The RX pin of the IUT shall show the 10 kHz signal. A maximum deviation of 10 % (time, voltage) is allowed.	Pass

[EPL–CT 1].2 [18 V to 7.0 V]

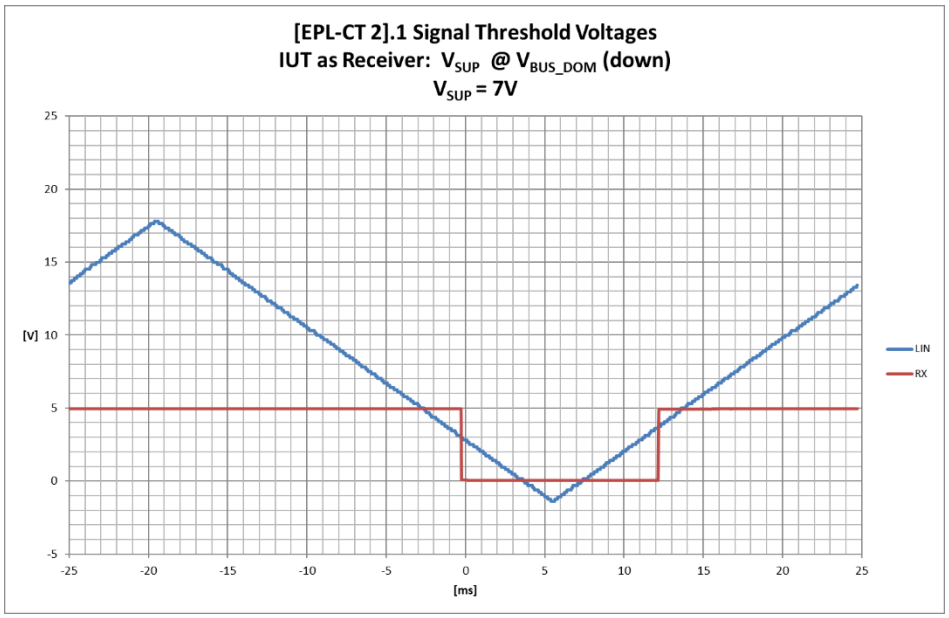
Comment	Test Result
Observed minimal Duty Cycle	50.00%
Observed maximal Duty Cycle	50.10%
The RX pin of the IUT shall show the 10 kHz signal. A maximum deviation of 10 % (time, voltage) is allowed.	Pass

5.2.3 Threshold voltages

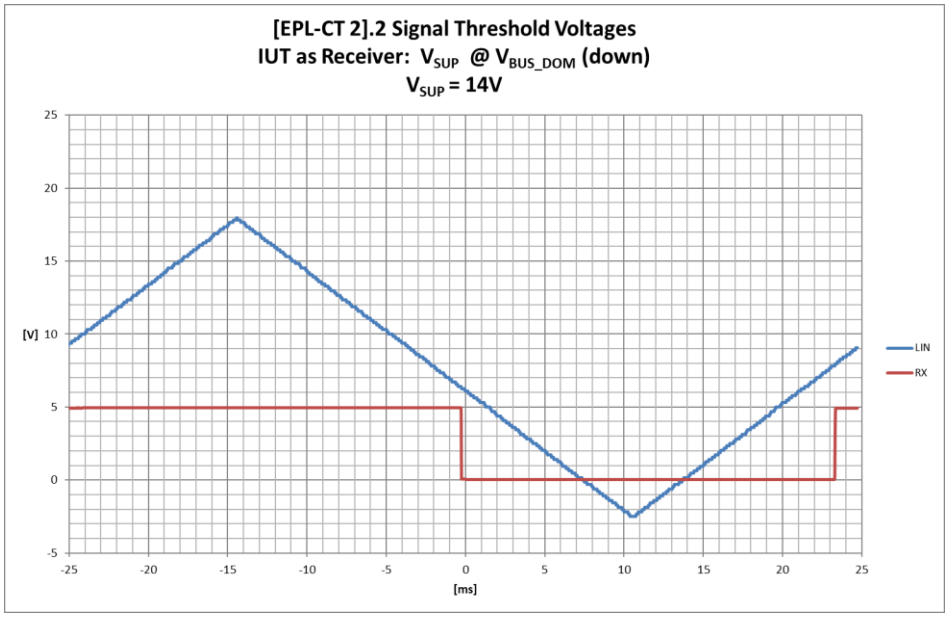
This group of tests checks whether the receiver threshold voltages of the IUT are implemented correctly within the entire specified operating supply voltage range. The LIN bus voltage is driven with a voltage ramp checking the entire dominant and recessive signal area with respect to the applied supply voltage. In 5.2.3.2 and 5.2.3.3 the signal shall stay continuously on recessive or dominant level depending on the test case. In 5.2.3.4 the RX output transition is detected.

5.2.3.2 [EPL–CT 2] IUT as receiver: V_{SUP} @ V_{BUS_dom} (down)

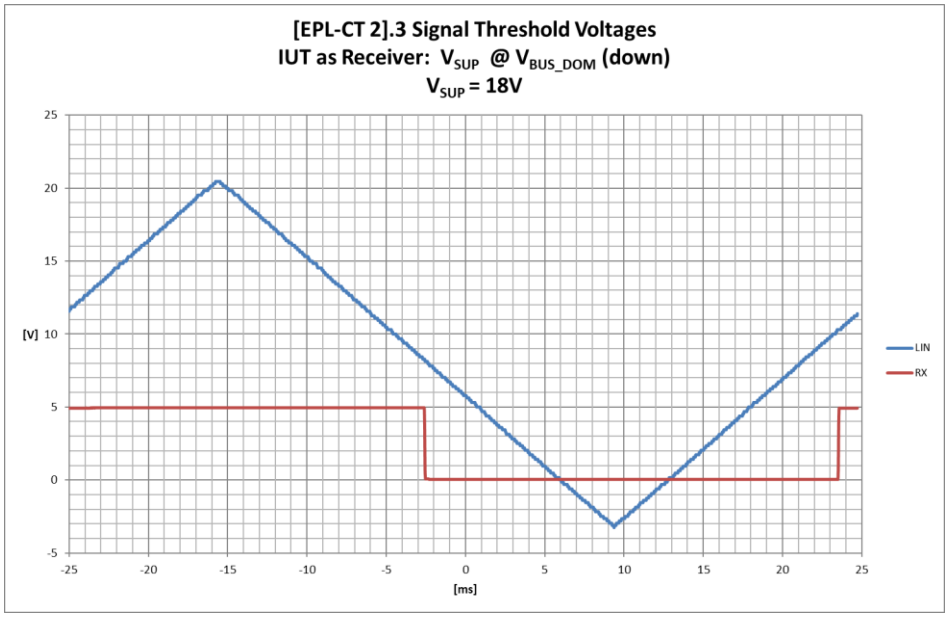
EPL–CT–TC	V_{IUT}: [V_{SUP}]	Signal range	Expected RX signal	Measured RX Signal
[EPL–CT 2].1	7V	[18V to 4.2V]	recessive	recessive
		[2.8V to –1.05V]	dominant	dominant



EPL–CT–TC	V_{IUT}: [V_{SUP}]	Signal range	Expected RX signal	Measured RX Signal
[EPL–CT 2].2	14V	[18V to 8.4V]	recessive	recessive
		[5.6V to -2.1V]	dominant	dominant



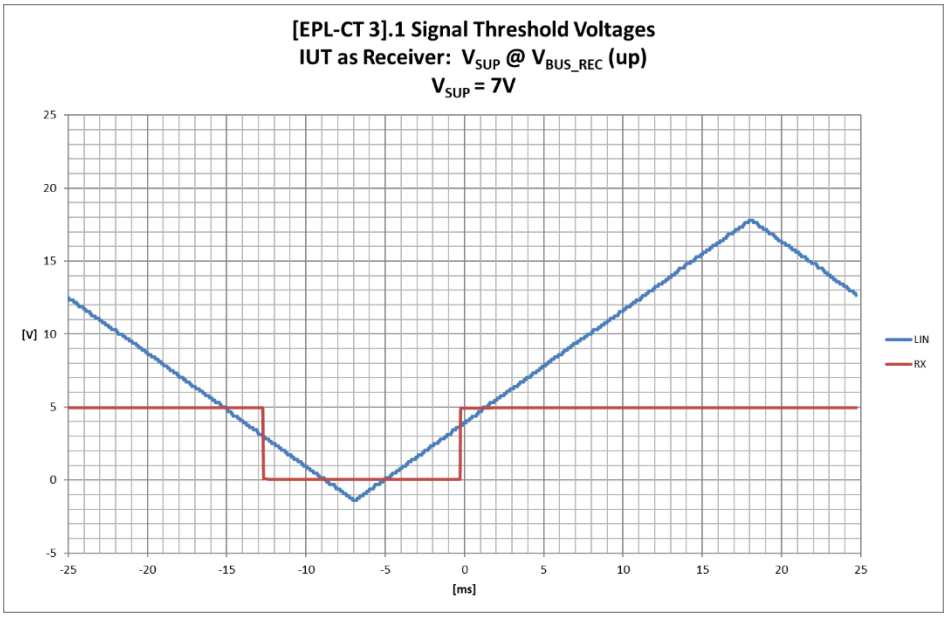
EPL–CT–TC	V_{IUT}: [V_{SUP}]	Signal range	Expected RX signal	Measured RX Signal
[EPL–CT 2].3	18V	[20.7V to 10.8V]	recessive	recessive
		[7.2V to -2.7V]	dominant	dominant



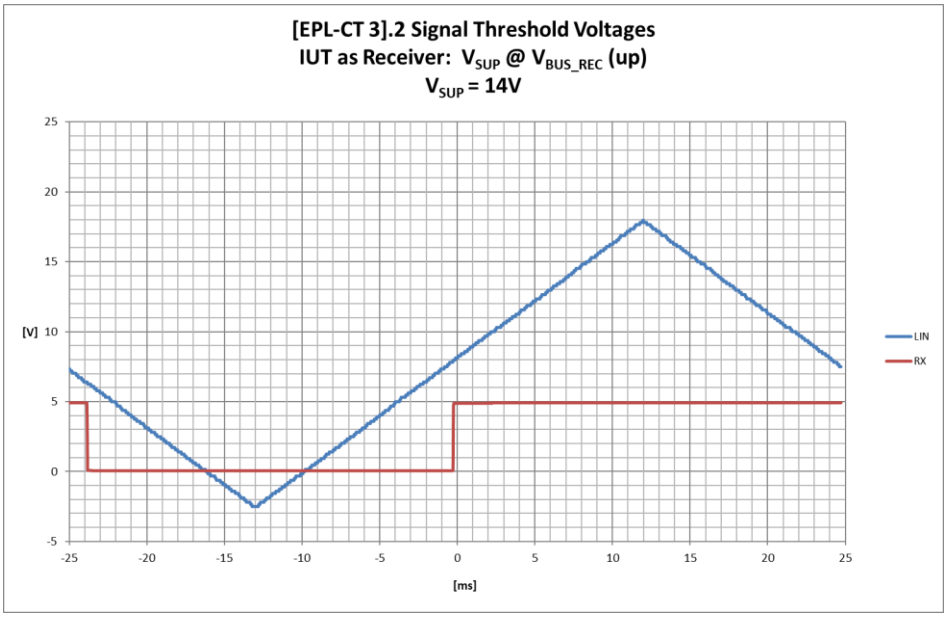
Comment	Test Result
The IUT shall generate a dominant or recessive value on RX as defined during the falling slope of the triangle signal.	Pass

5.2.3.3 [EPL–CT 3] IUT as receiver: V_{SUP} @ V_{BUS_dom} (up)

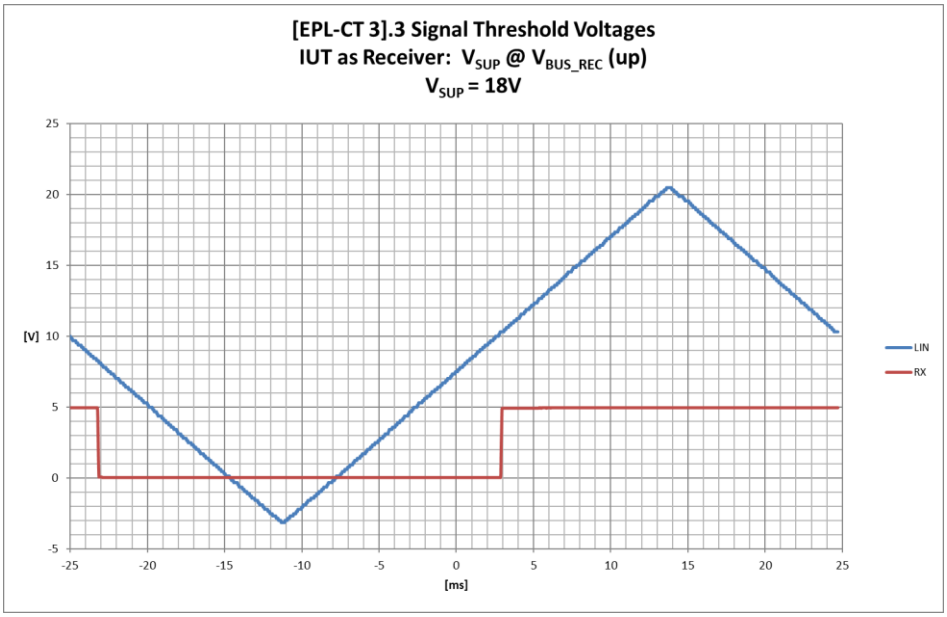
EPL–CT–TC	V_{IUT}: [V_{SUP}]	Signal range	Expected RX signal	Measured RX Signal
[EPL–CT 3].1	7V	[-1.05V to 2.8V]	dominant	dominant
		[4.2 V to 18 V]	recessive	recessive



EPL–CT–TC	V_{IUT}: [V_{SUP}]	Signal range	Expected RX signal	Measured RX Signal
[EPL–CT 3].2	14V	[–2.1 V to 5.6 V]	dominant	dominant
		[8.4 V to 18 V]	recessive	recessive



EPL–CT–TC	V_{IUT}: [V_{SUP}]	Signal range	Expected RX signal	Measured RX Signal
[EPL–CT 3].3	18V	[–2.7V to 7.2V]	dominant	dominant
		[10.8V to 20.7V]	recessive	recessive



Comment	Test Result
The IUT shall generate a dominant or recessive value on RX as defined during the rising slope of the triangle signal.	Pass

5.2.3.4 [EPL–CT 4] IUT as receiver: V_{SUP} @V_{BUS}

This test shall verify the symmetry of the receiver thresholds. For this purpose a voltage ramp on V_{BUS} shows the required threshold values.

EPL–CT–TC	V_{IUT}: [V_{SUP}]	Signal range up	Signal range down
[EPL–CT 4].1	7V	[-1.05V to 8.05V]	[8.05V to -1.05V]
	V_th_dom	3.281 V	-
	V_th_rec	-	3.969 V
	V_hys	0.688 V	
	V_bus_cnt	3.625 V	

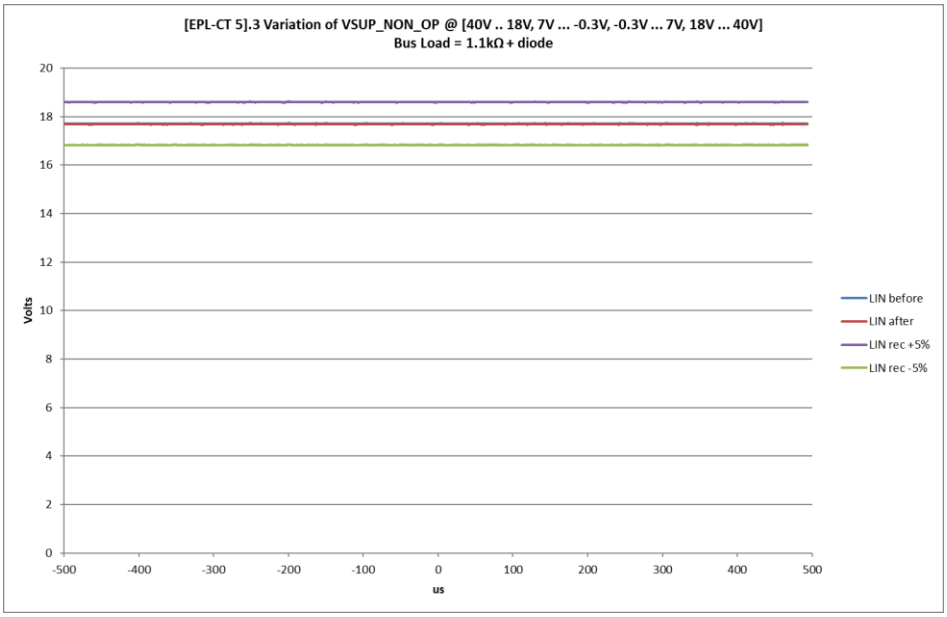
EPL–CT–TC	V_{IUT}: [V_{SUP}]	Signal range up	Signal range down
[EPL–CT 4].2	14V	[-2.1V to 16.1V]	[16.1 V to -2.1V]
	V_th_dom	6.500 V	-
	V_th_rec	-	8.125 V
	V_hys	1.625 V	
	V_bus_cnt	7.313 V	

EPL–CT–TC	V_{IUT}: [V_{SUP}]	Signal range up	Signal range down
[EPL–CT 4].3	18V	[-2.7V to 20.7V]	[20.7V to -2.7V]
	V_th_dom	8.375 V	-
	V_th_rec	-	10.500 V
	V_hys	2.125 V	
	V_bus_cnt	9.438 V	

Comment	Test Result
The RX output of the IUT shall switch from dominant to recessive when the LIN bus voltage ramps up and it shall switch from recessive to dominant when the LIN bus voltage ramps down. The RX output transition shall meet the following conditions: $V_{BUS\_CNT} = (V_{th\_dom} + V_{th\_rec})/2$ in the range of [0.475 to 0.525] x V_{SUP} $V_{HYS} = V_{th\_rec} - V_{th\_dom}$ shall be less than 0.175 x V_{SUP}	Pass

5.2.4 [EPL–CT 5] Variation of VSUP_NON_OP

EPL–CT–TC	V_{IUT} range: [V_{SUP} range]	V_{PS2}	Bus load
[EPL–CT 5].3	[–0.3 V to 7 V], [18 V to 40 V]	18V	1.1 k + diode (1N4148)



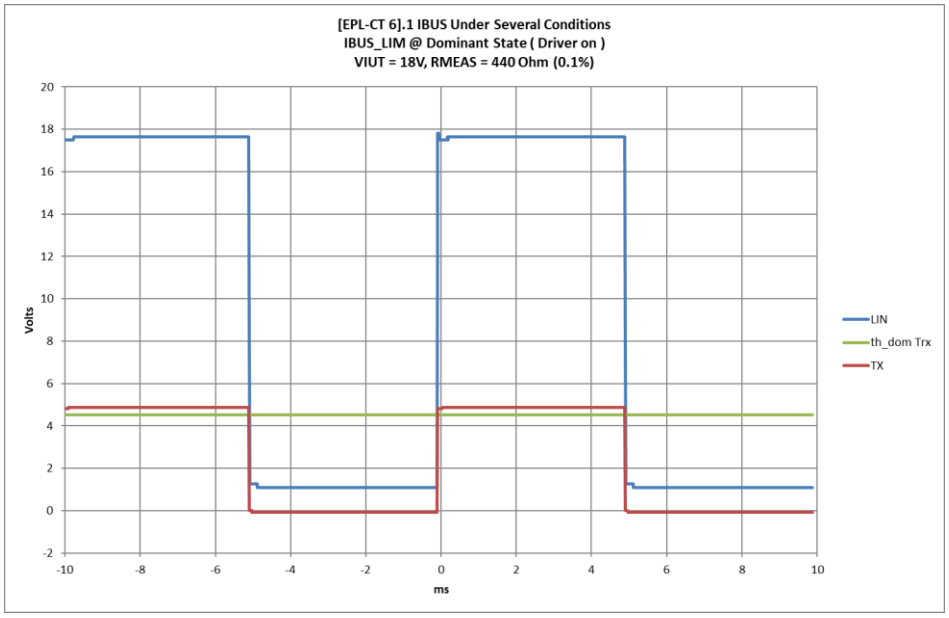
Comment	Test Result
No dominant state on LIN shall occur. The IUT shall not be destroyed during the test. The afterward recessive voltage shall have a maximum deviation of ±5 % from the before recessive voltage.	Pass

5.2.5 I_{BUS} under several conditions

5.2.5.1 [EPL–CT 6] I_{BUS_LIM} @ dominant state (driver on)

This test checks the drive capability of the output stage. A LIN driver shall pull the LIN bus below a certain voltage according to the LIN standard. The current limitation is measured indirectly.

EPL–CT–TC	V_{IUT}: [V_{SUP}]	R_{MEAS}
[EPL–CT 6].1	18V	440Ω (0.1%)



Comment	Test Result
LIN shall show the rectangular Signal. The dominant state bus level shall be lower than TH_DOM = 0.251 x V_{IUT}= 4.518 V for transceiver.	Pass

5.2.5.2 [EPL–CT 7] $I_{BUS\_PAS\_dom}$: IUT in recessive state: V_{BUS} = 0 V

This test case is intended to test the input Leakage Current IBUS_PAS_dom into a node during dominant state of the LIN bus.

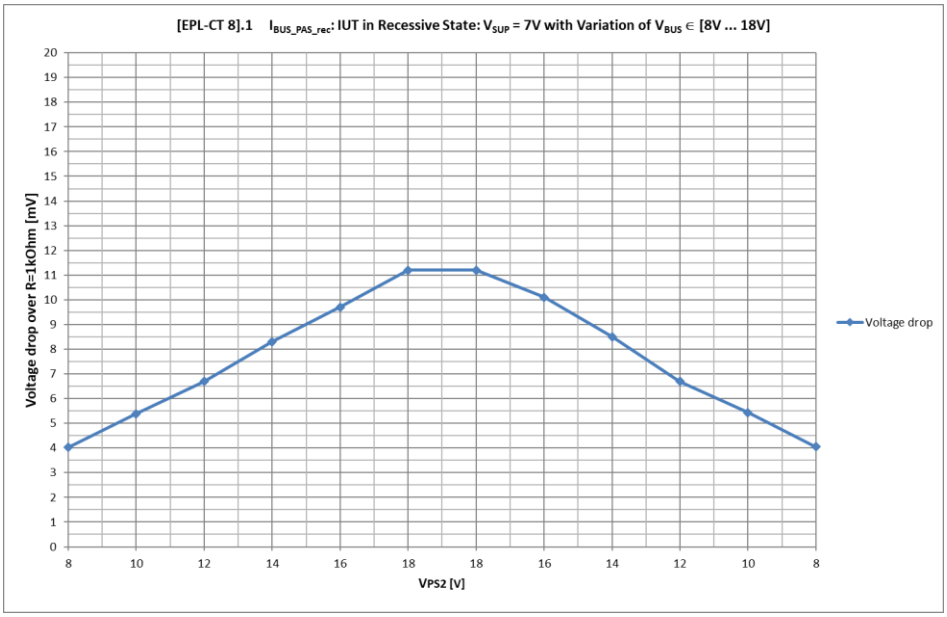
EPL–CT–TC	V_{IUT}: [V_{SUP}]	R_{MEAS}	Measured voltage drop
[EPL–CT 7].1	12V	499Ω (0.1%)	-216 mV

Comment	Test Result
The maximum value of voltage drop shall be higher than –500 mV.	Pass

5.2.5.3 [EPL–CT 8] $I_{BUS\_PAS\_rec}$: IUT in recessive state: V_{SUP} = 7.0 V with variation of $V_{BUS} \in$ [8.0 V to 18 V]

The [EPL–CT 8].1 is checking, whether there is a diode implementation within the termination path of the IUT. The reverse current should be limited to $I_{BUS\_PAS\_rec\ (Max)}$ from the LIN wire into the IUT even if V_{BUS} is higher than the IUTs supply voltage V_{IUT}.

EPL–CT–TC	V_{IUT}: [V_{SUP}]	R_{MEAS}
[EPL–CT 8].1	7V	1000Ω (0.1%)

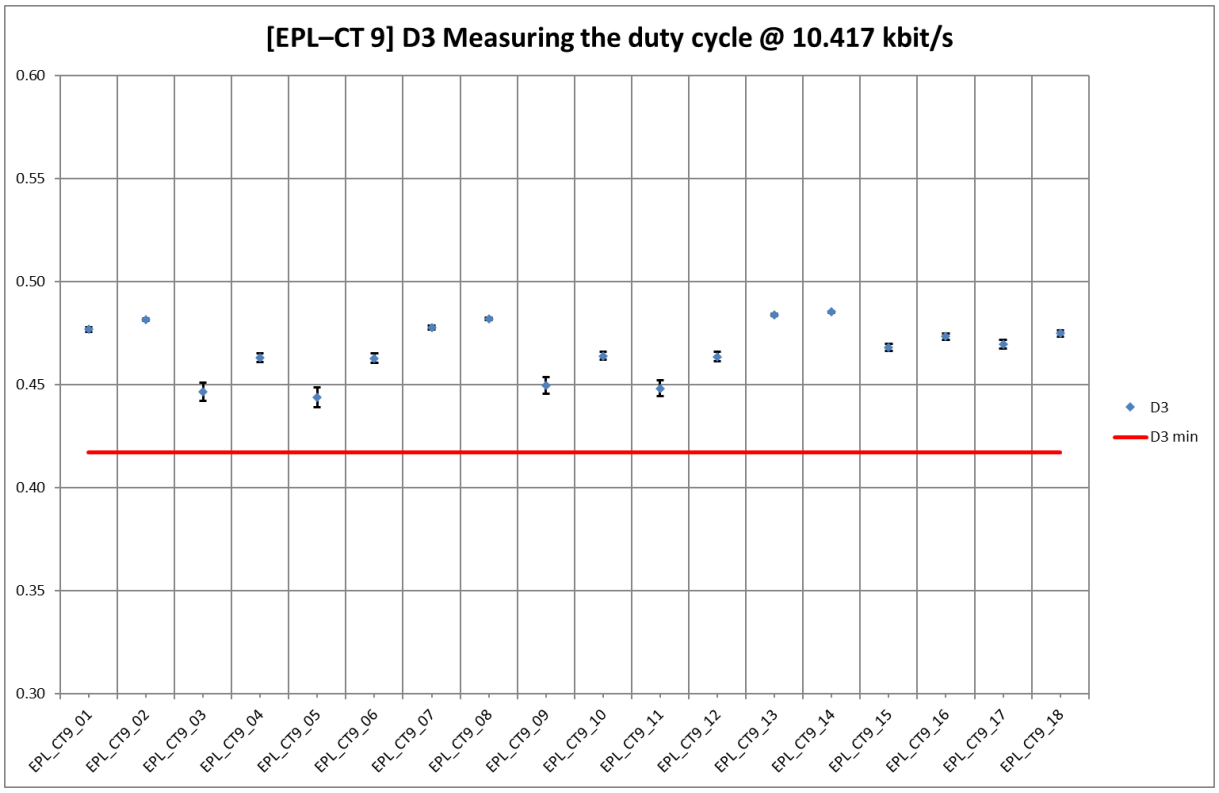


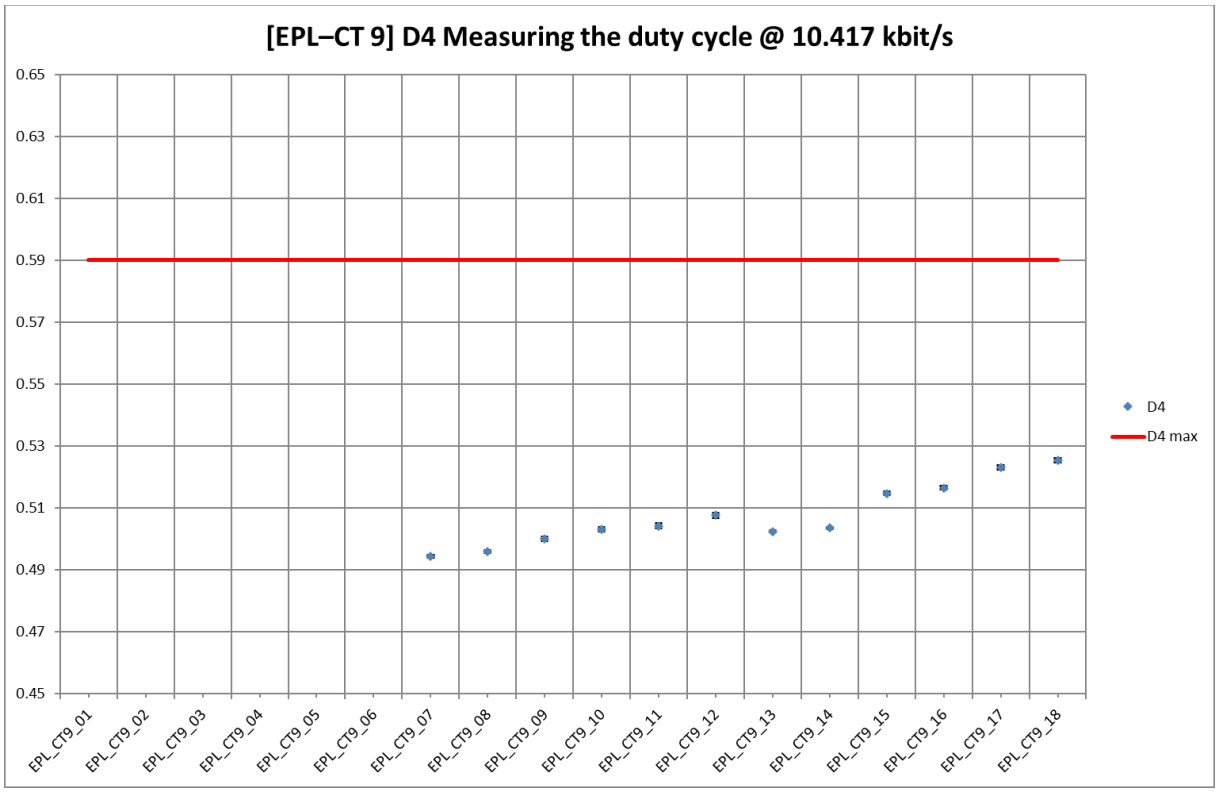
Comment	Test Result
The maximum value of voltage drop shall be less or equal 20 mV.	Pass

5.2.6 Slope control

Purpose of this test is checking the duty cycle of the driver stage.

5.2.6.2 [EPL–CT 9] Measuring the duty cycle @ 10.417 kbit/s – IUT as transmitter





EPL–CT–TC	V_{IUT}: [V_{SUP}] (PS 1)	V_{PS2} (PS 2)	Bus loads (CBUS; RBUS)	Duty cycle		Result
				D3 ±U*	D4 ±U*	
[EPL-CT 9].1	7.0V	6.0V	1nF (1%); 1kΩ (0.1%)	0.477 ±0.001	–	Pass
[EPL-CT 9].2	7.0V	6.6V	1nF (1%); 1kΩ (0.1%)	0.481 ±0.001	–	Pass
[EPL-CT 9].3	7.0V	6.0V	6.8nF (1%); 660 Ω (0.1%)	0.446 ±0.004	–	Pass
[EPL-CT 9].4	7.0V	6.6V	6.8nF (1%); 660 Ω (0.1%)	0.463 ±0.002	–	Pass
[EPL-CT 9].5	7.0V	6.0V	10nF (1%); 500 Ω (0.1%)	0.444 ±0.005	–	Pass
[EPL-CT 9].6	7.0V	6.6V	10nF (1%); 500 Ω (0.1%)	0.463 ±0.002	–	Pass
[EPL-CT 9].7	7.6V	6.6V	1nF (1%); 1kΩ (0.1%)	0.478 ±0.001	0.494 ±0.00	Pass
[EPL-CT 9].8	7.6V	7.2V	1nF (1%); 1kΩ (0.1%)	0.482 ±0.001	0.496 ±0.00	Pass
[EPL-CT 9].9	7.6V	6.6V	6.8nF (1%); 660 Ω (0.1%)	0.450 ±0.004	0.500 ±0.001	Pass
[EPL-CT 9].10	7.6V	7.2V	6.8nF (1%); 660 Ω (0.1%)	0.464 ±0.002	0.503 ±0.001	Pass
[EPL-CT 9].11	7.6V	6.6V	10nF (1%); 500 Ω (0.1%)	0.448 ±0.004	0.504 ±0.001	Pass
[EPL-CT 9].12	7.6V	7.2V	10nF (1%); 500 Ω (0.1%)	0.464 ±0.002	0.508 ±0.001	Pass
[EPL-CT 9].13	18V /	17.0V	1nF (1%); 1kΩ (0.1%)	0.484 ±0.00	0.502 ±0.00	Pass
[EPL-CT 9].14	18V	17.6V	1nF (1%); 1kΩ (0.1%)	0.485 ±0.00	0.504 ±0.00	Pass
[EPL-CT 9].15	18V	17.0V	6.8nF (1%); 660 Ω (0.1%)	0.468 ±0.002	0.515 ±0.001	Pass
[EPL-CT 9].16	18V	17.6V	6.8nF (1%); 660 Ω (0.1%)	0.473 ±0.001	0.516 ±0.00	Pass
[EPL-CT 9].17	18V	17.0V	10nF (1%); 500 Ω (0.1%)	0.469 ±0.002	0.523 ±0.001	Pass
[EPL-CT 9].18	18V	17.6V	10nF (1%); 500 Ω (0.1%)	0.475 ±0.002	0.525 ±0.001	Pass

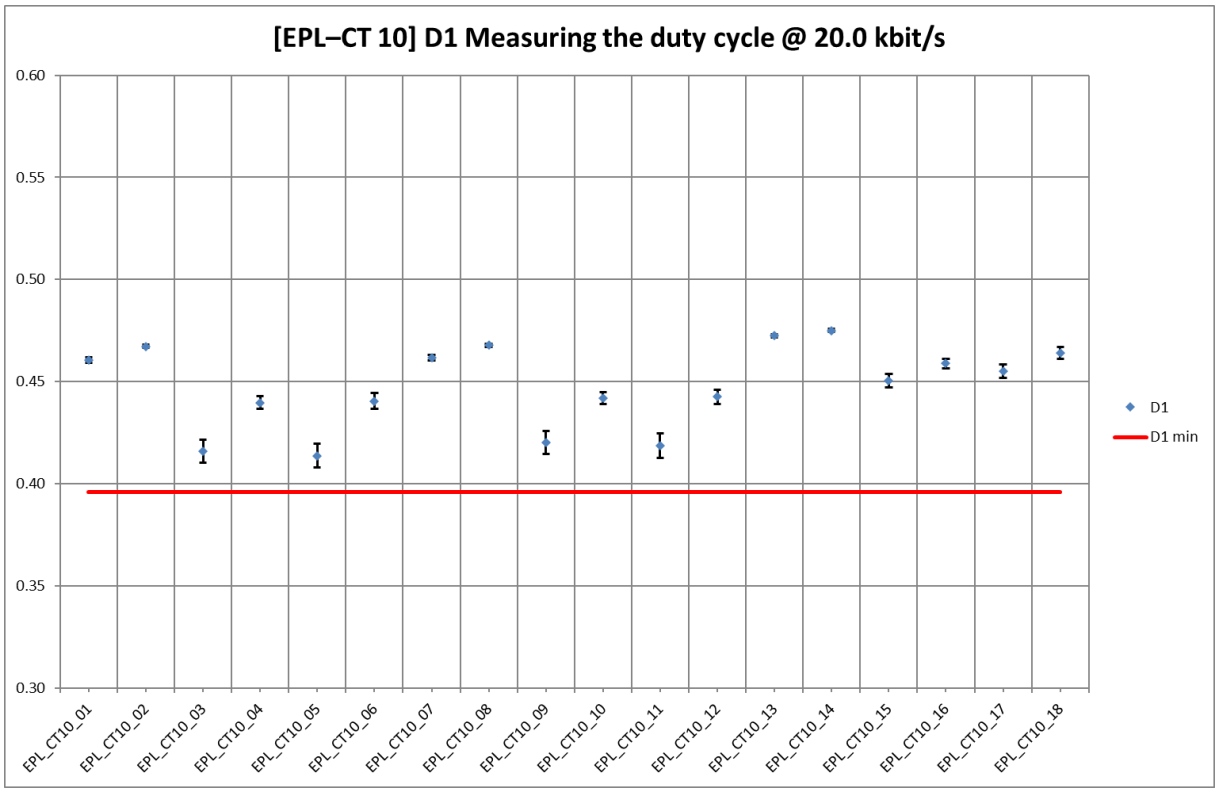
Comment	Test Result
The measured duty cycle D3 shall be greater or equal than 0.417 for V_{SUP} = [7.0 V to 18 V], the measured duty cycle D4 shall be less or equal than 0.590 for V_{SUP} = [7.6 V to 18 V]. If V_{SUP} is not accessible then V_{BAT} – 0.7 V shall be used for calculation of the duty cycle.	Pass

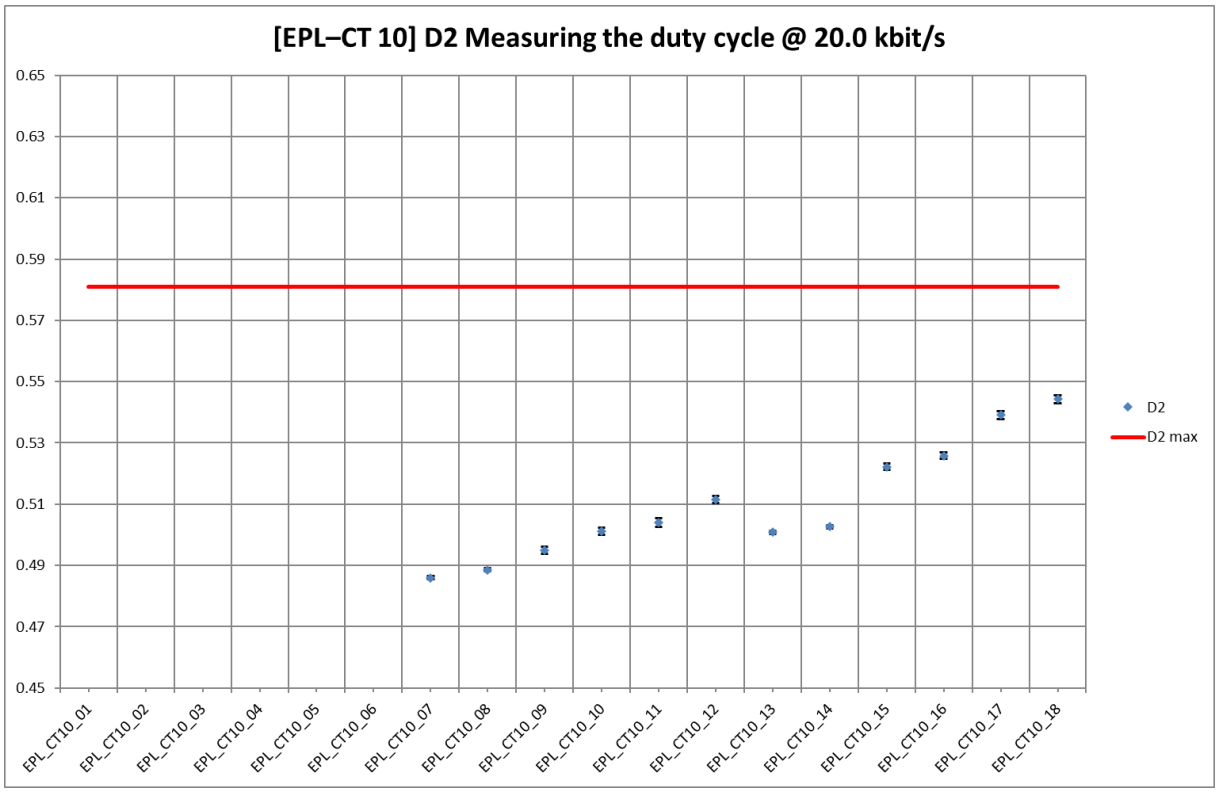
*The measurement uncertainty analysis based on the type B evaluation according to the “Guide to the Expression of Uncertainty in Measurement” (European Committee for Standardization, ENV 13005, 1999).

The steps involved are as follows:

1. Evaluation of the relationship between input quantities xi and the output quantity $y = f(x_1, x_2, \ldots, x_n)$
2. Identification of the standard uncertainty $u(x_i)$ for each input estimate x_i
3. Identification of the combined standard uncertainty $u_c(x_i)$ for the output quantity y
4. Calculation of the expanded uncertainty $U = k \cdot u_c(x_i)$, with coverage factor k=2. The coverage probability is approximately 95%.

5.2.6.3 [EPL–CT 10] Measuring the duty cycle @ 20.0 kbit/s – IUT as transmitter





EPL–CT–TC	V_{IUT}: [V_{SUP}] (PS 1)	V_{PS2} (PS 2)	Bus loads (CBUS; RBUS)	Duty cycle		Result
				D1 ±U*	D2 ±U*	
[EPL-CT 10].1	7.0V	6.0V	1nF (1%); 1kΩ (0.1%)	0.461 ±0.001	–	Pass
[EPL-CT 10].2	7.0V	6.6V	1nF (1%); 1kΩ (0.1%)	0.467 ±0.001	–	Pass
[EPL-CT 10].3	7.0V	6.0V	6.8nF (1%); 660 Ω (0.1%)	0.416 ±0.006	–	Pass
[EPL-CT 10].4	7.0V /	6.6V	6.8nF (1%); 660 Ω (0.1%)	0.440 ±0.003	–	Pass
[EPL-CT 10].5	7.0V	6.0V	10nF (1%); 500 Ω (0.1%)	0.414 ±0.006	–	Pass
[EPL-CT 10].6	7.0V	6.6V	10nF (1%); 500 Ω (0.1%)	0.441 ±0.004	–	Pass
[EPL-CT 10].7	7.6V	6.6V	1nF (1%); 1kΩ (0.1%)	0.462 ±0.001	0.486 ±0.001	Pass
[EPL-CT 10].8	7.6V	7.2V	1nF (1%); 1kΩ (0.1%)	0.468 ±0.001	0.489 ±0.00	Pass
[EPL-CT 10].9	7.6V	6.6V	6.8nF (1%); 660 Ω (0.1%)	0.420 ±0.006	0.495 ±0.001	Pass
[EPL-CT 10].10	7.6V	7.2V	6.8nF (1%); 660 Ω (0.1%)	0.442 ±0.003	0.501 ±0.001	Pass
[EPL-CT 10].11	7.6V	6.6V	10nF (1%); 500 Ω (0.1%)	0.419 ±0.006	0.504 ±0.001	Pass
[EPL-CT 10].12	7.6V	7.2V	10nF (1%); 500 Ω (0.1%)	0.443 ±0.004	0.512 ±0.001	Pass
[EPL-CT 10].13	18V	17.0V	1nF (1%); 1kΩ (0.1%)	0.472 ±0.001	0.501 ±0.001	Pass
[EPL-CT 10].14	18V	17.6V	1nF (1%); 1kΩ (0.1%)	0.475 ±0.001	0.503 ±0.001	Pass
[EPL-CT 10].15	18V	17.0V	6.8nF (1%); 660 Ω (0.1%)	0.450 ±0.003	0.522 ±0.001	Pass
[EPL-CT 10].16	18V	17.6V	6.8nF (1%); 660 Ω (0.1%)	0.459 ±0.002	0.526 ±0.001	Pass
[EPL-CT 10].17	18V	17.0V	10nF (1%); 500 Ω (0.1%)	0.455 ±0.003	0.539 ±0.001	Pass
[EPL-CT 10].18	18V	17.6V	10nF (1%); 500 Ω (0.1%)	0.464 ±0.003	0.544 ±0.001	Pass

Comment	Test Result
The measured duty cycle D1 shall be greater or equal than 0.396 for V_{SUP} = [7.0 V to 18 V], the measured duty cycle D2 shall be less or equal than 0.581 for V_{SUP} = [7.6 V to 18 V]. If V_{SUP} is not accessible then V_{BAT} – 0.7 V shall be used for calculation of the duty cycle.	Pass

*The measurement uncertainty analysis based on the type B evaluation according to the “Guide to the Expression of Uncertainty in Measurement” (European Committee for Standardization, ENV 13005, 1999).

The steps involved are as follows:

1. Evaluation of the relationship between input quantities xi and the output quantity $y = f(x_1, x_2, \ldots, x_n)$
2. Identification of the standard uncertainty $u(x_i)$ for each input estimate x_i
3. Identification of the combined standard uncertainty $u_c(x_i)$ for the output quantity y
4. Calculation of the expanded uncertainty $U = k \cdot u_c(x_i)$, with coverage factor k=2. The coverage probability is approximately 95%.

5.2.7 Propagation delay

The following test checks the receiver's internal delay and its symmetry. The method for measuring the values is shown in ISO 17987–4 Figure 5 subclause 5.3.3.

5.2.7.2 [EPL–CT 11] Propagation delay of the receiver

EPL–CT–TC	V_{IUT}: [V_{SUP}]	RX Load	t_{rx_pdf}	t_{rx_pdr}	t_{rx_pd}	t_{rx_sym}
EPL–CT 11].1	7V	20pF, 2.4kΩ	0.740 µs	1.400 µs	1.400 µs	-0.660 µs
EPL–CT 11].2	14V	20pF, 2.4kΩ	0.495 µs	1.000 µs	1.000 µs	-0.505 µs
EPL–CT 11].3	18V	20pF, 2.4kΩ	0.440 µs	0.895 µs	0.895 µs	-0.455 µs

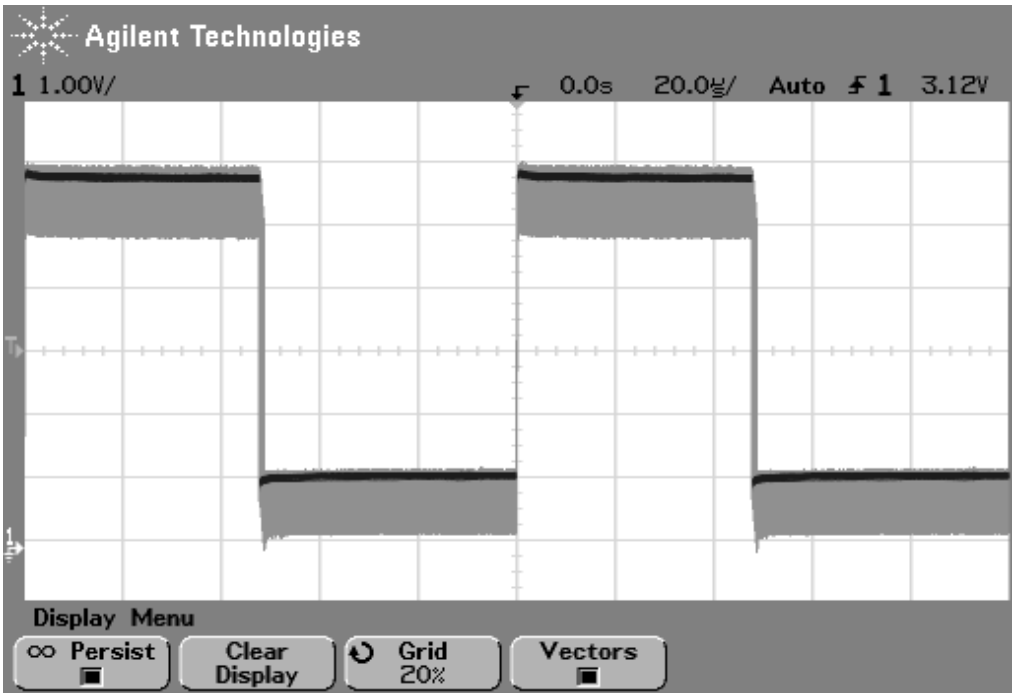
Comment	Test Result
The measured time t_{rx_pd} shall be less than 6 µs. $t_{rx\_sym} = t_{rx\_pdf} - t_{rx\_pdr}$ shall be in the range –2 to +2 µs.	Pass

5.2.8 Supply voltage offset

The purpose of the test is to check the robustness in case of V_{BAT} and Ground shift.

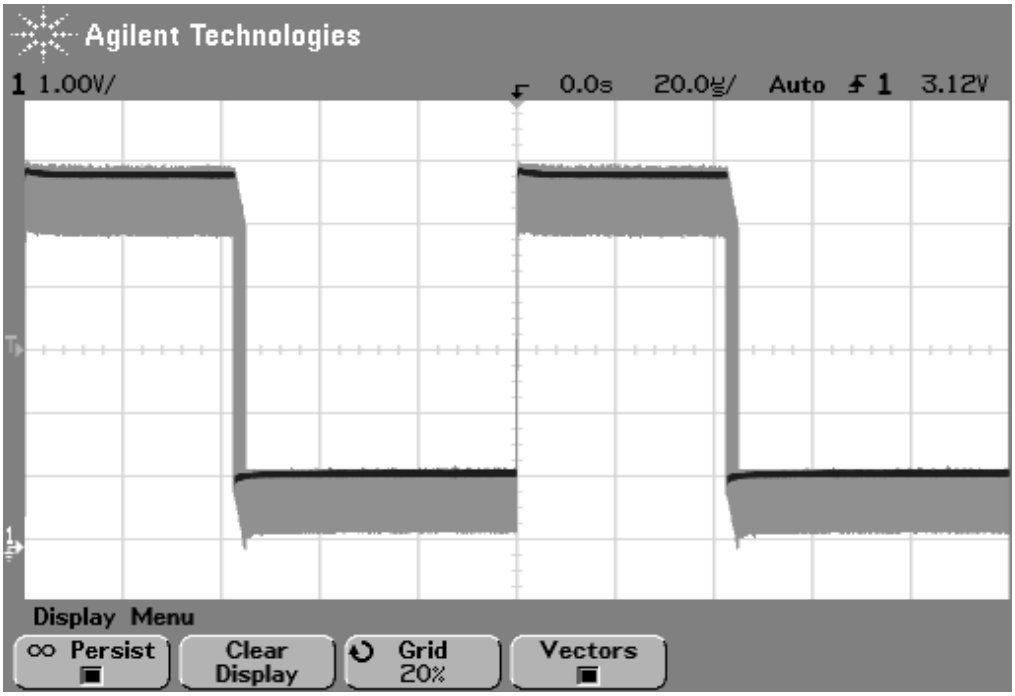
5.2.8.3 [EPL–CT 12] GND shift test – Dynamic – IUT as class A device

IUT as receiver



1kΩ/1nF

IUT as receiver

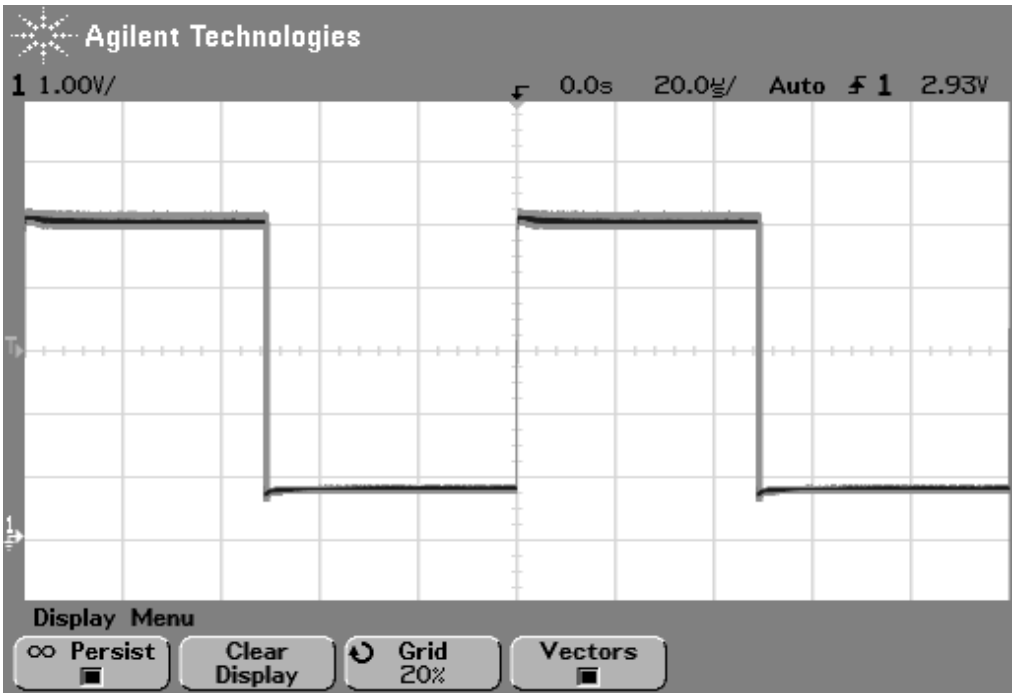


500Ω/10nF

Comment	Test Result
Observed Duty Cyle Range 1kΩ/1nF	47.6% – 48.8%
Observed Duty Cyle Range 500Ω/10nF	42.6% – 45.0%
The duty cycle measured at RXD2 shall be in the range of 0.376 to 0.601 (D1 – 2 µs to D2 + 2 µs).	Pass

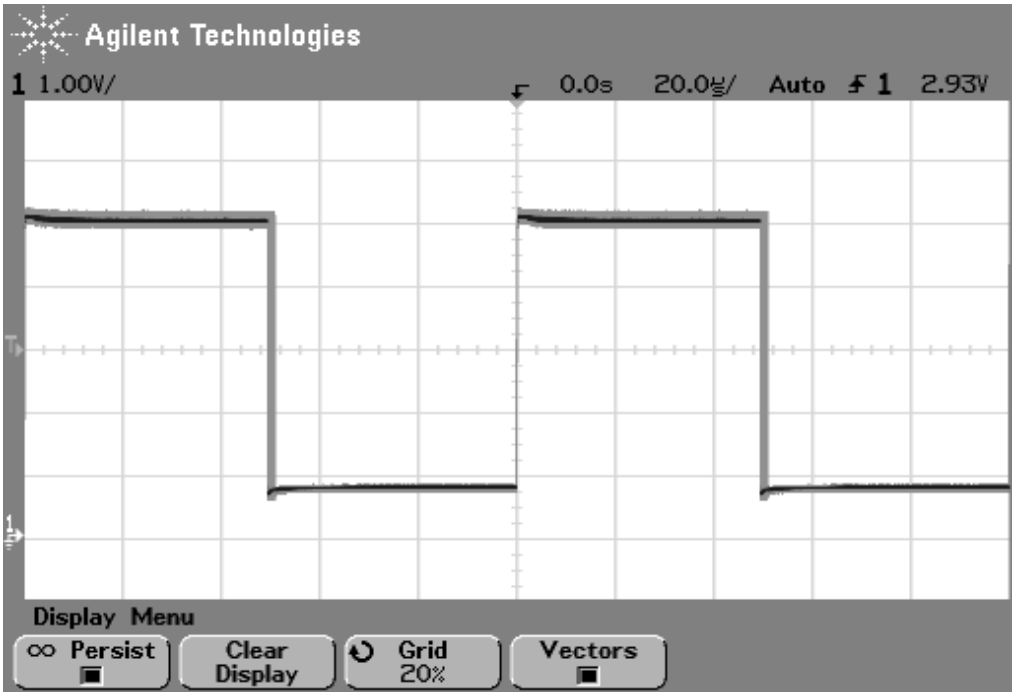
5.2.8.4 [EPL–CT 13] GND shift test – Dynamic – IUT as class A device

IUT as transmitter



1kΩ/1nF

IUT as transmitter

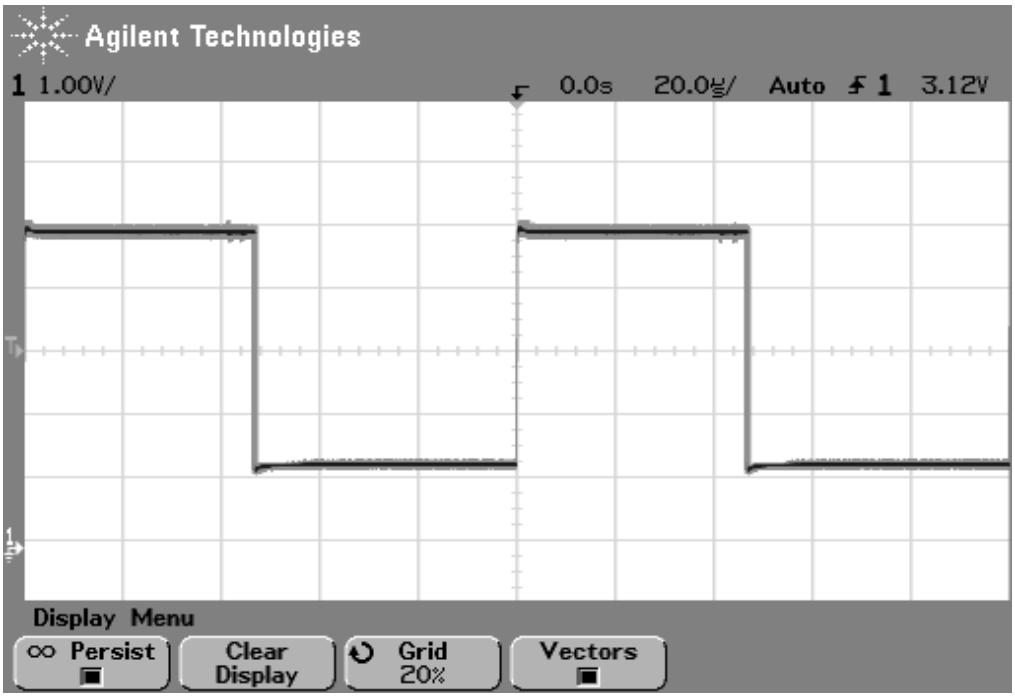


500Ω/10nF

Comment	Test Result
Observed Duty Cyle Range 1kΩ/1nF	48.8% – 49.8%
Observed Duty Cyle Range 500Ω/10nF	49.6% – 51.0%
The duty cycle measured at RXD2 shall be in the range of 0.376 to 0.601 (D1 – 2 µs to D2 + 2 µs).	Pass

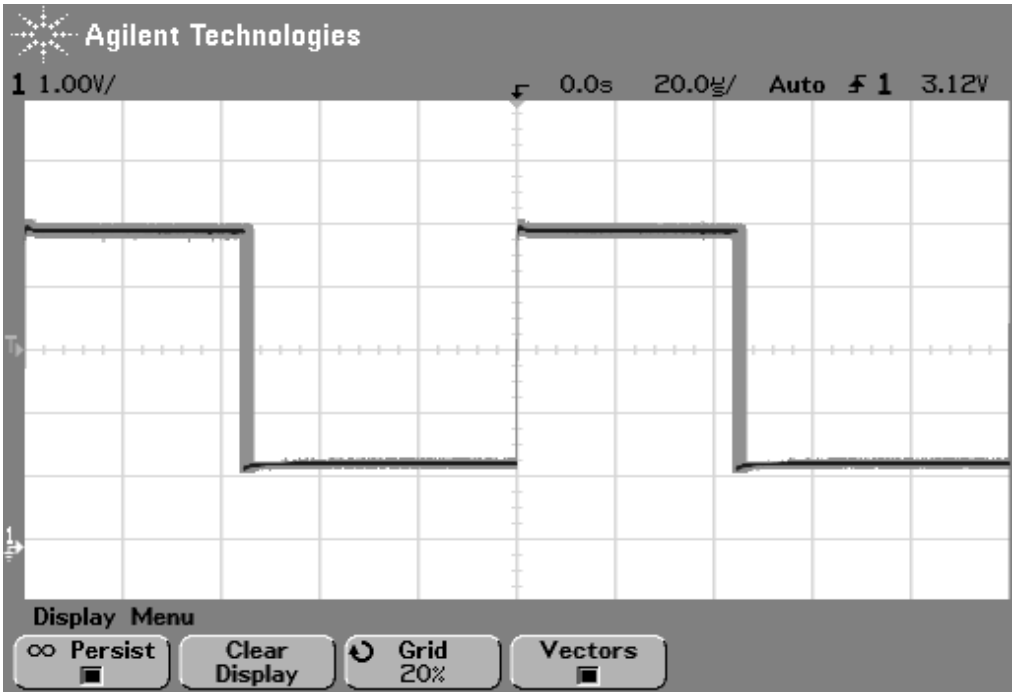
5.2.8.5 [EPL–CT 14] V_{BAT} shift test – Dynamic – IUT as class A device

IUT as transmitter



1kΩ/1nF

IUT as transmitter

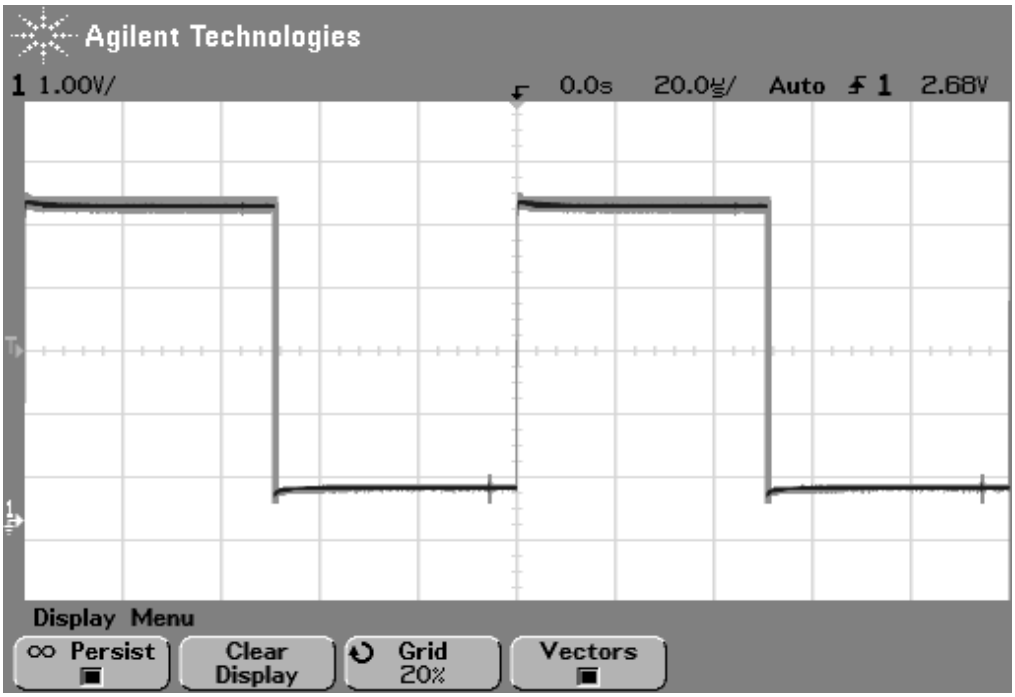


500Ω/10nF

Comment	Test Result
Observed Duty Cyle Range 1kΩ/1nF	46.3% – 47.4%
Observed Duty Cyle Range 500Ω/10nF	44.1% – 46.6%
The duty cycle measured at RXD2 shall be in the range of 0.376 to 0.601 (D1 – 2 µs to D2 + 2 µs).	Pass

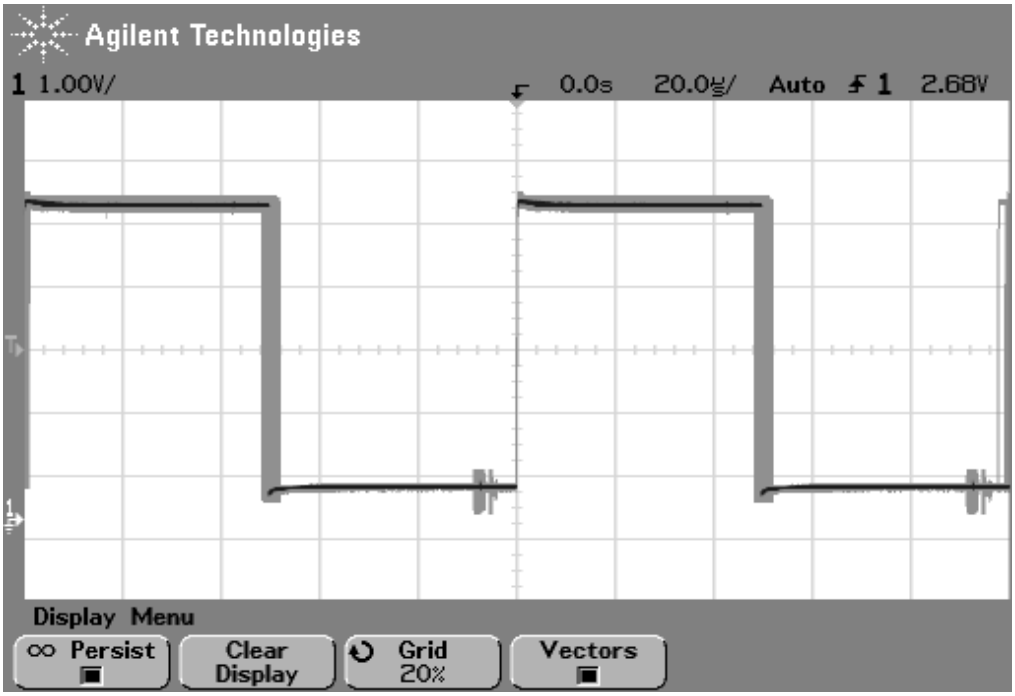
5.2.8.6 [EPL–CT 15] VBAT shift test – Dynamic – IUT as class A device

IUT as receiver



1kΩ/1nF

IUT as receiver



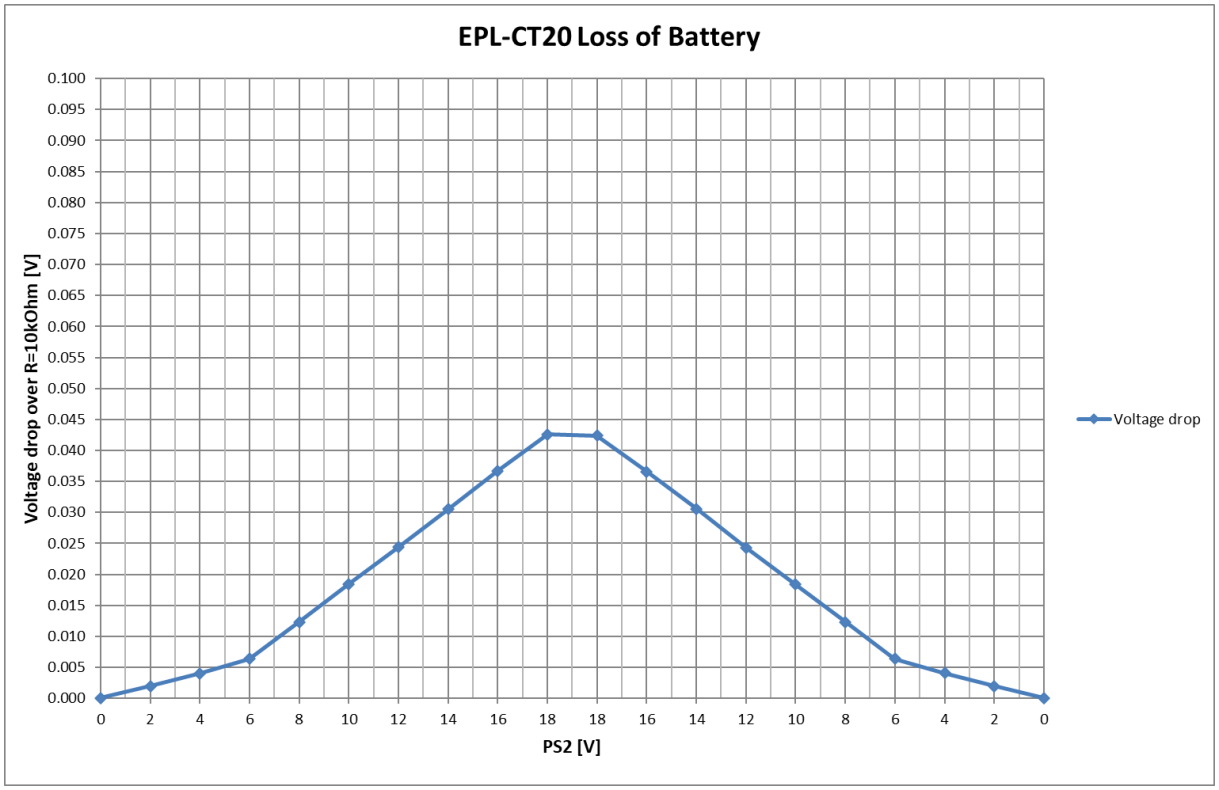
500Ω/10nF

Comment	Test Result
Observed Duty Cyle Range 1kΩ/1nF	50.5% – 51.5%
Observed Duty Cyle Range 500Ω/10nF	49.1% – 50.8%
The duty cycle measured at RXD2 shall be in the range of 0.376 to 0.601 (D1 – 2 µs to D2 + 2 µs).	Pass

5.2.9 Failure

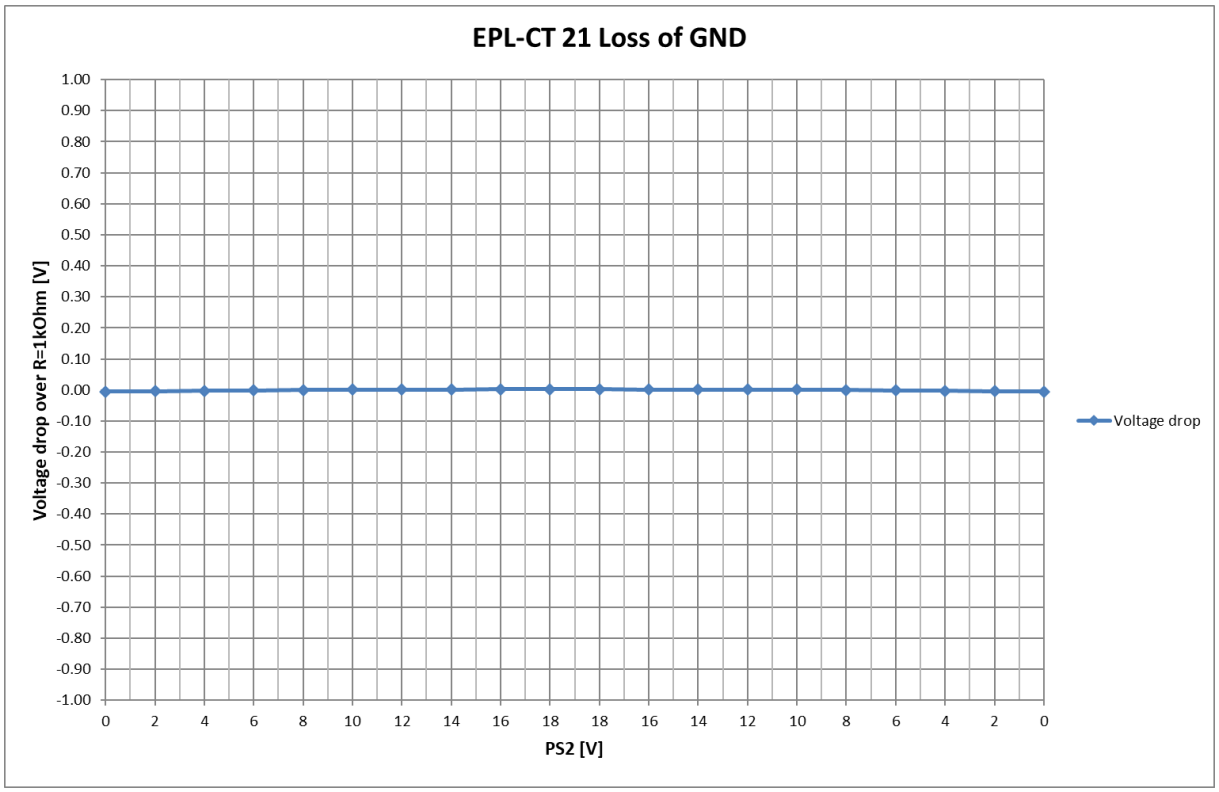
Purpose of this test is to check, whether some parasitic reverse currents are flowing into the IUT.

5.2.9.2 [EPL–CT 20] Loss of Battery



Comment	Test Result
During all test, no parasitic current paths shall be formed between the bus line and the IUT. I_{BUS} shall be less than 100 µA, means 1 V voltage drop over R=10 kΩ. After reconnecting battery line, the IUT shall restart after failure recovery.	Pass

5.2.9.3 [EPL–CT 21] Loss of GND

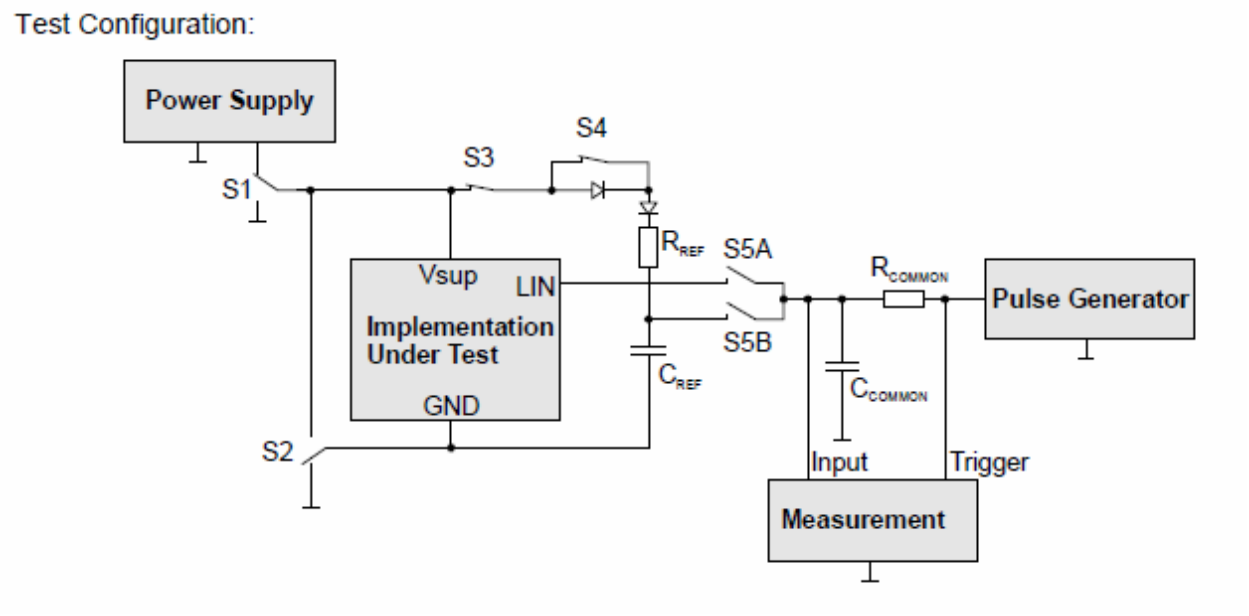


Comment	Test Result
During all test, no parasitic current paths shall be formed between the bus line and the IUT. I_{BUS} shall be included in ± 1 mA, means 1 V voltage drop over R=1 kΩ. After reconnecting ground line: The IUT shall restart after failure recovery.	Pass

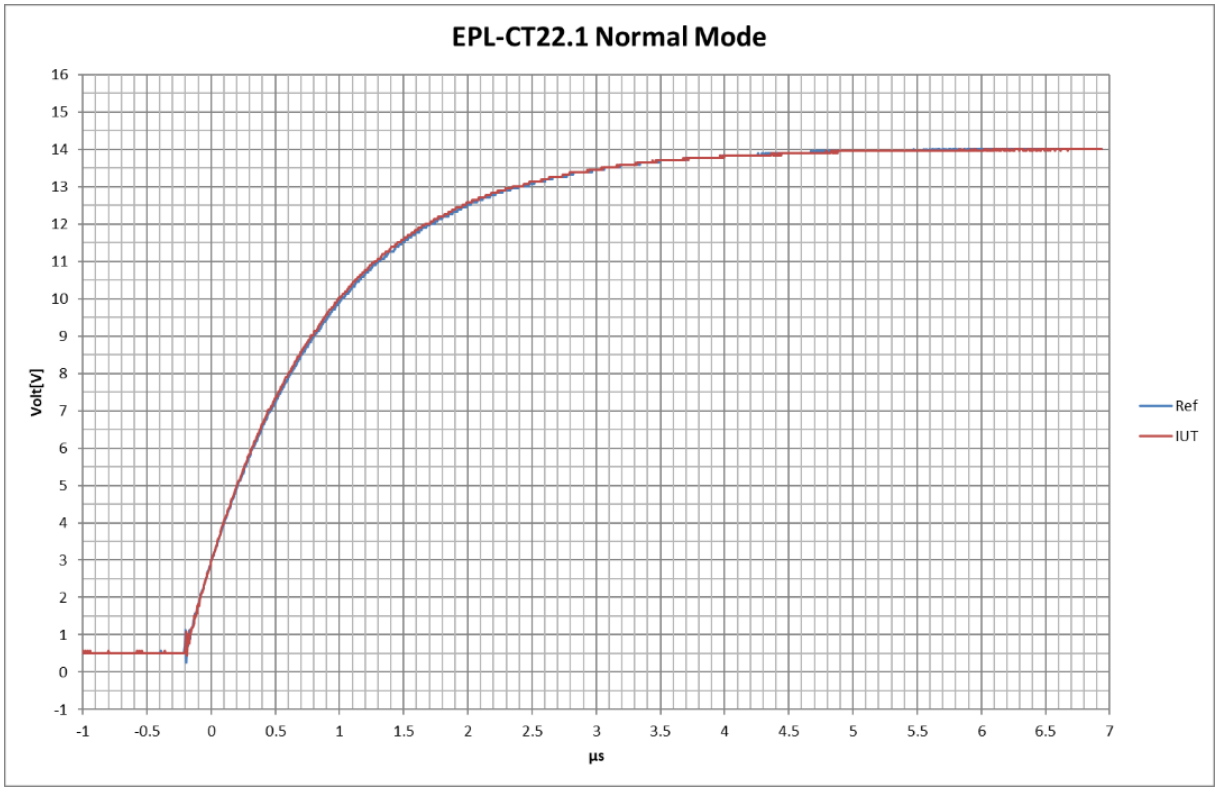
5.2.10 [EPL–CT 22] Verifying internal capacitance and dynamic interference – IUT as slave

Purpose of this test is checking the internal capacitance of the IUT under normal and fault conditions. The IUT shall not interfere dynamically with bus signals when it is in passive (non–transmitting) or unpowered state.

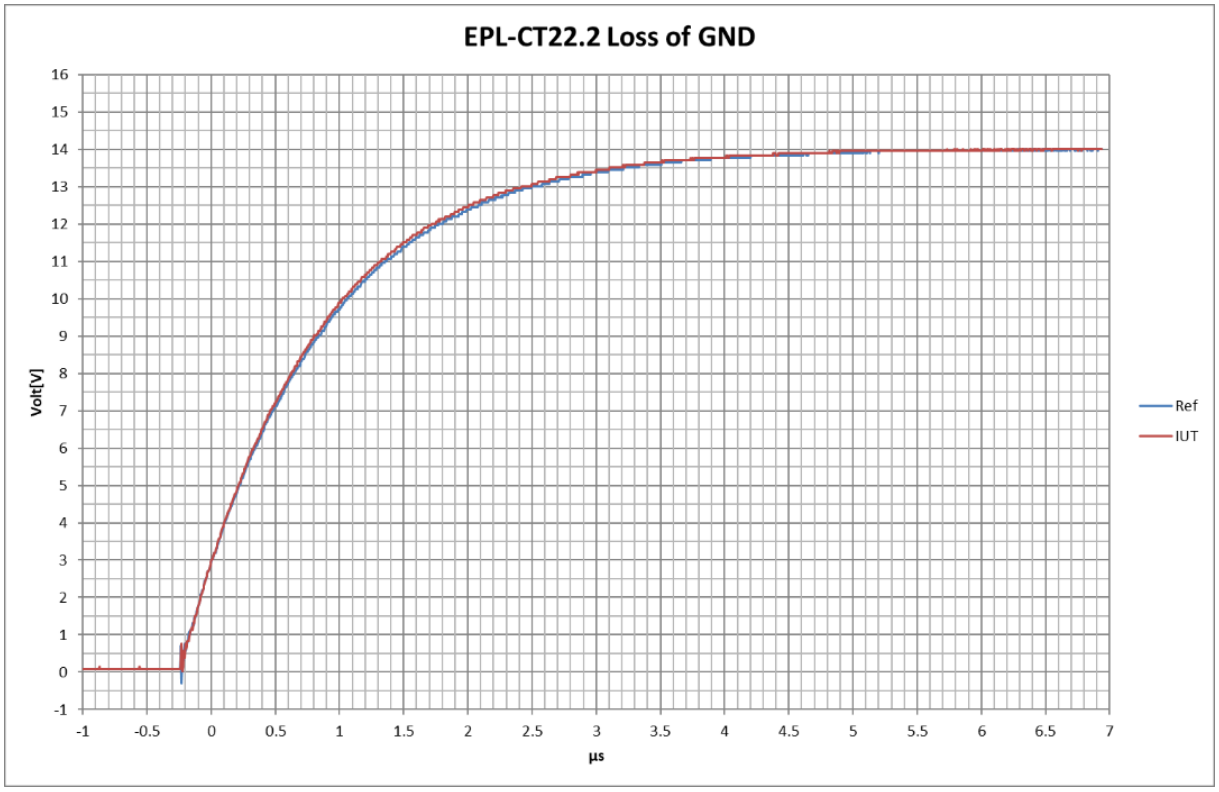
Test Configuration:



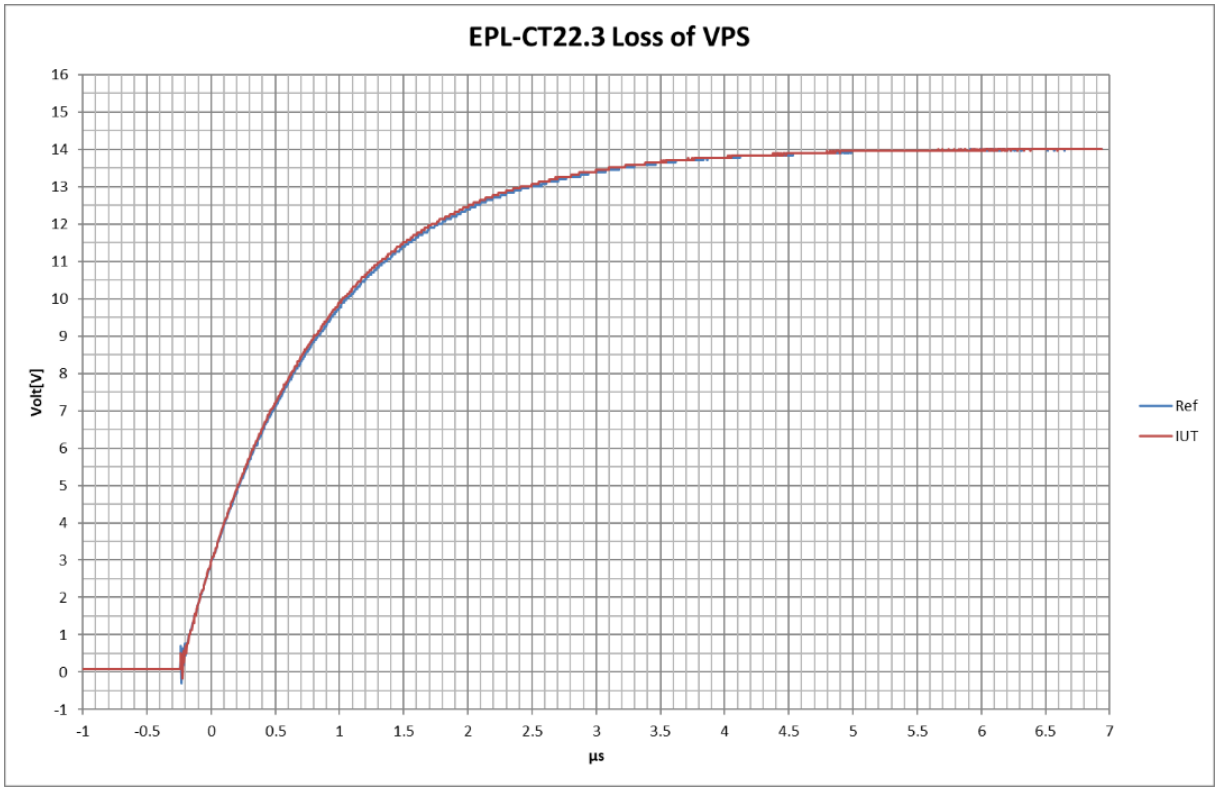
EPL–CT–TC	Condition	Result
[EPL–CT 22].1	Normal power supply IUT shall be in normal mode.	
	T_{INT}	0.985 µs
	T_{REF}	1.010 µs



EPL–CT–TC	Condition	Result
[EPL–CT 22].2	IUT loss of GND (IUT GND shorted to power supply).	
	T_{INT}	1.015 µs
	T_{REF}	1.045 µs



EPL–CT–TC	Condition	Result
[EPL–CT 22].3	IUT loss of V_{PS} (V_{IUT}: [V_{SUP} / V_{BAT}] shorted to GND).	
	T_{INT}	1.015 µs
	T_{REF}	1.045 µs



Comment	Test Result
C_{SLAVE} shall be less or equal than 250 pF: $T_{INT} \leq T_{REF}$. The IUT shall not interfere with the dynamic stimulus.	Pass

5.3 Operation Mode Termination

5.3.2 [EPL–CT 23] Measuring internal resistor – IUT as slave

Test parameter	
V_{IUT}: [V_{SUP}]	14V
R_{meas1}	10k (0.1%)
R_{meas2}	20k (0.1%)

	I_{meas}	V_{meas}	R_{meas}
10k	0.348 mA	3.486 V	10006 Ω
20k	0.276 mA	5.530 V	20007Ω
		R_{INT}	28372 Ω

Comment	Test Result
R_{INT} value shall be included in the range [20 kΩ; 60 kΩ]	Pass