CA-IS1300B25G-Q1 5-kV$_{RMS}$ Isolated Amplifier for Current Sensing

1 Key Features

- Differential Input Voltage Range: ±250 mV
- Fixed Initial Gain: 8.2
- Low Input Offset and Drift:
  - ±0.2 mV (max) at 25°C, ±3.5 µV/°C (max)
- Low Gain Error and Drift:
  - ±0.3% (max) at 25°C, ±50 ppm/°C (max)
- Low Nonlinearity and Drift:
  0.01% (typ) for Full Scale, ±1 ppm/°C (typ)
- 3.3-V or 5-V Operation for Both High- and Low-Side
- High CMTI: ±150 kV/µs (typ)
- Wide Operating Temperature Range: –40°C to 125°C
- Safety-Related Certifications:
  - 7070-V$_{PK}$ Isolation per DIN EN IEC 60747-17 (VDE 0884-17)
  - 5-kV$_{RMS}$ Isolation for 1 Minute per UL 1577
  - TUV Certification Approvals
- >40-year Life at Rated Working Voltage
- AEC-Q100 Qualified for Automotive Applications: Grade 1, –40°C to 125°C (T$_A$)

2 Applications

- Automotive Motor Controls and Drives
- Onboard Chargers
- Traction Inverters
- Charging Piles

3 Description

The CA-IS1300B25G-Q1 devices are high-precision isolated amplifiers and optimized for shunt-resistor-based current sensing. Low offset and gain error and drift guarantee that measuring accuracy is maintained over the entire operating temperature range.

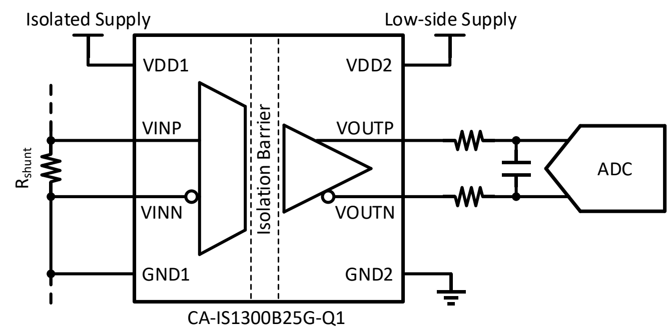
The CA-IS1300B25G-Q1 devices utilize silicon oxide (SiO_2) isolation barriers and support up to 5-kV$_{RMS}$ galvanic isolation per UL 1577. This technology separates high- and low-voltage domain to protect lower-voltage parts from damage and provides low emissions as well as strong anti-interference capability from magnetic changes. The high common-mode transient immunity (CMTI) means that the CA-IS1300B25G-Q1 devices transmit correct signals through isolation barriers and are suitable for automotive motor controls and drives which require high-voltage and high-power switching. The internal input common-mode overvoltage and missing high-side supply voltage detection functions contribute to fault diagnostics and system safety.

The CA-IS1300B25G-Q1 devices are packaged in wide body, 8-pin SOIC packages and specified over the automotive temperature range of –40°C to 125°C.

Device Information

PART NUMBER	PACKAGE	BODY SIZE (NOM)
CA-IS1300B25G-Q1	SOIC8-WB (G)	5.85 mm × 7.50 mm

Simplified Schematic



4 Ordering Guide

Table 4-1 Ordering Guide for Valid Ordering Part Number

Ordering Part Number	Specified Input Range	Gain	Gain Error	Input V_{OS}	Isolation Rating	Package
CA-IS1300B25G-Q1	±250 mV	8.2	±0.3%	±0.2 mV	5 kV_{RMS}	SOIC8-WB

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5 Revision History

Revision	Description	Page
Version 1.00	NA	NA
Version 1.01	Updated TUV certification information	6,7

6 Pin Descriptions and Functions

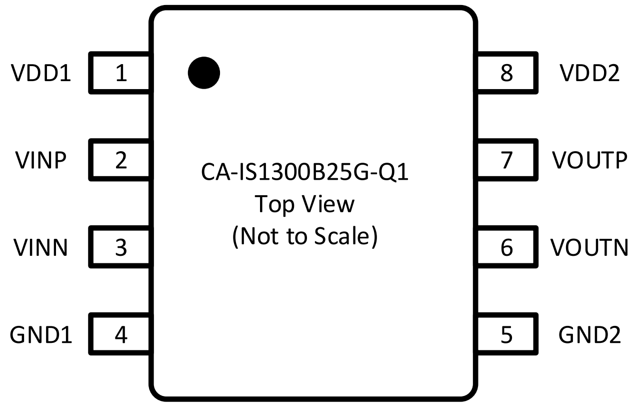


Figure 6-1 CA-IS1300B25G-Q1 Top View

Table 6-1 CA-IS1300B25G-Q1 Pin Description and Functions

NAME	PIN NUMBER	TYPE	DESCRIPTION
VDD1	1	Power	High-side power supply, 3 V to 5.5 V
VINP	2	Input	Noninverting analog input
VINN	3	Input	Inverting analog input
GND1	4	Ground	High-side ground
GND2	5	Ground	Low-side ground
VOUTN	6	Output	Inverting analog output
VOUTP	7	Output	Noninverting analog output
VDD2	8	Power	Low-side power supply, 3 V to 5.5 V

7 Specifications

7.1 Absolute Maximum Ratings[1]

PARAMETER		MIN	MAX	UNIT
VDD1, VDD2	Supply voltage[2]	–0.5	6.5	V
VINP, VINN	Analog input voltage	GND1 – 6	6.5	V
VOUTP, VOUTN	Analog output voltage	GND2 – 0.5	VDD2 + 0.5[3]	V
I_{IN}	Input current to any pin except supply pins	–10	10	mA
T_J	Junction Temperature		150	°C
T_{STG}	Storage Temperature	–65	150	°C

NOTE:

1. Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. All voltage values are with respect to the local ground terminal (GND1 or GND2) and are peak voltage values.
3. Maximum voltage must not exceed 6.5 V.

7.2 ESD Ratings

			VALUE	UNIT
V_{ESD}	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins	±4000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins	±2000	

7.3 Recommended Operating Conditions

PARAMETER		MIN	NOM	MAX	UNIT
VDD1	High-side supply voltage, with respect to GND1	3.0	5.0	5.5	V
VDD2	Low-side supply voltage, with respect to GND2	3.0	3.3	5.5	V
T_A	Ambient Temperature	–40		125	°C

7.4 Thermal Information

THERMAL METRIC		VALUE	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	110.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	51.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	66.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	16.0	°C/W
ψ_{JB}	Junction-to-board characterization parameter	64.5	°C/W
$R_{\theta JC(bottom)}$	Junction-to-case (bottom) thermal resistance	NA	°C/W

7.5 Power Ratings

PARAMETER		TEST CONDITIONS	VALUE	UNIT
P_D	Maximum power dissipation for both sides	VDD1 = VDD2 = 5.5 V	134.75	mW
P_{D1}	Maximum power dissipation for high-side	VDD1 = 5.5 V	90.75	mW
P_{D2}	Maximum power dissipation for low-side	VDD2 = 5.5 V	44.00	mW

7.6 Insulation Specifications

PARAMETR		TEST CONDITIONS	VALUE	UNIT
CLR	External clearance[1]	Shortest terminal-to-terminal distance through air	8	mm
CPG	External creepage[1]	Shortest terminal-to-terminal distance across the package surface	8	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	28	µm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	> 600	V
	Material group	According to IEC 60664-1	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 300 V_{RMS}	I-IV	
		Rated mains voltage ≤ 600 V_{RMS}	I-IV	
		Rated mains voltage ≤ 1000 V_{RMS}	I-III	
DIN EN IEC 60747-17 (VDE 0884-17)[2]				
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	1414	V_{PK}
V_{IOWM}	Maximum working isolation voltage	AC voltage; Time dependent dielectric breakdown (TDDB) Test	1000	V_{RMS}
		DC voltage	1414	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t = 60 s (qualification); $V_{TEST} = 1.2 \times V_{IOTM}$, t= 1 s (100% production)	7070	V_{PK}
V_{IOSM}	Maximum surge isolation voltage[3]	Test method per IEC 60065, 1.2/50 µs waveform, $V_{TEST} = 1.6 \times V_{IOSM}$ (qualification)	8000	V_{PK}
q_{pd}	Apparent charge[4]	Method a, After input/output safety test subgroup 2/3, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)} = 1.2 \times V_{IORM}$, t_m = 10 s	≤ 5	pC
		Method a, After environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)} = 1.6 \times V_{IORM}$, t_m = 10 s	≤ 5	
		Method b1, At routine test (100% production) and preconditioning (type test) $V_{ini} = 1.2 \times V_{IOTM}$, t_{ini} = 1 s; $V_{pd(m)} = 1.875 \times V_{IORM}$, t_m = 1 s	≤ 5	
C_{IO}	Barrier capacitance, input to output[5]	$V_{IO} = 0.4 \times \sin(2\pi ft)$, f = 1 MHz	~ 1	pF
R_{IO}	Isolation resistance[5]	V_{IO} = 500 V, T_A = 25°C	> 10^{12}	Ω
		V_{IO} = 500 V, 100°C ≤ T_A ≤ 125°C	> 10^{11}	
		V_{IO} = 500 V at T_S = 150°C	> 10^{9}	
	Pollution degree		2	
UL 1577				
V_{ISO}	Maximum withstanding isolation voltage	$V_{TEST} = V_{ISO}$, t = 60 s (qualification), $V_{TEST} = 1.2 \times V_{ISO}$, t = 1 s (100% production)	5000	V_{RMS}

NOTE:

1. Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications.
2. This coupler is suitable for safe electrical insulation only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
3. Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
4. Apparent charge is electrical discharge caused by a partial discharge (pd).
5. All pins on each side of the barrier tied together creating a two-terminal device.

7.7 Safety-Related Certifications

VDE (Pending)	UL	TUV
Certified according to DIN EN IEC 60747-17 (VDE 0884-17):2021-10	Recognized under UL 1577 Component Recognition Program and CSA Component Acceptance Service Notice No. 5A	Certified according to EN 61010-1: 2010+A1
Reinforced insulation Maximum repetitive peak isolation voltage: 1414 V_{PK} Maximum transient isolation voltage: 7070 V_{PK} Maximum surge isolation voltage: 8000 V_{PK}	Single protection 5000 V_{RMS}	5000 V_{RMS}
Certification Number:	Certification Number: E511334-20200520	Certification Number: CN23RC4J 001

7.8 Electrical Characteristics

All minimum and maximum specifications apply from T_A = –40°C to 125°C, VDD1 = VDD2 = 3 V to 5.5 V, VINP = –250 mV to 250 mV, and VINN = GND1 = 0 V (unless otherwise noted). All typical specifications are at T_A = 25°C, VDD1 = 5 V, and VDD2 = 3.3 V (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUT						
$V_{Clipping}$	Maximum input voltage before clipping output	VINP – VINN		±320		mV
V_{FSR}	Specified linear full-scale input range	VINP – VINN	–250		250	mV
V_{CM}	Operating common-mode input voltage	(VINP + VINN) / 2 to GND1	–0.16		VDD1 – 2.1	V
V_{CMOV}	Common-mode overvoltage threshold	(VINP + VINN) / 2 to GND1	VDD1 – 2			V
V_{CMOV_HYS}	Hysteresis of common-mode over-voltage threshold			100		mV
V_{OS}	Input offset voltage	Initial, at T_A = 25°C, VINP = VINN = GND1	–0.2	±0.05	0.2	mV
TCV_{OS}	Input offset voltage drift		–3.5	±1	3.5	µV/°C
$CMRR_{IN}$	Input common-mode rejection ratio	DC, VINP = VINN		–98		dB
		f_{IN} = 10 kHz, VINP = VINN		–98		
C_{IN}	Single-ended input capacitance	f_{IN} = 275 kHz, VINN = GND1		2		pF
C_{IND}	Differential input capacitance	f_{IN} = 275 kHz		1		pF
R_{IN}	Single-ended input resistance	VINN = GND1		19		kΩ
R_{IND}	Differential input resistance			22		kΩ
I_{IN}	Input current	VINP = VINN = GND1, $I_{IN} = (I_{INP} + I_{INN}) / 2$	–41	–30	–24	µA
TCI_{IN}	Input current drift			±1		nA/°C
I_{INOS}	Input offset current			±5		nA
BW_{IN}	Input bandwidth			1000		kHz
ANALOG OUTPUT						
	Gain[1]	Initial, at T_A = 25°C		8.2		V/V
E_G	Gain error	Initial, at T_A = 25°C	–0.3%	±0.05%	0.3%	
TCE_G	Gain error drift		–50	±15	50	ppm/°C
NL	Nonlinearity[2]		–0.03%	±0.01%	0.03%	
TCNL	Nonlinearity drift			±1		ppm/°C
	Output noise	VINP = VINN = GND1, BW = 100 kHz		330		$µV_{RMS}$
THD	Total harmonic distortion	V_{IN} = 500 mV_{pp}, f_{IN} = 10 kHz, BW = 100 kHz		–85		dB
SNR	Signal-to-noise ratio	V_{IN} = 500 mV_{pp}, f_{IN} = 1 kHz, BW = 10 kHz		83		dB
		V_{IN} = 500 mV_{pp}, f_{IN} = 10 kHz, BW = 100 kHz		68		
PSRR	Power supply rejection ratio[3]	At VDD1, DC		–100		dB
		At VDD1, 100-mV and 10-kHz ripple		–96		
		At VDD2, DC		–100		
		At VDD2, 100-mV and 10-kHz ripple		–98		
V_{CMOUT}	Common-mode output voltage		1.39	1.44	1.49	V
$V_{FAILSAFE}$	Fail-safe differential output voltage	$V_{CMOV} \le V_{CM}$ or VDD1 missing		–2.6	–2.5	V
I_{OSC}	Output short-circuit current	VOUTP or VOUTN shorts to VDD2 or GND2		±13		mA
R_{OUT}	Output resistance	On VOUTP or VOUTN		< 0.2		Ω
BW_{OUT}	Output bandwidth (–3 dB)		250	310		kHz
CMTI	Common-mode transient immunity	|GND1 – GND2| = 1.5 kV; *See Figure 8-1*	100	150		kV/µs

POWER SUPPLY						
VDD_{UV}	VDD undervoltage threshold	VDD1 or VDD2 rising		2.5	2.7	V
IDD1	High-side supply current	3.0 V ≤ VDD1 ≤ 3.6 V		10.5	15.0	mA
		4.5 V ≤ VDD1 ≤ 5.5 V		11.5	16.5	
IDD2	Low-side supply current	3.0 V ≤ VDD2 ≤ 3.6 V		5.2	7.2	mA
		4.5 V ≤ VDD2 ≤ 5.5 V		5.7	8.0	
t_r	Rise time of VOUT (10% – 90%)	VINP = 0 to 0.5 V step; *See Figure 8-2*		1.2		µs
t_f	Fall time of VOUT (90% – 10%)	VINP = 0.5 V to 0 step; *See Figure 8-2*		1.2		µs
t_{PD}	VIN to VOUT signal delay (50% – 50%)	Output unfiltered; *See Figure 8-3*		1.5	2.1	µs
t_{AS}	Analog settling time	VDD1 = 0 to 3 V step and 3.0 V ≤ VDD2, to VOUT valid (0.1% settling)		500		µs

NOTE:

1. The gain is defined as the slope of the optimum line derived by the method of least squares between differential input voltage (VINP – VINN) and differential output voltage (VOUTP – VOUTN) over the specified input range.
2. Nonlinearity is defined as a fraction of the half of the peak-to-peak value of differential output voltage deviation divided by the full-scale differential output voltage.
3. This parameter is input referred.

7.9 Typical Characteristics

All typical specifications are at VINP = –250 mV to 250 mV, and VINN = GND1 = 0 V, VDD1 = 5 V, and VDD2 = 3.3 V (unless otherwise noted).

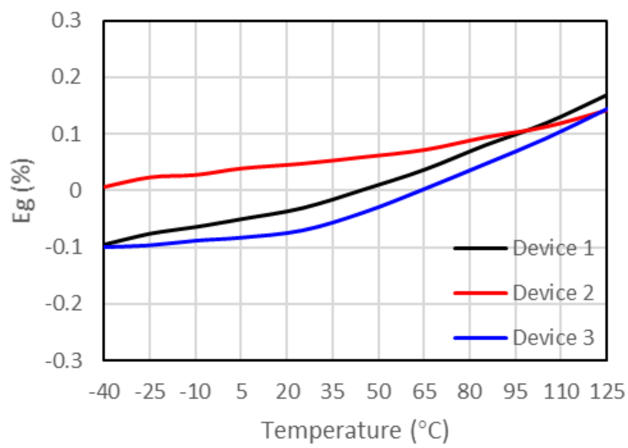


Figure 7-1 Gain Error vs Temperature

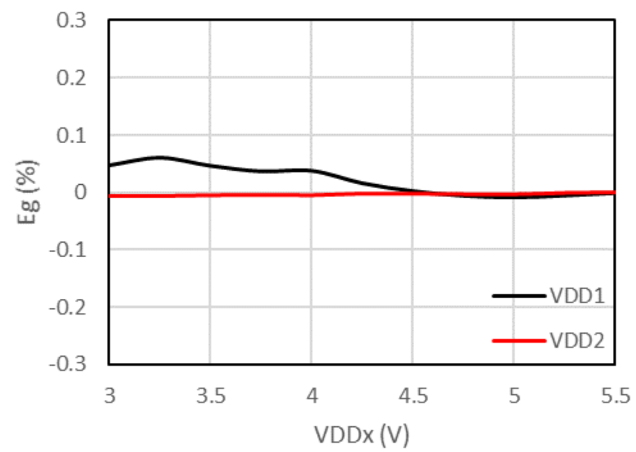


Figure 7-2 Gain Error vs Supply Voltage

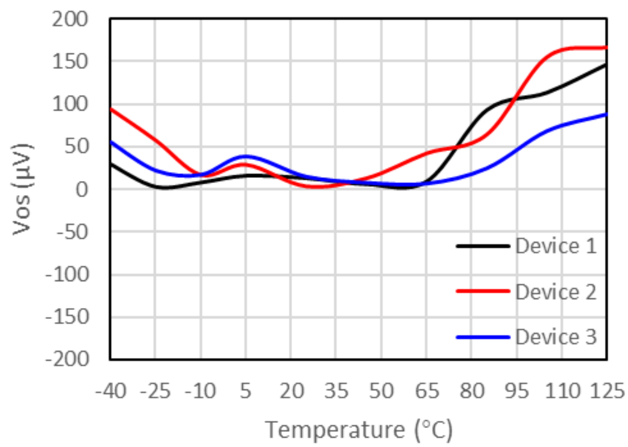


Figure 7-3 Input Offset vs Temperature

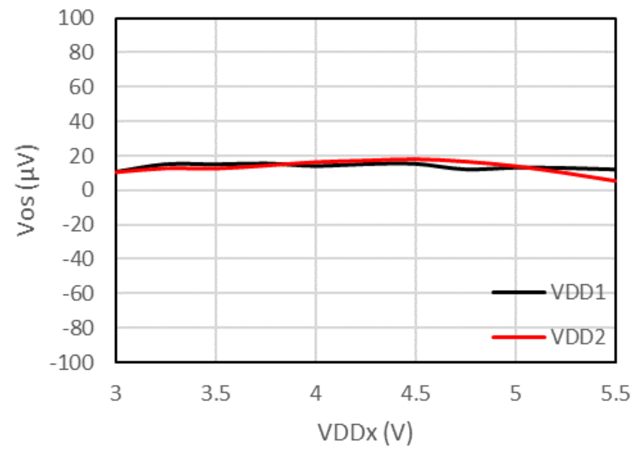


Figure 7-4 Input Offset vs Supply Voltage

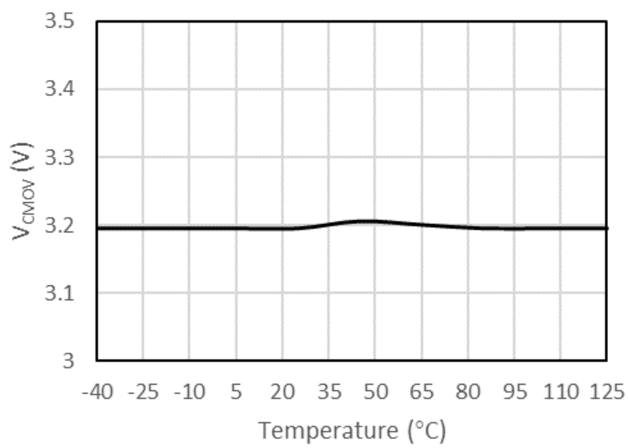


Figure 7-5 High-Side V_{CMOV} vs Temperature

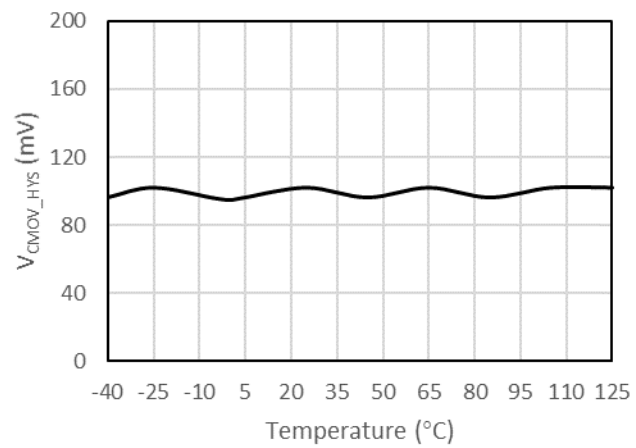


Figure 7-6 High-Side V_{CMOV_HYS} vs Temperature

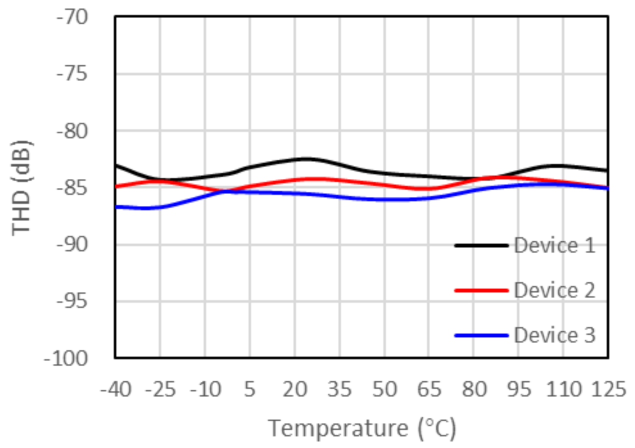


Figure 7-7 Total Harmonic Distortion vs Temperature @ f_{IN} = 10 kHz

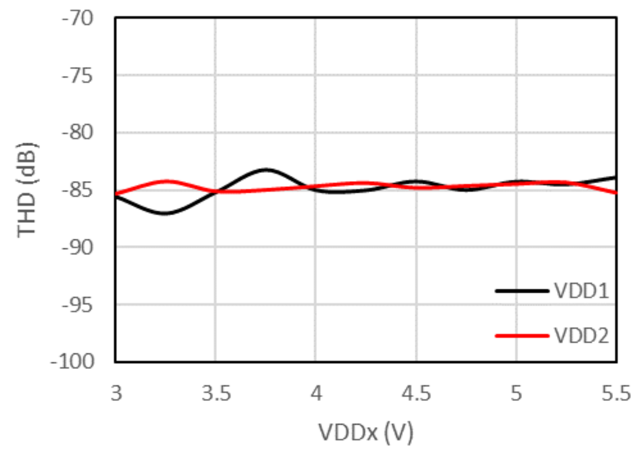


Figure 7-8 Total Harmonic Distortion vs Supply Voltage @ f_{IN} = 10 kHz

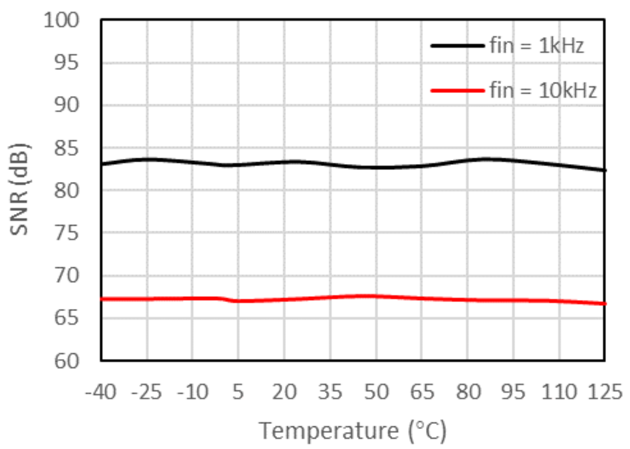


Figure 7-9 SNR vs Temperature

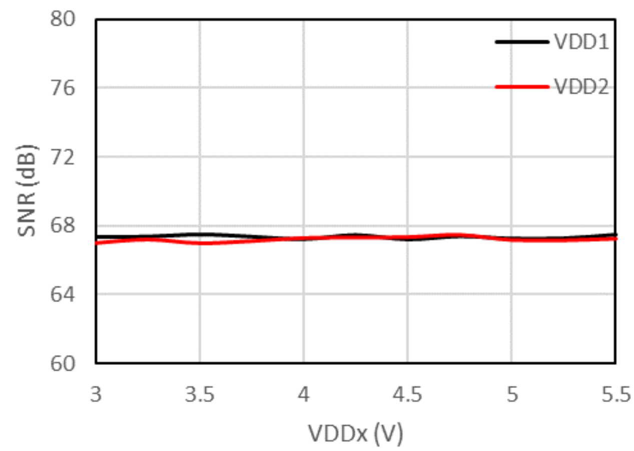


Figure 7-10 SNR vs Supply Voltage @ f_{IN} = 10 kHz

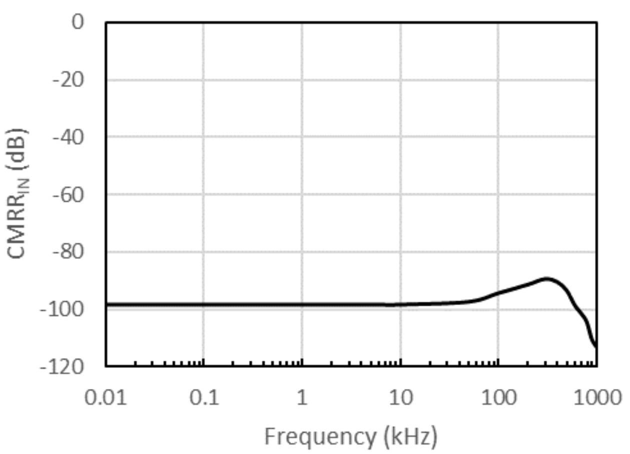


Figure 7-11 Input CMRR vs Frequency

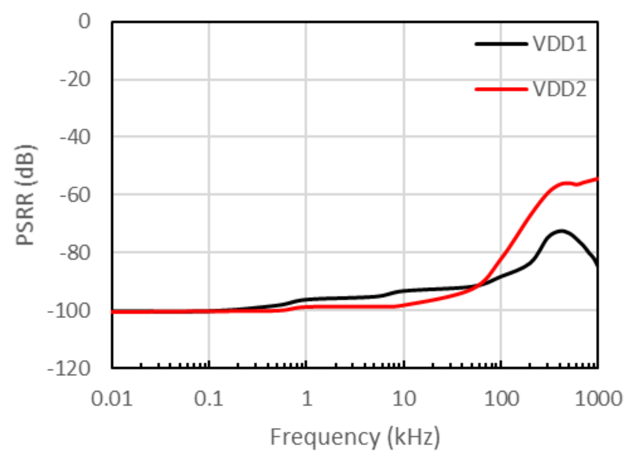


Figure 7-12 PSRR vs Frequency

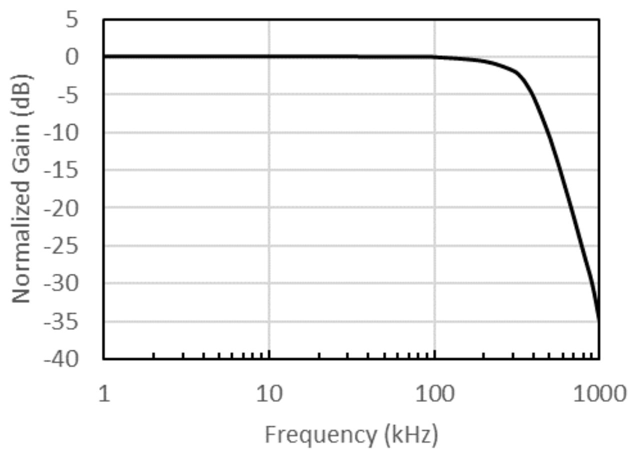


Figure 7-13 Normalized Gain vs Frequency

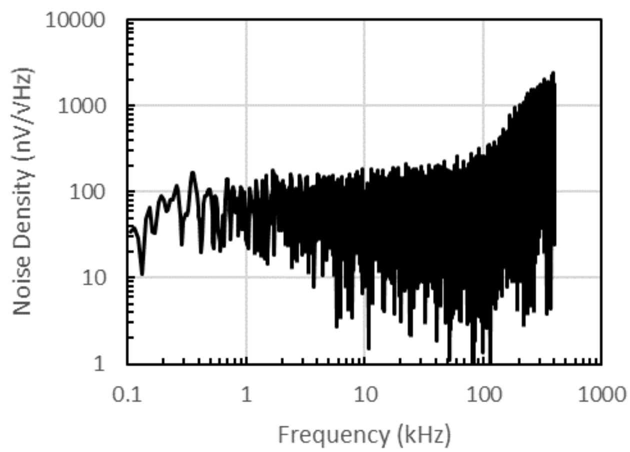


Figure 7-14 Input-Referred Noise Density vs Frequency

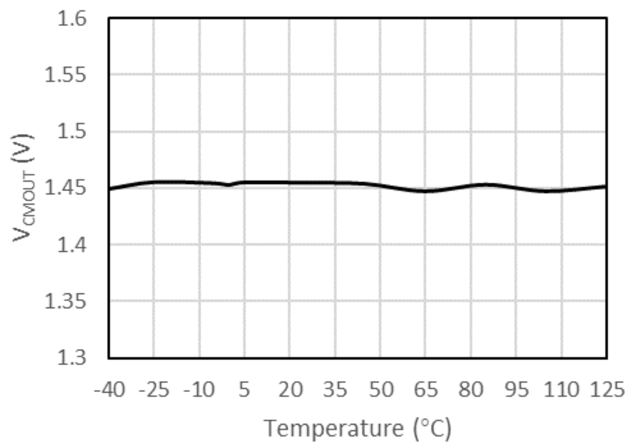


Figure 7-15 Low-Side V_{CMOUT} vs Temperature

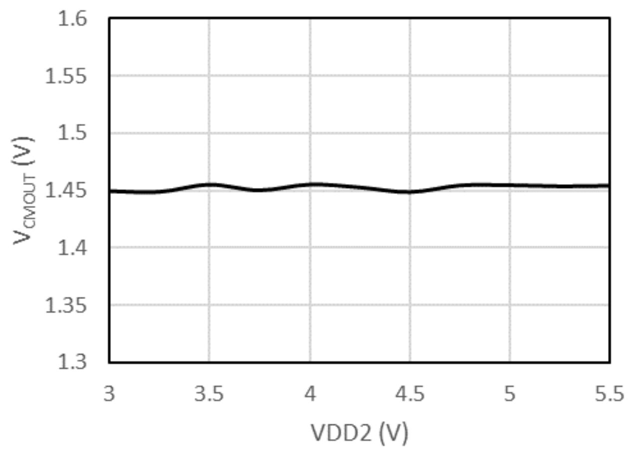


Figure 7-16 Low-Side VCMOUT vs VDD2

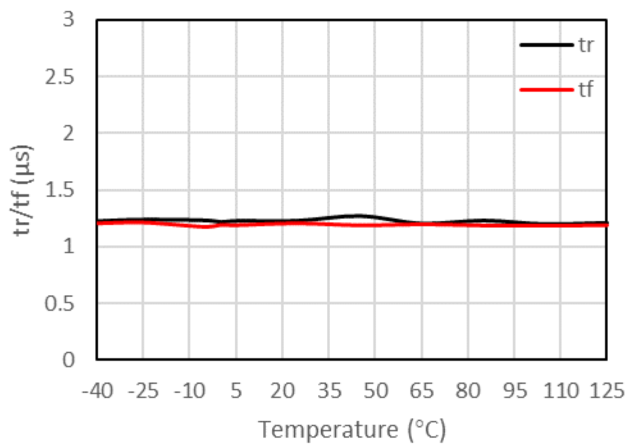


Figure 7-17 Output Rise and Fall Time vs Temperature

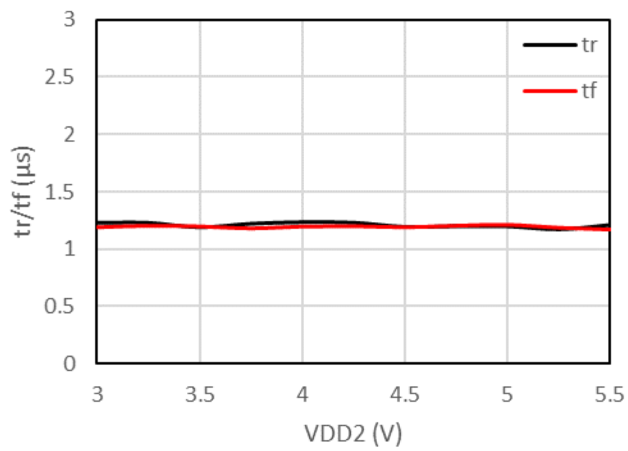


Figure 7-18 Output Rise and Fall Time vs VDD2

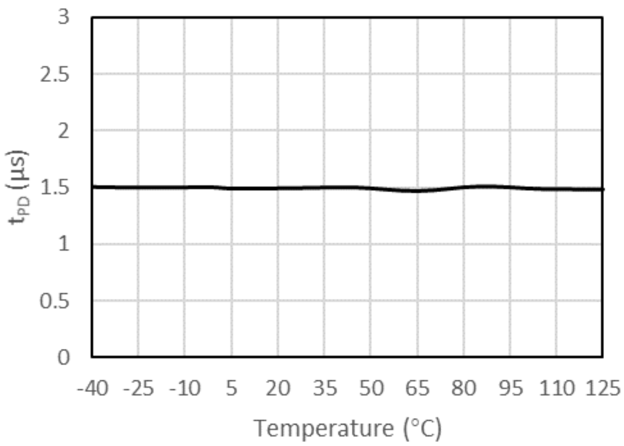


Figure 7-19 VIN to VOUT Signal Delay vs Temperature

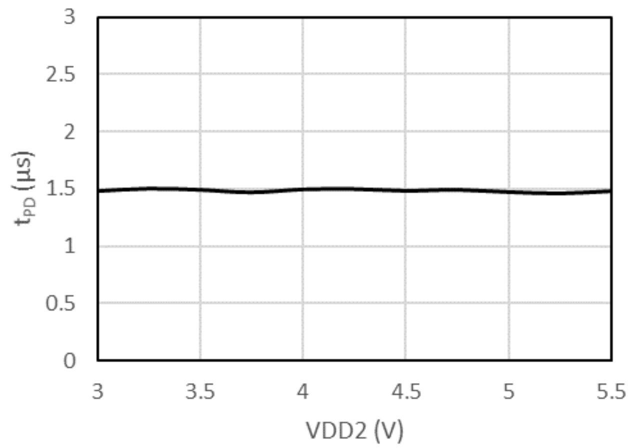


Figure 7-20 VIN to VOUT Signal Delay vs VDD2

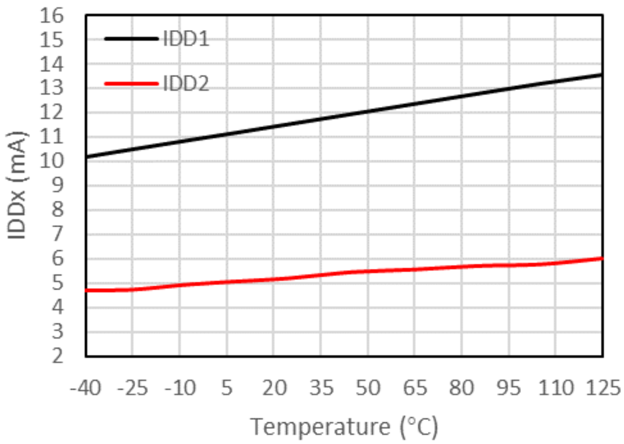


Figure 7-21 Supply Current vs Temperature

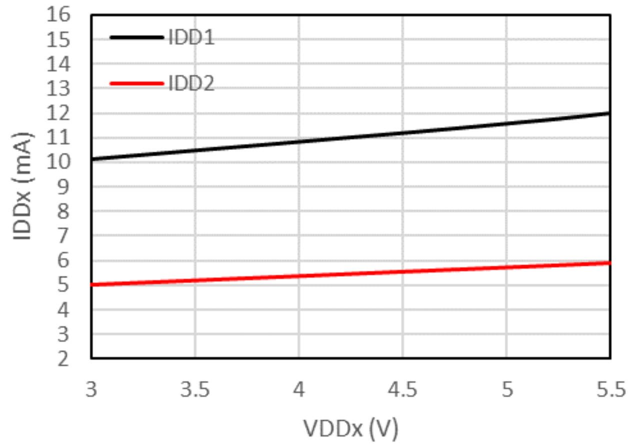


Figure 7-22 Supply Current vs Supply Voltage

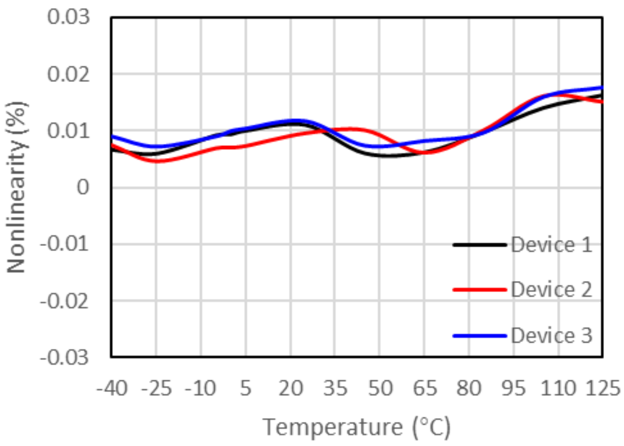


Figure 7-23 Nonlinearity vs Temperature

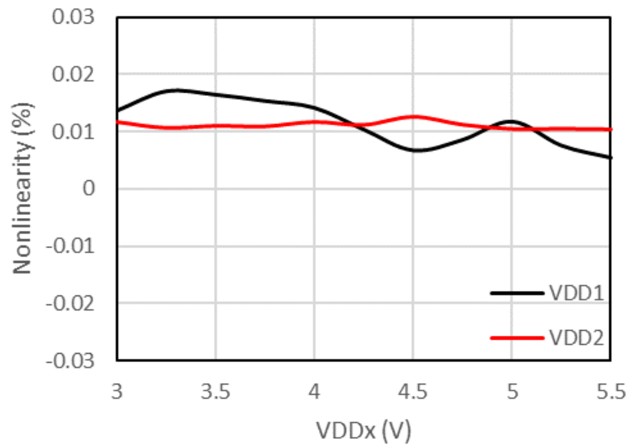
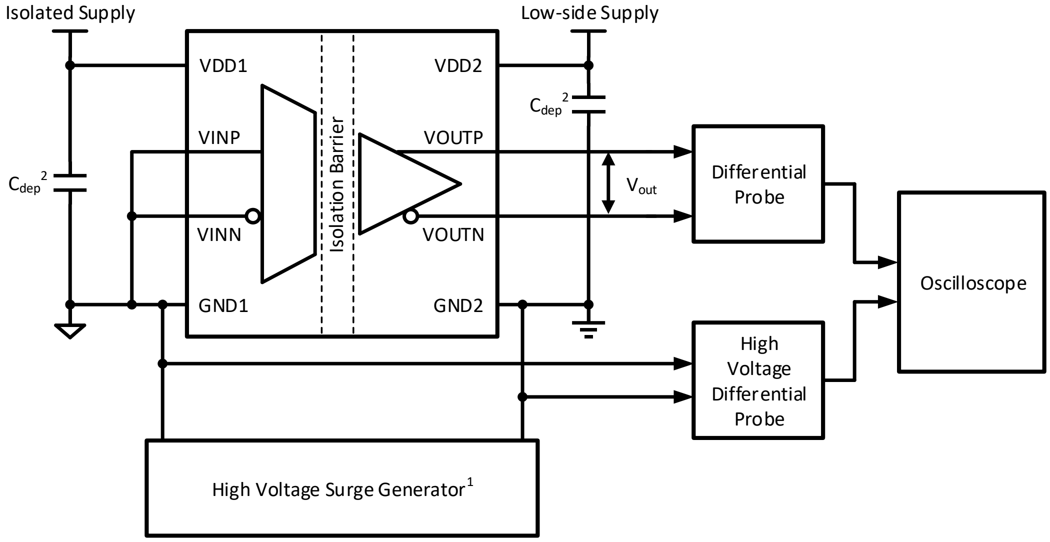


Figure 7-24 Nonlinearity vs Supply Voltage

8 Parameter Measurement Information



Note:

1. The High Voltage Surge Generator generates repetitive high voltage surges with > 1 kV amplitude and < 10 ns rise time or fall time to generate common-mode transient noise with > 150 kV/µs slew rate.
2. C_{dep} is the 0.1~1 µF decoupling capacitor.

Figure 8-1 Common-Mode Transient Immunity Test Circuit

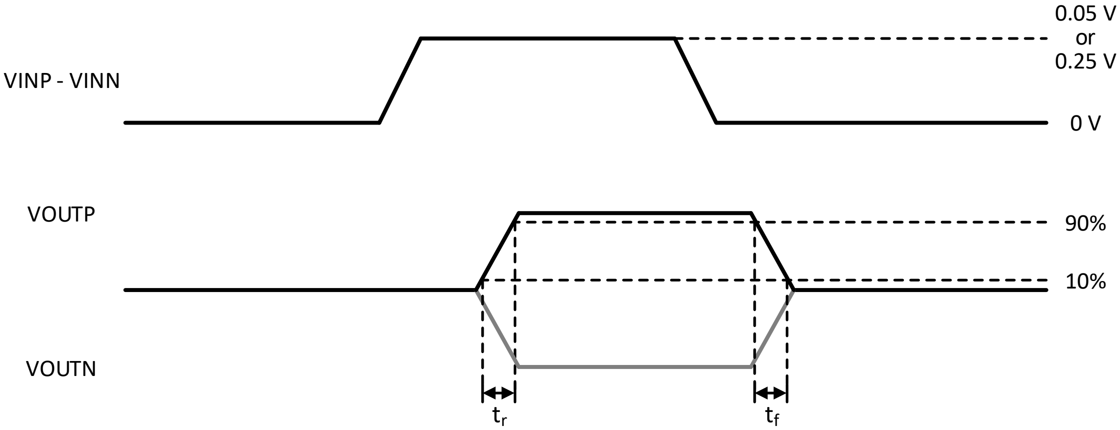


Figure 8-2 Rise and Fall Time Test Waveforms

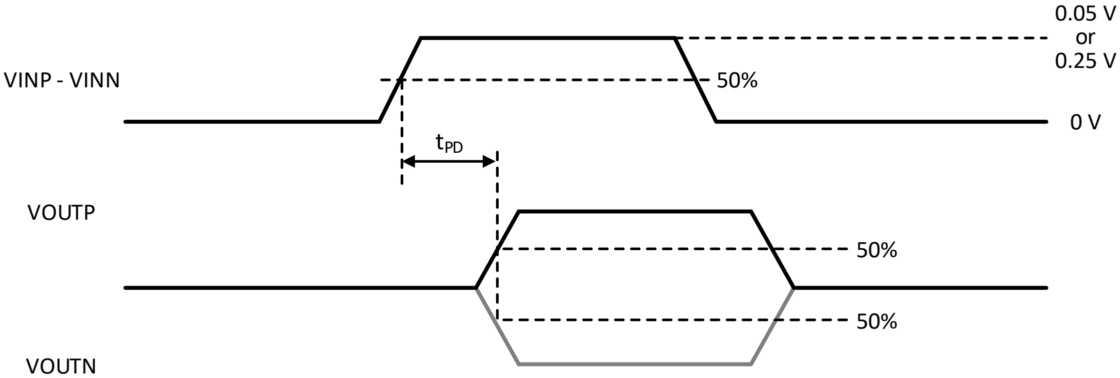


Figure 8-3 Delay Time Test Waveforms

9 Detailed Description

9.1 System Overview

The CA-IS1300B25G-Q1 devices are high-precision isolated amplifiers designed for shunt-resistor-based current sensing. The functional block diagram of this device is shown in Figure 9-1. At high side, the fully differential amplifier pre-amplifies the measuring voltage across a shunt resistor and then drives a 2nd-order Sigma-Delta (ΣΔ) modulator. This modulator converts the analog signal to a digital bitstream. For transmission across the SiO_2-based isolation barrier, the digital stream is further modulated with a high-frequency carrier using a simple on-off keying (OOK) modulation scheme. The receiver (RX) recoveries the modulated signal to the original digital bitstream at low side. After processed by a 1-bit digital-to-analog converter (DAC), the digital bitstream is sent to an active low-pass filter to produce the analog output. For synchronization of the whole chip, the clock is generated at low side and sent back to high side ensuring that all clocks come from one source.

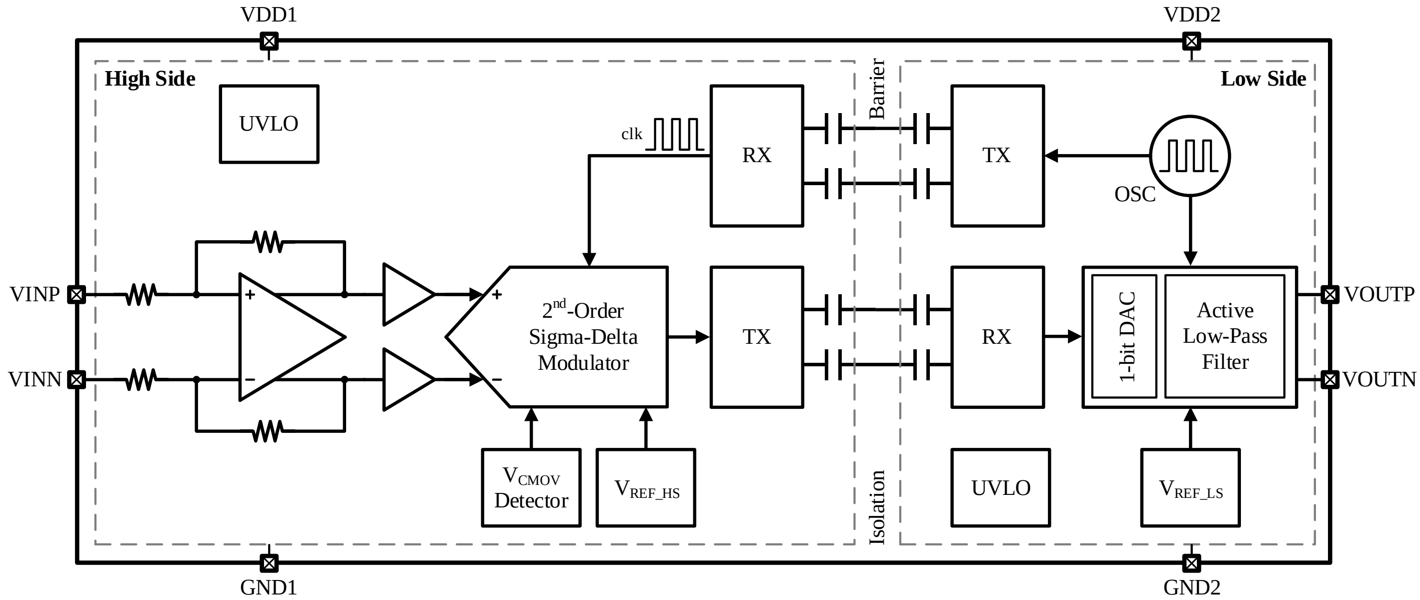


Figure 9-1 Functional Block Diagram of CA-IS1300B25G-Q1

9.2 Feature Description

9.2.1 Analog Input

The CA-IS1300B25G-Q1 device utilizes a fully differential amplifier stage to pre-amplify the measuring voltage across the shunt resistor. CA-IS1300B25G-Q1 (±250 mV input voltage range) is 8.2. The above gain contributing part of the total gain and ensuring that the 2nd-order Sigma-Delta modulator is not saturated when the analog input is within the specific input voltage range. This gain is set by the internal high-precision resistor network. The several- or tens-of-several-kΩ input resistance means it can bring in more gain error and offset if CA-IS1300B25G-Q1 devices are applied in measurement where the input signal sources are high-impedance (refer to Error Analysis in Voltage Sensing for detailed information).

The ESD structure of CA-IS1300B25G-Q1 supports the absolute maximum analog input voltage (with respect to GND1) to range from GND1 – 6 V to VDD1 + 0.5 V. To guarantee the long-term reliability and device performance, the differential analog input voltage and the input common-mode voltage of CA-IS1300B25G-Q1 must be kept within the specific range.

9.2.2 Signal Transmission Across Isolation Barrier

The CA-IS1300B25G-Q1 devices utilize a simple on-off keying (OOK) modulation scheme to transmit the digital bitstream across the SiO_2-based isolation barrier which supports up to 5-kV_{RMS} galvanic isolation between high- and low-voltage domain. The block diagram of an isolation channel is shown in Figure 9-2. As shown in Figure 9-3, the transmitter (TX) modulates the digital bitstream with a high-frequency carrier when the signal is HIGH while sends no signal when the signal is LOW. The receiver (RX) demodulates the signal across the isolation barrier and reproduces the digital bitstream faithfully. The isolation channel adopts fully differential capacitive-coupled structure which is insensitive to common-mode transient noises, thus the CMTI performance can be maximized. This structure and related circuitry also provide low emissions and strong anti-interference capability from magnetic changes.

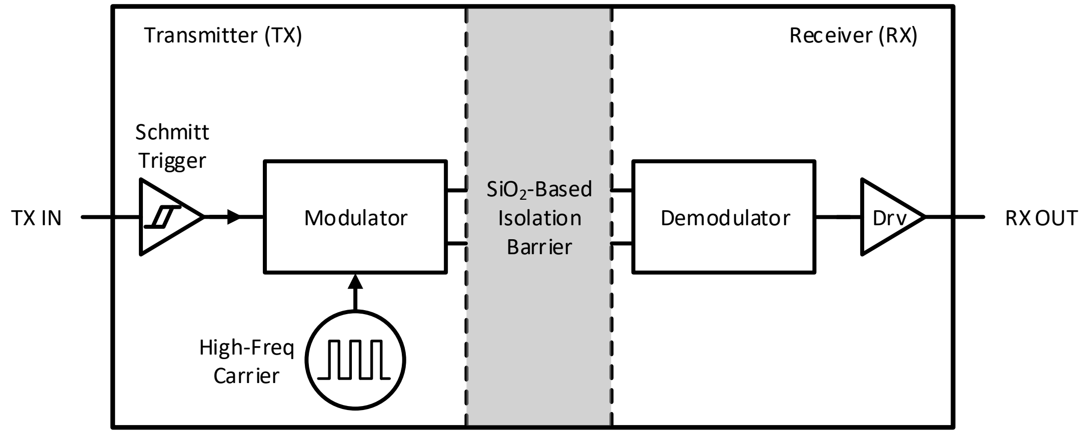


Figure 9-2 Block Diagram of an Isolation Channel

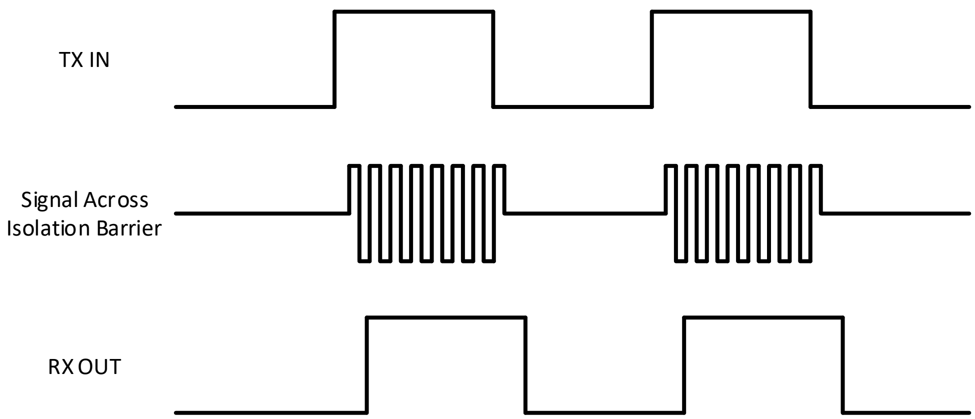


Figure 9-3 Conceptual Operation Waveforms of OOK Modulation Scheme

9.2.3 Fail-Safe Output

The CA-IS1300B25G-Q1 devices have fail-safe output function which is activated in two conditions:

- The high-side power supply is missing;
- The common-mode input voltage V_{CM} exceeds the common-mode overvoltage threshold V_{CMOV}.

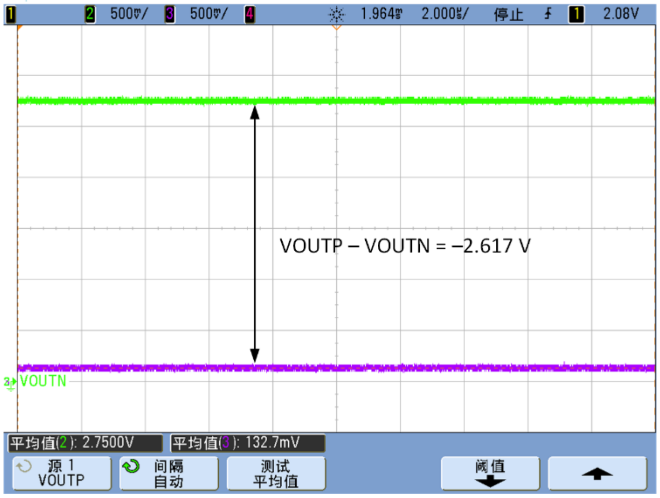


Figure 9-4 Typical Fail-safe Output Waveform

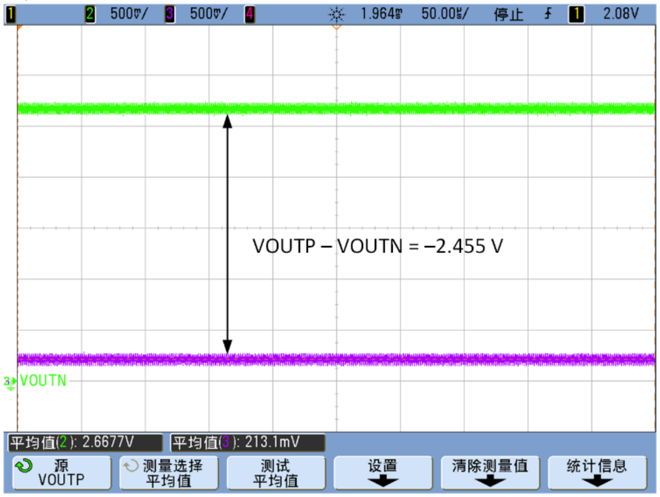


Figure 9-5 Typical Negative Clipping Output Waveform

As shown in Figure 9-4 and Figure 9-5, the fail-safe output is a more negative differential output voltage which can be distinguished from the negative clipping output voltage. This function contributes to fault diagnostics and system safety.

10 Application and Implementation

10.1.1 Typical Application for Current Sensing

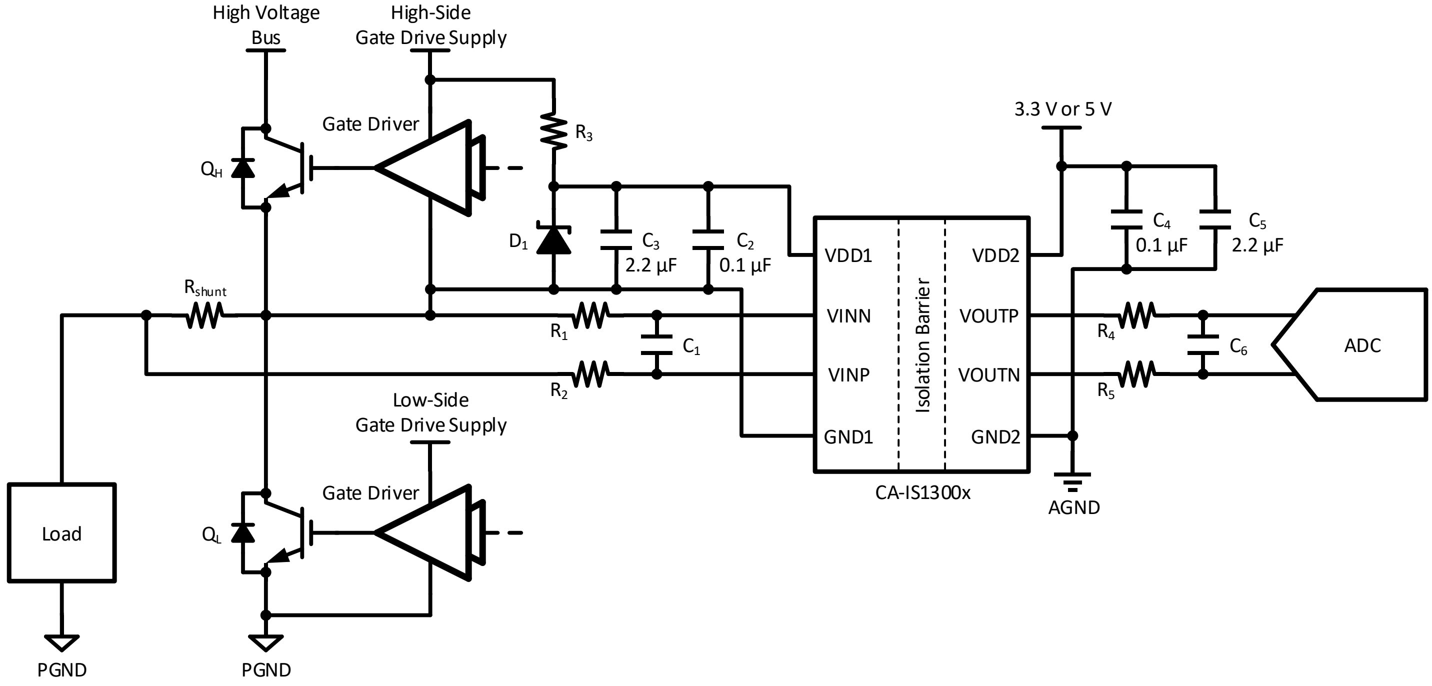


Figure 10-1 Typical Application for Current Sensing

The typical application for current sensing is shown in Figure 10-1. The CA-IS1300B25G-Q1 device is used to amplify the voltage across the shunt resistor (R_{shunt}) and transmit it to the low-voltage side for control circuit to process. The differential input and the high CMTI of CA-IS1300B25G-Q1 ensure the reliable and accurate measurement in the high-noise and high-power switching applications such as automotive motor drives. The voltage of R_{shunt} with respect to PGND varies from 0 V to the high voltage bus when switching, thus isolation is required. The CA-IS1300B25G-Q1 devices support up to 5-kV_{RMS} galvanic isolation, making them suitable for these high-voltage automotive applications.

In a three-phase motor drive application, this circuit could be repeated three times and one for each phase in order to measure each phase current.

10.1.2 Choose Proper R_{shunt}

The value chosen of shunt resistor is a trade off between power dissipation and measuring accuracy. Small value resistors minimize power dissipation, while large value resistors take advantage of the full performance input range of the Sigma-Delta modulator.

Consider the following restrictions to choose proper value of the shunt resistor R_{shunt}:

- The voltage drop across R_{shunt} caused by the nominal measured current is within the linear differential input voltage range V_{FSR};
- The voltage drop across R_{shunt} caused by the maximum allowed current must not exceed the maximum input voltage before clipping output $|V_{Clipping}|$.

For best performance, place the shunt resistor close to the inputs of CA-IS1300B25G-Q1 and keep the layout of both connections symmetrical. This ensures that any noises occurring at high side are coupled equally to the inputs and would be rejected as a common-mode signal. Kelvin connection is recommended between R_{shunt} and the inputs of CA-IS1300B25G-Q1 to remove the impact from any voltage drops across the trace and leads.

10.1.3 Input Filter

The typical input bandwidth of CA-IS1300B25G-Q1 is 1 MHz. A first-order passive RC low-pass filter could be placed between R_{shunt} and the inputs to narrow the input bandwidth. Choose $R_1 = R_2 = 10\ \Omega$ and $C_1 = 20$ nF could provide a cutoff frequency of approximately 400 kHz. R_1 and R_2 should be low-value enough compared to the input impedance of CA-IS1300B25G-Q1 to reduce gain error.

10.1.4 Power Supply Recommendations

The high-side power supply of CA-IS1300B25G-Q1 could be generated directly derived from the high-side gate drive power supply by utilizing a Zener diode (D_1) to produce a 3.3-V or 5-V (±10%) voltage. And a low-ESR decoupling capacitor of 0.1 µF (C_2) is recommended to place as close as possible to the VDD1 pin of CA-IS1300B25G-Q1. Additional 2.2-µF capacitor (C_3) is recommended for better filtering to the high-side power-supply path.

Similarly, a 0.1-µF decoupling capacitor (C_4) followed by an additional capacitor (C_5) from 2.2 µF to 10 µF should be placed as close as to the VDD2 pin of CA-IS1300B25G-Q1 to filter the low-side power supply path.

10.1.5 Output Filter

Another first-order passive RC low-pass filter could be placed between the outputs of CA-IS1300B25G-Q1 and the ADC to satisfy the potential requirement for anti-aliasing filtering. The characteristics of this filter depends on the structure and sampling frequency of the ADC. Choose $R_4 = R_5 = 4.7$ kΩ and $C_6 = 180$ pF could provide a cutoff frequency of approximately 94 kHz.

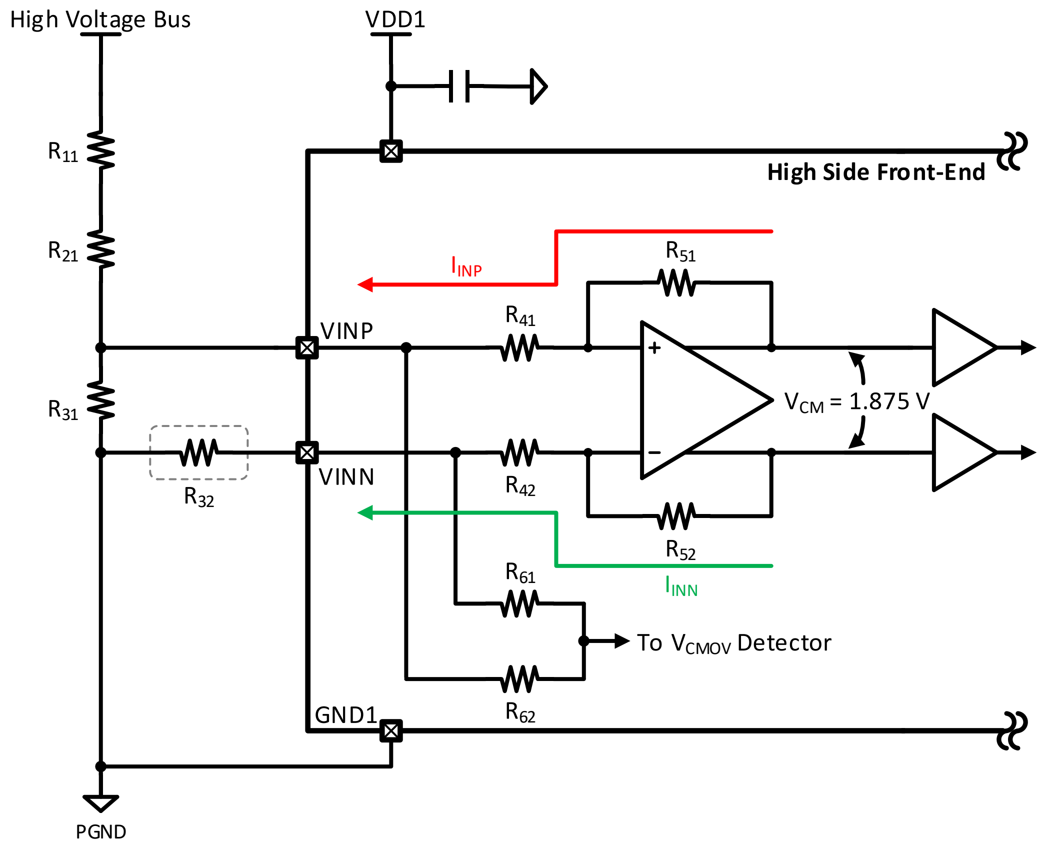


Figure 10-2 Typical Application for Voltage Sensing

10.1.6 Error Analysis in Voltage Sensing

The CA-IS1300B25G-Q1 devices may also be used in the applications of voltage sensing as shown in Figure 10-2. The resistors R_{11}, R_{21} and R_{31} make up the resistor divider to scale down the high voltage from bus. Typically, the value of R_{11} and R_{21} is much larger than R_{31} to keep the input voltage of CA-IS1300B25G-Q1 within the specific range.

In CA-IS1300B25G-Q1, resistors R_{41} and R_{51} (or R_{42} and R_{52}) are used to set the gain of front-end amplifier. The typical values are $R_{41} = R_{42} = 12.5$ kΩ, and $R_{51} = R_{52} = 50$ kΩ. Resistors R_{61} and R_{62} are used to sense the common-mode voltage of the input in CA-IS1300B25G-Q1. The typical values are $R_{61} = R_{62} = 100$ kΩ.

First, consider the situation in which R_{32} is not used. Additional gain error and offset would arise in these applications for CA-IS1300B25G-Q1. On the one hand, the limited input impedance of CA-IS1300B25G-Q1 is parallel with the external sensing resistor R_{31}, resulting in impedance change and thus additional gain error. On the other hand, the output common-mode voltage V_{CM} of the front-end differential amplifier in CA-IS1300B25G-Q1 is biased to 1.875 V, which would generate bias current I_{INP} and I_{INN} flowing through the front-end resistor network. The bias current I_{INP} also flows through R_{31} while I_{INN} flows directly to PGND in the case of omitting R_{32}, which results in unbalance and thus additional offset.

To eliminate the effect of the bias current, resistor R_{32} equal to sensing resistor R_{31} is recommended to be added between VINN and PGND. The resistor R_{31} would bring in additional gain error E_{GA} and could be calculated as Eq. 1 describes.

$$E_{GA} = R_{31} / (R_{31} + R_{41}) \quad \textbf{(Eq. 1)}$$

To reduce the effect of this gain error, the value of R_{31} should be chosen much smaller compared to R_{41}. And this gain error could also be minimized by the system-level gain calibration.

10.1.7 Caution

Do not leave the inputs of CA-IS1300B25G-Q1 floating. If the VINP and VINN are left floating, the input common-mode voltage would be pulled to a high level by internal bias, which could activate the fail-safe mode under certain power supply and may lead to system-level abnormal reaction (refer to Fail-Safe Output for detailed information).

11 Package Information

11.1 8-Pin Wide Body SOIC Package

The figure below illustrates the package details and the recommended land pattern details for the CA-IS1300B25G-Q1 isolated amplifier in an 8-pin wide-body SOIC package. The values for the dimensions are shown in millimeters.

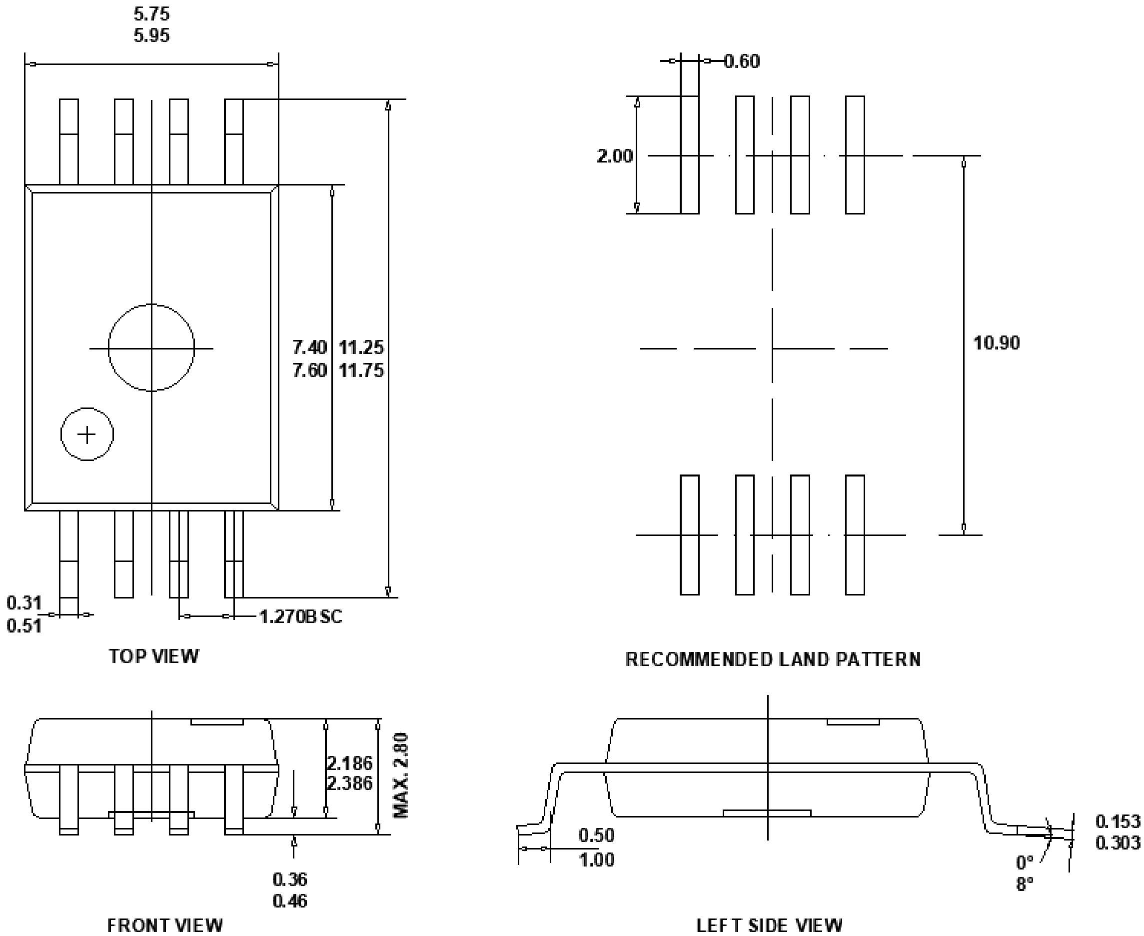


Figure 11-1 SOIC8 Wide-body Package

12 Soldering Information

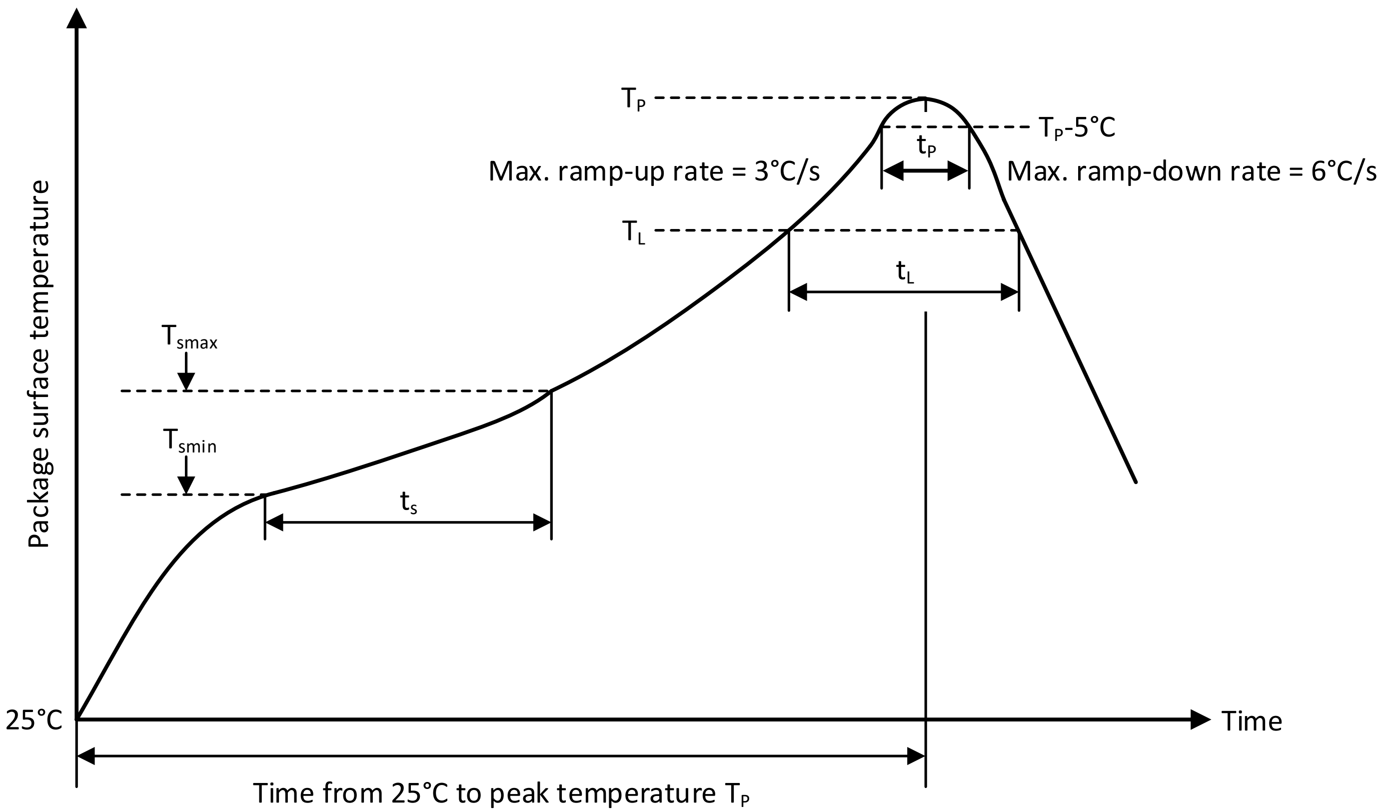


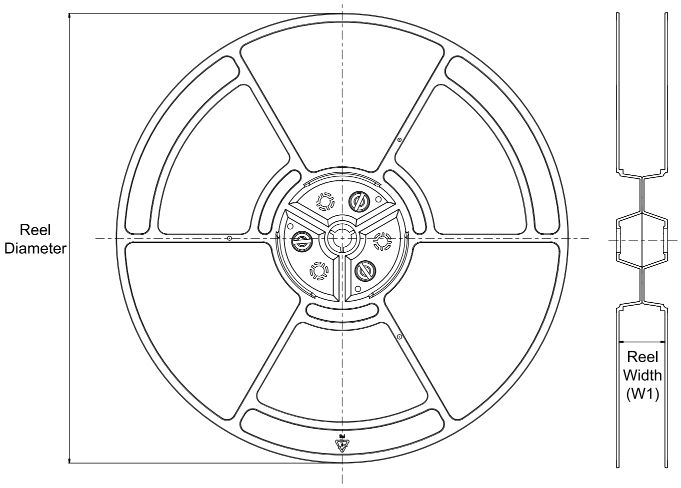
Figure 12-1 Soldering Temperature Curve

Table 12-1 Soldering Temperature Parameters

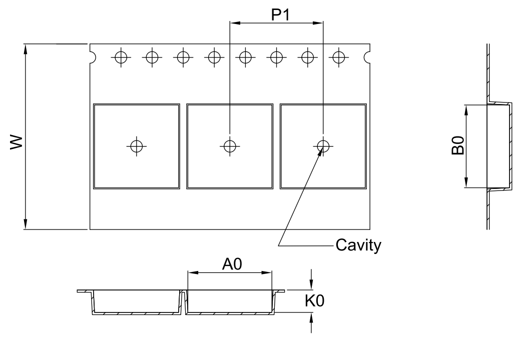
Profile Feature	Pb-Free Soldering
Ramp-up rate (T_L = 217°C to peak T_P)	3°C/s max
Time t_s of preheat temp (T_{smin} = 150°C to T_{smax} = 200°C)	60~120 seconds
Time t_L to be maintained above 217°C	60~150 seconds
Peak temperature T_P	260°C
Time t_P within 5°C of actual peak temp	30 seconds max
Ramp-down rate (peak T_P to T_L = 217°C)	6°C/s max
Time from 25°C to peak temperature T_P	8 minutes max

13 Tape and Reel Information

REEL DIMENSIONS

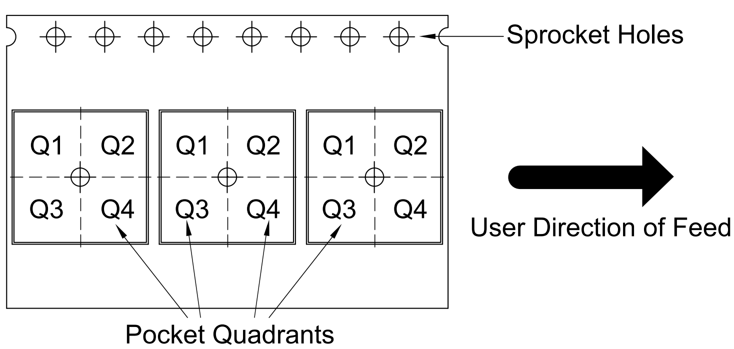


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CA-IS1300B25G-Q1	SOIC	G	8	1000	330	16.4	11.95	6.15	3.20	16.0	16.0	Q1

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