

CA-IS1305 5kV_{RMS} Isolated Sigma-Delta Modulator

1 Key Features

- Differential Input Voltage Range: ± 250 mV
- Ultra-Low Input Offset Voltage and Drift
 - $\pm 150\mu\text{V}(\text{max})$ @ 25°C input offset voltage
- Low Gain Error and Drift
 - $\pm 0.3\%(\text{max})$ @ 25°C gain error
 - $\pm 40\text{ppm}/^\circ\text{C}(\text{max})$ gain drift
- Excellent AC Performance
 - SNR: 85dB (typ)
 - THD: -93dB (typ)
- 16-Bit Resolution with No Missing Codes
- Robust Isolation Barrier
 - High lifetime: >40 years
 - Up to 5000V_{RMS} isolation rating
 - ± 150 kV/ μs typical CMTI
- Fault Diagnostic Functions Improve System Safety
- Wide Operating Temperature Range: -40°C to 125°C
- 16-pin wide-body SOIC package
- Safety Regulatory Approvals
 - 7070 V_{PK} isolation per DIN EN IEC 60747-17 (VDE 0884-17): 2021-10
 - 5000 V_{RMS} isolation for 1 minute per UL 1577
 - CQC and TUV certification approvals

2 Applications

- Industrial Motor Controls and Drives
- Uninterruptible Power Supplies(UPS)
- Isolated Power Supply

3 Description

The CA-IS1305x family of devices is series of precision isolated sigma-delta (Σ - Δ) modulator and optimized for shunt resistor-based current sensing or other small signal measurement applications. The input current-sense amplifier monitors current flow through a shunt (sense) resistor and the sigma-delta modulator converts the analog input to a digital bit stream of 1's and 0's at a much higher frequency. The digital output stage of CA-IS1305x provides uncoded bit-stream.

The analog input-side (high-side) and digital output-side (low-side) are separated by unique silicon oxide (SiO₂) capacitive isolation barriers that provide up to 5kV_{RMS} galvanic isolation per UL1577 certification, and isolator drivers transfer the output of the modulator across this isolation barrier. In systems with different voltage domains, this isolation technical is typically used to protect the low voltage side from the high voltage side in case of any faults. These devices also feature up to 150kV/ μs common mode transient immunity and enable efficient bit-stream transmission in noisy environments.

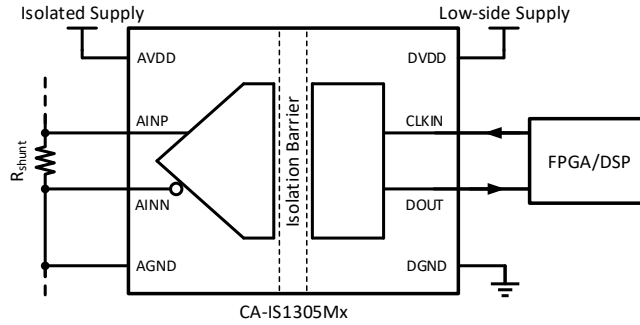
The CA-IS1305x devices' ultra-low input voltage range ($\pm 250\text{mV}$) allows the use of small sense resistor to reduce power dissipation and a very low, 0.3% gain error ensures measurement accuracy. This family of devices also features fail-safe output to support high safety system design. The CA-IS1305x devices specified for operation with 5MHz to 21MHz clock input. The internal sigma-delta modulator combined with an external digital decimation sinc³ filter can achieve 85 dB signal-to-noise ratio (SNR) at 78.1 Ksps.

The CA-IS1305x family is specified over the -40°C to $+125^\circ\text{C}$ operating temperature range and is available in 16-pin SOIC wide body package.

Device Information

Part Number	Package	Body Size(NOM)
CA-IS1305x	SOIC16-WB (W)	10.30 mm × 7.50 mm

Simplified Schematic



4 Ordering Information

Table 4-1. Valid Parts Ordering Information

Ordering Part Number	Specified Input Range	Galvanic Isolation ($\pm V$)	Differential Input Resistance	Digital Output Encoded Mode
CA-IS1305AM25W	± 250 mV	5000	22 k Ω	Uncoded CMOS
CA-IS1305M25W	± 250 mV	5000	22 k Ω	Uncoded CMOS

Note:
The only difference between CA-IS1305M25W and CA-IS1305AM25W is pin arrangement. See Pin Configuration and Descriptions for more detail.

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5 Revision History

Revision Number	Description	Page Changed
Version 1.00	Revised the CA-IS1305x specs	7 - 9
	Added typical characteristics and waveforms.	10 - 13
Version 1.01	Updated CMRR、PSRR、INL data	9
	Updated IDVDD data and typical curves	10, 15
	Added INL, DNL, CMRR and PSRR typical curves	16
Version 1.02	Updated CA-IS1305M25 Pin description: PIN 1 connected to AVDD internally	5
Version 1.03	Updated UL Certification Information	7
Version 1.04	Updated TUV and VDE Certification Information	6~7

6 Pin Configuration and Descriptions

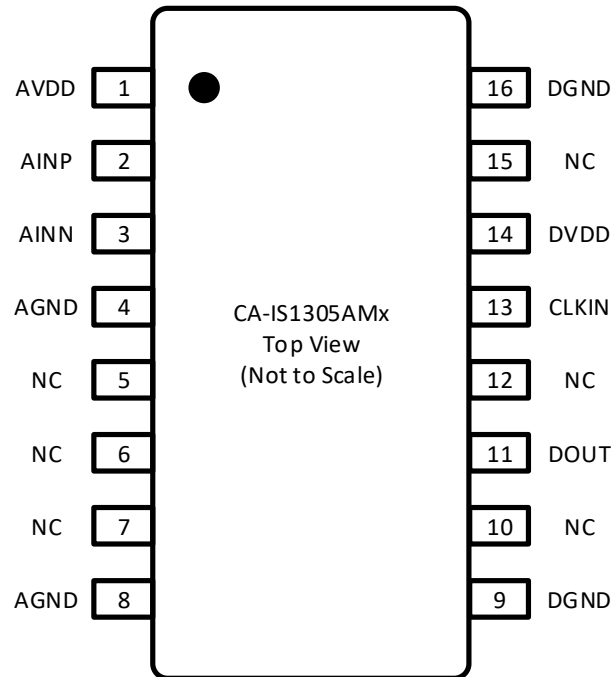


Figure 6-1. CA-IS1305AM25W Top View

Table 6-1. CA-IS1305AM25W Pin Configuration and Description

NAME	Pin #	TYPE	DESCRIPTION
AVDD	1	Power	Power supply input for the input-side (analog input-side), 4.5V to 5.5V.
AINP	2	Input	Noninverting analog input. External shunt resistor connection input (power-side) for current sense.
AINN	3	Input	Inverting analog input. External shunt resistor connection input (load-side)for current sense.
AGND	4, 8	Ground	High-side (input-side) ground.
DGND	9, 16	Ground	Low-side (output-side) ground.
DOUT	11	Output	Modulator bit-stream output.
CLKIN	13	Output	Modulator clock input(5 MHz to 21 MHz) with internal 1.5-MΩ pulldown resistor.
DVDD	14	Power	Low-side (digital output-side) power supply. Bypass DVDD to DGND
NC	5, 6, 7	–	No connection. Leave them open or connect to AVDD or AGND.
	10, 12, 15	–	No connection. Leave them open or connect to DVDD or DGND.

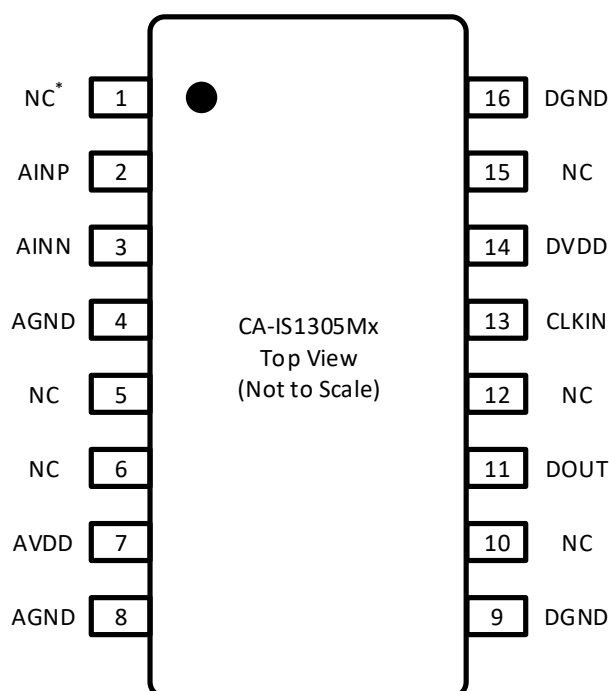


Figure 6-2. CA-IS1305M25W Top View

Table 6-2. CA-IS1305M25W Pin Configuration and Description

NAME	Pin #	TYPE	DESCRIPTION
AVDD	7	Power	Power supply input for the input-side (analog input-side), 4.5V to 5.5V.
AINP	2	Input	Noninverting analog input. External shunt resistor connection input (power-side) for current sense.
AINN	3	Input	Inverting analog input. External shunt resistor connection input (load-side)for current sense.
AGND	4, 8	Ground	High-side (input-side) ground.
NC	1, 5, 6	---	No connection. Leave them open or connect to AVDD or AGND.
DGND	9, 16	Ground	Low-side (output-side) ground.
NC	10, 12, 15	---	No connection. Leave them open or connect to DVDD or DGND.
DOUT	11	Output	Modulator bit-stream output.
CLKIN	13	Output	Modulator clock input(5 MHz to 21 MHz) with internal 1.5-MΩ pulldown resistor.
DVDD	14	Power	Low-side (digital output-side) power supply, 3.0V to 5.5V.
NC	1*	-	No connection. But connected to AVDD internally. Leave it open or connect to AVDD
	5, 6	-	No connection. Leave them open ,connect to AVDD or AGND
	10, 12, 15	-	No connection. Leave them open ,connect to DVDD or DGND

7 Specifications

7.1 Absolute Maximum Ratings¹

PARAMETER		MIN	MAX	UNIT
AVDD, DVDD	Supply voltage ²	-0.5	6.5	V
AINP, AINN	Analog input voltage	AGND - 6	6.5	V
CLKIN, DOUT	Digital input or output voltage	DGND - 0.5	DVDD + 0.5 ³	V
I _{IN}	Input current to any pin except supply pins	-10	10	mA
T _J	Junction Temperature		150	°C
T _{STG}	Storage Temperature	-65	150	°C

Notes:

- The stresses listed under "Absolute Maximum Ratings" are stress ratings only, not for functional operation condition. Exposure to absolute maximum rating conditions for extended periods may cause permanent damage to the device.
- All voltage values are with respect to the local ground terminal (AGND or DGND) and are peak voltage values.
- Maximum voltage must not exceed 6.5V.

7.2 ESD Ratings

		VALUE	UNIT
V _{ESD} Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ¹	±4000	V
	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ²	±2000	

Notes:

- Per JEDEC document JEP155, 500V HBM allows safe manufacturing of standard ESD control process.
- Per JEDEC document JEP157, 250V CDM allows safe manufacturing of standard ESD control process.

7.3 Recommended Operating Conditions

PARAMETER		MIN	NOM	MAX	UNIT
AVDD	High-side (analog input) supply voltage, with respect to AGND	4.5	5.0	5.5	V
DVDD	Low-side (digital output) supply voltage, with respect to DGND	3.0	3.3	5.5	V
T _A	Operating ambient temperature range	-40		125	°C

7.4 Thermal Information

THERMAL METRIC		VALUE	UNIT
R _{θJA}	Junction-to-ambient thermal resistance	86.5	°C/W

7.5 Power Ratings

PARAMETER		TEST CONDITIONS	VALUE	UNIT
P _D	Maximum power dissipation for both sides	AVDD = DVDD = 5.5 V	129.25	mW
P _{D1}	Maximum power dissipation for high-side	AVDD = 5.5 V	90.75	mW
P _{D2}	Maximum power dissipation for low-side	DVDD = 5.5 V	38.50	mW

7.6 Insulation Specifications

PARAMETR		TEST CONDITIONS	VALUE	UNIT
CLR	External clearance ¹	Shortest terminal-to-terminal distance through air	8	mm
CPG	External creepage ¹	Shortest terminal-to-terminal distance across the package surface	8	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	28	μm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	> 600	V
	Material group	According to IEC 60664-1	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 300 V _{RMS}	I-IV	
		Rated mains voltage ≤ 600 V _{RMS}	I-IV	
		Rated mains voltage ≤ 1000 V _{RMS}	I-III	
DIN EN IEC 60747-17 (VDE 0884-17)²				
V _{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	1414	V _{PK}
V _{IOWM}	Maximum working isolation voltage	AC voltage; Time dependent dielectric breakdown (TDDB) Test	1000	V _{RMS}
		DC voltage	1414	V _{DC}
V _{IOTM}	Maximum transient isolation voltage	V _{TEST} = V _{IOTM} , t = 60 s (qualification); V _{TEST} = 1.2 × V _{IOTM} , t = 1 s (100% production)	7070	V _{PK}
V _{IOSM}	Maximum surge isolation voltage ³	Test method per IEC 60065, 1.2/50 μs waveform, V _{TEST} = 1.6 × V _{IOSM} (qualification)	8000	V _{PK}
q _{pd}	Apparent charge ⁴	Method a, After input/output safety test subgroup 2/3, V _{ini} = V _{IOTM} , t _{ini} = 60 s; V _{pd(m)} = 1.2 × V _{IORM} , t _m = 10 s	≤ 5	pC
		Method a, After environmental tests subgroup 1, V _{ini} = V _{IOTM} , t _{ini} = 60 s; V _{pd(m)} = 1.6 × V _{IORM} , t _m = 10 s	≤ 5	
		Method b1, At routine test (100% production) and preconditioning (type test) V _{ini} = 1.2 × V _{IOTM} , t _{ini} = 1 s; V _{pd(m)} = 1.875 × V _{IORM} , t _m = 1 s	≤ 5	
C _{IO}	Barrier capacitance, input to output ⁵	V _{IO} = 0.4 × sin(2πft), f = 1 MHz	~ 1	pF
R _{IO}	Isolation resistance ⁴	V _{IO} = 500 V, T _A = 25°C	> 10 ¹²	Ω
		V _{IO} = 500 V, 100°C ≤ T _A ≤ 125°C	> 10 ¹¹	
		V _{IO} = 500 V at T _S = 150°C	> 10 ⁹	
	Pollution degree		2	
UL 1577				
V _{ISO}	Maximum withstanding isolation voltage	V _{TEST} = V _{ISO} , t = 60s (qualification), V _{TEST} = 1.2 × V _{ISO} , t = 1s (100% production)	5000	V _{RMS}

Notes:

- Apply creepage distance and clearance requirements according to application-specific equipment isolation standards. Take care to maintain the creepage distance and clearance distance of the circuit board design to ensure that the isolator mounting pad on the printed circuit board does not shorten the distance. In some cases the creepage distance and gap on the printed circuit board become equal. Techniques such as inserting grooves into printed circuit boards are used to help increase these specifications.
- This coupler is suitable for “safe electrical insulation” only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
- Devices are immersed in oil during surge characterization.
- The characterization charge is discharging charge (pd) caused by partial discharge.
- Capacitance and resistance are measured with all pins on high-side and low-side tied together.

7.7 Safety-Related Certifications

VDE	UL	TUV
Certified according to DIN EN IEC 60747-17 (VDE 0884-17):2021-10	Recognized under UL 1577 Component Recognition Program and CSA Component Acceptance Service Notice No. 5A	Certified according to EN 61010-1: 2010+A1
Reinforced insulation Maximum repetitive peak isolation voltage: 1414 V _{PK} Maximum transient isolation voltage: 7070 V _{PK} Maximum surge isolation voltage: 8000 V _{PK}	Single protection 5000 V _{RMS}	5000 V _{RMS}
Certification Number: 40057278	Certification Number: E511334-20200520	Certification Number: CN23RC4J 001

7.8 Electrical Characteristics

All minimum/maximum specs are at $T_A = -40^{\circ}\text{C}$ to 125°C , $AVDD = 4.5\text{ V}$ to 5.5 V , $DVDD = 3.0\text{ V}$ to 5.5 V , $AINP = -250\text{ mV}$ to 250 mV , $AINN = AGND = 0\text{V}$, and sinc³ filter output configured to 16 bits with $OSR = 256$ (unless otherwise noted). All typical values are at 25°C with $CLKIN = 20\text{ MHz}$, $AVDD = 5\text{ V}$, and $DVDD = 3.3\text{ V}$ (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUT						
V_{clipping}	Maximum input voltage before clipping output	$AINP - AINN$		± 320		mV
V_{FSR}	Specified linear full-scale input range	$AINP - AINN$	-250		250	mV
V_{CM}	Operating common-mode input voltage	$(AINP + AINN) / 2$ to AGND	-0.16		$AVDD - 2.1$	V
V_{CMOV}	Common-mode overvoltage threshold	$(AINP + AINN) / 2$ to AGND	$AVDD - 2$			V
$V_{\text{CMOV_HYS}}$	Hysteresis of common-mode overvoltage threshold			100		mV
C_{IN}	Single-ended input capacitance	$f_{\text{IN}} = 270\text{ kHz}$, $AINN = AGND$		2		pF
C_{IND}	Differential input capacitance	$f_{\text{IN}} = 270\text{ kHz}$		1		pF
R_{IN}	Single-ended input resistance	$AINN = AGND$		19		k Ω
R_{IND}	Differential input resistance			22		k Ω
I_{IN}	Input current	$AINP = AINN = AGND$, $I_{\text{IN}} = (I_{\text{INP}} + I_{\text{INN}}) / 2$	-41	-30	-24	μA
TC_{IIN}	Input current drift			± 1		nA/ $^{\circ}\text{C}$
I_{INOS}	Input offset current	$I_{\text{INOS}} = I_{\text{INP}} - I_{\text{INN}}$		± 5		nA
$CMRR_{\text{IN}}$	Input common-mode rejection ratio	DC, $AINP = AINN$		-85		dB
		$f_{\text{IN}} = 10\text{ kHz}$, $AINP = AINN$		-85		
PSRR	Power supply rejection ratio	At $AVDD$, DC, $AINP = AINN = AGND$		-98		dB
		At $AVDD$, 100-mV and 10-kHz ripple, $AINP = AINN = AGND$		-98		
BW_{IN}	-3 dB input bandwidth			1000		kHz
CMTI	Common-mode transient immunity	$ AGND - DGND = 1.5\text{ kV}$	100	150		kV/ μs
MODULATOR ACCURACY						
DNL	Differential nonlinearity	Resolution: 16 bits	-0.99		0.99	LSB
INL	Integral nonlinearity ¹	Resolution: 16 bits	-6	± 2	6	LSB
E_{O}	Offset error	Initial, at $T_A = 25^{\circ}\text{C}$, $AINP = AINN = AGND$	-150	± 4.5	150	μV
TCE_{O}	Offset drift		-3.5	± 0.5	3.5	$\mu\text{V}/^{\circ}\text{C}$
E_{G}	Gain error	Initial, at $T_A = 25^{\circ}\text{C}$	-0.3%	$\pm 0.05\%$	0.3%	
TCE_{G}	Gain drift		-40	± 20	40	ppm/ $^{\circ}\text{C}$
SNR	Signal-to-noise ratio	$f_{\text{IN}} = 1\text{ kHz}$, $BW = 10\text{ kHz}$		85		dB
SINAD	Signal-to-noise-and-distortion ratio	$f_{\text{IN}} = 1\text{ kHz}$, $BW = 10\text{ kHz}$		84		dB
THD	Total harmonic distortion	$f_{\text{IN}} = 1\text{ kHz}$, $BW = 10\text{ kHz}$		-93		dB
SFDR	Spurious-free dynamic range	$f_{\text{IN}} = 1\text{ kHz}$, $BW = 10\text{ kHz}$		94		dB
Note:						
1. The INL is defined as the maximum deviation from a straight line passing through the end-point of the ideal ADC transfer function once the gain and offset errors have been nullified and expressed as number of LSBs over the specified linear full-scale input range.						

Electrical Characteristics (Continued)

All minimum/maximum specs are at $T_A = -40^{\circ}\text{C}$ to 125°C , $AVDD = 4.5\text{ V}$ to 5.5 V , $DVDD = 3.0\text{ V}$ to 5.5 V , $AINP = -250\text{ mV}$ to 250 mV , $AINN = AGND = 0\text{V}$, and sinc³ filter output configured to 16 bits with $OSR = 256$ (unless otherwise noted). All typical values are at 25°C with $CLKIN = 20\text{ MHz}$, $AVDD = 5\text{ V}$, and $DVDD = 3.3\text{ V}$ (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL INPUT						
I_{IN}	Input current	$2.7\text{ V} \leq V_{IN} \leq 5.5\text{ V}$	0		7	μA
C_{IN}	Input capacitance			4		pF
V_{IH}	Logic high-level input voltage		$0.7 \times DVDD$		$DVDD + 0.3$	V
V_{IL}	Logic low-level input voltage		-0.3		$0.3 \times DVDD$	V
DIGITAL OUTPUT						
C_L	Output load capacitance			30		pF
V_{OH}	Logic high-level output voltage	$I_{OH} = -20\ \mu\text{A}$	$DVDD - 0.1$			V
		$I_{OH} = -4\text{ mA}$	$DVDD - 0.4$			
V_{OL}	Logic low-level output voltage	$I_{OL} = 20\ \mu\text{A}$			0.1	V
		$I_{OL} = 4\text{ mA}$			0.4	
POWER SUPPLY						
$AVDD_{UV}$	AVDD undervoltage threshold	AVDD rising		2.5	2.7	V
I_{AVDD}	High-side supply current	$4.5\text{ V} \leq AVDD \leq 5.5\text{ V}$		11.5	16.5	mA
I_{DVDD}	Low-side supply current with $C_L = 15\text{ pF}^1$	$3.0\text{ V} \leq DVDD \leq 3.6\text{ V}$		3.3	5.3	mA
		$4.5\text{ V} \leq DVDD \leq 5.5\text{ V}$		4.0	7.0	
Note:						
1. C_L is approximately 15pF including external (probe and stray) capacitance.						

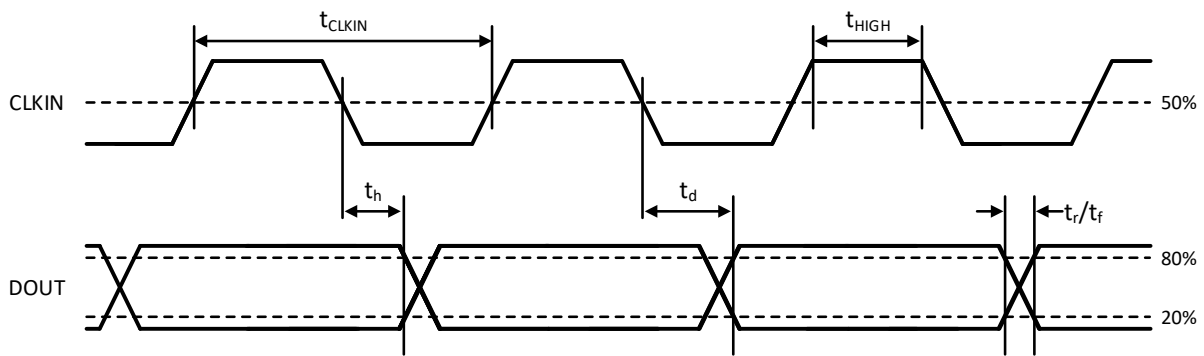
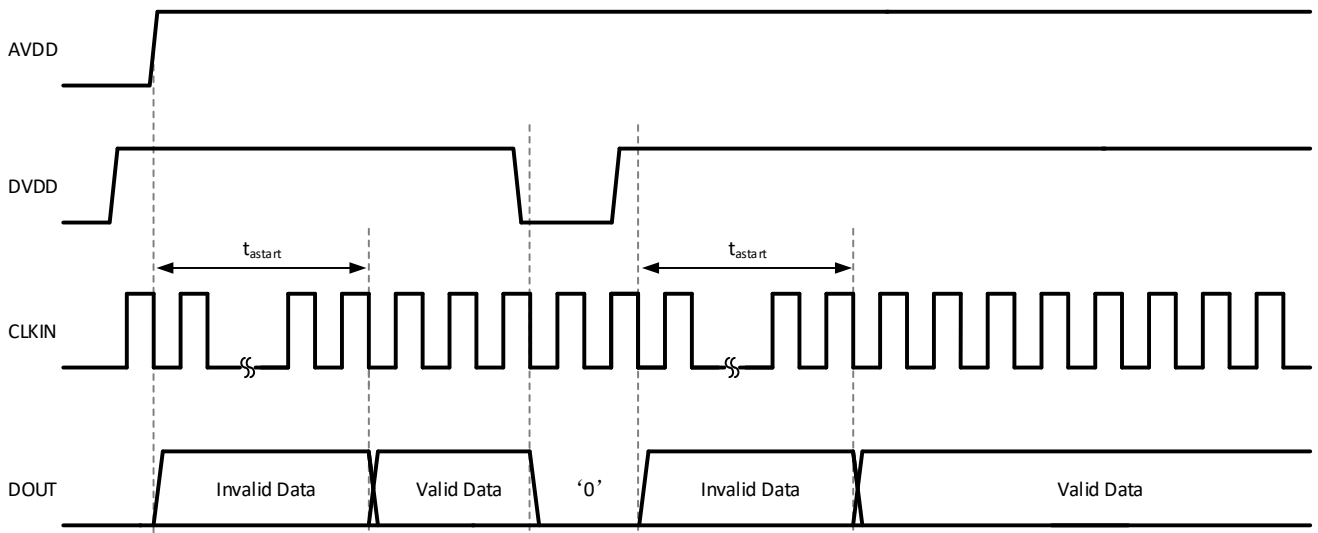
7.9 Switching Characteristics

All minimum/maximum specs are at $T_A = -40^{\circ}\text{C}$ to 125°C , $AVDD = 4.5\text{ V}$ to 5.5 V , $DVDD = 3.0\text{ V}$ to 5.5 V , $A\text{INP} = -250\text{ mV}$ to 250 mV , $A\text{INN} = \text{AGND} = 0\text{ V}$, and sinc³ filter output configured to 16 bits with $\text{OSR} = 256$ (unless otherwise noted). All typical values are at 25°C with $\text{CLKIN} = 20\text{ MHz}$, $AVDD = 5\text{ V}$, and $DVDD = 3.3\text{ V}$ (unless otherwise noted).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT		
f_{CLKIN}	CLKIN clock frequency	$4.5\text{ V} \leq AVDD \leq 5.5\text{ V}$		5	21	MHz	
Duty Cycle	CLKIN clock duty cycle	$t_{\text{HIGH}} / t_{\text{CLKIN}}, 4.5\text{ V} \leq AVDD \leq 5.5\text{ V}$		42.5%	50%	57.5%	
t_{h}	Hold time of DOUT after rising edge of CLKIN ¹	$C_L = 15\text{ pF}^2$; <i>See Figure</i>		3.5		ns	
t_{d}	Delay time of DOUT after rising edge of CLKIN ¹	$C_L = 15\text{ pF}^2$; <i>See Figure</i>			16	ns	
t_{r}	Rise time of DOUT (10%–90%)	$C_L = 15\text{ pF}^2$		1.8	5.0	ns	
t_{f}	Fall time of DOUT (90%–10%)	$C_L = 15\text{ pF}^2$		1.8	5.0	ns	
t_{astart}	Analog startup time	AVDD step to 4.5 V with $3.0\text{ V} \leq DVDD$; <i>See Figure</i>		500		μs	

Note:

- C_L is approximately 15pF including external (probe and stray) capacitance.


Figure 7-1. CA-IS1305x Digital Output Timing

Figure 7-2. CA-IS1305x Startup Timing

7.10 Typical Characteristics and Waveforms

All minimum/maximum specs are at $T_A = -40^{\circ}\text{C}$ to 125°C , $AVDD = 4.5\text{ V}$ to 5.5 V , $DVDD = 3.0\text{ V}$ to 5.5 V , $A\text{INP} = -250\text{ mV}$ to 250 mV , $A\text{INN} = \text{AGND} = 0\text{V}$, and sinc³ filter output configured to 16 bits with $\text{OSR} = 256$ (unless otherwise noted). All typical values are at 25°C with $\text{CLKIN} = 20\text{ MHz}$, $AVDD = 5\text{ V}$, and $DVDD = 3.3\text{ V}$ (unless otherwise noted).

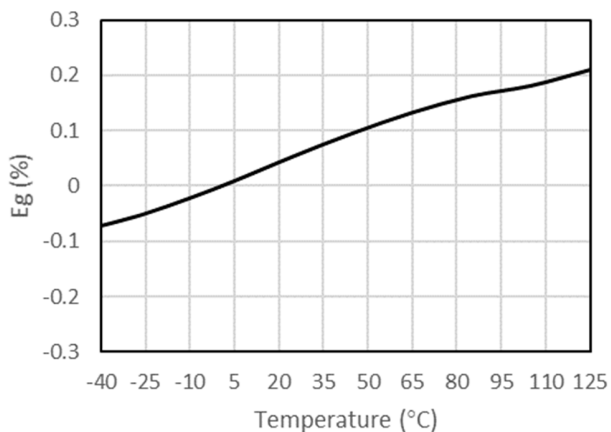


Figure 7-1. Gain vs. Temperature

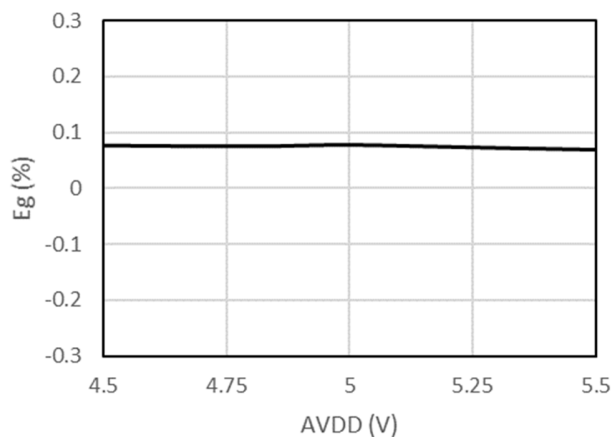


Figure 7-2. Gain Error vs. High-side Supply Voltage

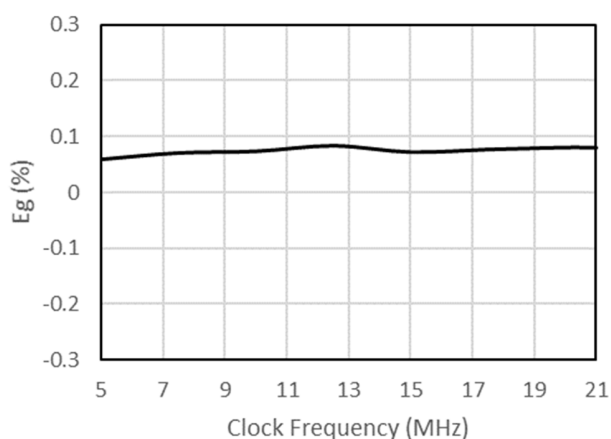


Figure 7-3. Gain Error vs. Clock Frequency

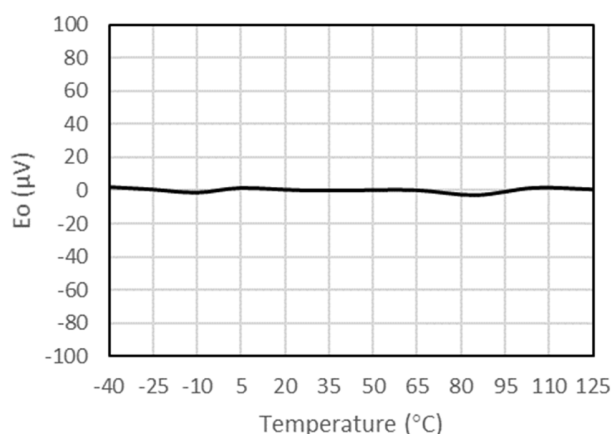


Figure 7-4. Offset vs. Temperature

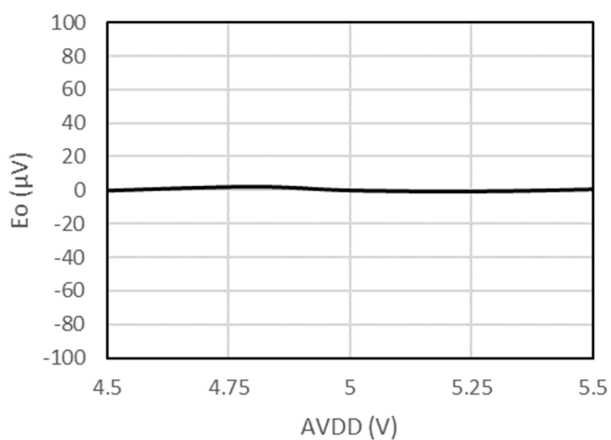


Figure 7-5. Offset Error vs. High-side Supply Voltage

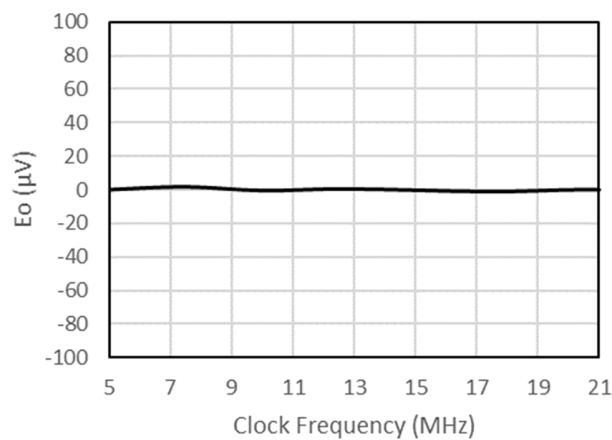
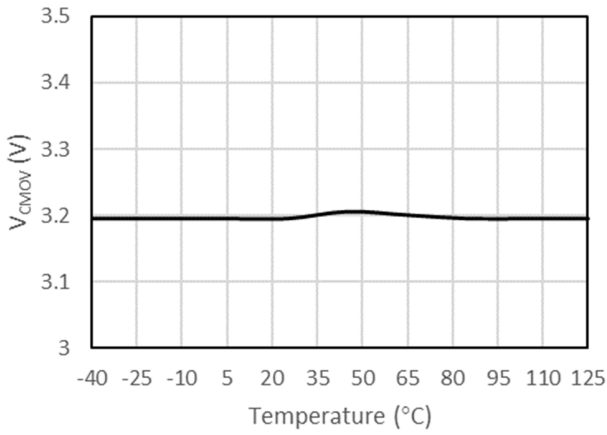
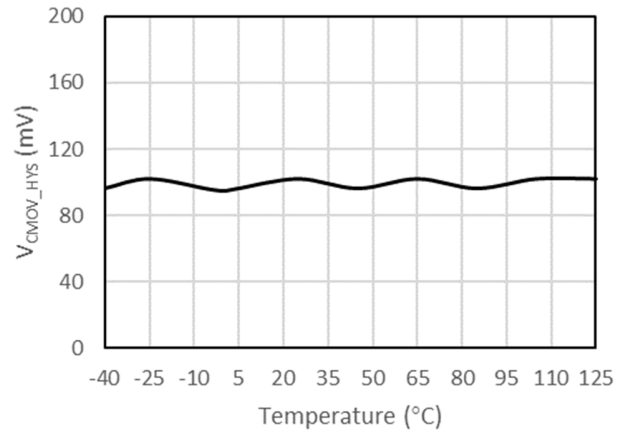
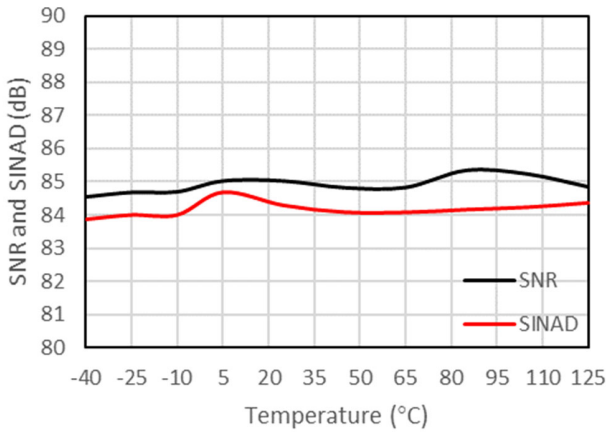
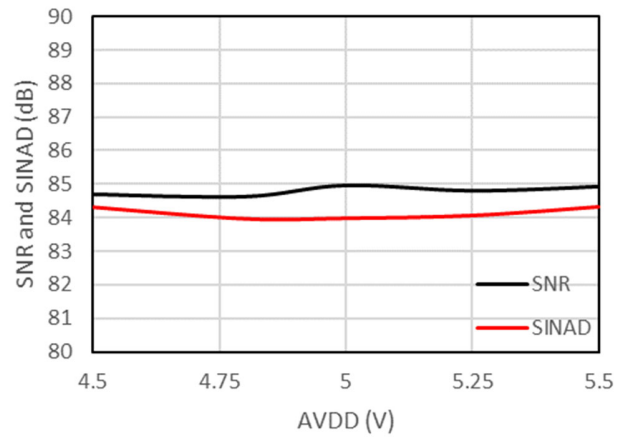
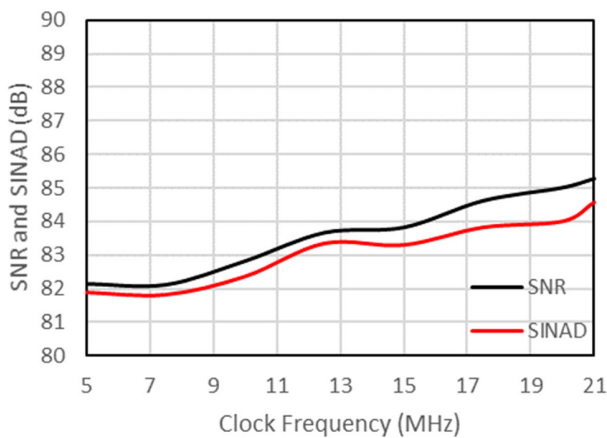
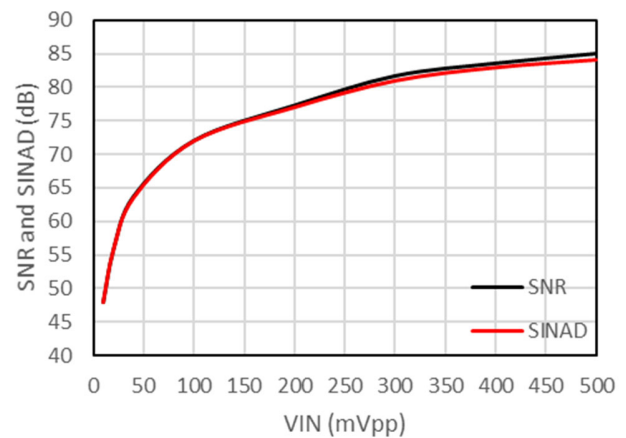


Figure 7-6. Offset Error vs. Clock Frequency

Typical Characteristics and Waveforms (Continued)

All minimum/maximum specs are at $T_A = -40^\circ\text{C}$ to 125°C , $AVDD = 4.5\text{ V}$ to 5.5 V , $DVDD = 3.0\text{ V}$ to 5.5 V , $AINP = -250\text{ mV}$ to 250 mV , $AINN = AGND = 0\text{V}$, and sinc³ filter output configured to 16 bits with $OSR = 256$ (unless otherwise noted). All typical values are at 25°C with $CLKIN = 20\text{ MHz}$, $AVDD = 5\text{ V}$, and $DVDD = 3.3\text{ V}$ (unless otherwise noted).


Figure 7-7. Common-mode overvoltage threshold vs. Temperature

Figure 7-8. Hysteresis of common-mode over-voltage threshold vs. Temperature

Figure 7-9. SNR & SINAD vs. Temperature

Figure 7-10. SNR & SINAD vs. High-side Supply Voltage

Figure 7-11. SNR & SINAD vs. Clock Frequency

Figure 7-12. SNR & SINAD vs. Input

Typical Characteristics and Waveforms (Continued)

All minimum/maximum specs are at $T_A = -40^{\circ}\text{C}$ to 125°C , $AVDD = 4.5\text{ V}$ to 5.5 V , $DVDD = 3.0\text{ V}$ to 5.5 V , $AINP = -250\text{ mV}$ to 250 mV , $AINN = \text{AGND} = 0\text{V}$, and sinc³ filter output configured to 16 bits with $\text{OSR} = 256$ (unless otherwise noted). All typical values are at 25°C with $\text{CLKIN} = 20\text{ MHz}$, $AVDD = 5\text{ V}$, and $DVDD = 3.3\text{ V}$ (unless otherwise noted).

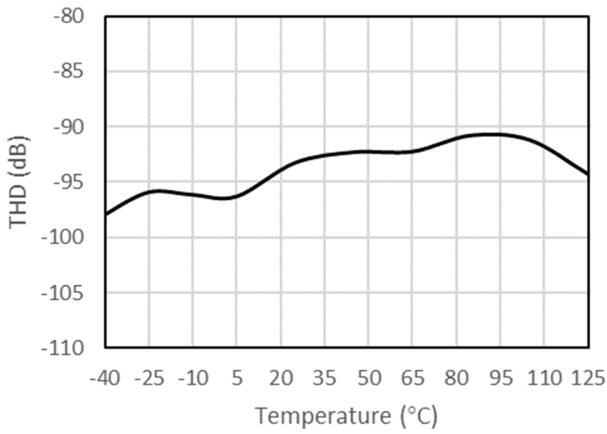


Figure 7-13. THD vs. Temperature

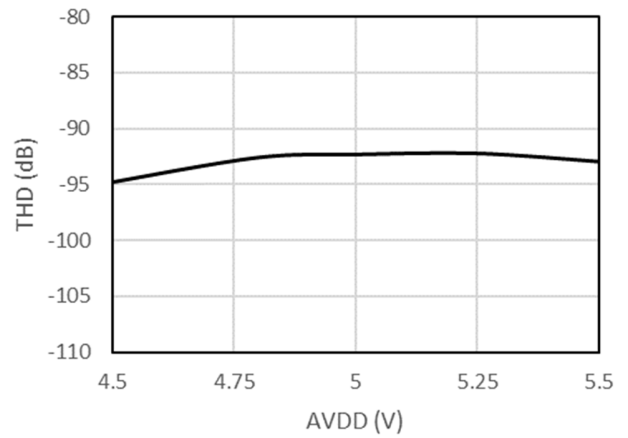


Figure 7-14. THD vs. High-side Supply Voltage

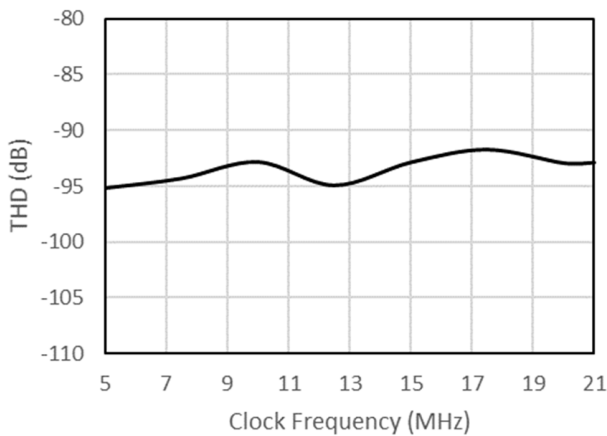


Figure 7-15. THD vs. Clock Frequency

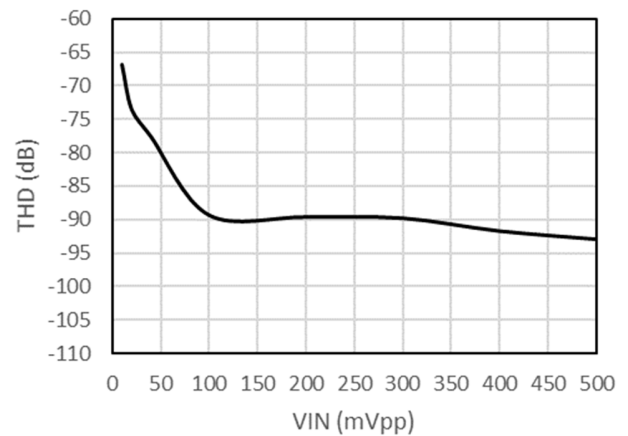


Figure 7-16. THD vs. Input

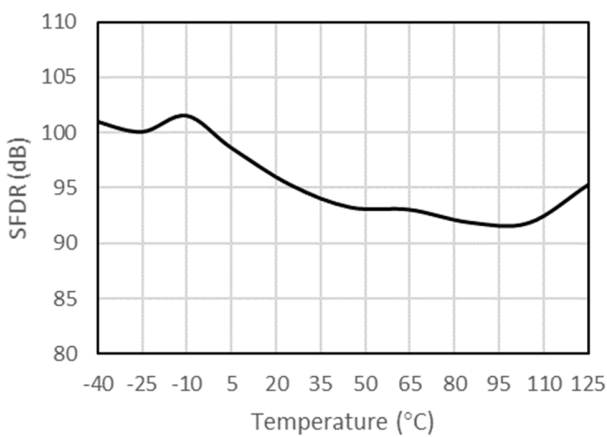


Figure 7-17. SFDR vs. Temperature

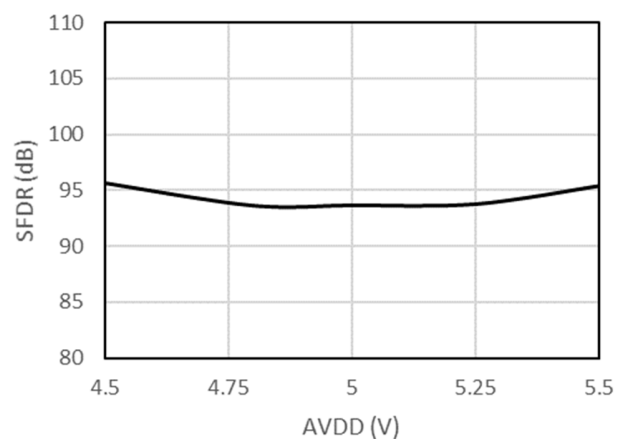


Figure 7-18. SFDR vs. High-side Supply Voltage

Typical Characteristics and Waveforms (Continued)

All minimum/maximum specs are at $T_A = -40^{\circ}\text{C}$ to 125°C , $AVDD = 4.5\text{ V}$ to 5.5 V , $DVDD = 3.0\text{ V}$ to 5.5 V , $AINP = -250\text{ mV}$ to 250 mV , $AINN = AGND = 0\text{V}$, and sinc³ filter output configured to 16 bits with $OSR = 256$ (unless otherwise noted). All typical values are at 25°C with $CLKIN = 20\text{ MHz}$, $AVDD = 5\text{ V}$, and $DVDD = 3.3\text{ V}$ (unless otherwise noted).

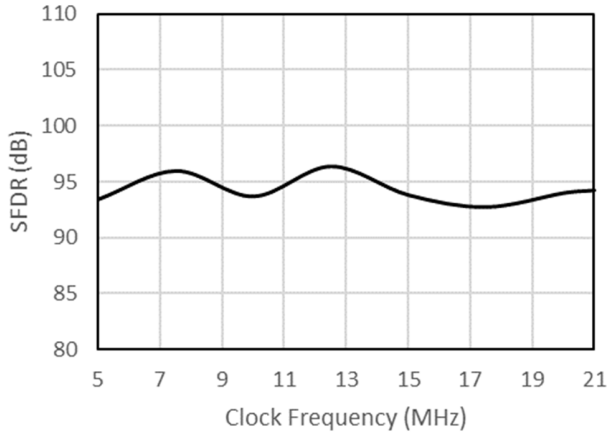


Figure 7-19. SFDR vs. Clock Frequency

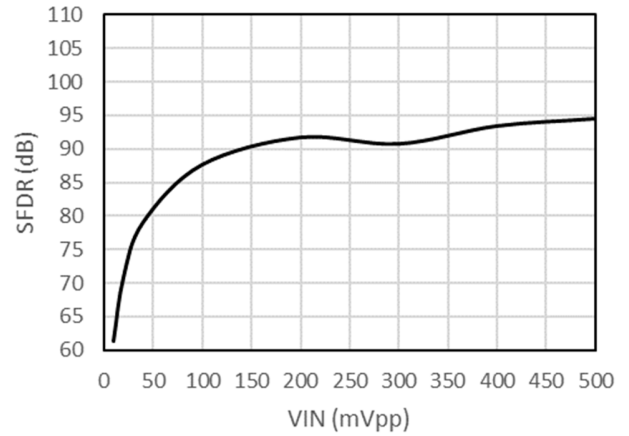


Figure 7-20. SFDR vs. Input

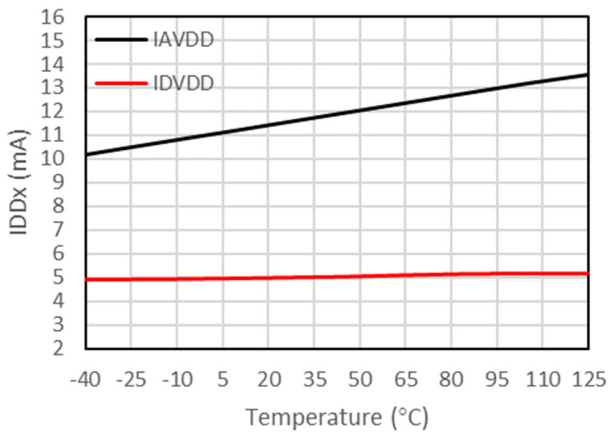


Figure 7-21. Supply Current vs. Temperature

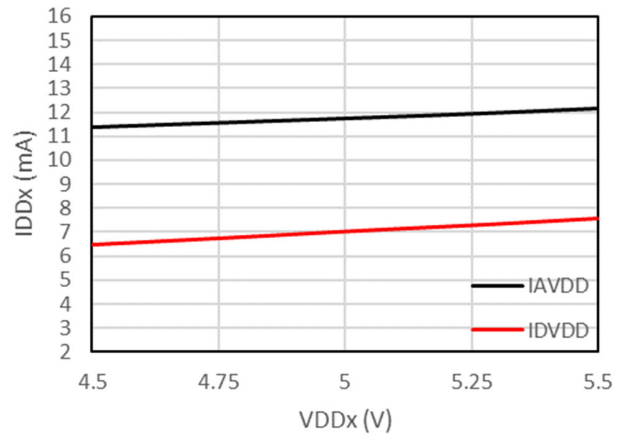


Figure 7-22. Supply Current vs. Supply Voltage

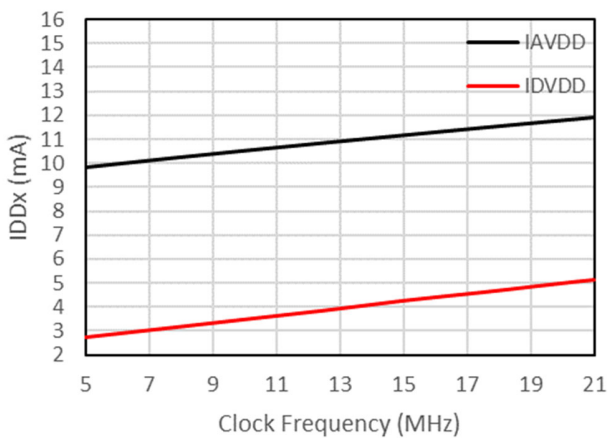


Figure 7-23. Supply Current vs. Clock Frequency

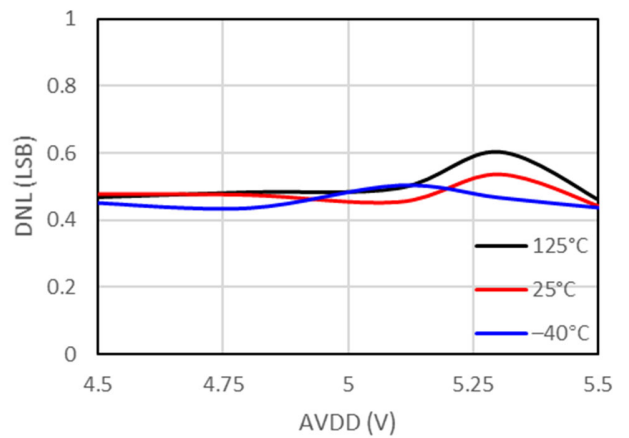


Figure 7-24. DNL vs. High-side Supply Voltage

Typical Characteristics and Waveforms (Continued)

All minimum/maximum specs are at $T_A = -40^{\circ}\text{C}$ to 125°C , $AVDD = 4.5\text{ V}$ to 5.5 V , $DVDD = 3.0\text{ V}$ to 5.5 V , $AINP = -250\text{ mV}$ to 250 mV , $AINN = AGND = 0\text{V}$, and sinc³ filter output configured to 16 bits with $OSR = 256$ (unless otherwise noted). All typical values are at 25°C with $CLKIN = 20\text{ MHz}$, $AVDD = 5\text{ V}$, and $DVDD = 3.3\text{ V}$ (unless otherwise noted).

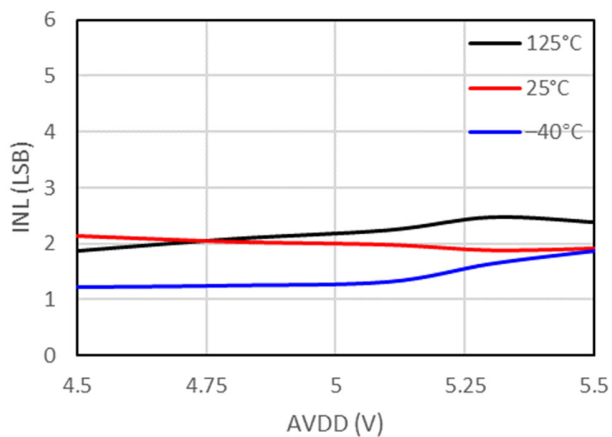


Figure 7-25. INL vs. High-side Supply Voltage

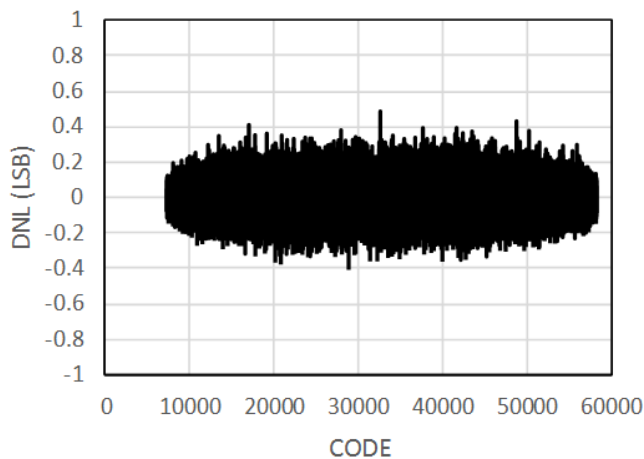


Figure 7-28. Typical DNL

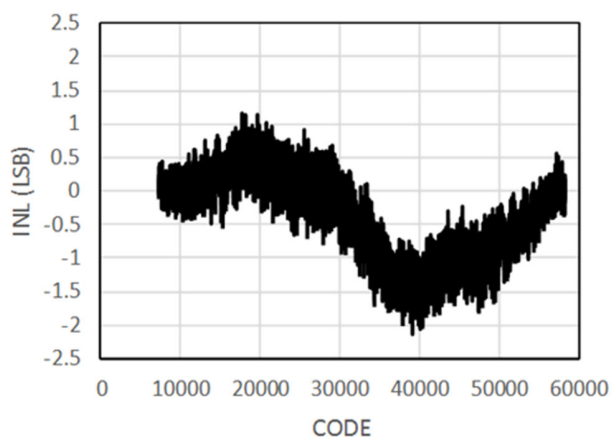


Figure 7-29. Typical INL

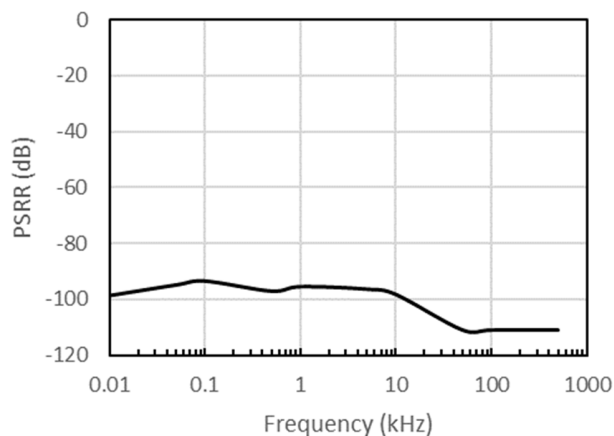


Figure 7-30. PSRR vs. frequency

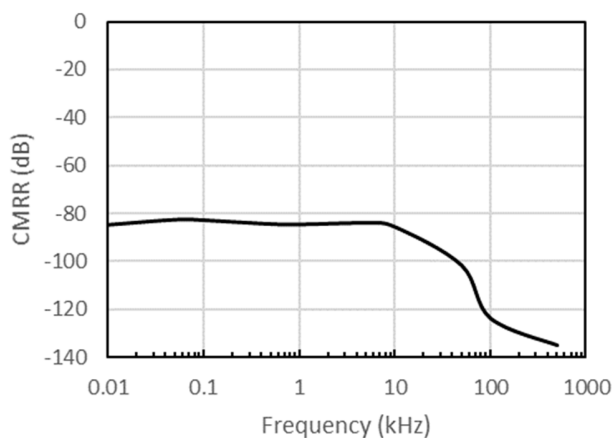


Figure 7-31. CMRR vs. frequency

8.3 Signal Isolation

The CA-IS1305x family of devices utilizes Chipanalog’s full differential capacitive isolation technology, as shown in Figure , that contains an ON-OFF keying (OOK) modulation scheme to transfer digital signals across the SiO₂ based isolation barrier between circuits with different power domains. The transmitter sends a high frequency carrier across the barrier to represent one digital state and sends no signal to represent the other digital state. The isolation receiver demodulates the signal and recovery input signal at output through a buffer stage, see Figure for more details. With this OOK architecture, the CA-IS1305x devices build a robust data transmission path between different power domains and support up to 5kV_{RMS} galvanic isolation between the analog input side and digital output side.

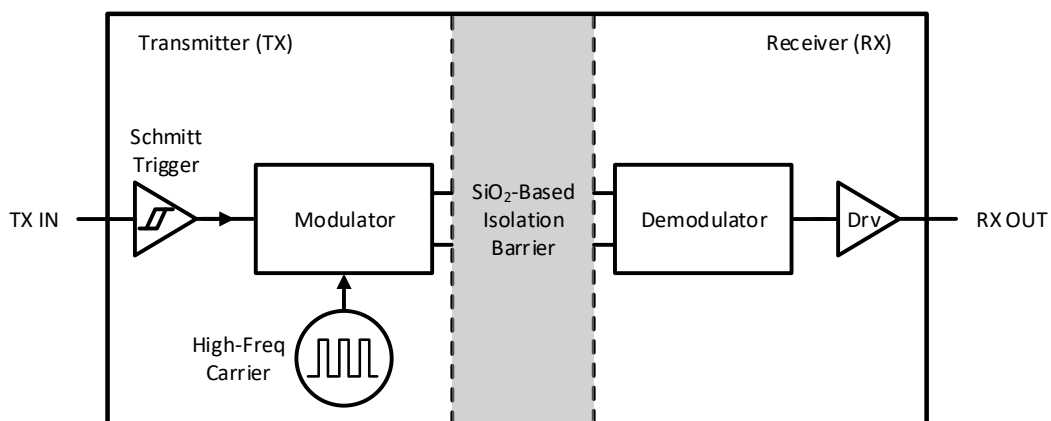


Figure 8-2. Block Diagram of the Isolation Channel

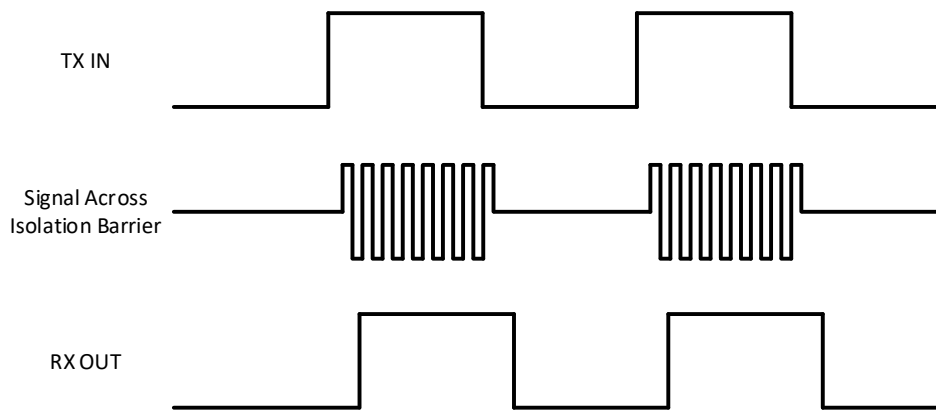


Figure 8-3. OOK Modulation

8.4 Digital Output (Low-side)

8.4.1 Bit stream output

The CA-IS1305x devices perform fully differential analog input to digital output conversion using a sigma-delta modulator. The sigma-delta modulator converts the input signal into a digital pulse train whose average duty cycle represents the digitized signal information. Figure shows the relationship between the bit stream output vs. analog input (AINP – AINN). The analog input of 0 V ideally produces to a digital bit-stream of “1” and “0” with high 50% of the time. For the analog input voltage within full-scale input range (± 320 mV), the digital output maintains a linear relationship with the analog input, and the density of 1s in the digital output bit-stream can be calculated as following equation:

$$Density|_{1s} = (V_{IN} + V_{Clipping}) / (2 \times V_{Clipping}) \quad \text{(Equation 1)}$$

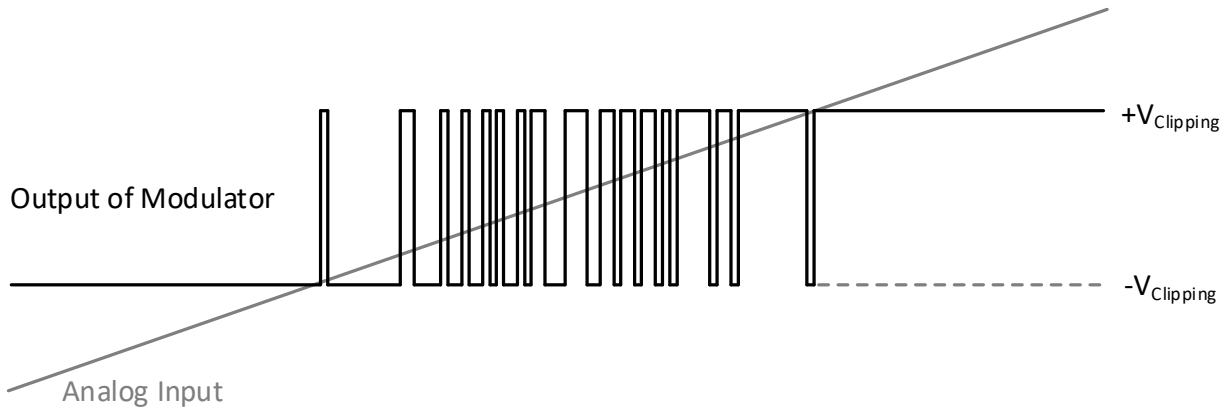


Figure 8-4. CA-IS1305x Modulator Output vs. Analog Input (AINP – AINN)

8.4.2 Over-range Output

For CA-IS1305x devices, the maximum input voltage before clipping output is $\pm 320\text{mV}$. If the analog input less than or equal to -320mV , the CA-IS1305x modulator will clip the bit-stream at “0”, and generate a single “1” every 128 clocks; If the analog input grater than or equal to $+320\text{mV}$, the CA-IS1305x modulator will clip the bit-stream at “1”, and generate a single “0” every 128 clocks, see Figure 8-5.

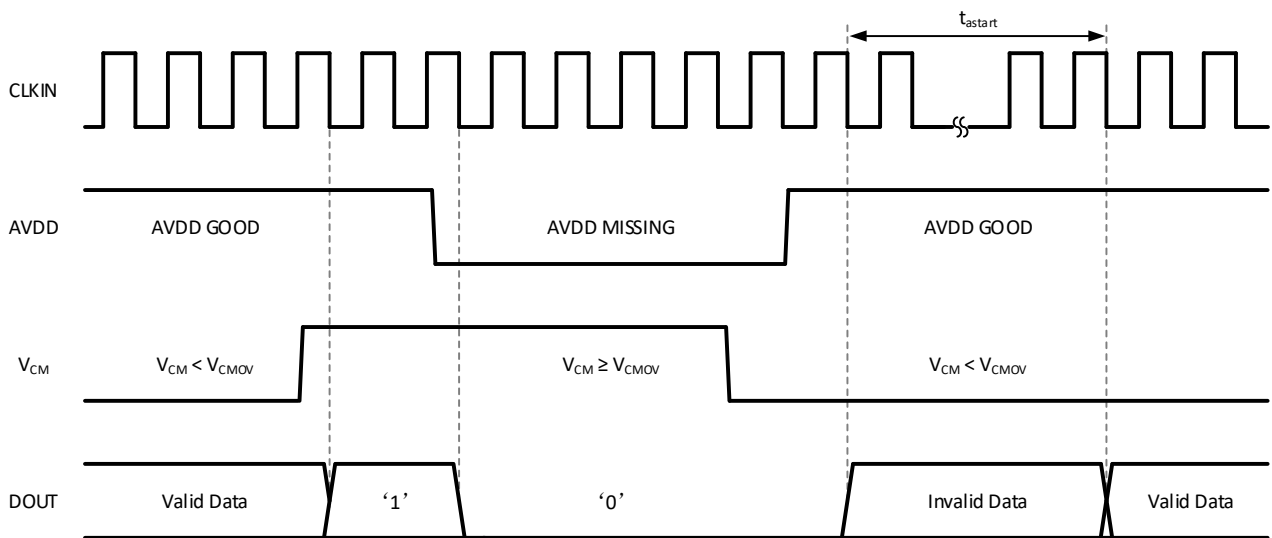


Figure 8-5. CA-IS1305x Over-range Output Waveforms

8.4.3 Fail-Safe Output

The CA-IS1305x devices feature fail-safe output indication which means the devices guarantee a logic-low on the digital output (DOUT) when the high-side power supply (AVDD) is off or loss, or a logic-high at DOUT when the common-mode input voltage V_{CM} exceeds the common-mode overvoltage threshold V_{CMOV} . When both cases occur at the same time, the priority of high side supply voltage (AVDD) loss is higher, so DOUT output will remain logic 0, see Figure 8-6 for more details. In the case of a missing high-side supply voltage AVDD, the output of Σ - Δ modulator is not defined and can cause a system fault or indeterminacy. The fail-safe output provides a fault indication for system and helps to improve system reliability. Also, in this way, differentiating between the AVDD loss and the over range input signal is possible on the system level.

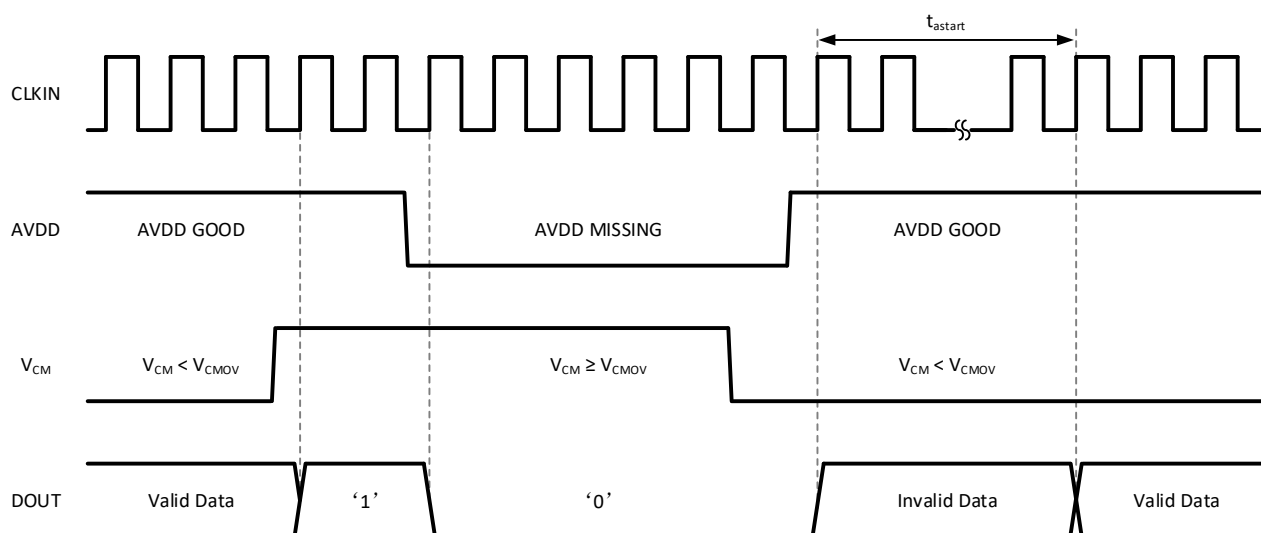


Figure 8-6. CA-IS1305x Fail-Safe Output

9 Application Information

9.1 Typical Application for Current Sense

9.1.1 Typical Application Circuit

The CA-IS1305x precision isolated sigma-delta (Σ - Δ) modulators are optimized for shunt resistor-based current sensing applications. A typical application circuit is shown in Figure, the CA-IS1305x device is used to amplify the voltage across the shunt resistor (R_{shunt}) with fixed gain (4x), and the internal sigma-delta modulator converts the amplified analog signal into digital bit-stream. The isolated bit stream output is then processed by an external digital decimation filter which can be implemented by FPGA or DSP, resulting in a conversion accuracy up to 16 bits. Robust isolation coupled with up to 150kV/ μ s typical CMTI enables accurate small signal measurement in noisy environments, making these devices ideal for motor drives, photovoltaic inverters, uninterruptible power supplies(UPS) etc. industrial applications. Figure shows the CA-IS1305x in one motor phase current sense circuit design.

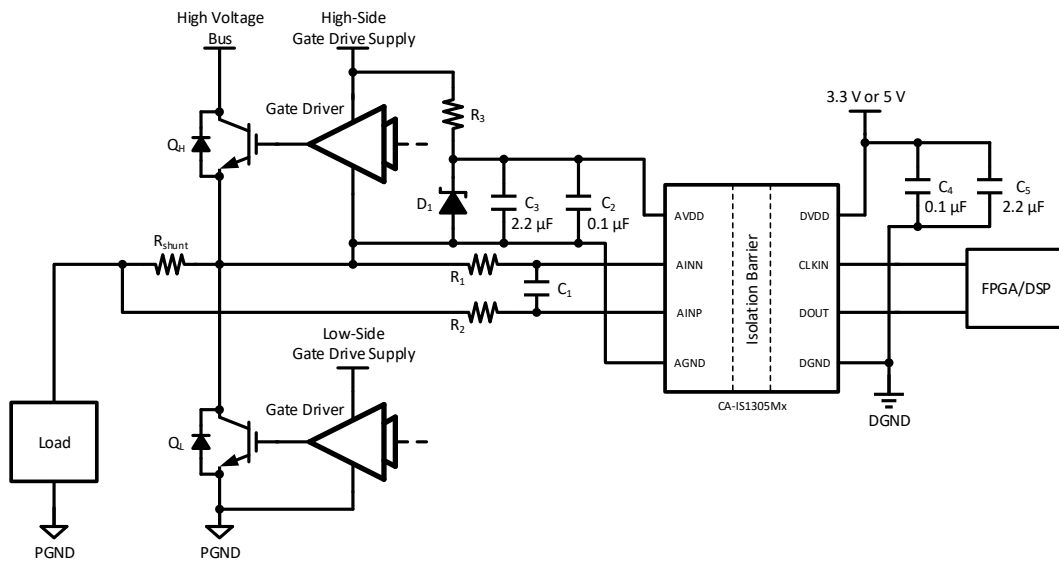


Figure 9-1. Typical Application for 1-phase Current Sensing

9.1.2 Choosing the Current Sense Resistor

The shunt resistor selection should be a trade off between power dissipation and measurement accuracy. Small value resistors minimize power dissipation, while large value resistors take advantage of the full performance input range of the sigma-delta modulator. Choose the shunt resistor based on the following criteria:

- **Accuracy:**

A high R_{shunt} value allows lower currents to be measured more accurately. This is because offsets become less significant when the sense voltage is larger. For best performance, select R_{shunt} to provide approximately V_{FSR} ($\pm 250\text{mV}$) of sense voltage for the nominal full-scale current in each application. And the voltage drop at R_{shunt} caused by the maximum current should be less than $V_{Clipping}$ ($\pm 320\text{mV}$).

- **Power dissipation**

At high current levels, the I^2R losses in R_{shunt} can be significant. Take this into consideration when choosing the resistor value and its power dissipation rating. Also, the sense resistor's value might drift if it is allowed to heat up excessively.

Due to the high currents that may flow through R_{shunt} , take care to eliminate solder and parasitic trace resistance from causing errors in the sense voltage. Either use a four-terminal current sense resistor or use Kelvin (force and sense) PCB layout technique. The Kelvin-sense traces should be as close as possible to the current-sense resistor's solder contact pads. If the Kelvin-sensing contact pads are spaced wider relative to the sense resistor, error is introduced from the additional trace resistance.

9.1.3 Analog Input Filter

To improve signal-to-noise performance of the CA-IS1305x's signal path, an external 1st-order RC filter is recommended in front of the amplifier, as shown in the typical application circuit, selecting $R_1 = R_2 = 10\Omega$ and $C_1 = 20\text{nF}$, the input bandwidth of the analog front-end of the device can be limited within 400kHz.

9.1.4 Digital Output Filter

The CA-IS1305x modulator provides 2nd-order frequency shaping of the quantization noise resulting from the single bit quantizer. To remove the frequency shaped quantization noise, a digital decimation filter is required. For the CA-IS1305x 2nd

order modulator circuit design, a sinc³ filter is recommended because of the low cost hardware design and better performance. A FPGA or DSP can be used to implement this filter to provide the transfer function of a sinc³ filter as below.

$$H(Z) = \left[\frac{1}{DR} \frac{(1 - Z^{-DR})}{(1 - Z^{-1})} \right]^3 \quad \text{(Equation 2)}$$

Where DR is the decimation rate, it is the ratio of modulator clock frequency f_{CLKIN} and throughput rate of the sinc³ filter f_{DATA} , which is also called oversampling rate (OSR).

$$DR = OSR = f_{CLKIN}/f_{DATA} \quad \text{(Equation 3)}$$

The output data width is shown in below equation.

$$\text{Data Width} = 3 \times \log_2 DR \quad \text{(Equation 4)}$$

All of the characterization in section of [Electrical Characteristics](#) is done with a sinc³ filter with an oversampling ratio(OSR) of 256 and an output word width of 16 bits.

The characteristics of the sinc³ filter are summarized in [Table 9-1](#). As the decimation rate increased, the output data width from sinc³ filter increased as well, while the throughput rate decreased, resulting higher SNR performance. Thus, designers can trade off between data rate and conversion accuracy based on the application requirements.

Table 9-1. Characteristics of sinc³ Filter at 20MHz f_{CLKIN}

Decimation Rate (DR)	f_{DATA} (kHz)	Output Data Width (Bits)	Filter Response (kHz)
32	625	15	163.7
64	312.5	18	81.8
128	156.2	21	40.9
256	78.1	24	20.4
512	39.1	27	10.2

9.2 Voltage Measurement

The CA-IS1305x current sense amplifiers, along with a voltage divider, can be used as an isolated voltage measurement solution, see [Figure 9-2](#) typical application circuit. The resistors of R_{41} , R_{42} , R_{51} , R_{52} , R_{61} and R_{62} are the internal resistors of the CA-IS1305x device, where R_{41} , R_{42} , R_{51} , and R_{52} are used to setup the amplifier gain, $R_{41} = R_{42} = 12.5 \text{ k}\Omega$, $R_{51} = R_{52} = 50 \text{ k}\Omega$; R_{61} and R_{62} are the common-mode voltage detector, $R_{61} = R_{62} = 100 \text{ k}\Omega$. The voltage-divider ($R_{21}+R_{11}$ and R_{31}) reduces the input voltage from the power supply bus voltage to $\pm 250\text{mV}$ to match the input range of the CA-IS1305x. Thus, for the high-voltage power supply bus, $(R_{21}+R_{11}) \gg R_{31}$.

Also, the bias current I_{INP} caused by V_{CM} (1.875V, typ.) passing through the voltage sense resistor R_{31} will cause significant offset error as well. To reduce the gain error and offset error, select R_{31} as small as possible. However, to limit the current consumption of the voltage-divider, choosing large resistance values for $R_{21}+R_{11}$ and R_{31} will minimize overall power consumption. Designers need to balance the choice of divider resistance.

In order to cancel out the offset error introduced by the bias current I_{INP} flowing through R_{31} , the resistor R_{32} is added at

VINN input. As the error compensating resistor, the ideal R_{32} should be the parallel resistance of $(R_{21}+R_{11})//R_{31}$, see below R_{32} calculation equation,

$$R_{32} = \frac{R_{31} \times (R_{21} + R_{11})}{R_{31} + R_{21} + R_{11}} \cong R_{31}, \quad (R_{11} + R_{21} \gg R_{31})$$

Adding R_{32} can remove the offset error caused by I_{INP} , but there will be an expected difference between the modulator’s differential input voltage ($A_{INP} - A_{INN}$) and the voltage drop on R_{31} given by the resistor divider. This discrepancy can be expressed as a gain error, as shown in below equation,

$$G_{ERROR} = \frac{R_{31}}{R_{31} + R_{41}}$$

Choosing appropriate R_{31} to balance gain error and power consumption, combine with offset compensating resistor R_{32} , the voltage measurement performance shown in [Figure 9-2](#) typical application circuit is acceptable for most applications.

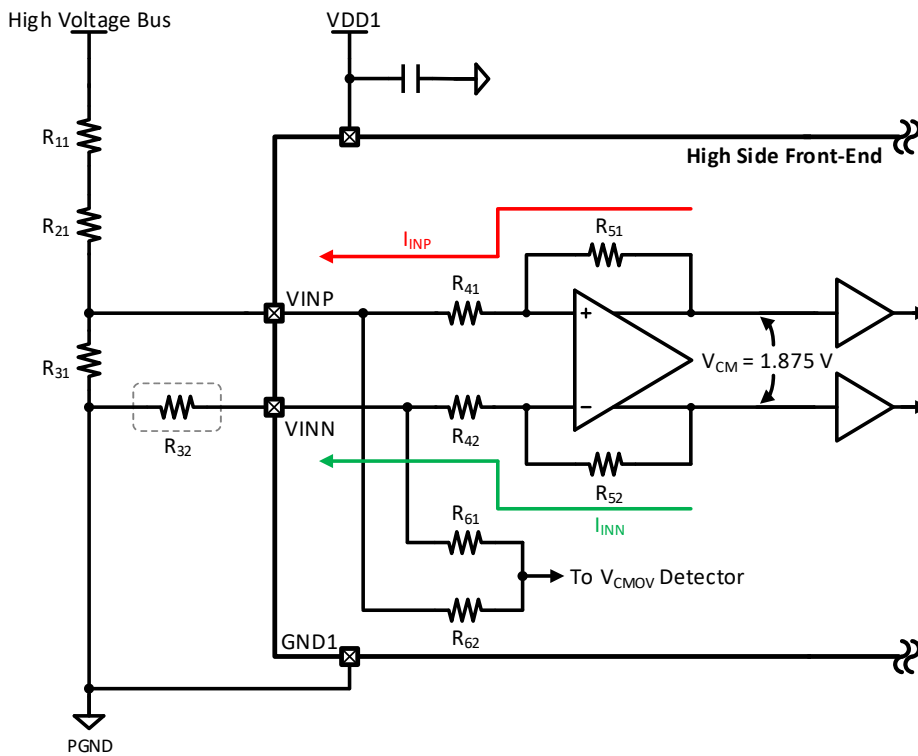


Figure 9-2. Typical Application Circuit for Voltage-Measurement

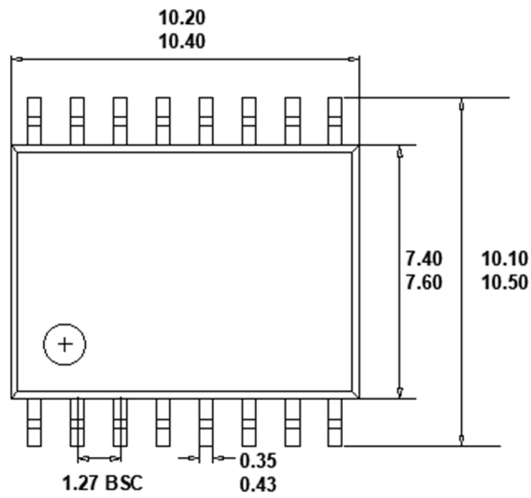
9.3 Power supply and PCB layout

The CA-IS1305x devices require dual power supply to provide supply for analog input-side and digital output-side in the different voltage domain. The supply range of AVDD is 4.5V to 5.5V; for DVDD, the supply range is 3.0V to 5.5V. To reduce system-level cost, the power supply of AVDD can be derived from the system main power supply by using a Zener diode (D_1 in [Figure 9-1](#)) to limit the voltage to 5V ($\pm 10\%$). Alternatively a low-cost low-drop regulator (LDO) can be used to produce a stable supply voltage level for AVDD and minimize noise on the power-supply as well.

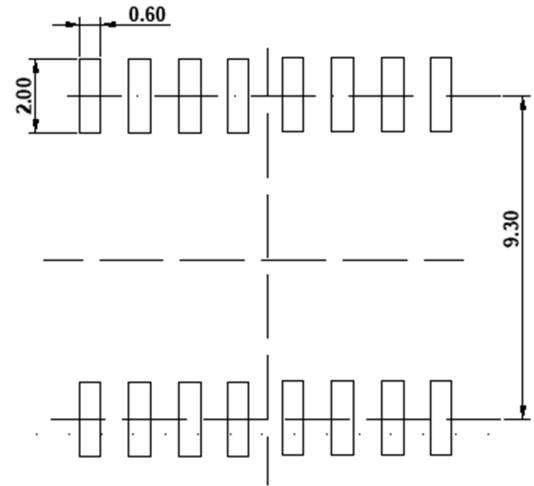
Good layout technique optimizes performance by decreasing the amount of stray capacitance at the high-side, current-sense-amplifier, common-mode inputs etc. Capacitive decoupling across the supply voltage AVDD to AGND(C₂), DVDD to DGND(C₄) of low-ESR 0.1μF is recommended as shown in [Figure 9-1](#). If better filtering is required, an extra bulk capacitor (2.2μF to 10μF) can be added(C₃, C₅). Since the CA-IS1305x devices feature ultra-low input offset voltage, board leakage and thermocouple effects can easily introduce errors in the input offset voltage readings when used with high-impedance signal sources. In order to dissipate sense-resistor heat from large sense currents, solder the AINP and the AINN pins to large copper traces. Keep the part away from other heat-generating devices. For accurate measurement of V_{shunt}, the Kelvin method is recommended. For noisy digital environments, keep digital signals far away from the sensitive analog inputs. The use of a multilayer PCB with separate ground and power-supply planes is recommended.

10 Package Information

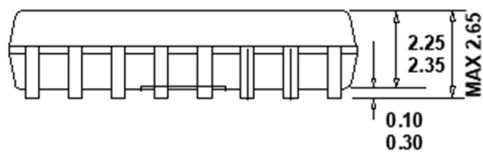
10.1 16-Pin Wide Body SOIC Package



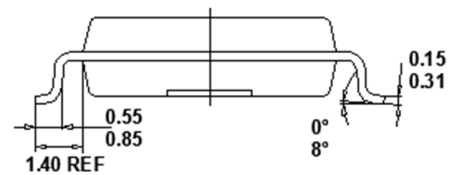
TOP VIEW



RECOMMENDED LAND PATTERN



FRONT VIEW



LEFT SIDE VIEW

Note: All dimensions are shown in millimeters.

11 Soldering Temperature (reflow) Profile

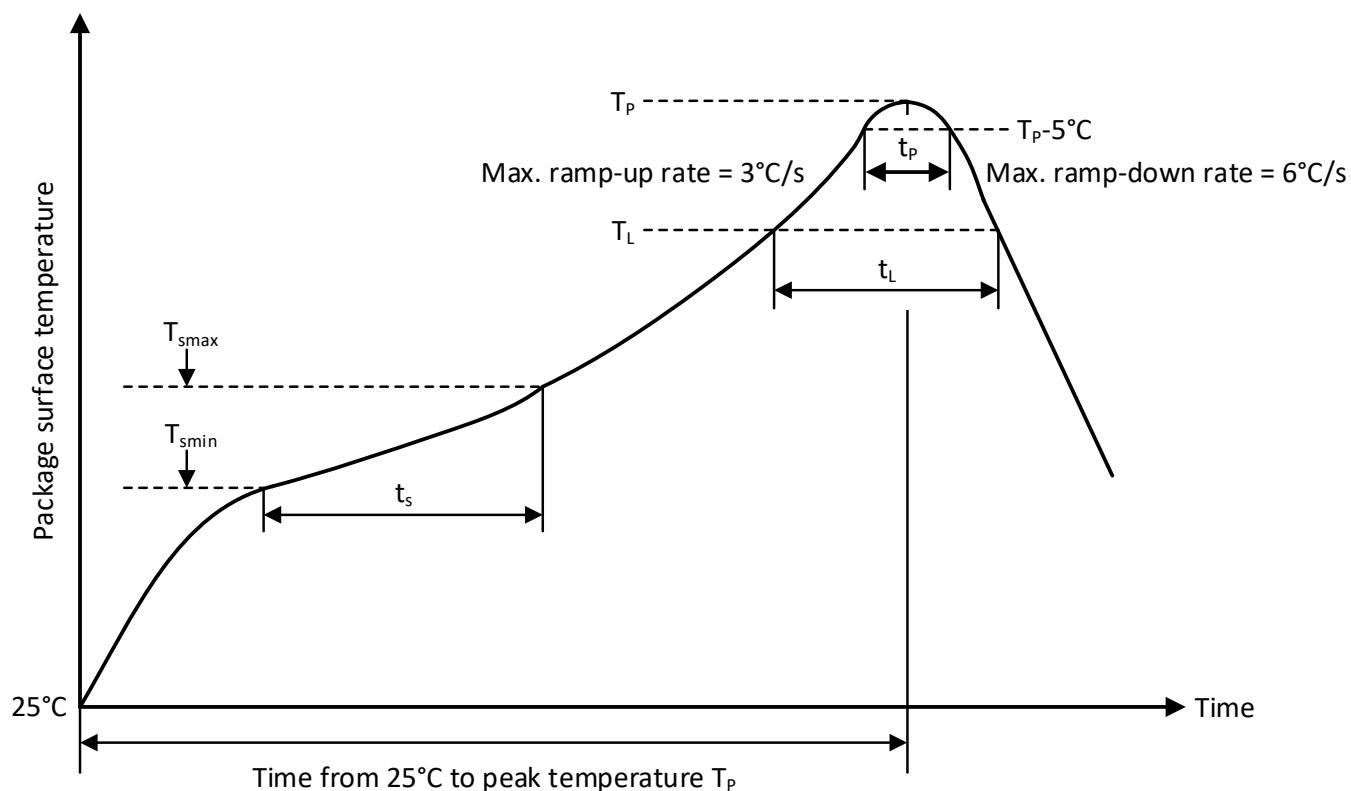


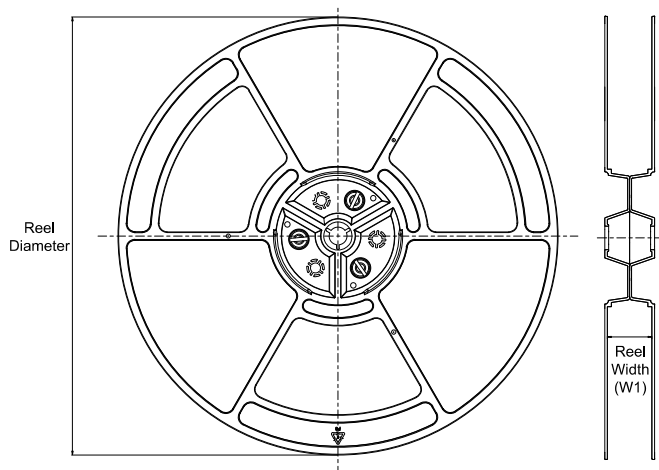
Figure 11-1. Soldering Temperature (reflow) Profile

Table 11-1. Soldering Temperature Parameter

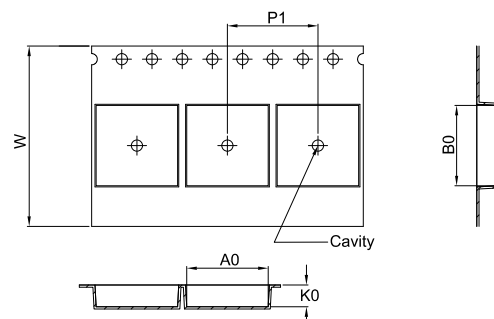
Profile Feature	Pb-Free Soldering
Ramp-up rate ($T_L = 217^\circ\text{C}$ to peak T_P)	3°C/s max
Time t_s of preheat temp ($T_{smin} = 150^\circ\text{C}$ to $T_{smax} = 200^\circ\text{C}$)	60~120 seconds
Time t_L to be maintained above 217°C	60~150 seconds
Peak temperature T_P	260°C
Time t_p within 5°C of actual peak temp	30 seconds max
Ramp-down rate (peak T_P to $T_L = 217^\circ\text{C}$)	6°C/s max
Time from 25°C to peak temperature T_P	8 minutes max

12 Tape and Reel Information

REEL DIMENSIONS

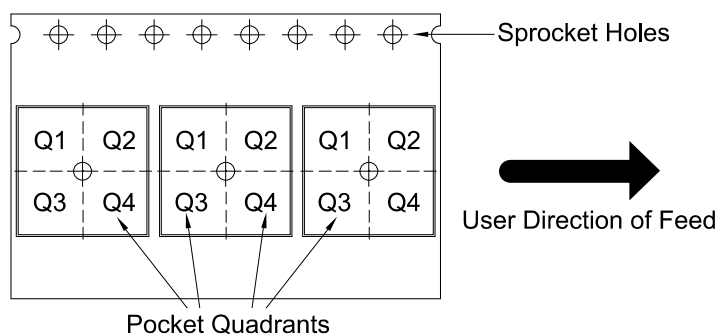


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CA-IS1305M25W	SOIC	W	16	1000	330	16.4	10.8	10.7	2.9	12.0	24.0	Q1
CA-IS1305AM25W	SOIC	W	16	1000	330	16.4	10.8	10.7	2.9	12.0	24.0	Q1

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