

CA-IS1200 Isolated Amplifier for Current Sensing

1 Key Features

- Differential Input Voltage Range: ± 250 mV
- Fixed Initial Gain: 8
- Low Input Offset and Drift: ± 1 mV (max) at 25°C, ± 4 $\mu\text{V}/^\circ\text{C}$ (max)
- Low Gain Error and Drift: $\pm 0.5\%$ (max) at 25°C, ± 50 ppm/ $^\circ\text{C}$ (max)
- Low Nonlinearity and Drift: 0.01% (typ) for Full Scale, ± 1 ppm/ $^\circ\text{C}$ (typ)
- 3.3-V or 5-V Operation for Both High- and Low-Side
- High CMTI: ± 150 kV/ μs (typ)
- Wide Operating Temperature Range: -40°C to 125°C
- Safety-Related Certifications:
 - VDE 0884-17 isolation certification(CA-IS1200G)
 - UL according to UL1577(CA-IS1200G)
 - IEC 61010-1:2010+A1 certifications

2 Applications

- Industrial Motor Controls and Drives
- Isolated Switch Mode Supplies
- Uninterruptible Power Supplies

3 Description

The CA-IS1200 devices are high-precision isolated amplifiers and optimized for shunt-resistor-based current sensing. Low offset and gain error and drift guarantee that measuring accuracy is maintained over the entire operating temperature range.

The CA-IS1200 devices utilize silicon oxide (SiO_2) isolation barriers and support up to $3750\text{-}V_{\text{RMS}}$ (CA-IS1200U) or $5000\text{-}V_{\text{RMS}}$ (CA-IS1200G) galvanic isolation per UL 1577. This technology separates high- and low-voltage domain to protect lower-voltage parts from damage and provides low emissions as well as strong anti-interference capability from magnetic changes. The high common-mode transient

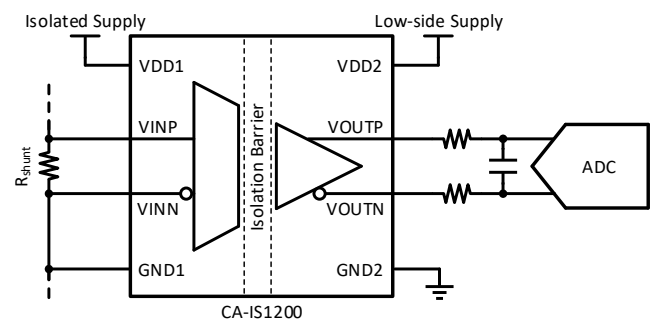
immunity (CMTI) means that the CA-IS1200 devices transmit correct signals through isolation barriers and are suitable for industrial motor controls and drives which require high-voltage and high-power switching. The internal input common-mode overvoltage and missing high-side supply voltage detection functions contribute to fault diagnostics and system safety.

The CA-IS1200 devices are packaged in 8-pin DUB or wide-body SOIC packages and specified over the extended industrial temperature range of -40°C to 125°C .

Device Information

PART NUMBER	PACKAGE	BODY SIZE (NOM)
CA-IS1200U	DUB8 (U)	9.20 mm \times 6.62 mm
CA-IS1200G	SOIC8-WB (G)	5.85 mm \times 7.50 mm

Simplified Schematic



4 Ordering Guide

Table 4-1 Ordering Guide for Valid Ordering Part Number

Ordering Part Number	Specified Input Range	Isolation Rating	Package
CA-IS1200U	± 250 mV	3750 V _{RMS}	DUB8
CA-IS1200G	± 250 mV	5000 V _{RMS}	SOIC8-WB

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5 Revision History

Revision	Description	Rev Date	Page
Version 1.00	NA		NA
Version 1.01	Changed POD and Type reel information	2022/12/20	21, 22, 24
Version 1.02	Update Certification information	2023/09/06	1, 6, 7
Version 1.03	Update TUV and VDE Certification information	2024/04/01	7

6 Pin Descriptions and Functions

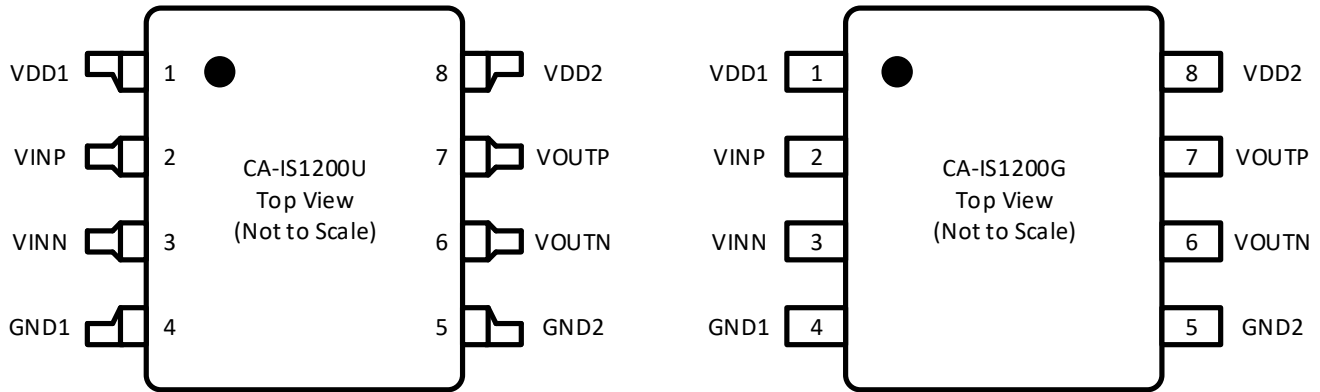


Figure 6-1 CA-IS1200 Top View

Table 6-1 CA-IS1200 Pin Description and Functions

NAME	PIN NUMBER	TYPE	DESCRIPTION
VDD1	1	Power	High-side power supply, 3 V to 5.5 V
VINP	2	Input	Noninverting analog input
VINN	3	Input	Inverting analog input
GND1	4	Ground	High-side ground
GND2	5	Ground	Low-side ground
VOUTN	6	Output	Inverting analog output
VOUTP	7	Output	Noninverting analog output
VDD2	8	Power	Low-side power supply, 3 V to 5.5 V

7 Specifications

7.1 Absolute Maximum Ratings¹

PARAMETER		MIN	MAX	UNIT
VDD1, VDD2	Supply voltage ²	-0.5	6.5	V
VINP, VINN	Analog input voltage	GND1 - 6	6.5	V
VOU TP, VOU TN	Analog output voltage	GND2 - 0.5	VDD2 + 0.5 ³	V
I _{IN}	Input current to any pin except supply pins	-10	10	mA
T _J	Junction Temperature		150	°C
T _{STG}	Storage Temperature	-65	150	°C

NOTE:

1. Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. All voltage values are with respect to the local ground terminal (GND1 or GND2) and are peak voltage values.
3. Maximum voltage must not exceed 6.5 V.

7.2 ESD Ratings

		VALUE	UNIT
V _{ESD} Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins	±4000	V
	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins	±2000	

7.3 Recommended Operating Conditions

PARAMETER		MIN	NOM	MAX	UNIT
VDD1	High-side supply voltage, with respect to GND1	3.0	5.0	5.5	V
VDD2	Low-side supply voltage, with respect to GND2	3.0	3.3	5.5	V
T _A	Ambient Temperature	-40		125	°C

7.4 Thermal Information

THERMAL METRIC		VALUE (U)	VALUE (G)	UNIT
R _{θJA}	Junction-to-ambient thermal resistance	73.3	110.1	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	63.2	51.7	°C/W
R _{θJB}	Junction-to-board thermal resistance	43.0	66.4	°C/W
ψ _{JT}	Junction-to-top characterization parameter	27.4	16.0	°C/W
ψ _{JB}	Junction-to-board characterization parameter	42.7	64.5	°C/W
R _{θJC(bottom)}	Junction-to-case (bottom) thermal resistance	NA	NA	°C/W

7.5 Power Ratings

PARAMETER		TEST CONDITIONS	VALUE	UNIT
P _D	Maximum power dissipation for both sides	VDD1 = VDD2 = 5.5 V	129.25	mW
		VDD1 = VDD2 = 3.6 V	76.32	
P _{D1}	Maximum power dissipation for high-side	VDD1 = 5.5 V	85.25	mW
		VDD1 = 3.6 V	50.40	
P _{D2}	Maximum power dissipation for low-side	VDD2 = 5.5 V	44.00	mW
		VDD2 = 3.6 V	25.92	

7.6 Insulation Specifications

PARAMETR		TEST CONDITIONS	VALUE (U)	VALUE (G)	UNIT
CLR	External clearance ¹	Shortest terminal-to-terminal distance through air	6.1	8	mm
CPG	External creepage ¹	Shortest terminal-to-terminal distance across the package surface	6.8	8	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	28	28	μm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	> 600	> 600	V
	Material group	According to IEC 60664-1	I	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 150 V _{RMS}	I-IV	I-IV	
		Rated mains voltage ≤ 300 V _{RMS}	I-III	I-IV	
		Rated mains voltage ≤ 600 V _{RMS}	N/A	I-IV	
		Rated mains voltage ≤ 1000 V _{RMS}	N/A	I-III	
DIN V VDE V 0884-17:2021-10²					
V _{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	566	1414	V _{PK}
V _{IOWM}	Maximum working isolation voltage	AC voltage; Time dependent dielectric breakdown (TDDB) Test	400	1000	V _{RMS}
		DC voltage	566	1414	V _{DC}
V _{IOTM}	Maximum transient isolation voltage	V _{TEST} = V _{IOTM} , t = 60 s (qualification); V _{TEST} = 1.2 × V _{IOTM} , t = 1 s (100% production)	5300	7070	V _{PK}
V _{IOSM}	Maximum surge isolation voltage ³	Test method per IEC 62368-1, 1.2/50 μs waveform, V _{TEST} = 1.6 × V _{IOSM} (qualification) (G) V _{TEST} = 1.3 × V _{IOSM} (qualification) (U)	4070	8000	V _{PK}
q _{pd}	Apparent charge ⁴	Method a, After input/output safety test subgroup 2/3, V _{ini} = V _{IOTM} , t _{ini} = 60 s; V _{pd(m)} = 1.2 × V _{IORM} , t _m = 10 s	≤ 5	≤ 5	pC
		Method a, After environmental tests subgroup 1, V _{ini} = V _{IOTM} , t _{ini} = 60 s; V _{pd(m)} = 1.6 × V _{IORM} , t _m = 10 s	≤ 5	≤ 5	
		Method b1, At routine test (100% production) and preconditioning (type test) V _{ini} = 1.2 × V _{IOTM} , t _{ini} = 1 s; V _{pd(m)} = 1.875 × V _{IORM} , t _m = 1 s (G) V _{pd(m)} = 1.5 × V _{IORM} , t _m = 1 s (U)	≤ 5	≤ 5	
C _{IO}	Barrier capacitance, input to output ⁵	V _{IO} = 0.4 × sin(2πft), f = 1 MHz	~ 1	~ 1	pF
R _{IO}	Isolation resistance ⁵	V _{IO} = 500 V, T _A = 25°C	> 10 ¹²	> 10 ¹²	Ω
		V _{IO} = 500 V, 100°C ≤ T _A ≤ 125°C	> 10 ¹¹	> 10 ¹¹	
		V _{IO} = 500 V at T _S = 150°C	> 10 ⁹	> 10 ⁹	
	Pollution degree		2	2	
UL 1577					
V _{ISO}	Maximum withstanding isolation voltage	V _{TEST} = V _{ISO} , t = 60 s (qualification), V _{TEST} = 1.2 × V _{ISO} , t = 1 s (100% production)	3750	5000	V _{RMS}
NOTE:					
<ol style="list-style-type: none"> Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications. This coupler is suitable for safe electrical insulation only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits. Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier. Apparent charge is electrical discharge caused by a partial discharge (pd). All pins on each side of the barrier tied together creating a two-terminal device. 					

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7.7 Safety-Related Certifications

VDE	UL	TUV	CQC
Certified according to DIN EN IEC 60747-17 (VDE 0884-17):2021-10; EN IEC 60747-17:2020+AC:2021	Recognized under UL 1577 Component Recognition Program and CSA Component Acceptance Service Notice No. 5A	Certified according to EN 61010-1: 2010+A1	Certified according to GB 4943.1-2022
Maximum repetitive peak isolation voltage: 1414 V _{PK} (SOIC8-WB) and 566 V _{PK} (DUB8) 1414 V _{PK} (DUB8 under certification) Maximum transient isolation voltage: 7070 V _{PK} (SOIC8-WB) and 5300 V _{PK} (DUB8) Maximum surge isolation voltage: 8000 V _{PK} (SOIC8-WB) and 4070 V _{PK} (DUB8) 6250 V _{PK} (DUB8 under certification)	Single protection SOIC8-WB: 5000 V _{RMS} DUB8: 3750 V _{RMS}	SOIC8-WB: 5000 V _{RMS} DUB8: 3750 V _{RMS}	SOIC8-WB: Reinforced insulation (Altitude ≤ 5000 m)
Certification Number: 40052786 (Basic insulation) 40057278 (Reinforced insulation)	Certification Number: E511334	Certification Number: AK 505918190001	Certificate number: SOIC8-WB:CQC24001434134

7.8 Electrical Characteristics

All minimum and maximum specifications apply from $T_A = -40^{\circ}\text{C}$ to 125°C , $V_{DD1} = 3\text{ V}$ to 5.5 V , $V_{DD2} = 3\text{ V}$ to 5.5 V , $V_{INP} = -250\text{ mV}$ to 250 mV , and $V_{INN} = \text{GND1} = 0\text{ V}$ (unless otherwise noted). All typical specifications are at $T_A = 25^{\circ}\text{C}$, $V_{DD1} = 5\text{ V}$, and $V_{DD2} = 3.3\text{ V}$ (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUT						
V_{Clipping}	Maximum input voltage before clipping output	$V_{\text{INP}} - V_{\text{INN}}$		± 320		mV
V_{FSR}	Specified linear full-scale input range	$V_{\text{INP}} - V_{\text{INN}}$	-250		250	mV
V_{CM}	Operating common-mode input voltage	$(V_{\text{INP}} + V_{\text{INN}}) / 2$ to GND1	-0.16		$V_{\text{DD1}} - 2.1$	V
V_{CMOV}	Common-mode overvoltage threshold	$(V_{\text{INP}} + V_{\text{INN}}) / 2$ to GND1	$V_{\text{DD1}} - 2$			V
$V_{\text{CMOV_HYS}}$	Hysteresis of common-mode overvoltage threshold			100		mV
V_{OS}	Input offset voltage	Initial, at $T_A = 25^{\circ}\text{C}$, $V_{\text{INP}} = V_{\text{INN}} = \text{GND1}$	-1	± 0.05	1	mV
TCV_{OS}	Input offset voltage drift		-4	± 1	4	$\mu\text{V}/^{\circ}\text{C}$
CMRR_{IN}	Input common-mode rejection ratio	DC, $V_{\text{INP}} = V_{\text{INN}}$		-98		dB
		$f_{\text{IN}} = 10\text{ kHz}$, $V_{\text{INP}} = V_{\text{INN}}$		-98		
C_{IN}	Single-ended input capacitance	$f_{\text{IN}} = 275\text{ kHz}$, $V_{\text{INN}} = \text{GND1}$		2		pF
C_{IND}	Differential input capacitance	$f_{\text{IN}} = 275\text{ kHz}$		1		pF
R_{IN}	Single-ended input resistance	$V_{\text{INN}} = \text{GND1}$		19		k Ω
R_{IND}	Differential input resistance			22		k Ω
I_{IN}	Input current	$V_{\text{INP}} = V_{\text{INN}} = \text{GND1}$, $I_{\text{IN}} = (I_{\text{INP}} + I_{\text{INN}}) / 2$	-41	-30	-24	μA
TCI_{IN}	Input current drift			± 1		nA/ $^{\circ}\text{C}$
I_{INOS}	Input offset current			± 5		nA
BW_{IN}	Input bandwidth			1000		kHz
ANALOG OUTPUT						
	Gain ¹	Initial, at $T_A = 25^{\circ}\text{C}$		8		V/V
E_{G}	Gain error	Initial, at $T_A = 25^{\circ}\text{C}$	-0.5%	$\pm 0.05\%$	0.5%	
TCE_{G}	Gain error drift		-50	± 15	50	ppm/ $^{\circ}\text{C}$
NL	Nonlinearity ²		-0.03%	$\pm 0.01\%$	0.03%	
TCNL	Nonlinearity drift			± 1		ppm/ $^{\circ}\text{C}$
	Output noise	$V_{\text{INP}} = V_{\text{INN}} = \text{GND1}$, $\text{BW} = 100\text{ kHz}$		330		μV_{RMS}
THD	Total harmonic distortion	$V_{\text{IN}} = 500\text{ mV}_{\text{pp}}$, $f_{\text{IN}} = 10\text{ kHz}$, $\text{BW} = 100\text{ kHz}$		-85		dB
SNR	Signal-to-noise ratio	$V_{\text{IN}} = 500\text{ mV}_{\text{pp}}$, $f_{\text{IN}} = 1\text{ kHz}$, $\text{BW} = 10\text{ kHz}$		83		dB
		$V_{\text{IN}} = 500\text{ mV}_{\text{pp}}$, $f_{\text{IN}} = 10\text{ kHz}$, $\text{BW} = 100\text{ kHz}$		68		
PSRR	Power supply rejection ratio ³	At V_{DD1} , DC		-100		dB
		At V_{DD1} , 100-mV and 10-kHz ripple		-90		
		At V_{DD2} , DC		-100		
		At V_{DD2} , 100-mV and 10-kHz ripple		-98		
V_{CMOUT}	Common-mode output voltage		1.39	1.45	1.51	V
V_{FAILSAFE}	Fail-safe differential output voltage	$V_{\text{CMOV}} \leq V_{\text{CM}}$ or V_{DD1} missing		-2.53	-2.43	V
I_{OSC}	Output short-circuit current	VOUTP or VOUTN shorts to V_{DD2} or GND2		± 13		mA
R_{OUT}	Output resistance	On VOUTP or VOUTN		< 0.2		Ω
BW_{OUT}	Output bandwidth (-3 dB)		250	310		kHz
CMTI	Common-mode transient immunity	$ \text{GND1} - \text{GND2} = 1.5\text{ kV}$; <i>See Figure 8-1</i>	100	150		kV/ μs
POWER SUPPLY						
V_{DDUV}	VDD undervoltage threshold	V_{DD1} or V_{DD2} rising		2.5	2.7	V

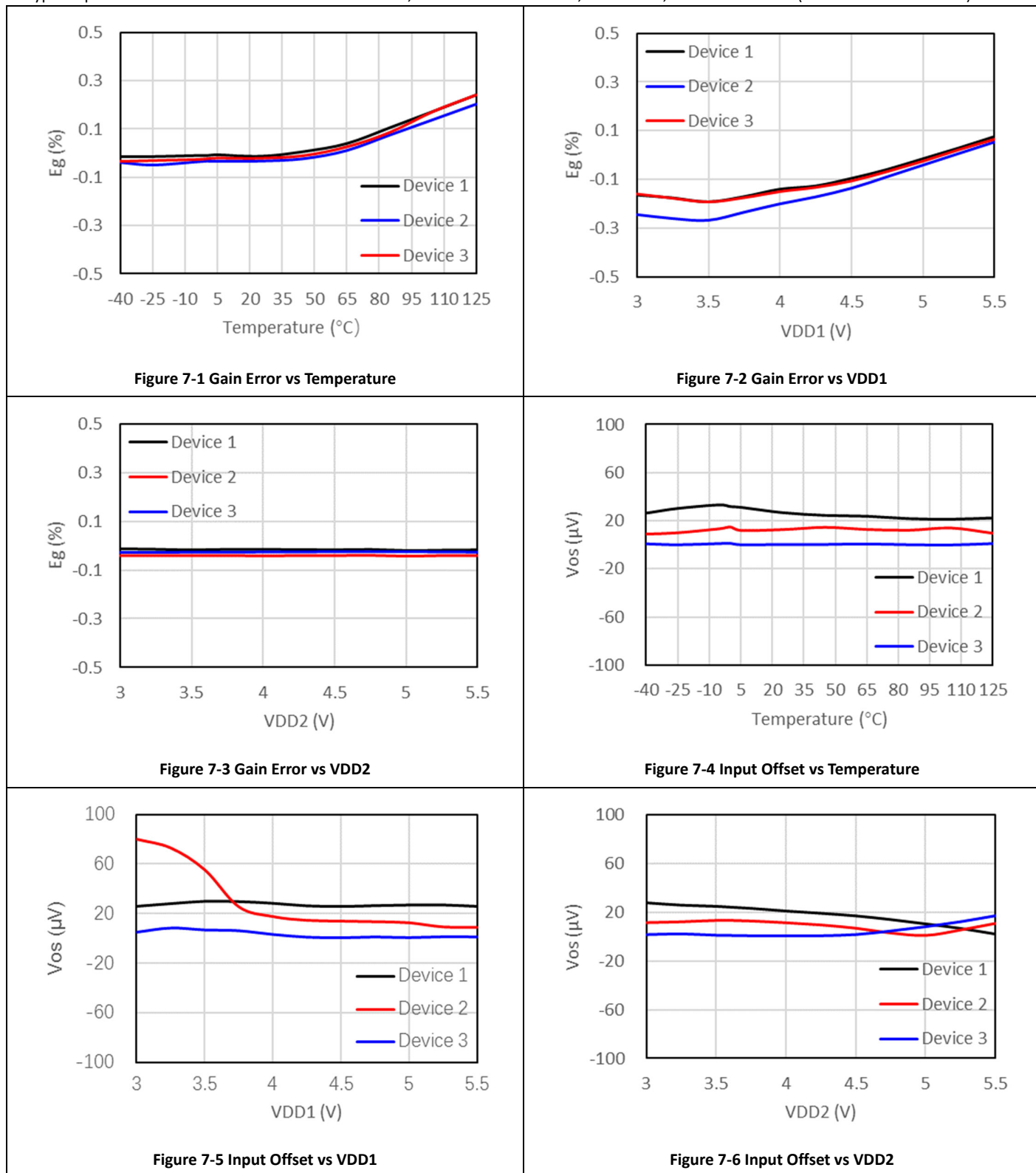
IDD1	High-side supply current	3.0 V ≤ VDD1 ≤ 3.6 V	9.3	14.0	mA
		4.5 V ≤ VDD1 ≤ 5.5 V	10.7	15.5	
IDD2	Low-side supply current	3.0 V ≤ VDD2 ≤ 3.6 V	5.2	7.2	mA
		4.5 V ≤ VDD2 ≤ 5.5 V	5.7	8.0	
t _r	Rise time of VOUT (10% – 90%)	VINP = 0 to 0.25 V step; <i>See Figure 8-2</i>	1.2		μs
t _f	Fall time of VOUT (90% – 10%)	VINP = 0.25 V to 0 step; <i>See Figure 8-2</i>	1.2		μs
t _{PD}	VIN to VOUT signal delay (50% – 50%)	Output unfiltered; <i>See Figure 8-3</i>	1.5	2.1	μs
t _{AS}	Analog settling time	VDD1 = 0 to 3 V step and 3.0 V ≤ VDD2, to VOUT valid (0.1% settling)	500		μs

NOTE:

1. The gain is defined as the slope of the optimum line derived by the method of least squares between differential input voltage (VINP – VINN) and differential output voltage (VOUTP – VOUTN) over the specified input range.
2. Nonlinearity is defined as a fraction of the half of the peak-to-peak value of differential output voltage deviation divided by the full-scale differential output voltage.
3. This parameter is input referred.

7.9 Typical Characteristics

All typical specifications are at $V_{INP} = -250\text{ mV to }250\text{ mV}$, and $V_{INN} = GND1 = 0\text{ V}$, $V_{DD1} = 5\text{ V}$, and $V_{DD2} = 3.3\text{ V}$ (unless otherwise noted).



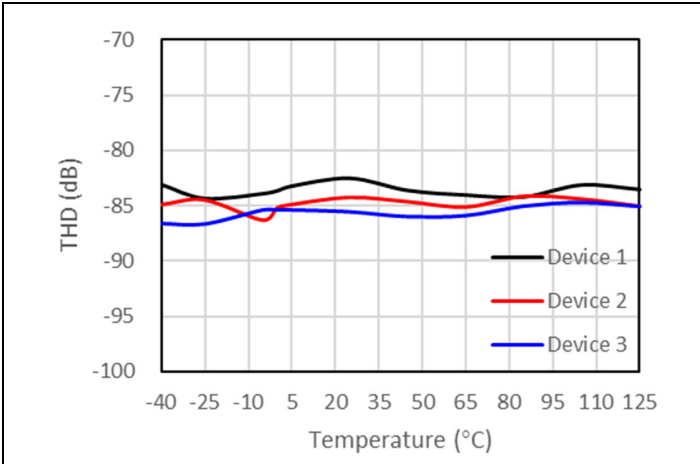


Figure 7-7 Total Harmonic Distortion vs Temperature @ $f_{IN} = 10$ kHz

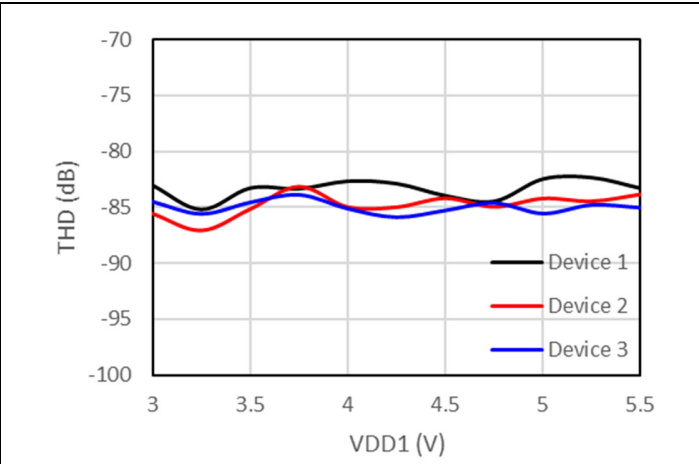


Figure 7-8 Total Harmonic Distortion vs VDD1 @ $f_{IN} = 10$ kHz

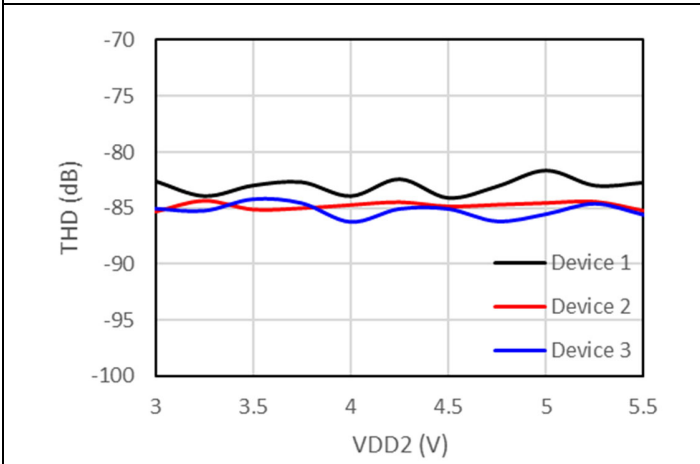


Figure 7-9 Total Harmonic Distortion vs VDD2 @ $f_{IN} = 10$ kHz

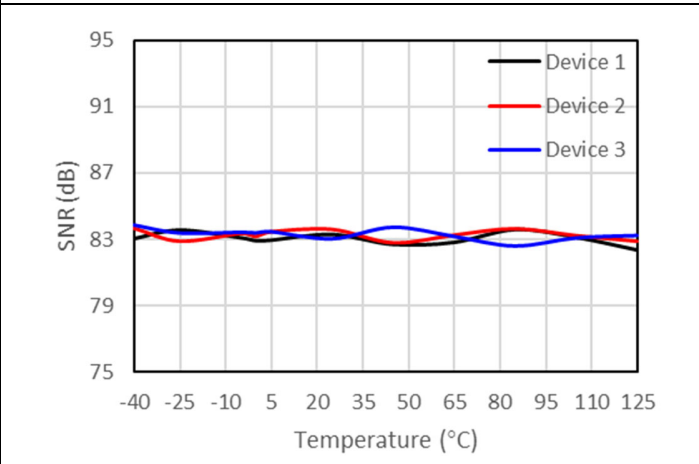


Figure 7-10 SNR vs Temperature @ $f_{IN} = 1$ kHz

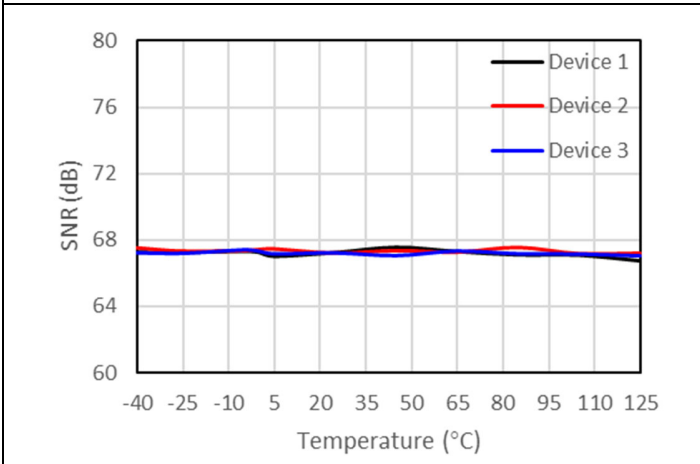


Figure 7-11 SNR vs Temperature @ $f_{IN} = 10$ kHz

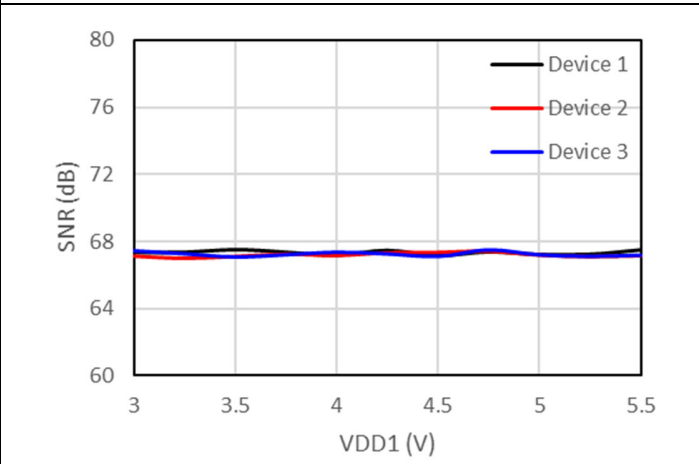
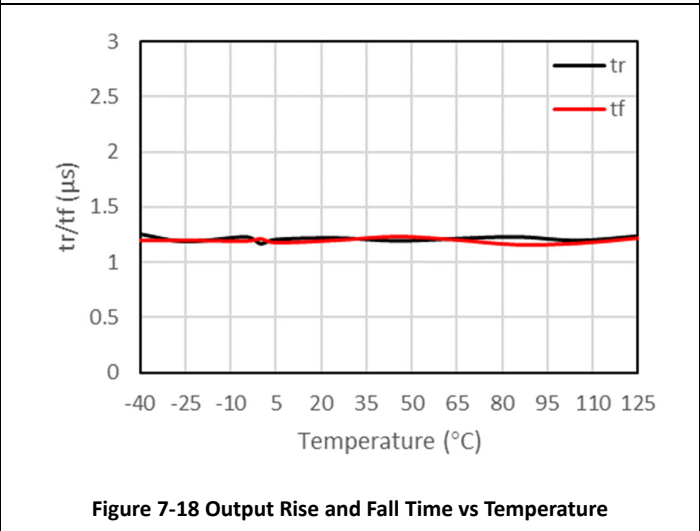
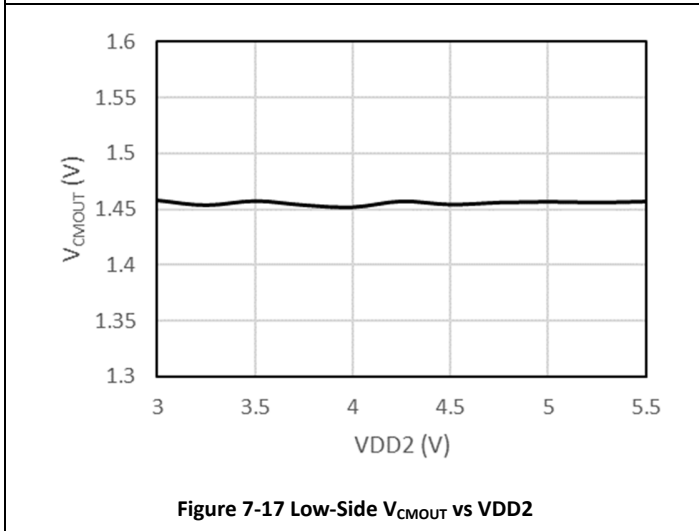
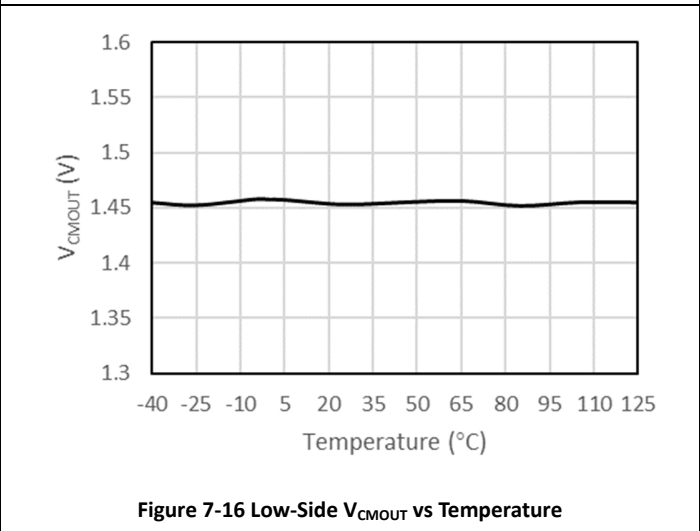
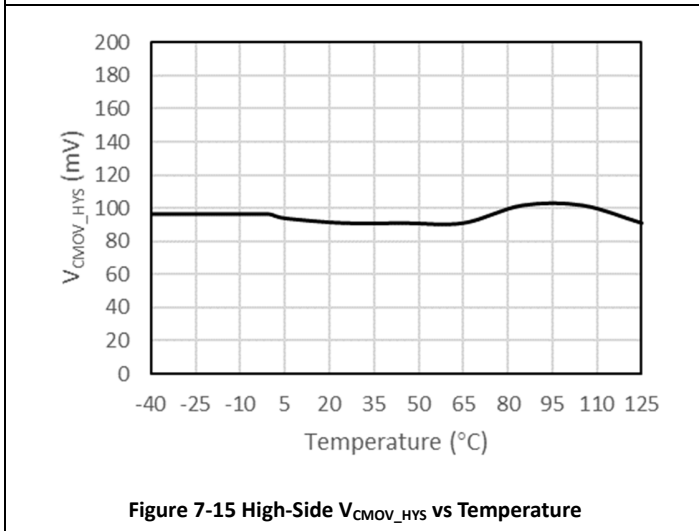
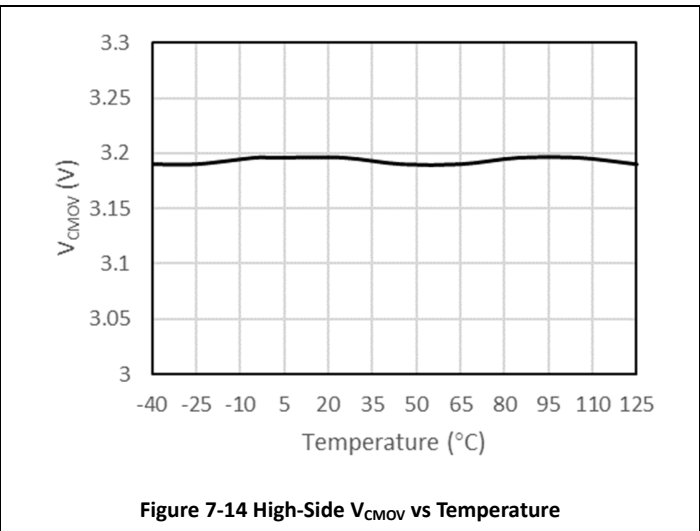
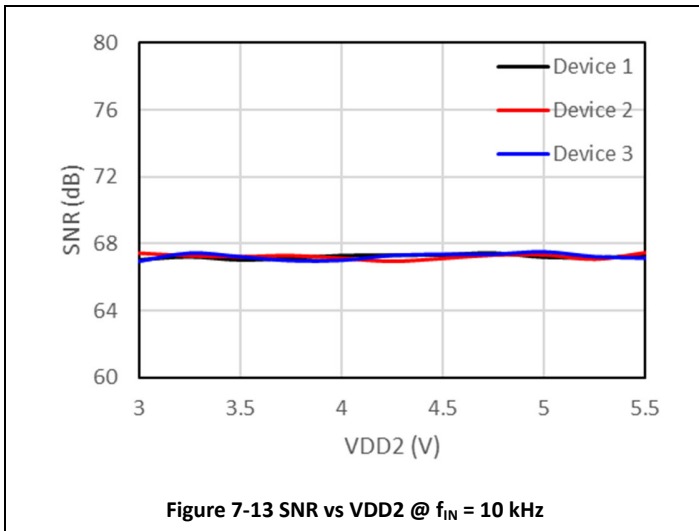
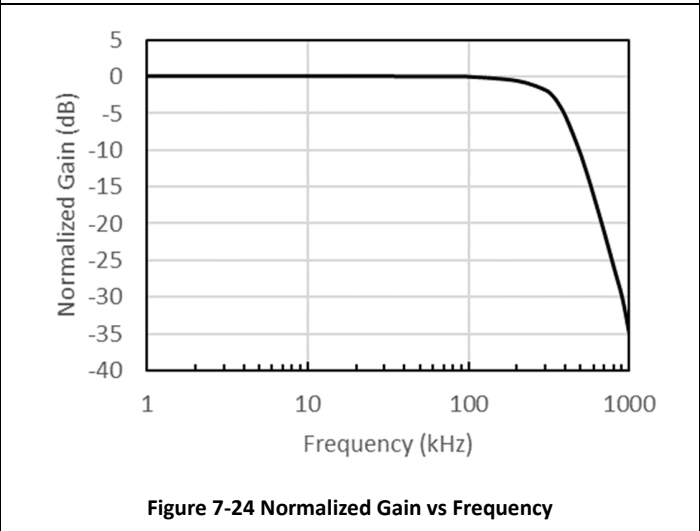
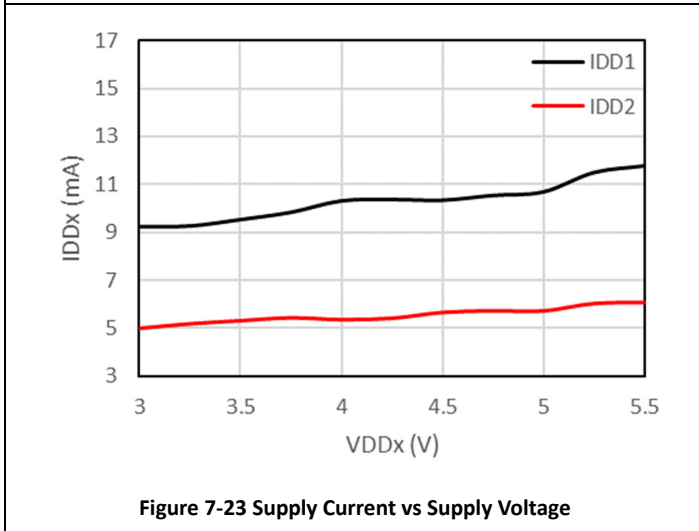
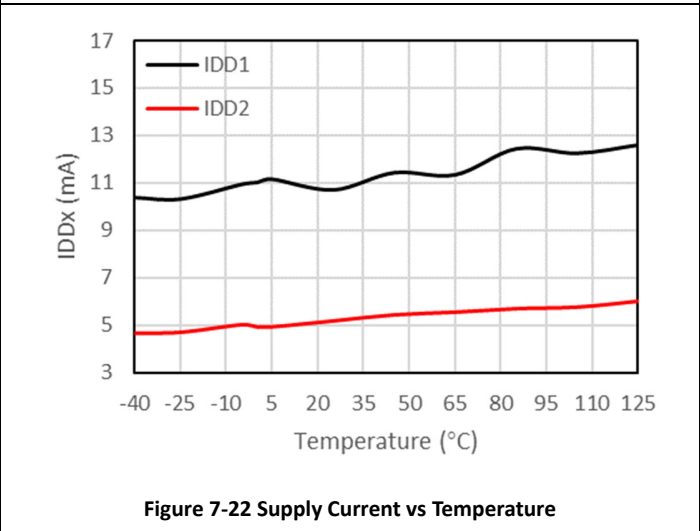
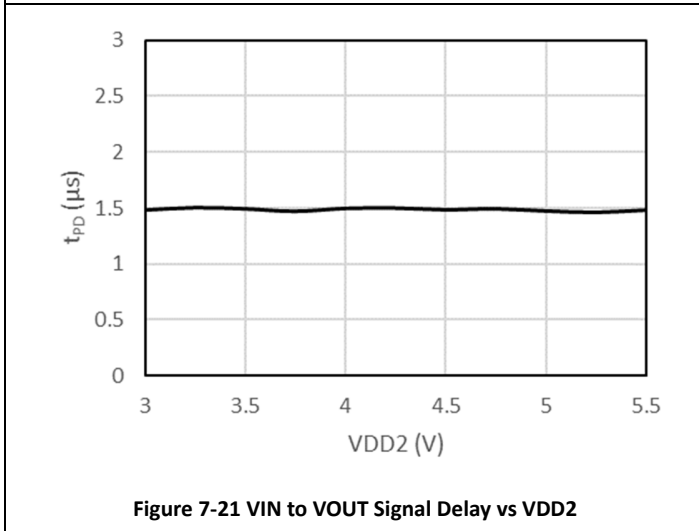
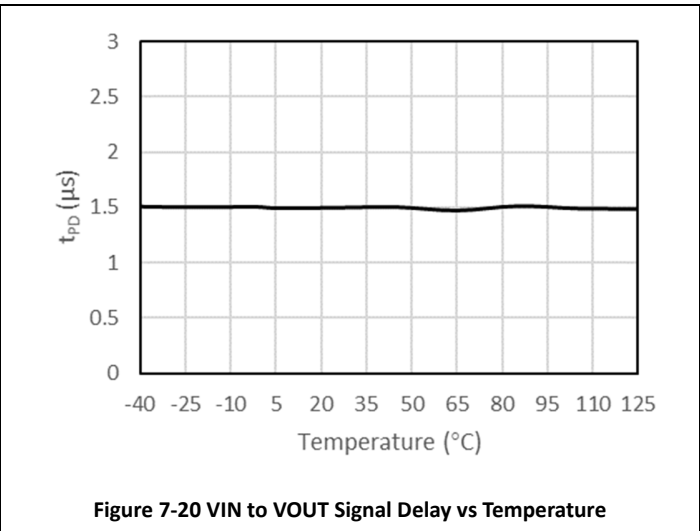
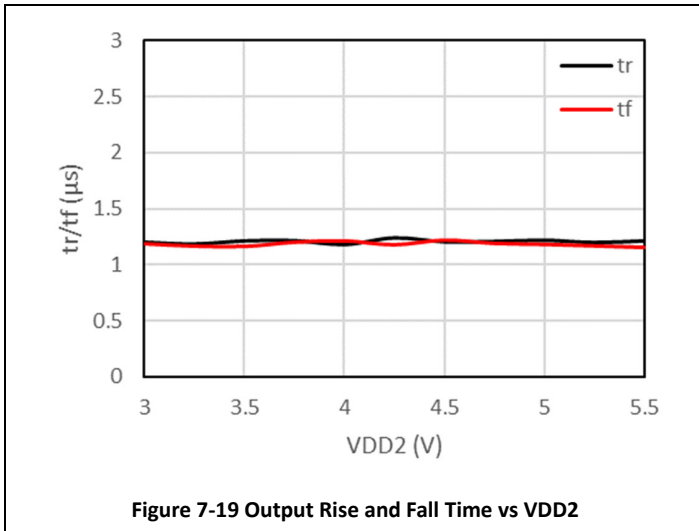
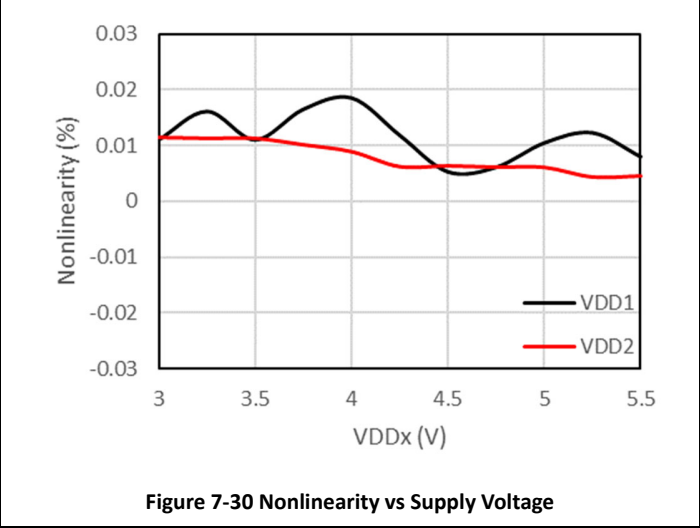
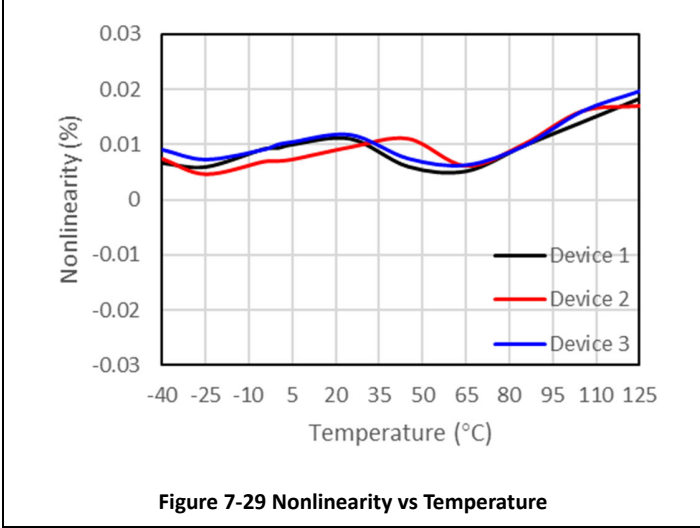
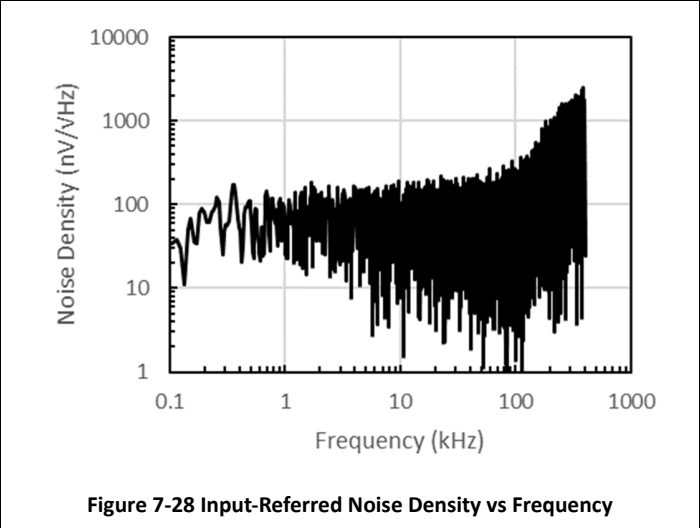
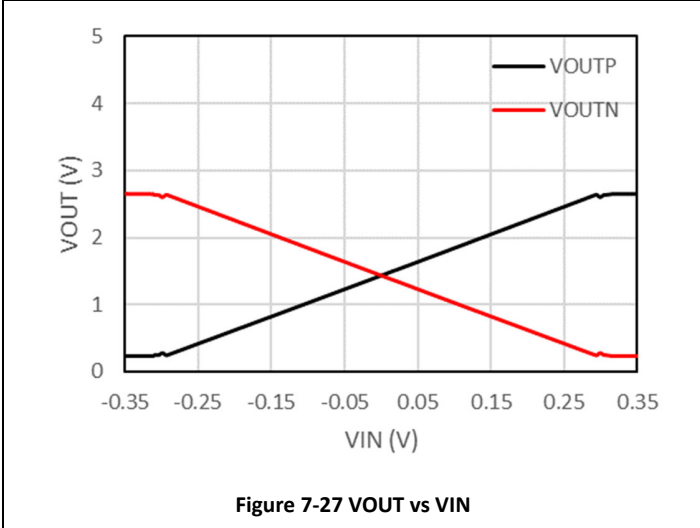
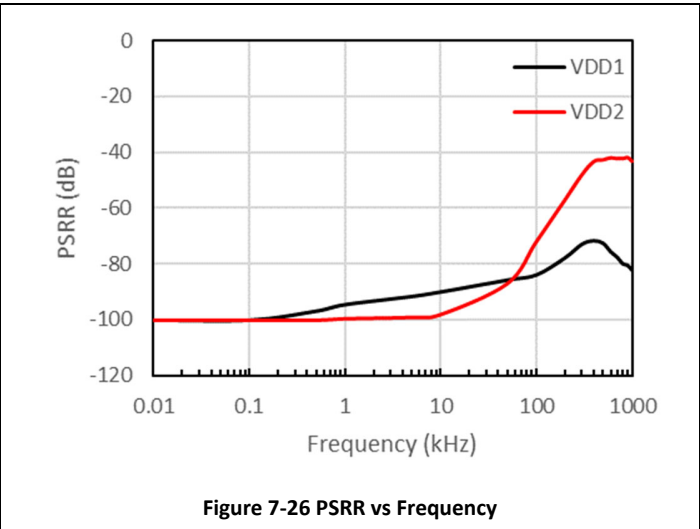
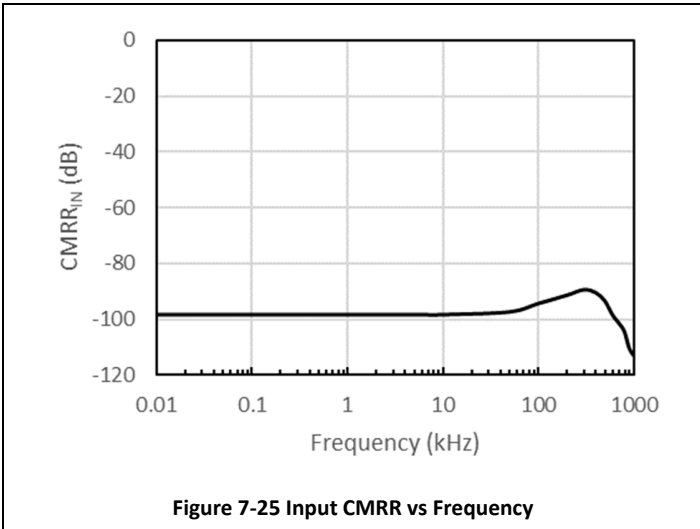


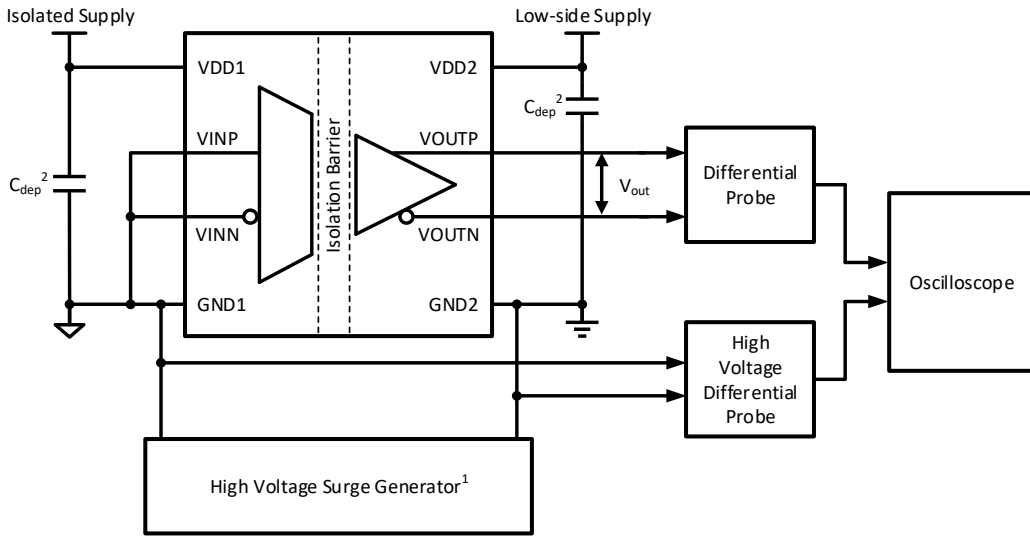
Figure 7-12 SNR vs VDD1 @ $f_{IN} = 10$ kHz







8 Parameter Measurement Information



- Note:**
1. The High Voltage Surge Generator generates repetitive high voltage surges with > 1 kV amplitude and < 10 ns rise time or fall time to generate common-mode transient noise with > 150 kV/μs slew rate.
 2. C_{dep} is the 0.1~1 μF decoupling capacitor.

Figure 8-1 Common-Mode Transient Immunity Test Circuit

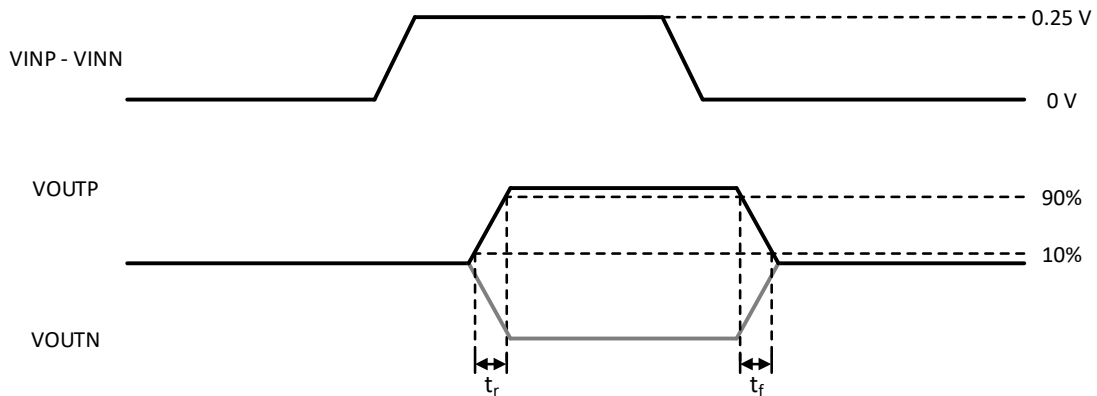


Figure 8-2 Rise and Fall Time Test Waveforms

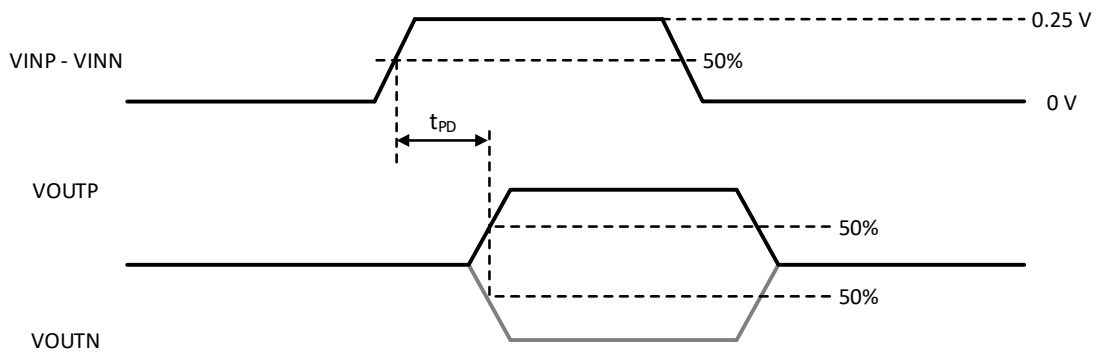


Figure 8-3 Delay Time Test Waveforms

9 Detailed Description

9.1 System Overview

The CA-IS1200 devices are high-precision isolated amplifiers designed for shunt-resistor-based current sensing. The functional block diagram of this device is shown in Figure 9-1. At high side, the fully differential amplifier pre-amplifies the measuring voltage across a shunt resistor and then drives a 2nd-order Sigma-Delta ($\Sigma\Delta$) modulator. This modulator converts the analog signal to a digital bitstream. For transmission across the SiO₂-based isolation barrier, the digital stream is further modulated with a high-frequency carrier using a simple on-off keying (OOK) modulation scheme. The receiver (RX) recovers the modulated signal to the original digital bitstream at low side. After processed by a 1-bit digital-to-analog converter (DAC), the digital bitstream is sent to an active low-pass filter to produce the analog output. For synchronization of the whole chip, the clock is generated at low side and sent back to high side ensuring that all clocks come from one source.

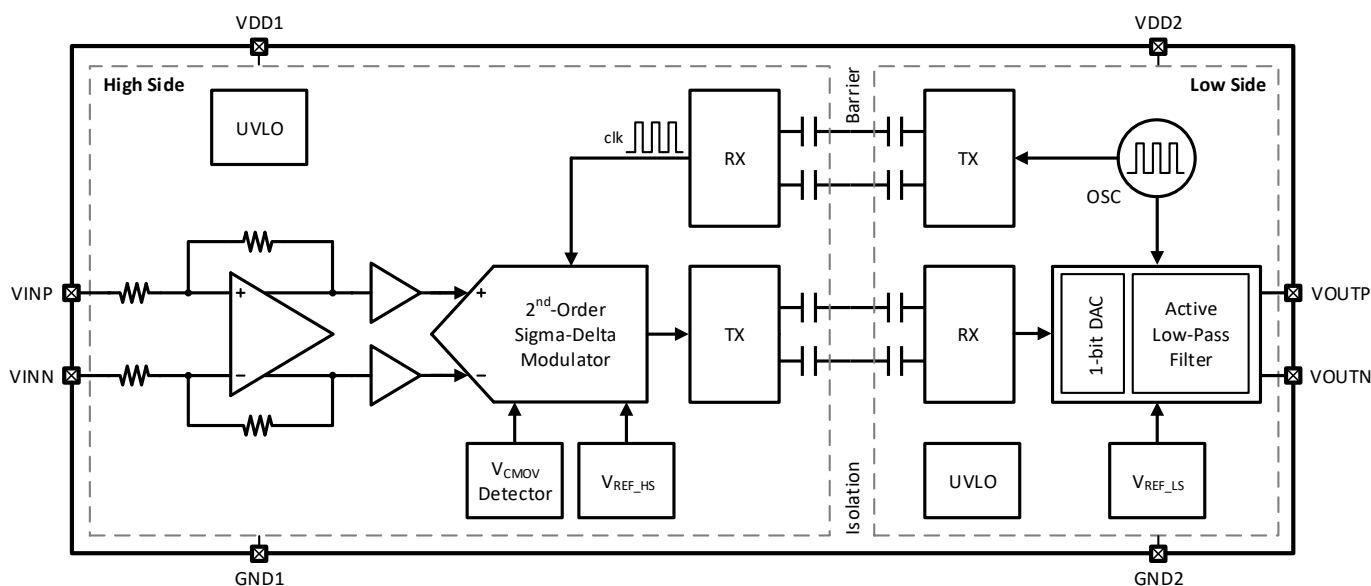


Figure 9-1 Functional Block Diagram of CA-IS1200

9.2 Feature Description

9.2.1 Analog Input

The CA-IS1200 device utilizes a fully differential amplifier stage to pre-amplify the measuring voltage across the shunt resistor. The nominal gain of the front-end differential amplifier is 4, contributing part of the total gain and ensuring that the 2nd-order Sigma-Delta modulator is not saturated when the analog input is within the specific input voltage range. This gain is set by the internal high-precision resistor network. The tens-of-several-k Ω input resistance means it can bring in more gain error and offset if CA-IS1200 devices are applied in measurement where the input signal sources are high-impedance (refer to [Error Analysis in Voltage Sensing](#) for detailed information).

The ESD structure of CA-IS1200 supports the absolute maximum analog input voltage (with respect to GND1) to range from GND1 – 6 V to VDD1 + 0.5 V. To guarantee the long-term reliability and device performance, the differential analog input voltage and the input common-mode voltage of CA-IS1200 must be kept within the specific range.

9.2.2 Signal Transmission Across Isolation Barrier

The CA-IS1200 devices utilize a simple on-off keying (OOK) modulation scheme to transmit the digital bitstream across the SiO₂-based isolation barrier which supports up to 3750-V_{RMS} (CA-IS1200U) or 5000-V_{RMS} (CA-IS1200G) galvanic isolation between high- and low-voltage domain. The block diagram of an isolation channel is shown in Figure 9-2. As shown in Figure 9-3, the transmitter (TX) modulates the digital bitstream with a high-frequency carrier when the signal is HIGH while sends no signal

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when the signal is LOW. The receiver (RX) demodulates the signal across the isolation barrier and reproduces the digital bitstream faithfully. The isolation channel adopts fully differential capacitive-coupled structure which is insensitive to common-mode transient noises, thus the CMTI performance can be maximized. This structure and related circuitry also provide low emissions and strong anti-interference capability from magnetic changes.

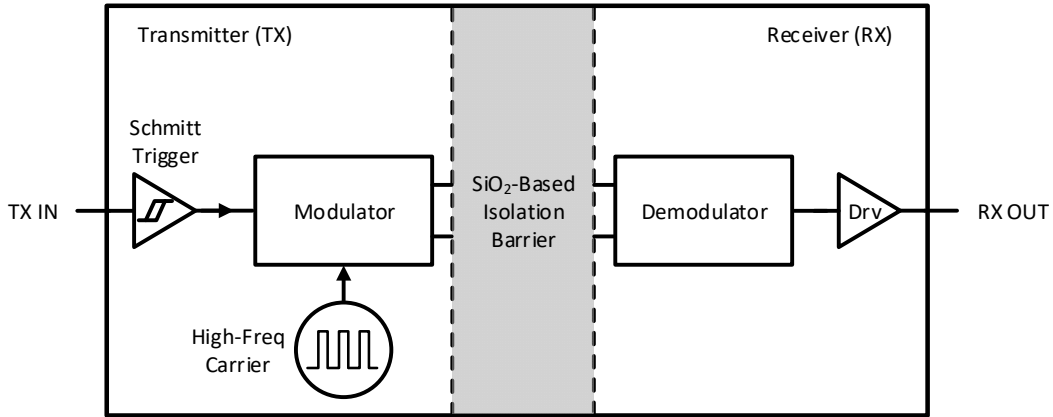


Figure 9-2 Block Diagram of an Isolation Channel

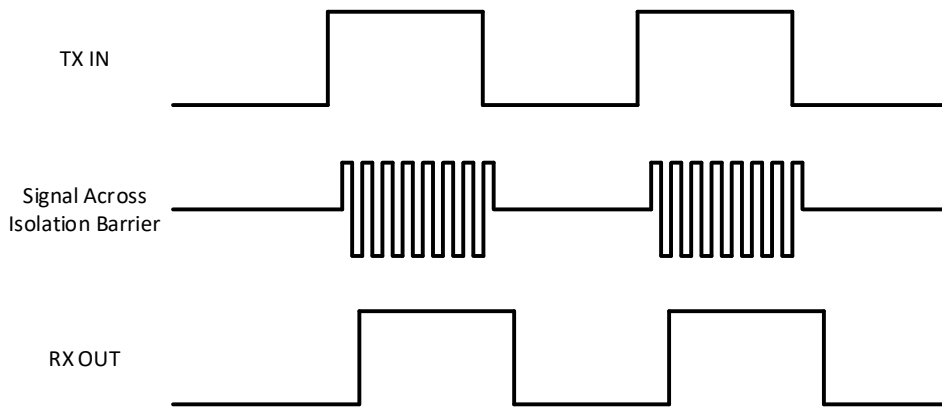


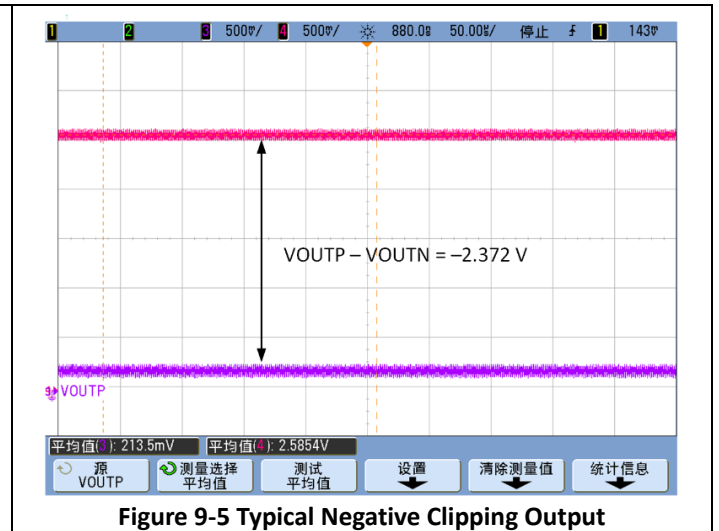
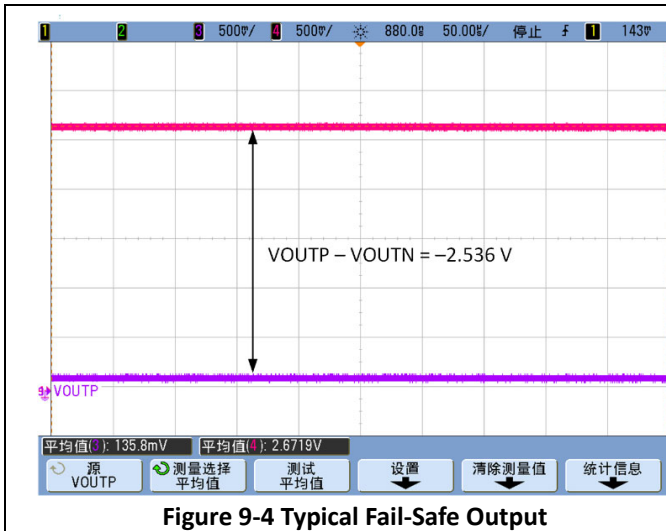
Figure 9-3 Conceptual Operation Waveforms of OOK Modulation Scheme

9.2.3 Fail-Safe Output

The CA-IS1200 devices have fail-safe output function which is activated in two conditions:

- The high-side power supply is missing;
- The common-mode input voltage V_{CM} exceeds the common-mode overvoltage threshold V_{CMOV} .

As shown in Figure 9-4 and Figure 9-5, the fail-safe output is a more negative differential output voltage which can be distinguished from the negative clipping output voltage. This function contributes to fault diagnostics and system safety.



10 Application and Implementation

10.1.1 Typical Application for Current Sensing

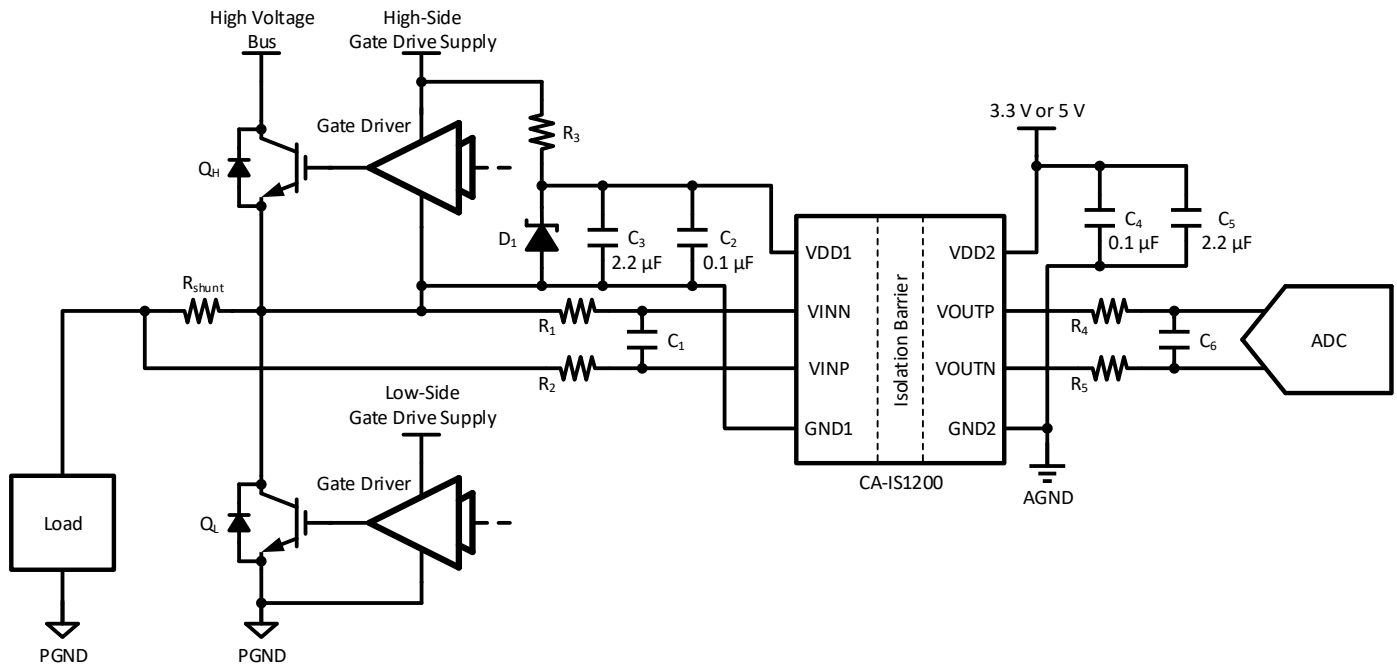


Figure 10-1 Typical Application for Current Sensing

The typical application for current sensing is shown in [Figure 10-1](#). The CA-IS1200 device is used to amplify the voltage across the shunt resistor (R_{shunt}) and transmit it to the low-voltage side for control circuit to process. The differential input and the high CMTI of CA-IS1200 ensure the reliable and accurate measurement in the high-noise and high-power switching applications such as industrial motor drives. The voltage of R_{shunt} with respect to PGND varies from 0 V to the high voltage bus when switching, thus isolation is required. The CA-IS1200 devices support up to 3750- V_{RMS} (CA-IS1200U) or 5000- V_{RMS} (CA-IS1200G) galvanic isolation, making them suitable for these high-voltage industrial applications.

In a three-phase motor drive application, this circuit could be repeated three times and one for each phase in order to measure each phase current.

10.1.2 Choose Proper R_{shunt}

The value chosen of shunt resistor is a trade off between power dissipation and measuring accuracy. Small value resistors minimize power dissipation, while large value resistors take advantage of the full performance input range of the Sigma-Delta modulator.

Consider the following restrictions to choose proper value of the shunt resistor R_{shunt} :

- The voltage drop across R_{shunt} caused by the nominal measured current is within the linear differential input voltage range V_{FSR} ;
- The voltage drop across R_{shunt} caused by the maximum allowed current must not exceed the maximum input voltage before clipping output $|V_{Clipping}|$.

For best performance, place the shunt resistor close to the inputs of CA-IS1200 and keep the layout of both connections symmetrical. This ensures that any noises occurring at high side are coupled equally to the inputs and would be rejected as a common-mode signal. Kelvin connection is recommended between R_{shunt} and the inputs of CA-IS1200 to remove the impact from any voltage drops across the trace and leads.

10.1.3 Input Filter

The typical input bandwidth of CA-IS1200 is 1 MHz. A first-order passive RC low-pass filter could be placed between R_{shunt} and the inputs to narrow the input bandwidth. Choose $R_1 = R_2 = 10 \Omega$ and $C_1 = 20 \text{ nF}$ could provide a cutoff frequency of approximately 400 kHz. R_1 and R_2 should be low-value enough compared to the input impedance of CA-IS1200 to reduce gain error.

10.1.4 Power Supply Recommendations

The high-side power supply of CA-IS1200 could be generated directly derived from the high-side gate drive power supply by utilizing a Zener diode (D_1) to produce a 3.3-V or 5-V ($\pm 10\%$) voltage. And a low-ESR decoupling capacitor of $0.1 \mu\text{F}$ (C_2) is recommended to place as close as possible to the VDD1 pin of CA-IS1200. Additional $2.2\text{-}\mu\text{F}$ capacitor (C_3) is recommended for better filtering to the high-side power-supply path.

Similarly, a $0.1\text{-}\mu\text{F}$ decoupling capacitor (C_4) followed by an additional capacitor (C_5) from $2.2 \mu\text{F}$ to $10 \mu\text{F}$ should be placed as close as to the VDD2 pin of CA-IS1200 to filter the low-side power supply path.

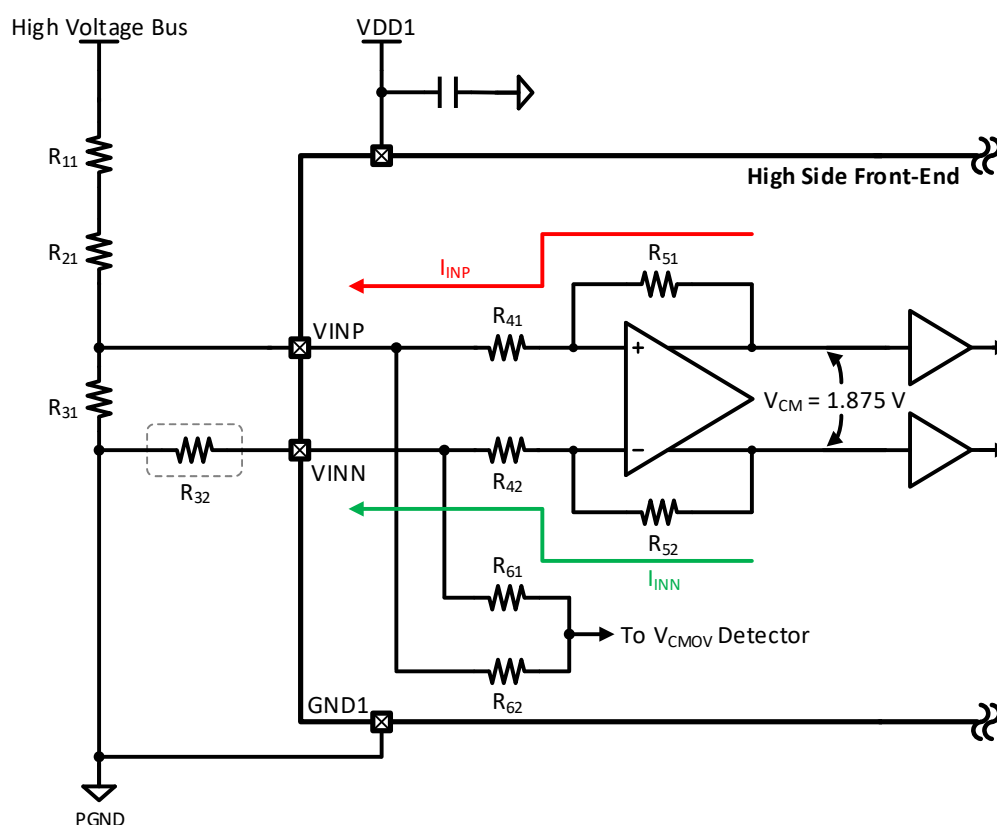


Figure 10-2 Typical Application for Voltage Sensing

10.1.5 Output Filter

Another first-order passive RC low-pass filter could be placed between the outputs of CA-IS1200 and the ADC to satisfy the potential requirement for anti-aliasing filtering. The characteristics of this filter depends on the structure and sampling frequency of the ADC. Choose $R_4 = R_5 = 4.7 \text{ k}\Omega$ and $C_6 = 180 \text{ pF}$ could provide a cutoff frequency of approximately 94 kHz.

10.1.6 Error Analysis in Voltage Sensing

The CA-IS1200 devices may also be used in the applications of voltage sensing as shown in [Figure 10-2](#). The resistors R_{11} , R_{21} and R_{31} make up the resistor divider to scale down the high voltage from bus. Typically, the value of R_{11} and R_{21} is much larger than R_{31} to keep the input voltage of CA-IS1200 within the specific range.

In CA-IS1200, resistors R_{41} and R_{51} (or R_{42} and R_{52}) are used to set the gain of front-end amplifier. The typical values are $R_{41} = R_{42} = 12.5 \text{ k}\Omega$ and $R_{51} = R_{52} = 50 \text{ k}\Omega$. Resistors R_{61} and R_{62} are used to sense the common-mode voltage of the input in CA-IS1200. The typical values are $R_{61} = R_{62} = 100 \text{ k}\Omega$.

First, consider the situation in which R_{32} is not used. Additional gain error and offset would arise in these applications for CA-IS1200. On the one hand, the limited input impedance of CA-IS1200 is parallel with the external sensing resistor R_{31} , resulting in impedance change and thus additional gain error. On the other hand, the output common-mode voltage V_{CM} of the front-end differential amplifier in CA-IS1200 is biased to 1.875 V, which would generate bias current I_{INP} and I_{INN} flowing through the front-end resistor network. The bias current I_{INP} also flows through R_{31} while I_{INN} flows directly to PGND in the case of omitting R_{32} , which results in unbalance and thus additional offset.

To eliminate the effect of the bias current, resistor R_{32} equal to sensing resistor R_{31} is recommended to be added between VINN and PGND. The resistor R_{31} would bring in additional gain error E_{GA} and could be calculated as [Eq. 1](#) describes.

$$E_{GA} = R_{31} / (R_{31} + R_{41}) \quad \text{(Eq. 1)}$$

To reduce the effect of this gain error, the value of R_{31} should be chosen much smaller compared to R_{41} . And this gain error could also be minimized by the system-level gain calibration.

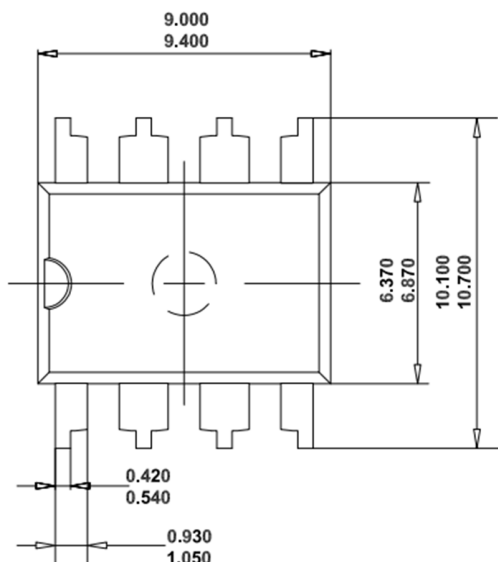
10.1.7 Caution

Do not leave the inputs of CA-IS1200 floating. If the VINP and VINN are left floating, the input common-mode voltage would be pulled to a high level by internal bias, which could activate the fail-safe mode under certain power supply and may lead to system-level abnormal reaction (refer to [Fail-Safe Output](#) for detailed information).

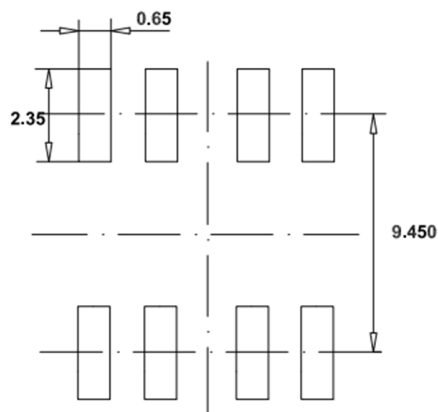
11 Package Information

11.1 DUB8 Package

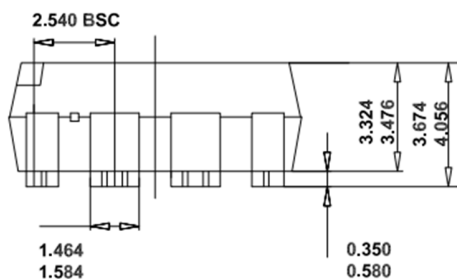
The figure below illustrates the package details for the CA-IS1200U isolated amplifier in an 8-pin DUB package. The values for the dimensions are shown in millimeters.



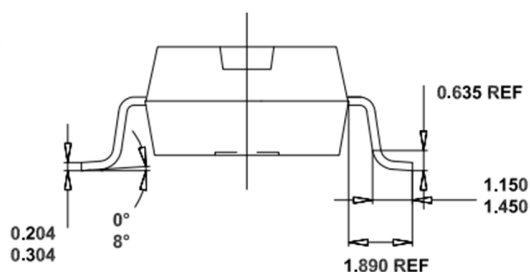
TOP VIEW



RECOMMENDED LAND PATTERN



BOTTOM VIEW

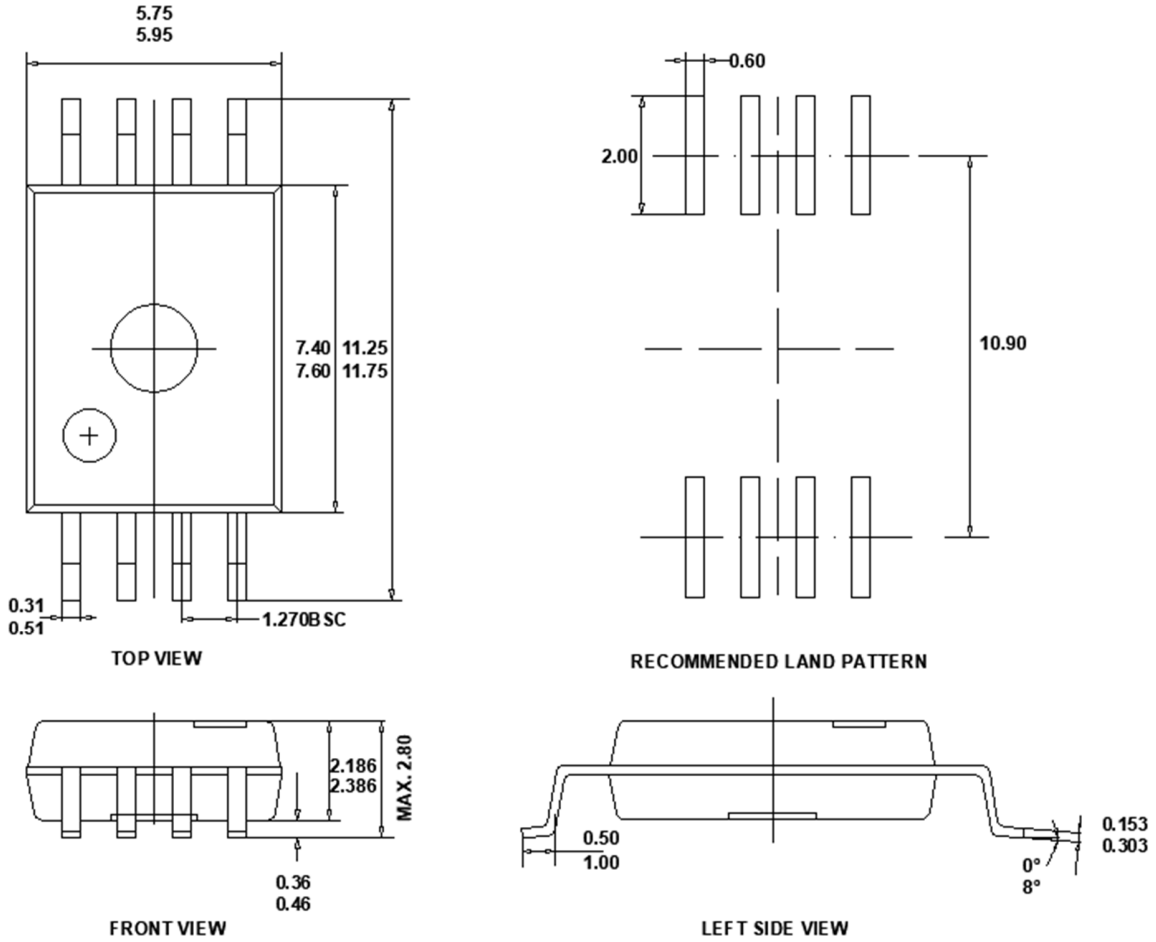


LEFT SIDE VIEW

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11.2 Wide Body SOIC8 Package

The figure below illustrates the package details and the recommended land pattern details for the CA-IS1200G isolated amplifier in an 8-pin wide-body SOIC package. The values for the dimensions are shown in millimeters.



12 Soldering Information

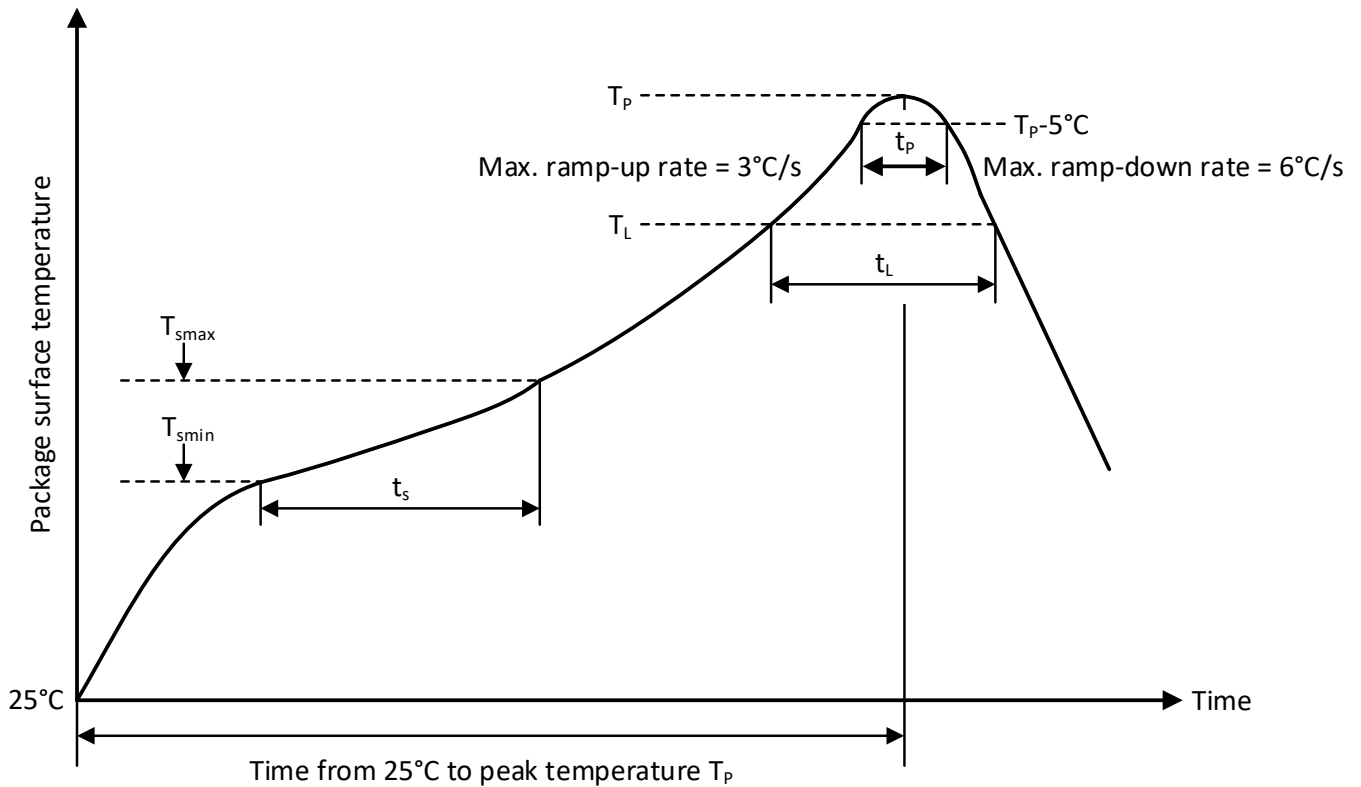


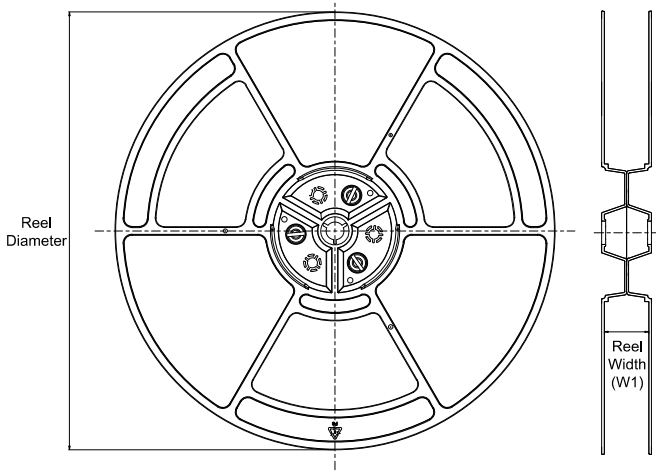
Figure 12-1 Soldering Temperature Curve

Table 12-1 Soldering Temperature Parameters

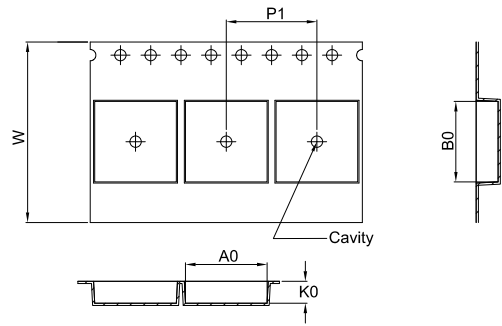
Profile Feature	Pb-Free Soldering
Ramp-up rate ($T_L = 217^\circ\text{C}$ to peak T_p)	3°C/s max
Time t_s of preheat temp ($T_{smin} = 150^\circ\text{C}$ to $T_{smax} = 200^\circ\text{C}$)	60~120 seconds
Time t_L to be maintained above 217°C	60~150 seconds
Peak temperature T_p	260°C
Time t_p within 5°C of actual peak temp	30 seconds max
Ramp-down rate (peak T_p to $T_L = 217^\circ\text{C}$)	6°C/s max
Time from 25°C to peak temperature T_p	8 minutes max

13 Tape and Reel Information

REEL DIMENSIONS

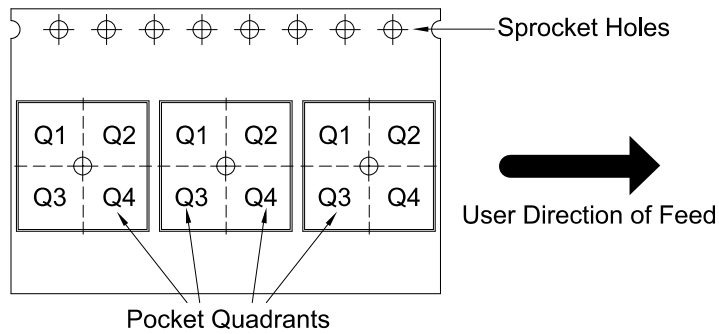


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CA-IS1200U	DUB	U	8	800	330	24.4	10.90	9.60	4.30	16.00	24.00	Q1
CA-IS1200G	SOIC	G	8	1000	330	16.4	11.95	6.15	3.20	16.00	16.00	Q1

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