CA-IS1311G-Q1 Automotive 5-kV$_{RMS}$ Reinforced Isolated Amplifier for Voltage Sensing

1 Key Features

- Input Voltage Range: –0.1 V to 2 V
- High Input Impedance: 1 GΩ (typ)
- Fixed Initial Gain: 1
- Low Input Offset and Drift:
  ±1.5 mV (max) at 25°C, ±15 µV/°C (max)
- Low Gain Error and Drift:
  ±0.3% (max) at 25°C, ±40 ppm/°C (max)
- 3.3-V or 5-V Operation for Both High- and Low-Side
- High CMTI: ±150 kV/µs (typ)
- Wide Operating Temperature Range: –40°C to 125°C
- Safety-Related Certifications:
  - VDE 0884-17 isolation certification
  - UL according to UL1577
  - IEC 61010-1:2010+A1 certifications
- >40-year Life at Rated Working Voltage
- AEC-Q100 Qualified for Automotive Applications:
  Grade 1, –40°C to 125°C (T_A)

2 Applications

- Automotive Motor Controls and Drives
- Onboard Chargers
- Traction Inverters
- Charging Piles

3 Description

The CA-IS1311G-Q1 devices are high-precision reinforced isolated amplifiers and optimized for voltage sensing. Low offset and gain error and drift guarantee that measuring accuracy is maintained over the entire operating temperature range.

The CA-IS1311G-Q1 devices utilize silicon oxide (SiO_2) isolation barriers and support up to 5-kV$_{RMS}$ galvanic isolation per UL 1577. This technology separates high- and low-voltage domain to protect lower-voltage parts from damage and provides low emissions as well as strong anti-interference capability from magnetic changes. The high common-mode transient immunity (CMTI) means that the CA-IS1311G-Q1 devices transmit correct signals through isolation barriers and are suitable for automotive motor controls and drives which require high-voltage and high-power switching. The internal missing or undervoltage lockout (UVLO) of high-side supply voltage detection functions contribute to fault diagnostics and system safety.

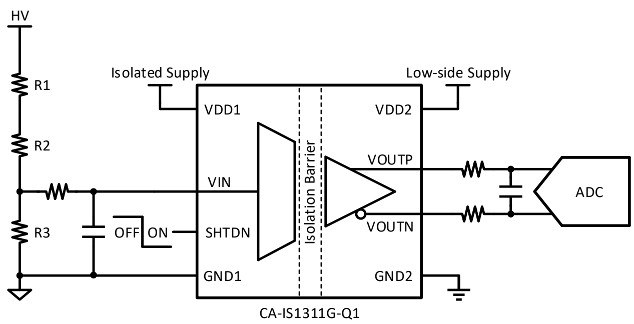
The input of CA-IS1311G-Q1 is high-impedance, making it suitable for applications where the measured signal sources have high output resistance (such as high-voltage resistive dividers). The CA-IS1311G-Q1 devices have shutdown mode, which could shut down the high-side circuit by pulling up SHTDN pin to save power.

The CA-IS1311G-Q1 devices are packaged in wide body, 8-pin SOIC packages and specified over the automotive temperature range of –40°C to 125°C.

Device Information

PART NUMBER	PACKAGE	BODY SIZE (NOM)
CA-IS1311G-Q1	SOIC8-WB (G)	5.85 mm × 7.50 mm

Simplified Schematic



4 Ordering Guide

Table 4-1 Ordering Guide for Valid Ordering Part Number

Ordering Part Number	Input Offset	Isolation Rating	Package
CA-IS1311G-Q1	±1.5 mV @ 25°C	5 kV_{RMS}	SOIC8-WB (G)

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5 Revision History

Revision	Description	Page
Version 1.00	NA	NA
Version 1.01	Update information of VDE certification	7
Version 1.02	Update information of TUV and UL certification	7

6 Pin Descriptions and Functions

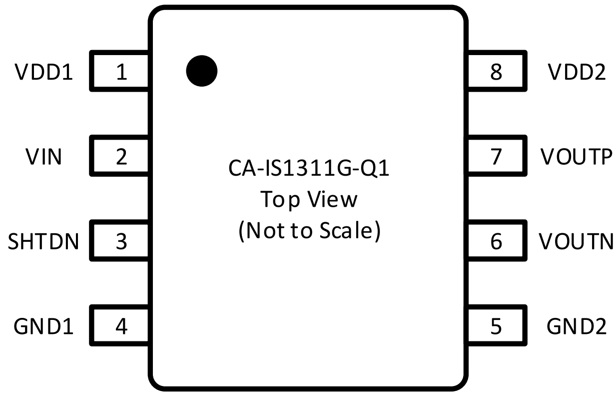


Figure 6-1 CA-IS1311G-Q1 Top View

Table 6-1 CA-IS1311G-Q1 Pin Description and Functions

NAME	PIN NUMBER	TYPE	DESCRIPTION
VDD1	1	Power	High-side power supply, 3 V to 5.5 V
VIN	2	Input	Analog input
SHTDN	3	Input	Shutdown-mode control input, active high, with internal pull-up
GND1	4	Ground	High-side ground
GND2	5	Ground	Low-side ground
VOUTN	6	Output	Inverting analog output
VOUTP	7	Output	Noninverting analog output
VDD2	8	Power	Low-side power supply, 3 V to 5.5 V

7 Specifications

7.1 Absolute Maximum Ratings[1]

PARAMETER		MIN	MAX	UNIT
VDD1, VDD2	Supply voltage[2]	–0.5	6.5	V
VIN	Analog input voltage	GND1 – 6	VDD1 + 0.5[3]	V
SHTDN	Shutdown mode control input voltage	GND1 – 0.5	VDD1 + 0.5[3]	V
VOUTP, VOUTN	Analog output voltage	GND2 – 0.5	VDD2 + 0.5[3]	V
I_{IN}	Input current to any pin except supply pins	–10	10	mA
T_J	Junction Temperature		150	°C
T_{STG}	Storage Temperature	–65	150	°C

NOTE:
1. Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. All voltage values are with respect to the local ground terminal (GND1 or GND2) and are peak voltage values.
3. Maximum voltage must not exceed 6.5 V.

7.2 ESD Ratings

			VALUE	UNIT
V_{ESD}	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins	±4000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins	±2000	

7.3 Recommended Operating Conditions

PARAMETER		MIN	NOM	MAX	UNIT
VDD1	High-side supply voltage, with respect to GND1	3.0	5.0	5.5	V
VDD2	Low-side supply voltage, with respect to GND2	3.0	3.3	5.5	V
$V_{Clipping}$	Maximum input voltage before clipping output		2.516		V
V_{FSR}	Specified linear full-scale input range	–0.1		2	V
	Absolute input voltage without damage	–2		VDD1	V
T_A	Ambient Temperature	–40		125	°C

7.4 Thermal Information

THERMAL METRIC		VALUE	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	110.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	51.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	66.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	16.0	°C/W
ψ_{JB}	Junction-to-board characterization parameter	64.5	°C/W
$R_{\theta JC(bottom)}$	Junction-to-case (bottom) thermal resistance	NA	°C/W

7.5 Power Ratings

PARAMETER		TEST CONDITIONS	VALUE	UNIT
P_D	Maximum power dissipation for both sides	VDD1 = VDD2 = 5.5 V	118.25	mW
		VDD1 = VDD2 = 3.6 V	69.12	
P_{D1}	Maximum power dissipation for high-side	VDD1 = 5.5 V	74.25	mW
		VDD1 = 3.6 V	43.20	
P_{D2}	Maximum power dissipation for low-side	VDD2 = 5.5 V	44.00	mW
		VDD2 = 3.6 V	25.92	

7.6 Insulation Specifications

PARAMETR		TEST CONDITIONS	VALUE	UNIT
CLR	External clearance[1]	Shortest terminal-to-terminal distance through air	8	mm
CPG	External creepage[1]	Shortest terminal-to-terminal distance across the package surface	8	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	28	μm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	> 600	V
	Material group	According to IEC 60664-1	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 300 V_{RMS}	I-IV	
		Rated mains voltage ≤ 600 V_{RMS}	I-IV	
		Rated mains voltage ≤ 1000 V_{RMS}	I-III	
DIN V VDE V 0884-17:2021-10[2]				
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	2121	V_{PK}
V_{IOWM}	Maximum working isolation voltage	AC voltage; Time dependent dielectric breakdown (TDDB) Test	1500	V_{RMS}
		DC voltage	2121	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t = 60 s (qualification); $V_{TEST} = 1.2 \times V_{IOTM}$, t= 1 s (100% production)	7070	V_{PK}
V_{IOSM}	Maximum surge isolation voltage[3]	Test method per IEC 62368-1, 1.2/50 μs waveform, $V_{TEST} = 1.6 \times V_{IOSM}$ (qualification)	8000	V_{PK}
q_{pd}	Apparent charge[4]	Method a, After input/output safety test subgroup 2/3, $V_{ini} = V_{IOTM}$, $t_{ini} = 60$ s; $V_{pd(m)} = 1.2 \times V_{IORM}$, $t_m = 10$ s	≤ 5	pC
		Method a, After environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, $t_{ini} = 60$ s; $V_{pd(m)} = 1.6 \times V_{IORM}$, $t_m = 10$ s	≤ 5	
		Method b1, At routine test (100% production) and preconditioning (type test) $V_{ini} = 1.2 \times V_{IOTM}$, $t_{ini} = 1$ s; $V_{pd(m)} = 1.875 \times V_{IORM}$, $t_m = 1$ s	≤ 5	
C_{IO}	Barrier capacitance, input to output[5]	$V_{IO} = 0.4 \times \sin(2\pi ft)$, f = 1 MHz	~ 1	pF
R_{IO}	Isolation resistance[5]	V_{IO} = 500 V, T_A = 25°C	$> 10^{12}$	Ω
		V_{IO} = 500 V, 100°C ≤ T_A ≤ 125°C	$> 10^{11}$	
		V_{IO} = 500 V at T_S = 150°C	$> 10^{9}$	
	Pollution degree		2	
UL 1577				
V_{ISO}	Maximum withstanding isolation voltage	$V_{TEST} = V_{ISO}$, t = 60 s (qualification), $V_{TEST} = 1.2 \times V_{ISO}$, t = 1 s (100% production)	5000	V_{RMS}

NOTE:

1. Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications.
2. This coupler is suitable for safe electrical insulation only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
3. Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
4. Apparent charge is electrical discharge caused by a partial discharge (pd).
5. All pins on each side of the barrier tied together creating a two-terminal device.

7.7 Safety-Related Certifications

VDE	UL	TUV	CQC
Certified according to DIN EN IEC 60747-17 (VDE 0884-17):2021-10; EN IEC 60747-17:2020+AC:2021	Recognized under UL 1577 Component Recognition Program	Certified according to EN 61010-1: 2010+A1	Certified according to GB 4943.1-2022
Reinforced insulation V_{IORM}: 2121 V_{PK} V_{IOTM}: 7070 V_{PK} V_{IOSM}: 8000 V_{PK}	Single protection 5000V_{RMS}	5000V_{RMS}	Reinforced insulation （Altitude ≤ 5000 m）
Certification Number: 40057278	Certification Number: E511334	Certification Number: AK 505918190001	Certificate number: CQC24001434134

7.8 Electrical Characteristics

All minimum and maximum specifications apply from T_A = –40°C to 125°C, VDD1 = 3 V to 5.5 V, VDD2 = 3 V to 5.5 V, VIN = –0.1 V to 2 V, and SHTDN = GND1 = 0 V (unless otherwise noted). All typical specifications are at T_A = 25°C, VDD1 = 5 V, and VDD2 = 3.3 V (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUT						
V_{OS}	Input offset voltage	Initial, at T_A = 25°C, VIN = GND1, 4.5 V ≤ VDD1 ≤ 5.5 V	–1.5	±0.4	1.5	mV
		Initial, at T_A = 25°C, VIN = GND1, 3.0 V ≤ VDD1 ≤ 5.5 V[1]	–2.5	±1	2.5	
TCV_{OS}	Input offset voltage drift		–15	±3	15	μV/°C
C_{IN}	Input capacitance	f_{IN} = 275 kHz		7		pF
R_{IN}	Input resistance			1		GΩ
I_{IB}	Input bias current	VIN = GND1	–15	±1	15	nA
TCI_{IB}	Input bias current drift			±10		pA/°C
ANALOG OUTPUT						
	Nominal gain[2]	Initial		1		V/V
E_G	Gain error	Initial, at T_A = 25°C	–0.3%	±0.05%	0.3%	
TCE_G	Gain error drift		–40	±10	40	ppm/°C
NL	Nonlinearity		–0.08%	±0.02%	0.08%	
TCNL	Nonlinearity drift			±1		ppm/°C
	Output noise	VIN = 1 V, BW = 100 kHz		230		μV_{RMS}
THD	Total harmonic distortion	VIN = 2 V, f_{IN} = 10 kHz, BW = 100 kHz		–83		dB
SNR	Signal-to-noise ratio	VIN = 2 V, f_{IN} = 1 kHz, BW = 10 kHz		78		dB
		VIN = 2 V, f_{IN} = 10 kHz, BW = 100 kHz		68		
PSRR	Power supply rejection ratio[3]	At VDD1, DC		–65		dB
		At VDD1, 100-mV and 10-kHz ripple		–65		
		At VDD2, DC		–90		
		At VDD2, 100-mV and 10-kHz ripple		–80		
V_{CMOUT}	Common-mode output voltage		1.39	1.44	1.49	V
$V_{FAILSAFE}$	Fail-safe differential output voltage	VDD1 missing or VDD1 < VDD_{UV}, or SHTDN = HIGH		–2.6	–2.5	V
I_{OSC}	Output short-circuit current	VOUTP or VOUTN shorts to VDD2 or GND2		±13		mA
R_{OUT}	Output resistance	On VOUTP or VOUTN		< 0.2		Ω
BW_{OUT}	Output bandwidth (–3 dB)		220	275		kHz
CMTI	Common-mode transient immunity	|GND1 – GND2| = 1.5 kV; *See Figure 8-1*	100	150		kV/μs
POWER SUPPLY						
VDD_{UV}	VDD undervoltage threshold	VDD1 or VDD2 rising		2.5	2.7	V
IDD1	High-side supply current	3.0 V ≤ VDD1 ≤ 3.6 V, SHTDN = GND1		8.5	12.0	mA
		4.5 V ≤ VDD1 ≤ 5.5 V, SHTDN = GND1		9.7	13.5	
		SHTDN = VDD1		1		μA
IDD2	Low-side supply current	3.0 V ≤ VDD2 ≤ 3.6 V		5.2	7.2	mA
		4.5 V ≤ VDD2 ≤ 5.5 V		5.7	8.0	
DIGITAL INPUT (SHTDN Pin: CMOS Logic)						
I_{IN}	Input current	GND1 ≤ SHTDN ≤ VDD1	–70		1	μA
C_{IN}	Input capacitance			5		pF
V_{IH}	Logic high-level input voltage		0.7 × VDD1		VDD1 + 0.3	V
V_{IL}	Logic low-level input voltage		–0.3		0.3 × VDD1	V
TIMING						
t_r	Rise time of VOUT (10% – 90%)	VIN = 0 V to 2 V step; *See Figure 8-2*		1.2		μs
t_f	Fall time of VOUT (90% – 10%)	VIN = 2 V to 0 V step; *See Figure 8-2*		1.2		μs

t_{PD}	VIN to VOUT signal delay (50% – 50%)	Output unfiltered; *See Figure 8-3*	1.5	2.1	µs
t_{AS}	Analog settling time	VDD1 = 0 to 3 V step and 3.0 V ≤ VDD2, to VOUT valid (0.1% settling)	180	350	µs
t_{EN}	Device enable time	SHTDN high to low, tf < 10 ns; *See Figure 8-4*	180	350	µs
t_{SHTDN}	Device shutdown time	SHTDN low to high, tr < 10 ns; *See Figure 8-4*	1.6	5	µs

NOTE:
1. The typical value is at VDD1 = 3.3 V.
2. The gain is defined as the slope of the optimum line derived by the method of least squares between differential input voltage (VINP – VINN) and differential output voltage (VOUTP – VOUTN) over the specified input range.
3. This parameter is output referred.

7.9 Typical Characteristics

All typical specifications are at T_A = 25°C, VDD1 = 5 V, VDD2 = 3.3 V, SHTDN = GND1 = 0 V (unless otherwise noted).

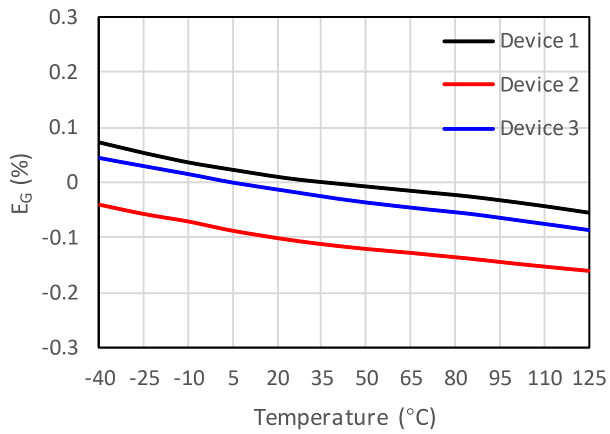


Figure 7-1 Gain Error vs Temperature

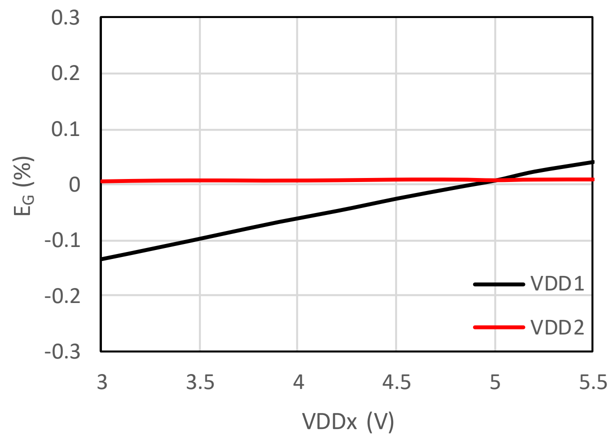


Figure 7-2 Gain Error vs Supply Voltage

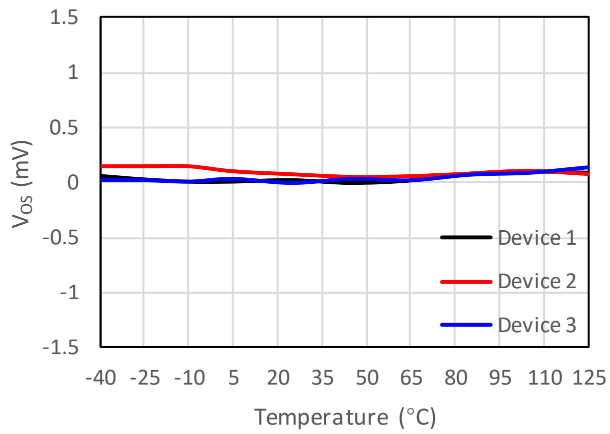


Figure 7-3 Input Offset vs Temperature

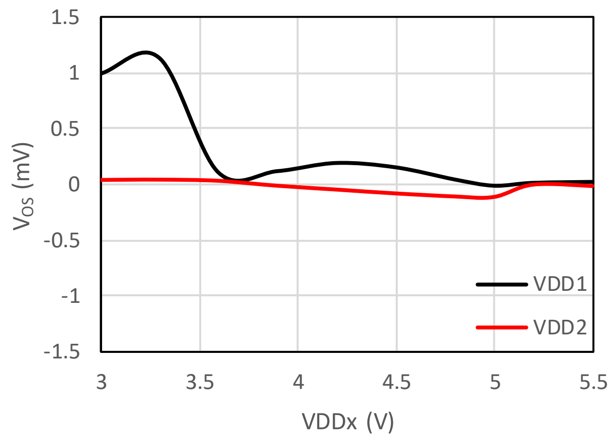


Figure 7-4 Input Offset vs Supply Voltage

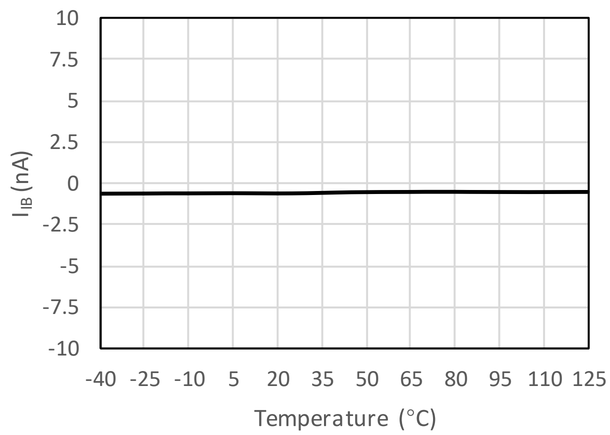


Figure 7-5 Input Bias vs Temperature @ VIN Pin

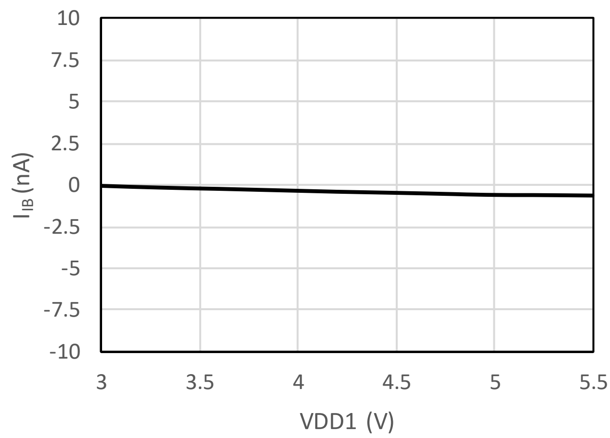


Figure 7-6 Input Bias vs Supply Voltage @ VIN Pin

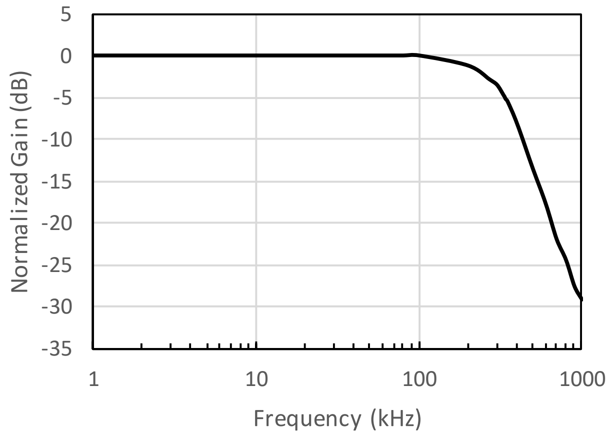


Figure 7-7 Normalized Gain vs Frequency

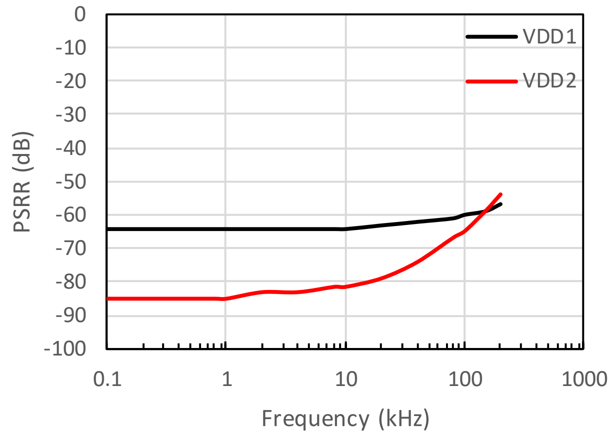


Figure 7-8 PSRR vs Frequency

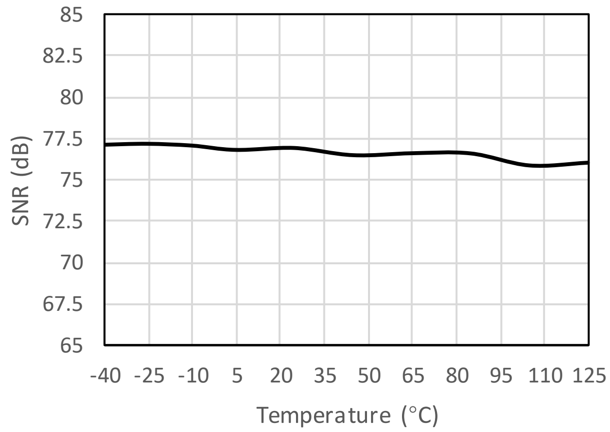


Figure 7-9 SNR vs Temperature @ f_{IN} = 1 kHz

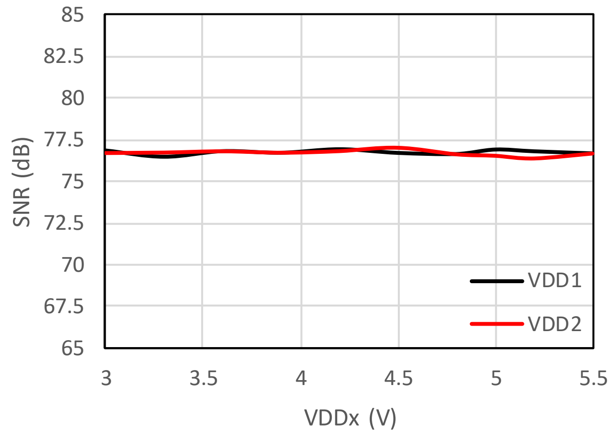


Figure 7-10 SNR vs Supply Voltage @ f_{IN} = 1 kHz

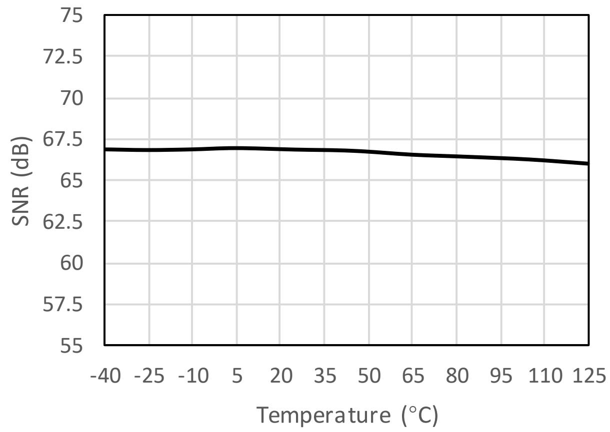


Figure 7-11 SNR vs Temperature @ f_{IN} = 10 kHz

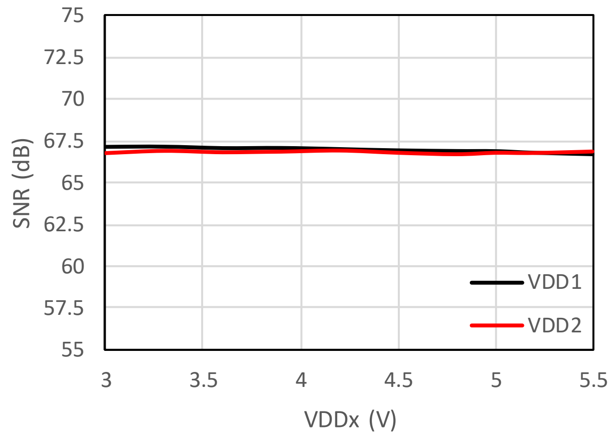


Figure 7-12 SNR vs Supply Voltage @ f_{IN} = 10 kHz

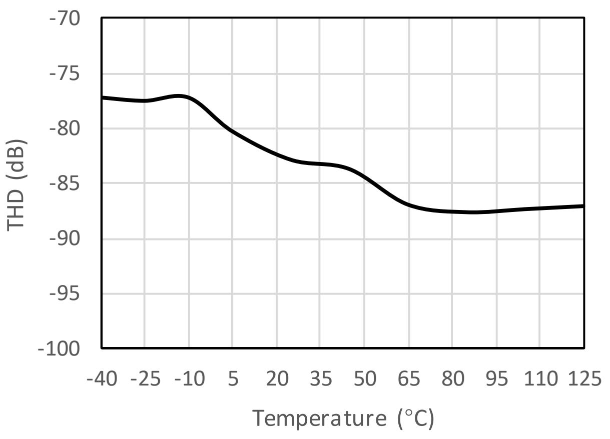


Figure 7-13 Total Harmonic Distortion vs Temperature @ f_{IN} = 10 kHz

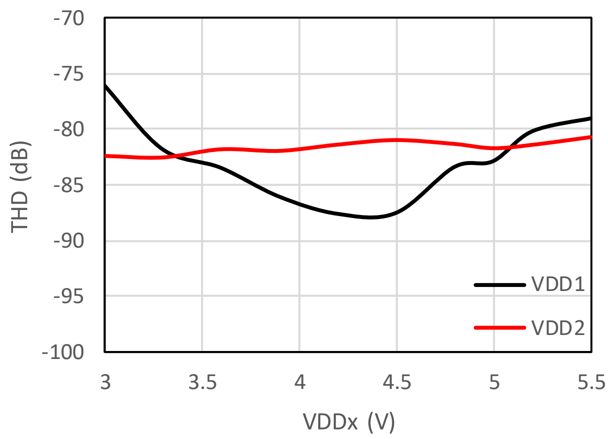


Figure 7-14 Total Harmonic Distortion vs Supply Voltage @ f_{IN} = 10kHz

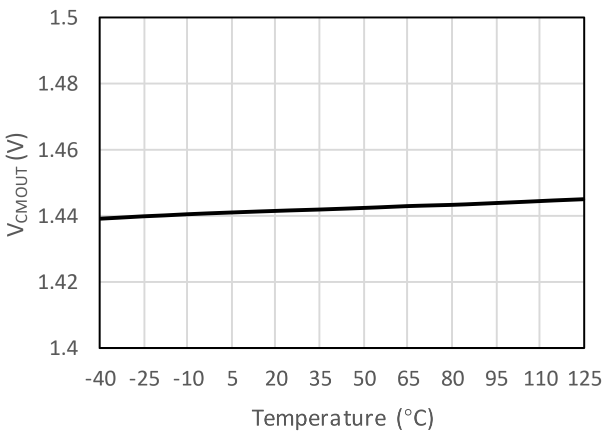


Figure 7-15 Low-Side V_{CMOUT} vs Temperature

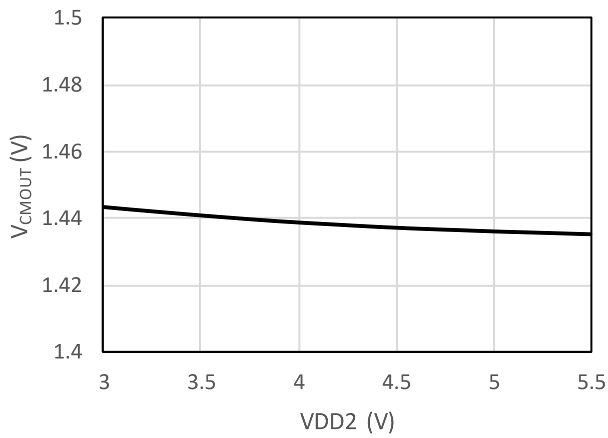


Figure 7-16 Low-Side V_{CMOUT} vs VDD2

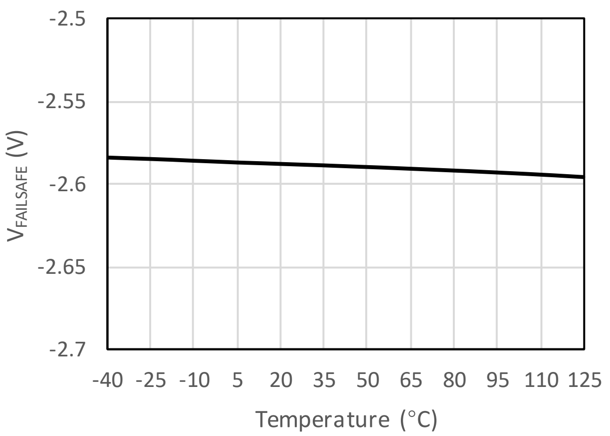


Figure 7-17 Fail-Safe Output Voltage vs Temperature

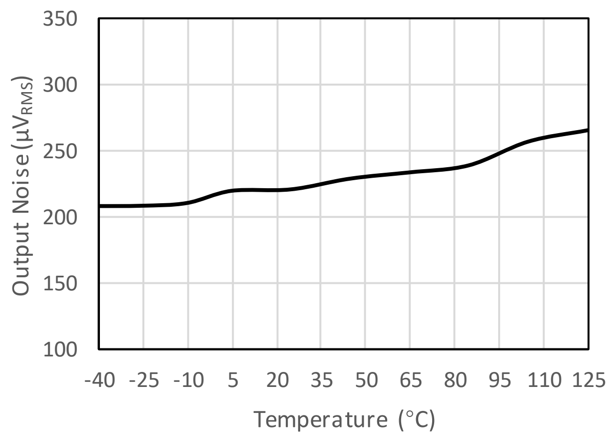


Figure 7-18 Output Noise vs Temperature @ VIN = 1 V

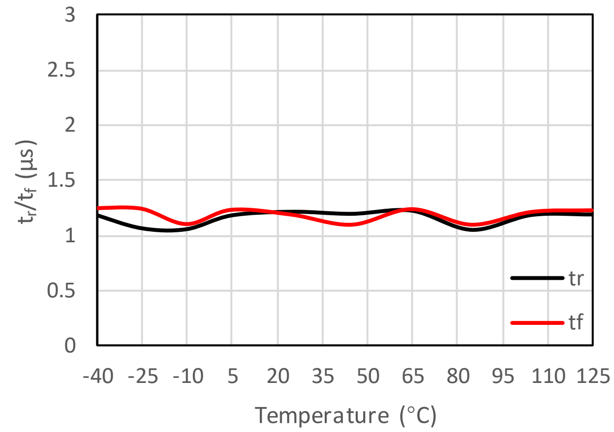


Figure 7-19 Output Rise and Fall Time vs Temperature

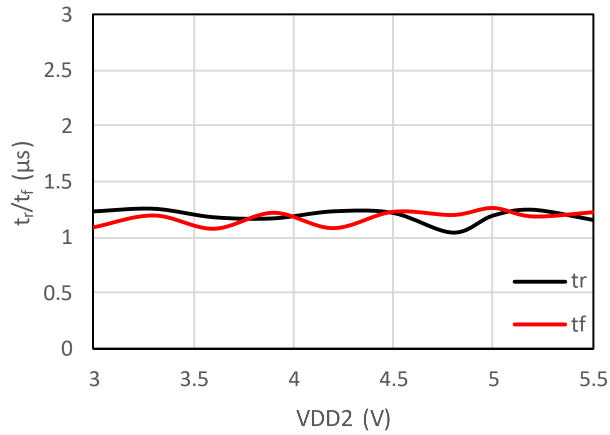


Figure 7-20 Output Rise and Fall Time vs VDD2

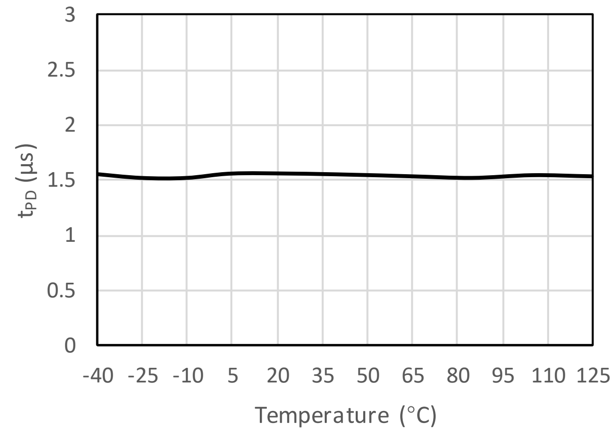


Figure 7-21 VIN to VOUT Signal Delay vs Temperature

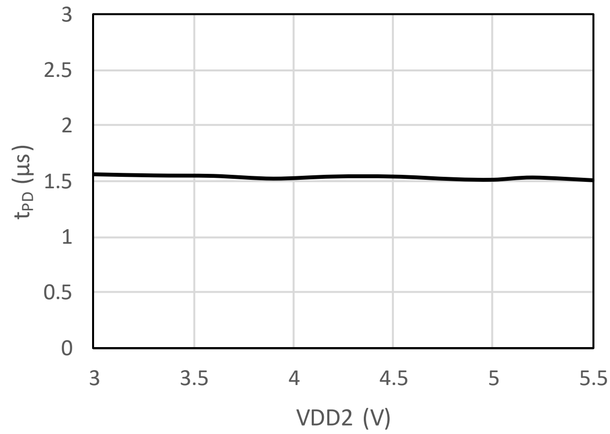


Figure 7-22 VIN to VOUT Signal Delay vs VDD2

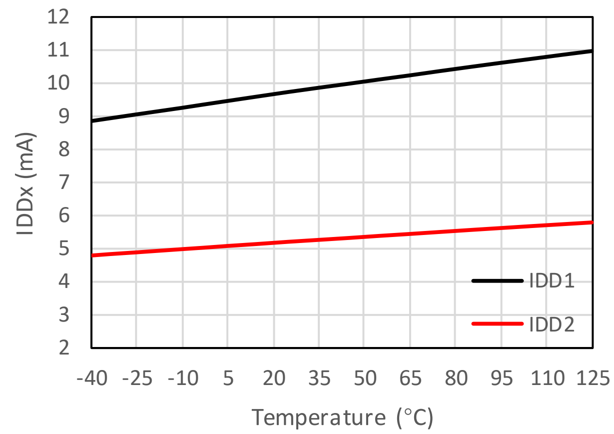


Figure 7-23 Supply Current vs Temperature

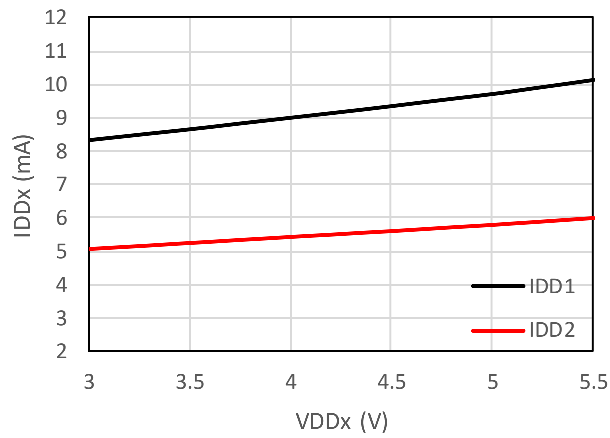
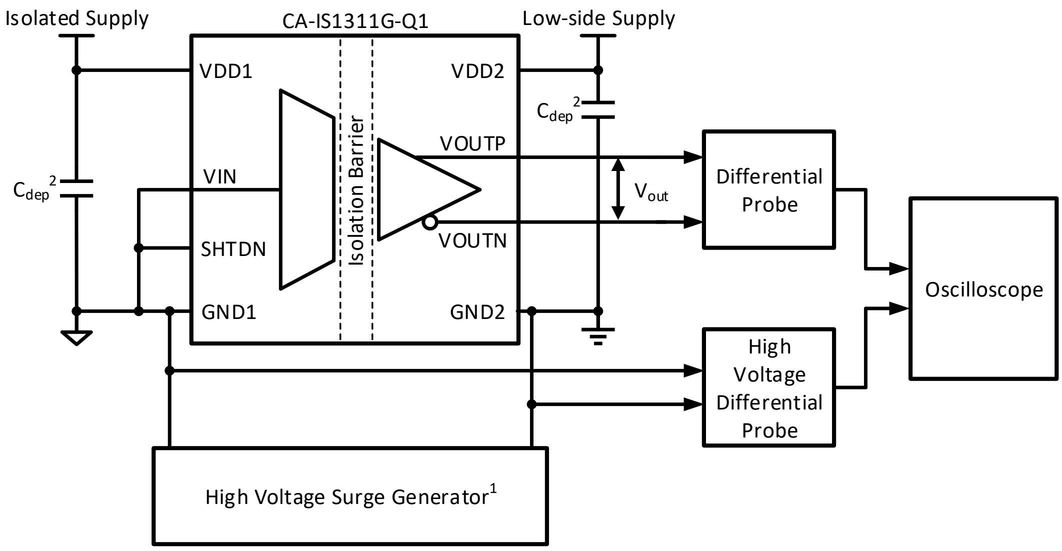


Figure 7-24 Supply Current vs Supply Voltage

8 Parameter Measurement Information



Note:

1. The High Voltage Surge Generator generates repetitive high voltage surges with > 1 kV amplitude and < 10 ns rise time or fall time to generate common-mode transient noise with > 150 kV/µs slew rate.
2. C_{dep} is the 0.1~1 µF decoupling capacitor.

Figure 8-1 Common-Mode Transient Immunity Test Circuit

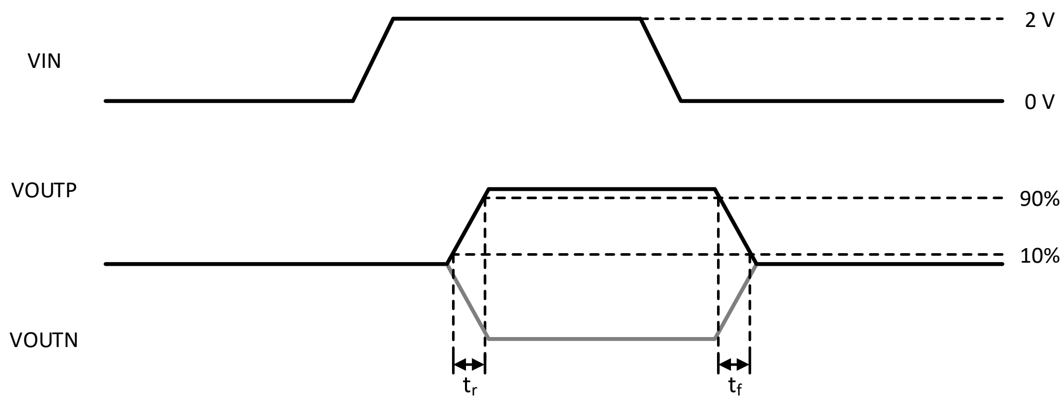


Figure 8-2 Rise and Fall Time Test Waveforms

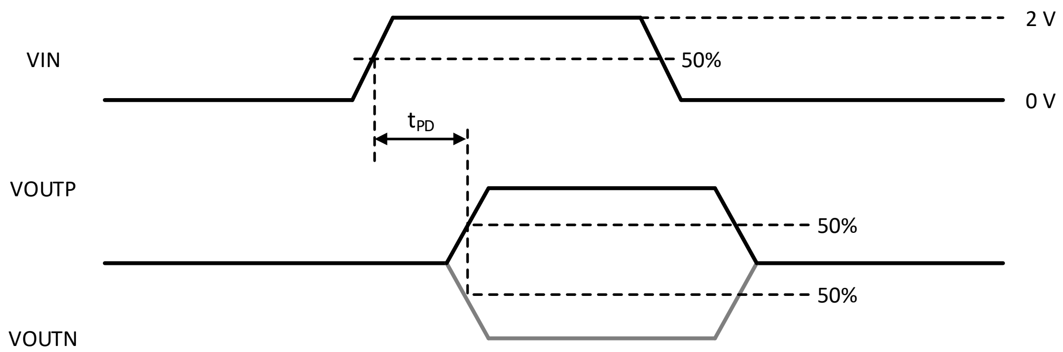


Figure 8-3 Delay Time Test Waveforms

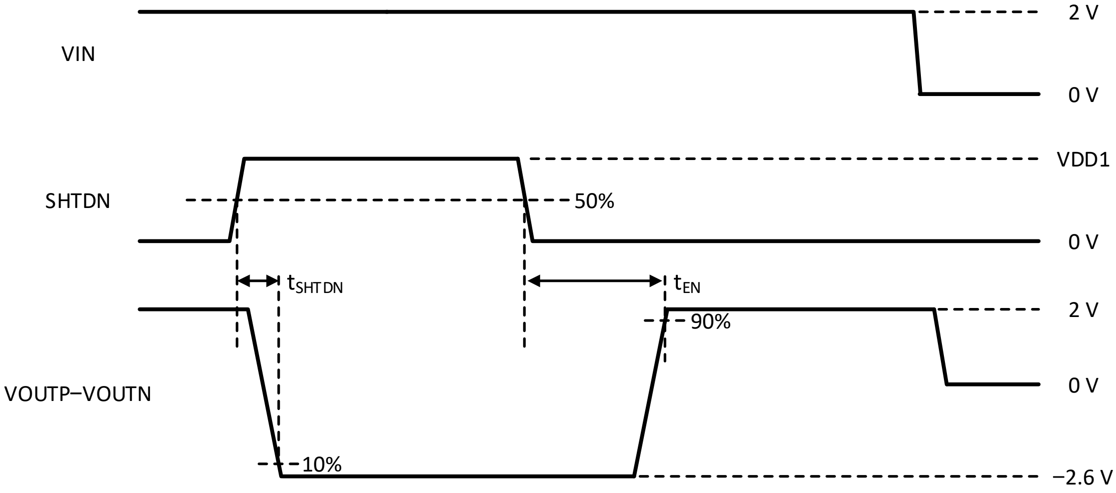


Figure 8-4 Device Shutdown and Enable Time Test Waveforms

9 Detailed Description

9.1 System Overview

The CA-IS1311G-Q1 devices are high-precision reinforced isolated amplifiers designed for voltage sensing. The functional block diagram of this device is shown in Figure 9-1. At high side, the high input-impedance buffer drives a 2nd-order Sigma-Delta (ΣΔ) modulator. This modulator converts the analog signal to a digital bitstream. For transmission across the SiO_2-based isolation barrier, the digital stream is further modulated with a high-frequency carrier using a simple on-off keying (OOK) modulation scheme. The receiver (RX) recoveries the modulated signal to the original digital bitstream at low side. After processed by a 1-bit digital-to-analog converter (DAC), the digital bitstream is sent to an active low-pass filter to produce the analog output. For synchronization of the whole chip, the clock is generated at low side and sent back to high side ensuring that all clocks come from one source.

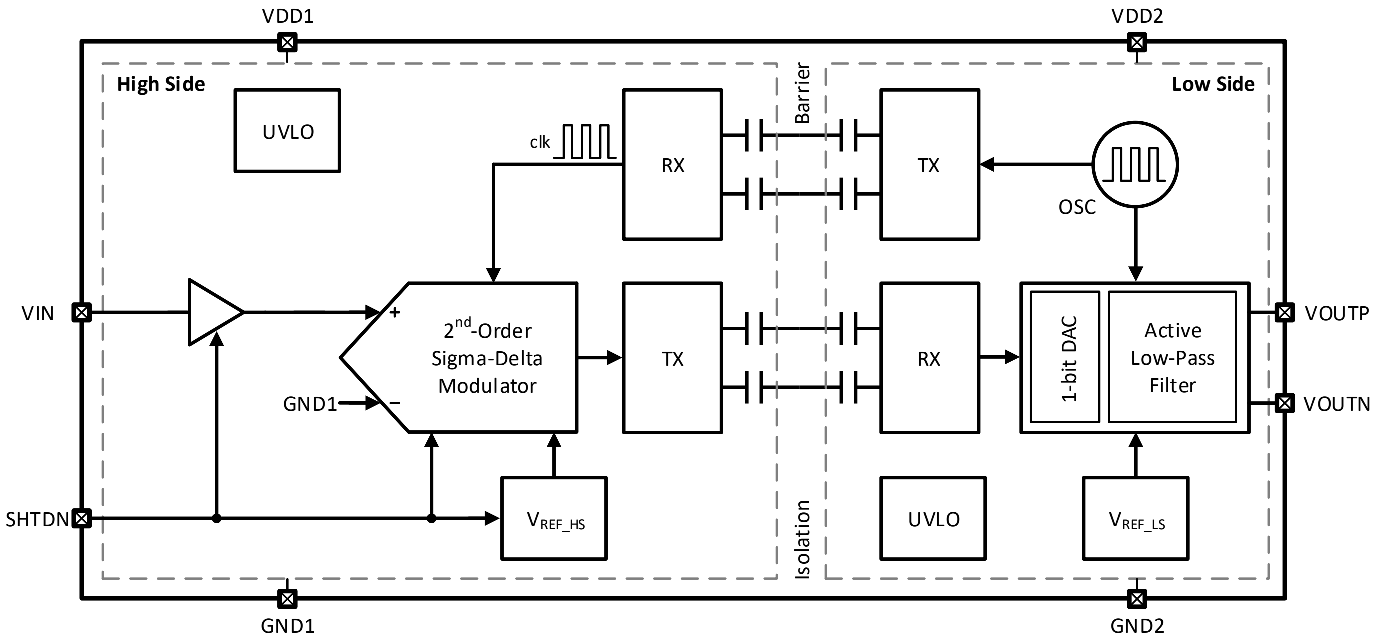


Figure 9-1 Functional Block Diagram of CA-IS1311G-Q1

9.2 Feature Description

9.2.1 Analog Input

The CA-IS1311G-Q1 devices are suitable for applications where the measured signal sources have high output resistance (such as high-voltage resistive dividers) due to their high-impedance and low bias-current input.

The ESD structure of VIN pin in CA-IS1311G-Q1 supports the absolute maximum analog input voltage (with respect to GND1) to range from GND1 – 6 V to VDD1 + 0.5 V. If the input voltage VIN exceeds this voltage range, the input current must be limited to 10 mA in order not to cause damage. To guarantee the long-term reliability and device performance, the analog input voltage of CA-IS1311G-Q1 must be kept within the specific range.

9.2.2 Shutdown Mode

The CA-IS1311G-Q1 devices have shutdown mode, which could shut down the high-side circuit by pulling up SHTDN pin to save power. The SHTDN pin is pulled up by an internal resistor and the typical value of this resistor is 100 kΩ. During normal operation, SHTDN pin should be connected to GND1 or held to logical LOW.

9.2.3 Signal Transmission Across Isolation Barrier

The CA-IS1311G-Q1 devices utilize a simple on-off keying (OOK) modulation scheme to transmit the digital bitstream across the SiO_2-based isolation barrier which supports up to 5-kV_{RMS} galvanic isolation between high- and low-voltage domain. The block diagram of an isolation channel is shown in Figure 9-2. As shown in Figure 9-3, the transmitter (TX) modulates the digital bitstream with a high-frequency carrier when the signal is HIGH while sends no signal when the signal is LOW. The receiver (RX) demodulates the signal across the isolation barrier and reproduces the digital bitstream faithfully. The isolation channel adopts fully differential capacitive-coupled structure which is insensitive to common-mode transient noises, thus the CMTI performance can be maximized. This structure and related circuitry also provide low emissions and strong anti-interference capability from magnetic changes.

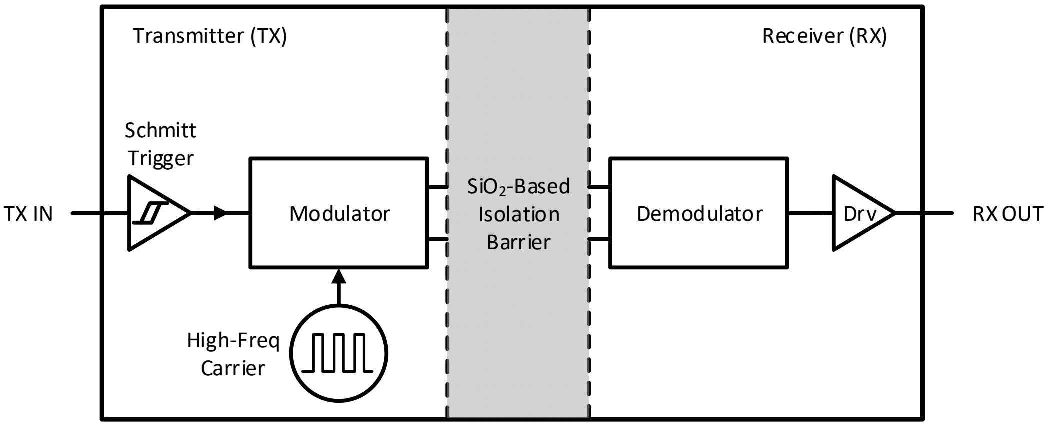


Figure 9-2 Block Diagram of an Isolation Channel

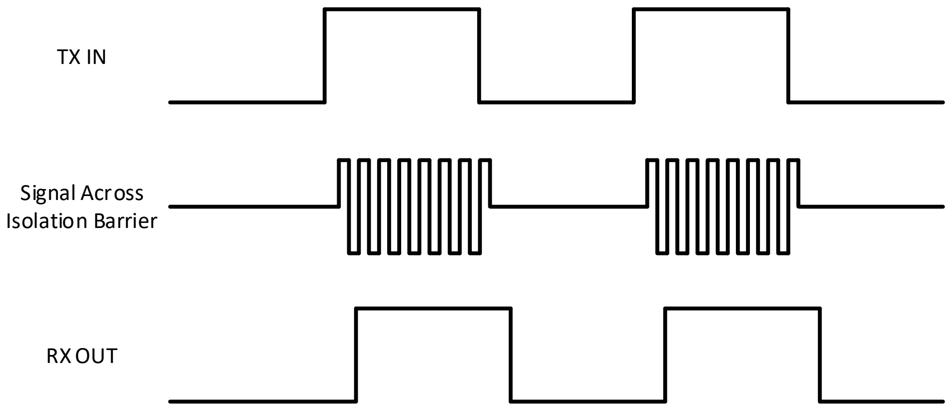


Figure 9-3 Conceptual Operation Waveforms of OOK Modulation Scheme

9.2.4 Fail-Safe Output

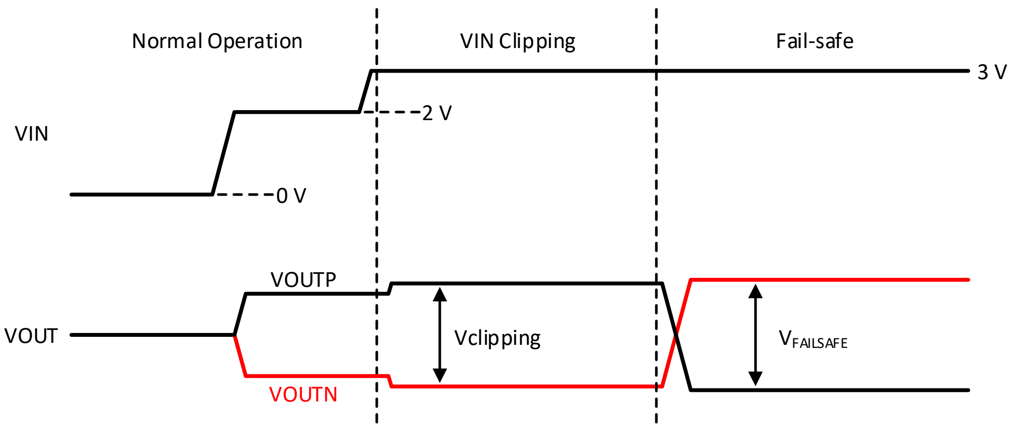


Figure 9-4 Typical Operation Waveforms in Different Conditions

The CA-IS1311G-Q1 devices have fail-safe output function which is activated in three conditions:

- The high-side power supply VDD1 is missing;
- The high-side power supply VDD1 is under the undervoltage threshold VDD_{UV};
- The SHTDN pin is pulled high.

The fail-safe output is the most negative differential output voltage which can be distinguished from the output under normal operation or when VIN is clipping. This function contributes to fault diagnostics and system safety.

10 Application and Implementation

10.1.1 Typical Application for Voltage Sensing

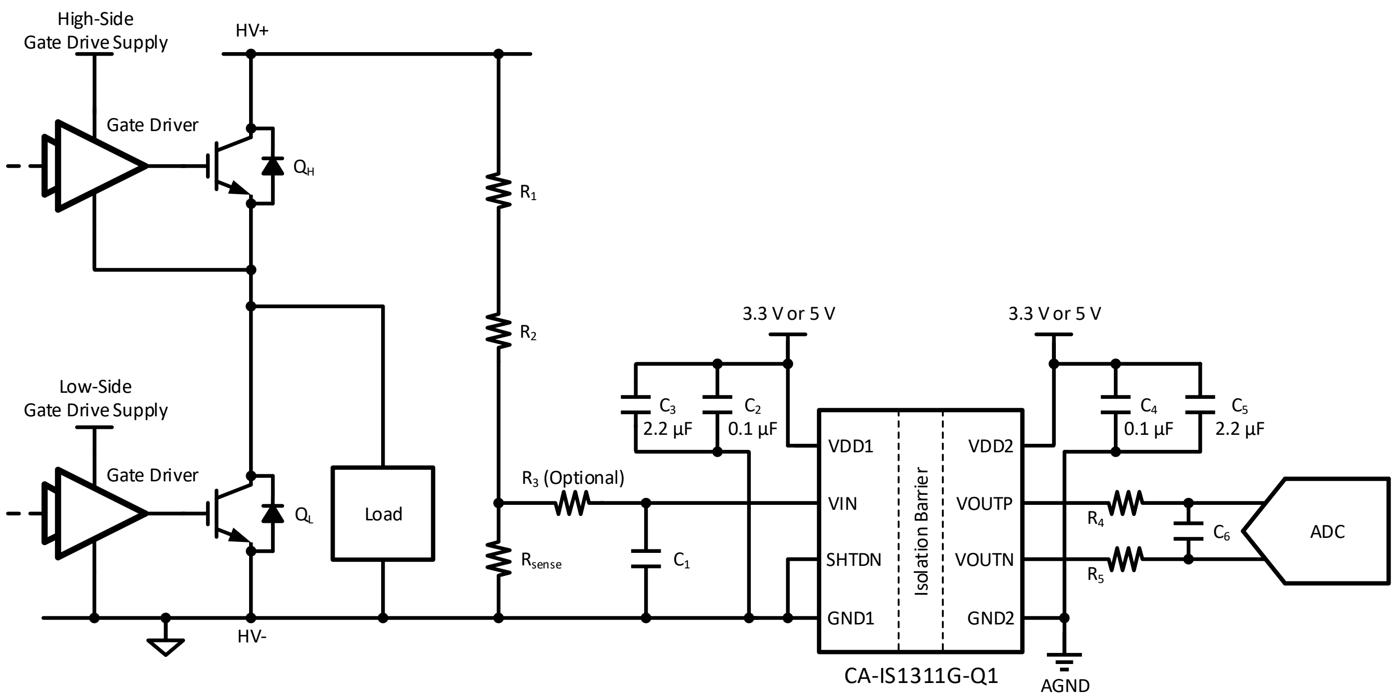


Figure 10-1 Typical Application for Voltage Sensing

The typical application for DC bus voltage sensing is shown in Figure 10-1. The R_1, R_2 and R_{sense} make up a resistor divider network, which divides the high bus voltage down to a level within the specific range.

The CA-IS1311G-Q1 device is used to measure the voltage across the sense resistor (R_{sense}) and transmit it to the low-voltage side for control circuit to process. The high CMTI and low bias-current input of CA-IS1311G-Q1 ensure the reliable and accurate measurement in the high-noise and high-power switching applications such as automotive motor drives. The CA-IS1311G-Q1 devices support up to 5-kV_{RMS} galvanic isolation, making them suitable for these high-voltage automotive applications.

10.1.2 Choose Proper R_{sense}

Consider the following restrictions to choose proper value of the shunt resistor R_{sense}:

- The voltage drop across R_{sense} caused by the nominal measured current is within the linear differential input voltage range V_{FSR};
- The voltage drop across R_{sense} caused by the maximum allowed current must not exceed the maximum input voltage before clipping output $V_{Clipping}$.

10.1.3 Input Filter

A first-order passive RC low-pass filter could be placed between R_{sense} and the input to serve as anti-aliasing filter. Since R_1 and R_2 are typically large enough, R_3 is optional and a single capacitor C_1 is sufficient.

10.1.4 Power Supply Recommendations

A low-ESR decoupling capacitor of 0.1 µF (C_2) is recommended to place as close as possible to the VDD1 pin of CA-IS1311G-Q1. Additional 2.2-µF capacitor (C_3) is recommended for better filtering to the high-side power-supply path.

Similarly, a 0.1-µF decoupling capacitor (C_4) followed by an additional capacitor (C_5) from 2.2 µF to 10 µF should be placed as close as to the VDD2 pin of CA-IS1311G-Q1 to filter the low-side power supply path.

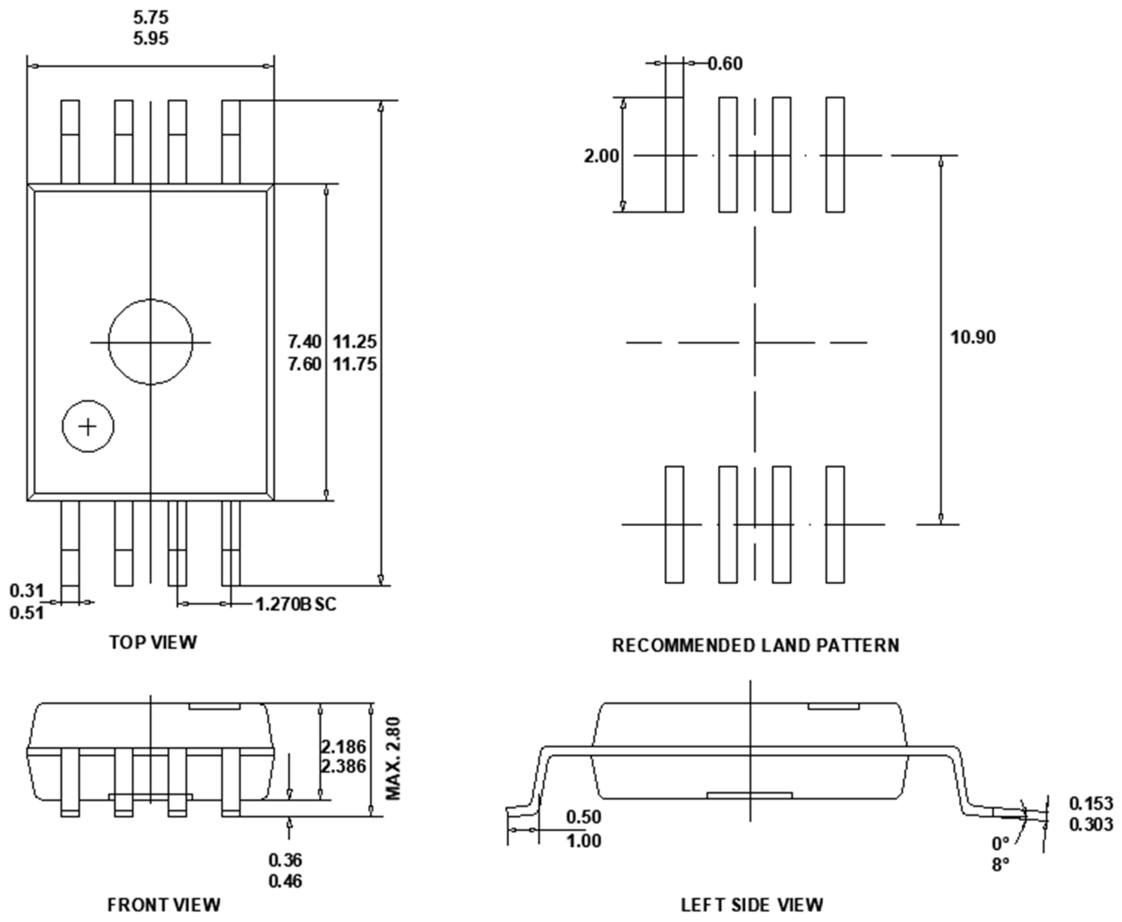
10.1.5 Output Filter

Another first-order passive RC low-pass filter could be placed between the outputs of CA-IS1311G-Q1 and the ADC to satisfy the potential requirement for anti-aliasing filtering. The characteristics of this filter depends on the structure and sampling frequency of the ADC. Choose $R_4 = R_5 = 4.7\ k\Omega$ and $C_6 = 180\ pF$ could provide a cutoff frequency of approximately 94 kHz.

11 Package Information

11.1 8-Pin Wide Body SOIC Package

The figure below illustrates the package details and the recommended land pattern details for the CA-IS1311G-Q1 reinforced isolated amplifier in an 8-pin wide-body SOIC package. The values for the dimensions are shown in millimeters.



12 Soldering Information

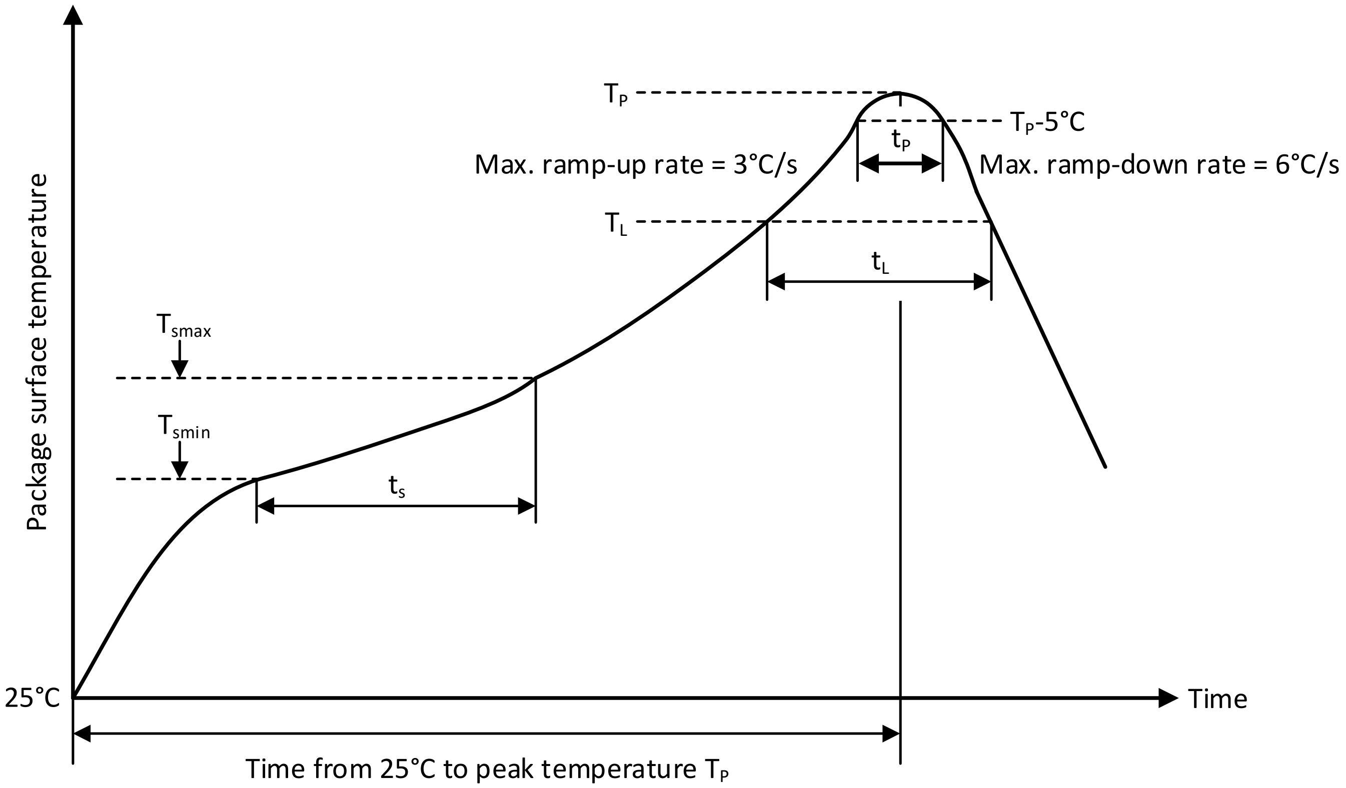


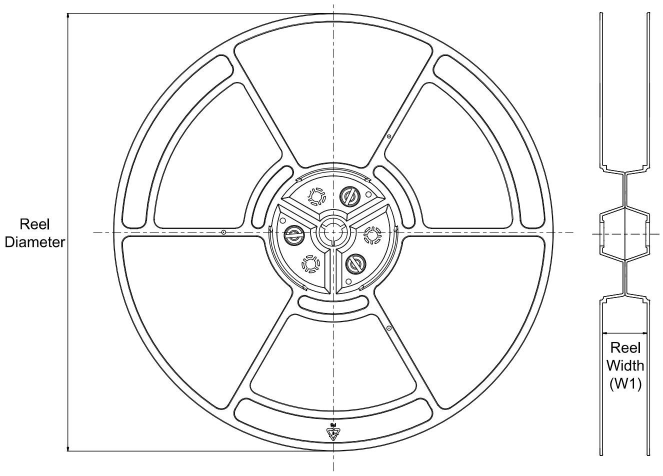
Figure 12-1 Soldering Temperature Curve

Table 12-1 Soldering Temperature Parameters

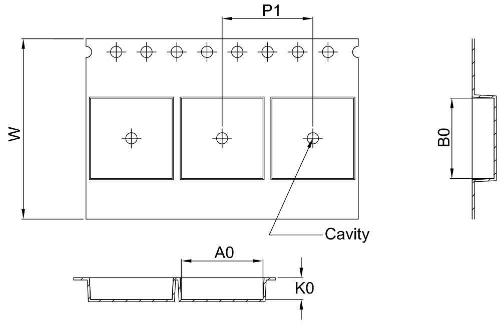
Profile Feature	Pb-Free Soldering
Ramp-up rate (T_L = 217°C to peak T_P)	3°C/s max
Time t_s of preheat temp (T_{smin} = 150°C to T_{smax} = 200°C)	60~120 seconds
Time t_L to be maintained above 217°C	60~150 seconds
Peak temperature T_P	260°C
Time t_P within 5°C of actual peak temp	30 seconds max
Ramp-down rate (peak T_P to T_L = 217°C)	6°C/s max
Time from 25°C to peak temperature T_P	8 minutes max

13 Tape and Reel Information

REEL DIMENSIONS

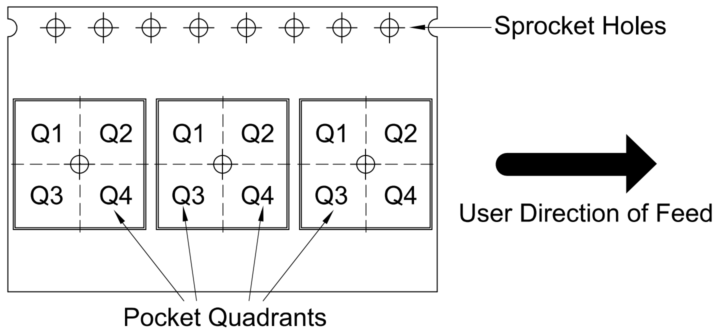


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CA-IS1311G-Q1	SOIC	G	8	1000	330	16.4	11.95	6.15	3.20	16.0	16.0	Q1

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