CA-IS2082B 3.0kV$_{RMS}$ Isolated Half-Duplex RS-485 Transceiver

1. Features

- **High-Performance and Compliant with RS-485 EIA/TIA-485 Standard**
  - Up to 20Mbps data rate
  - 1/8 unit load enables up to 256 nodes on the bus
  - 2.375V to 5.5V logic side supply voltage and 3.0 V to 5.5 V bus side supply voltage
- **Integrated Protection for Robust Communication**
  - 3.0kV$_{RMS}$ withstand isolation voltage for 60s (galvanic isolation)
  - ±100kV/μs typical CMTI
  - High lifetime: >40 years
  - ±8kV Human Body Model (HBM) ESD on BUS I/O, ±4kV HBM ESD protection on logic I/Os and other pins of bus side
  - Short-circuit protection and thermal shutdown
  - True fail-safe guarantees known receiver output state
- **Wide Operating Temperature Range: –40°C to 125°C**
- **Compact SSOP16 (B) Package**
- **Safety Regulatory Approvals**
  - VDE certification according to DIN EN IEC60747-17(VDE 0884-17):2021-10
  - UL certification according to UL1577

2. Applications

- Industrial automation equipment
- Grid infrastructure
- Solar inverter
- Motor drivers
- HVAC

3. General Description

The CA-IS2082B device is a galvanically-isolated RS-485 transceiver that has superior isolation rating and RS-485 performance to meet the critical needs of the industrial applications. This device has the logic input and output buffers separated by a silicon oxide (SiO_2) insulation barrier that provides galvanic isolation, features up to 3000V$_{RMS}$ (60s) of galvanic isolation and ±100kV/μs typical CMTI. Isolation improves communication by breaking ground loops and reduces noise where there are large differences in ground potential between different ports.

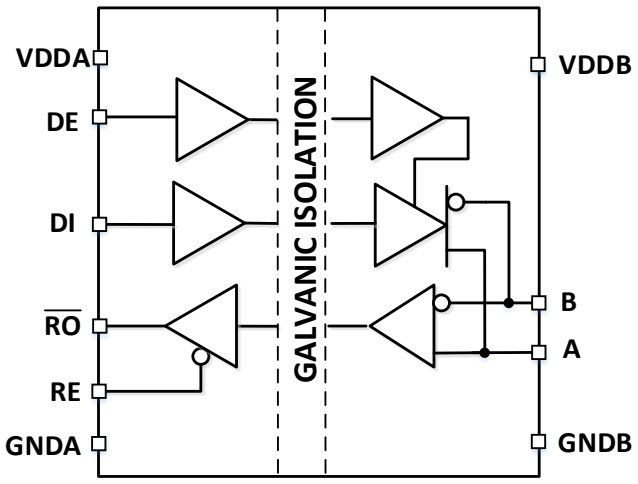
The CA-IS2082B is designed for high-speed (up to 20Mbps) multidrop operation with high ESD protection of up to ±8kV HBM. The receiver is 1/8-unit load, allowing up to 256 transceivers (loads) on a common bus. Maintaining multidrop operation and increasing the maximum data rate offer a more robust system design for reliable data transmission in the harsh environments. This device provides half-duplex transceiver, the driver and receiver enable pins let any node at any given moment be configured in either transmit or receive mode which decreases cable requirements.

The CA-IS2082B is available in compact 16-pin SSOP package which is the industry standard isolated RS-485 package, and operates over -40°C to +125°C temperature range.

Device information

Part #	Package	Package size (NOM)
CA-IS2082B	SSOP16(B)	4.9 mm × 3.9 mm

CA-IS2082B half-duplex block diagram



4. Ordering Information

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Table 4-1. Ordering Information

Part #	V_{DDA}（V）	V_{DDB}（V）	Full/half-duplex	Transmission speed (Mbps)	Rated voltage (V_{RMS})	Package
CA-IS2082B	2.375~5.5	3.0~5.5	Half-duplex	20	3000	SSOP16

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Contents

5. Revision History

Revision Number	Description	Revised Date	Page Changed
Version 1.00	N/A	2023/05/12	N/A
Version 1.01	Updated UL certification information	2023/05/14	6
Version 1.02	Update electrical characteristic data Update POD information	2023/06/29	3-9 16
Version 1.03	Update VDE information Update data rate to 20Mbps	2023/10/17	6
Version 1.04	Update VDE, UL, CQC information Update the test conditions of V_{IOSM}	2024/04/14	1,6,7

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6. Pin Configuration and Description

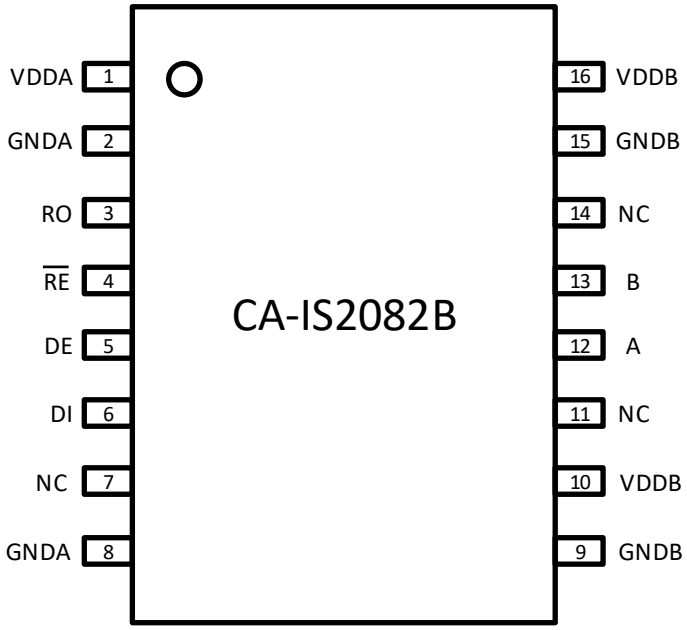

Figure 6-1. CA-IS2082B Top View

Table 6-1. CA-IS2082B Pin Description

Pin name	Pin number	Type	Description
VDDA	1	Power supply	Logic-Side Power Input. Bypass VDDA to GNDA with both 0.1μF and 1μF capacitors as close to the device as possible.
GNDA	2, 8	Ground	Logic-Side Ground. GNDA is the ground reference for logic signals.
RO	3	Digital I/O	Receiver Data Output. Drive $\overline{RE}$ low to enable receiver R_X. With $\overline{RE}$ low, RO is high when $(V_A - V_B) > V_{IT+(IN)}$ and is low when $(V_A - V_B) < V_{IT-(IN)}$.
$\overline{RE}$	4	Digital I/O	Receiver Output Enable. Drive $\overline{RE}$ low or connect to GNDA to enable receiver (R_X) operation. Drive $\overline{RE}$ high to disable R_X, RO is high-impedance when $\overline{RE}$ is high.
DE	5	Digital I/O	Driver Output Enable. Drive DE high to enable bus driver outputs. Drive DE low or connect to GNDA to disable bus driver outputs. DE has an internal weak pull-down to GNDA.
DI	6	Digital I/O	Driver Input. With DE high, a logic low on DI forces the noninverting output (A) low and the inverting output (B) high; a logic high on DI forces the noninverting output high and the inverting output low.
NC	7	---	No internal connection on side-A.
GNDB	9, 15	Ground	Cable Side Ground. GNDB is the ground reference for the RS-485 bus signals.
NC	11, 14	---	No internal connection on side-B.
A	12	Bus I/O	Noninverting RS-485 receiver input and driver output.
B	13	Bus I/O	Inverting RS-485 receiver input and driver output.
VDDB	10, 16	Power supply	Cable Side Power Input. Bypass VDDB to GNDB with both 0.1μF and 1μF capacitor as close to the device as possible.

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7. Specifications

7.1. Absolute Maximum Ratings[1]

Parameters		Minimum value	Maximum value	Unit
V_{DDA}, V_{DDB}	Power supply voltage[2]	-0.5	6.0	V
V_{IO}	Logic voltage (A,B)	-8	13	
V_{IO}	Logic voltage (DI, DE, $\overline{RE}$, RO)	-0.5	V_{DDA}+0.5[3]	V
I_O	Output current on RO	-20	20	mA
T_J	Junction temperature		150	°C
T_{STG}	Storage temperature range	-65	150	°C

Notes:
1. The stresses listed under "Absolute Maximum Ratings" are stress ratings only, not for functional operation condition. Exposure to absolute maximum rating conditions for extended periods may cause permanent damage to the device.
2. All voltage values except differential I/O bus voltages are with respect to the local ground (GNDA or GNDB) and are peak voltage values.
3. Maximum voltage must not be exceed 6V.

7.2. ESD Ratings

			Value	Unit
V_{ESD} Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	Bus pin to GNDA	±4000	V
		Bus pin to GNDB	±8000	
		All other pins	±4000	
	Charged device model (CDM), per JEDEC Specification JESD22-C101, all pins[2]		±2000	

Notes:
1. Per JEDEC document JEP155, 500V HBM allows safe manufacturing of standard ESD control process.
2. Per JEDEC document JEP157, 250V CDM allows safe manufacturing of standard ESD control process.

7.3. Recommended Operating Conditions

Parameters		Minimum value	Typical value	Maximum value	Unit
V_{DDA}	Power supply voltage on side A	2.375	3.3/5.0	5.5	V
V_{DDB}	Power supply voltage on side B	3	3.3/5.0	5.5	V
V_{OC}	Common mode voltage at bus pins: A, B	-7		12	V
V_{ID}	Differential input voltage V_{AB}	-12		12	V
R_L	Differential input resistance	54			Ω
V_{IH}	Input high voltage (DI, DE)	2.0		V_{DDA} + 0.3	V
V_{IL}	Input low voltage (DI, DE)	-0.3		0.8	V
V_{IH}	Input high voltage($\overline{RE}$)	0.7 × V_{DDA}		V_{DDA} + 0.3	V
V_{IL}	Input low voltage($\overline{RE}$)	-0.3		0.3 × V_{DDA}	V
DR	Data rate			20	Mbps
T_A	Environmental temperature	-40	27	125	°C

7.4. Thermal Information

Thermal Metric		CA-IS2082B	Unit
$R_{\theta JA}$	Junction-to-ambient thermal resistance	115	°C/W

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7.5. Insulation Specifications

Parameters		Test conditions	Specifications	Unit
			B	
CLR	External Clearance[1]	Shortest terminal-to-terminal distance through air	4	mm
CPG	External Creepage[1]	Shortest terminal-to-terminal distance across the package surface	4	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	28	μm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11)；IEC 60112	>600	V
	Material group	According to IEC 60664-1	I	
	IEC 60664-1 over-voltage category	Rated mains voltage ≤ 150 V_{RMS}	I-IV	
		Rated mains voltage ≤ 300 V_{RMS}	I-III	
		Rated mains voltage ≤ 600 V_{RMS}	N/A	
		Rated mains voltage ≤ 1000 V_{RMS}	N/A	
DIN V VDE V 0884-17:2021-10				
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	566	V_{PK}
V_{IOWM}	Maximum operating isolation voltage	AC voltage; time-dependent dielectric breakdown (TDDB) test	400	V_{RMS}
		DC voltage	556	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t=60 s (qualification); $V_{TEST} = 1.2 \times V_{IOTM}$, t=1 s (100% product test)	5300	V_{PK}
V_{IOSM}	Maximum surge isolation voltage[2]	Test method in accordance with IEC 62368-1, 1.2/50 μs waveform, $V_{TEST} = 1.3\times V_{IOSM}$ (certified)	4076	V_{PK}
q_{pd}	Apparent charge[3]	Method a, after input/output safety tests subgroup 2/3, $V_{ini} = V_{IOTM}$, t_{ini} = 60s; $V_{pd(m)} = 1.2 \times V_{IORM}$, t_m = 10s	≤5	pC
		Method a, after environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, t_{ini} = 60s; $V_{pd(m)} = 1.3 \times V_{IORM}$, t_m = 10s	≤5	
		Method b1, at routine test (100% production test) and preconditioning (sample test) $V_{ini} = 1.2 \times V_{IOTM}$, t_{ini} = 1s; $V_{pd(m)} = 1.5 \times V_{IORM}$, t_m = 1s	≤5	
C_{IO}	Barrier capacitance, input to output[4]	V_{IO} = 0.4 × sin (2πft), f = 1 MHz	~0.5	pF
R_{IO}	Isolation resistance, input to output[4]	V_{IO} = 500 V, T_A = 25°C	$>10^{12}$	Ω
		V_{IO} = 500 V, 100°C ≤ T_A ≤ 125°C	$>10^{11}$	
		V_{IO} = 500 V at T_S = 150°C	$>10^{9}$	
	Pollution degree		2	
UL 1577				
V_{ISO}	Maximum isolation voltage	$V_{TEST} = V_{ISO}$, t = 60 s (certified) $V_{TEST} = 1.2 \times V_{ISO}$, t = 1 s (100% production test)	3000	V_{RMS}

Notes:

1. This coupler is suitable for “safe electrical insulation” only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
2. Devices are immersed in oil during surge characterization test.
3. The characterization charge is discharging charge (pd) caused by partial discharge.
4. Capacitance and resistance are measured with all pins on field-side and logic-side tied together.

7.6. Safety-Related Certifications

VDE	UL
Certified according to DIN EN IEC60747-17(VDE 0884-17):2021-10; EN IEC60747-17:2020+AC:2021	Certified according to UL 1577 Component Recognition Program
Maximum transient isolation voltage: 5300V_{pk} Maximum repetitive peak isolation voltage: 566V_{pk} Maximum surge isolation voltage: 4076V_{pk}	Maximum isolation voltage V_{ISO}: 3750 V_{RMS}
Certification NO.: 40052786（basic isolation）	Certification number: E511334

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7.7. Electrical Characteristics

7.7.1. Driver

All typical specs are at V_{DDA} = 3.3V, V_{DDB} = 5V, T_A = 25°C,Min/Max specs are over recommended operating conditions unless otherwise specified.

Parameters		Test conditions	Minimum value	Typical value	Maximum value	Unit
$\|V_{OD1}\|$	Driver differential-output voltage	Open circuit voltage, unloaded bus.	2.7	4.6	5.5	V
$\|V_{OD2}\|$	Driver differential-output voltage	R_L = 54Ω, see Figure 8-1	1.5	3.6	3.18	V
$\Delta\|V_{OD}\|$	Change in differential output voltage between two states		-0.2		0.2	
V_{OC}	Common-mode output voltage		1		3	
ΔV_{OC}	change in steady-state common-mode output voltage between two states		-0.2		0.2	
I_{IL}	Input current	V_{DI}, V_{DE} = 0V or V_{DDA}	-20		20	μA
I_{os}	Short-circuit output current	DE=V_{DDA}, V_A or V_B = –7V	-150		150	mA
		DE=V_{DDA}, V_A or V_B = 12V				
CMTI	Common mode transient immunity	V_{CM} = 1500V; see Figure 8-8	85	100		kV/μs
C_I	Input capacitance	VI = V_{DDA}/ 2 + 0.4×sin(2πft), f = 1 MHz, V_{DDA} = 5 V		2		pF

7.7.2. Receiver

All typical specs are at V_{DDA} = 3.3V, V_{DDB} = 5V, T_A = 25°C. Min/Max specs are over recommended operating conditions unless otherwise specified.

Parameters		Test conditions	Minimum value	Typical value	Maximum value	Unit
V_{OH}	Output voltage high level	I_{OH} = -4mA;	V_{DDA}-0.4	4.8		V
V_{OL}	Output voltage low level	I_{OL} = 4mA;		0.2	0.4	V
$V_{IT+(IN)}$	Positive-going input threshold voltage			-100	-50	mV
$V_{IT-(IN)}$	Negative-going input threshold voltage		-200	-140		mV
$V_{I(HYS)}$	Receiver input hysteresis			30		mV
I_I	Bus input current	V_A or V_B = 12 V, other logic input pins are connected to 0 V		75	125	μA
		V_A or V_B = 12 V, powered down, other logic input pins are connected to 0 V		80	125	
		V_A or V_B = -7 V, other logic input pins are connected to 0 V	-100	-40		
		V_A or V_B = -7 V, powered down, other logic input pins are connected to 0 V	-100	-40		
I_{IH}	Input current on the $\overline{RE}$ pin	V_{RE} = HIGH	-20		20	μA
I_{IL}	Input current on the $\overline{RE}$ pin	V_{RE} = LOW	-20		20	μA
R_{ID}	Differential input resistance	Measured between A and B	96			kΩ
C_D	Differential input capacitance	Input signal is f = 1.5 MHz, V_{pp} = 1V sinusoidal signals; measured between A and B		12		pF
C_I	Single-ended input capacitance	VI = 0.4 × sin (2πft), f = 1MHz		18		pF

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7.8. Supply Current

All typical specs are at V_{DDA} = 3.3V, V_{DDB} = 5V, T_A = 25°C. Min/Max specs are over recommended operating conditions unless otherwise specified.

Parameters		Test conditions		Minimum value	Typical value	Maximum value	Unit
I_{CCA}	Logic side supply current	$\overline{RE}$ = 0 or 1, DE=0 or 1	V_{DDA} = 3.3V			7.6	mA
		$\overline{RE}$ = 0 or 1, DE =0 or 1	V_{DDA} = 5.0V			8.0	mA
I_{CCB}	Bus side supply current	$\overline{RE}$ = 0 or 1, DE =0, no load				6.8	mA

7.9. Switching Characteristics

7.9.1. Driver

All typical specs are at V_{DDA} = 3.3V, V_{DDB} = 5V, T_A = 25°C. Min/Max specs are over recommended operating conditions unless otherwise specified.

Parameters		Test conditions	Minimum value	Typical value	Maximum value	Unit
t_{PLH}, t_{PHL}	Driver Propagation Delay	See Figure 8-2, Figure 8-3; Figure 8-7		20	50	ns
PWD	Driver output skew $\lvert t_{PLH} - t_{PHL} \rvert$			3	12.5	ns
t_r	Differential output rise time			5	25	ns
t_f	Differential output fall time			5	25	ns
t_{PZH}/ t_{PZL}	Driver enable time			15	35	ns
t_{PHZ}/ t_{PLZ}	Driver disable time			15	35	ns

7.9.2. Receiver

All typical specs are at V_{DDA} = 3.3V, V_{DDB} = 5V, T_A = 25°C. Min/Max specs are over recommended operating conditions unless otherwise specified.

Parameters		Test conditions	Minimum value	Typical value	Maximum value	Unit
t_{PLH}, t_{PHL}	Receiver propagation delay	See Figure 8-4, Figure 8-5; Figure 8-6.		50	100	ns
PWD	Receiver output skew $\lvert t_{PLH} - t_{PHL} \rvert$				8	ns
t_r	Receiver output rise time			2.5	4	ns
t_f	Receiver output fall time			2.5	4	ns
t_{PHZ}/ t_{PLZ}	Receiver disable time			12	25	ns
t_{PZH}/ t_{PZL}	Receiver enable time			12	25	ns

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8. Parameter Measurement Information

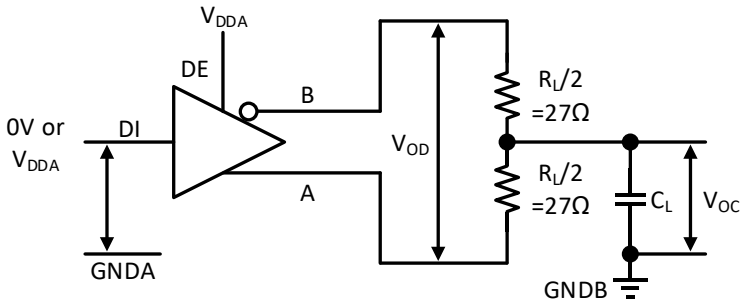

Figure 8-1. Driver DC test circuit

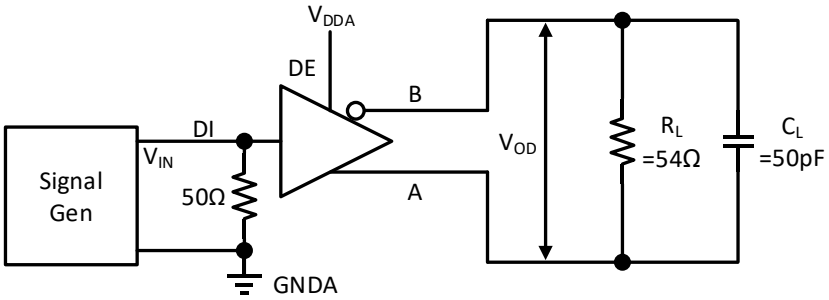

Figure 8-2. Driver propagation delay test circuit

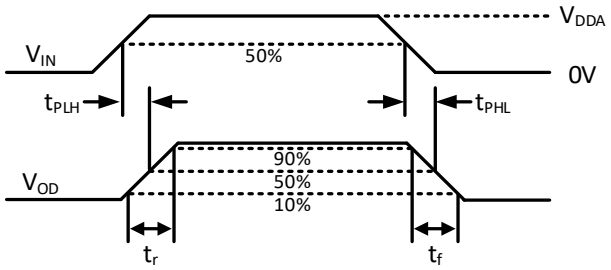

Figure 8-3. Driver propagation delay test waveform

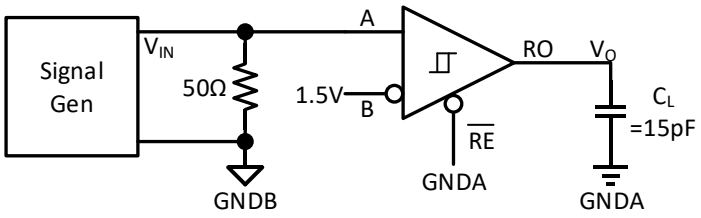

Figure 8-4. Receiver propagation delay test circuit

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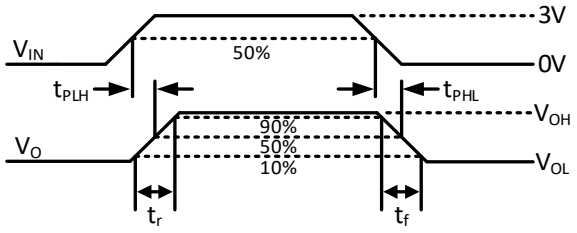

Figure 8-5. Receiver propagation delays test waveform

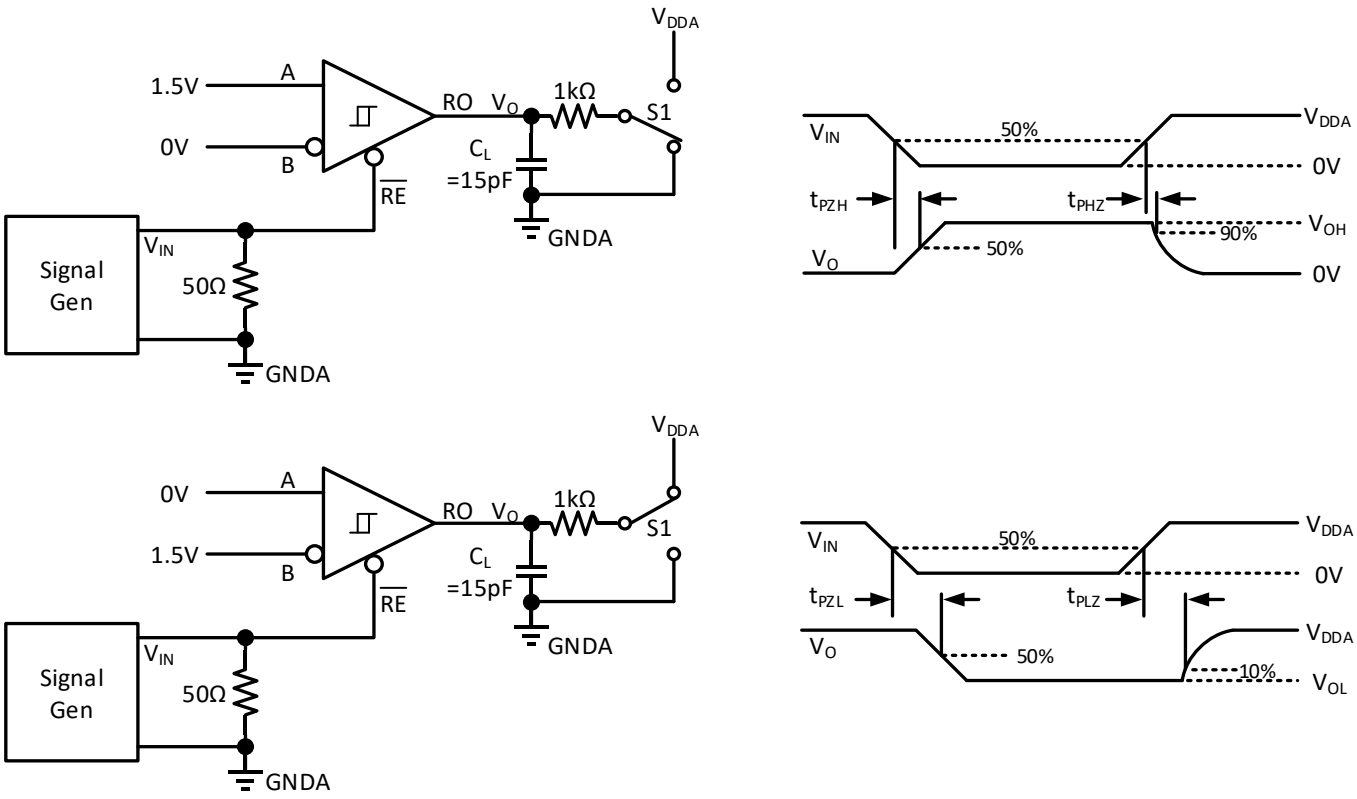

Figure 8-6. Receiver enable and disable timing

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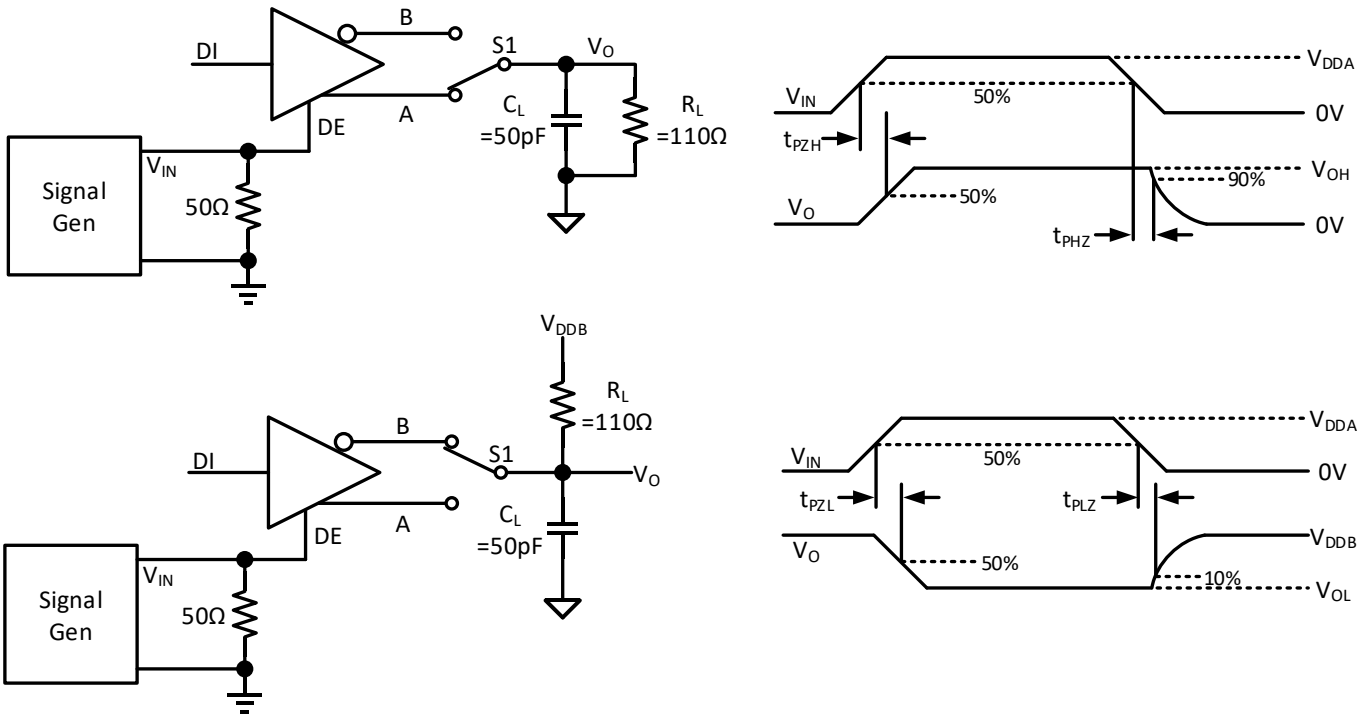

Figure 8-7. Driver enable and disable timing

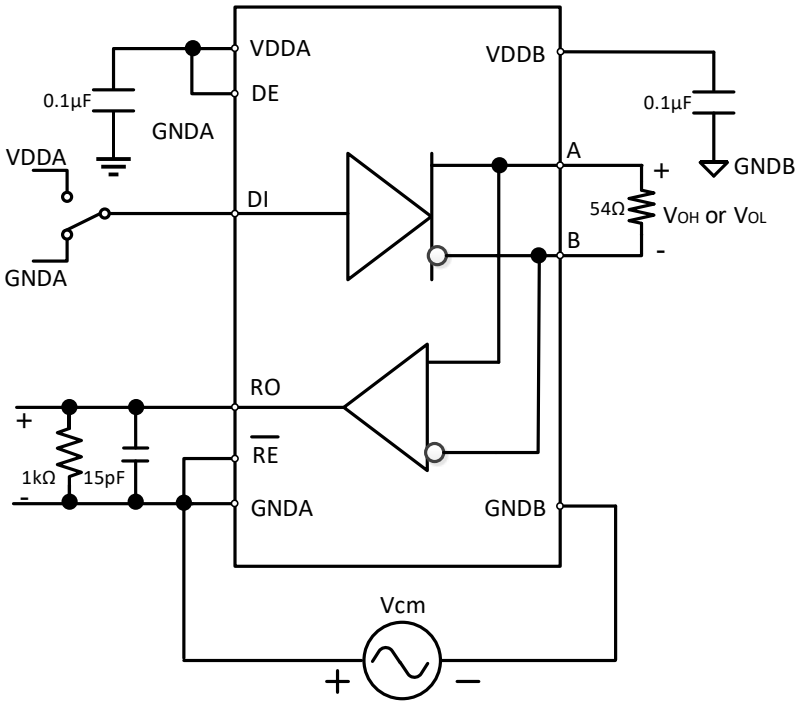

Figure 8-8. Common Mode Transient Immunity (CMTI) test

Notes:

1. R_L = 54 Ω for RS-485.
2. C_L includes external circuit (fixture and instrumentation etc.) capacitance.

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9. Detailed Description

The CA-IS2082B isolated, half-duplex RS-485 transceiver provides up to 3kV$_{RMS}$ of galvanic isolation between the cable side (bus-side) of the network and the controller side (logic-side). This device features up to 100 kV/μs common mode transient immunity, allow up to 20Mbps communication data rate across an isolation barrier. Robust isolation coupled with extended ESD protection and increased speed enables efficient communication in noisy environments, making them ideal for communication between logic-side and bus-side in a wide range of applications, such as motor drives, PLC communication modules, telecom system, elevators, HVACs etc. designs. Two mechanisms against excessive power dissipation caused by faults or bus contention. The first, a current limit on the output stage, provides immediate protection against short circuits over the entire common-mode voltage range. The second, a thermal shutdown circuit, forces the driver outputs into a high-impedance state.

9.1. Logic Input

The CA-IS2082B device includes three digital inputs on the logic side: receiver enable, driver enable and driver digital input. The driver enable pin DE has an internal weak pull-down to GNDA； while the digital input DI and receiver enable $\overline{RE}$ pins have an internal pull-up to V_{DDA}. All logic inputs use 1.5MΩ pull-up or pull-down resistor, see Figure 9-1 for the inputs equivalent circuit of the CA-IS2082B.

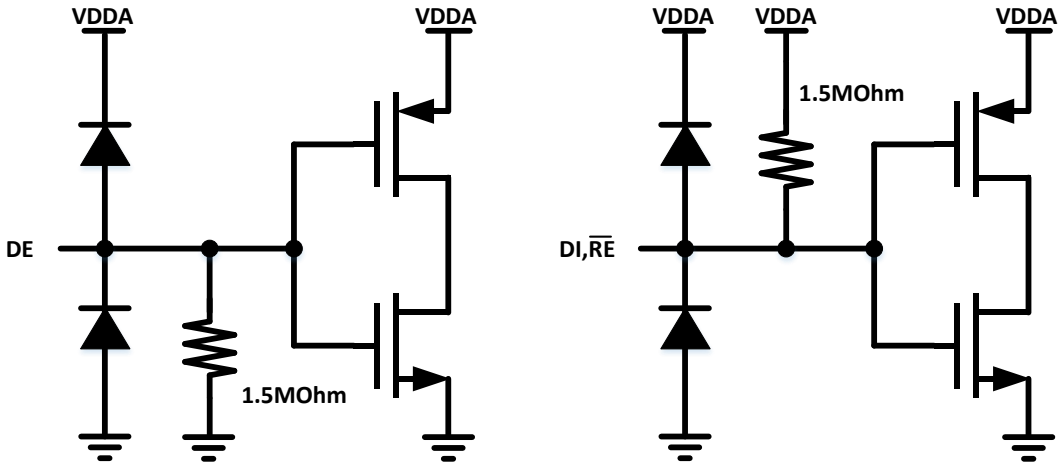

Figure 9-1. Input equivalent circuit

9.2. Receiver

The receiver reads the differential input from the bus line (A and B) and transfers this data as a single-ended, logic-level output RO to the controller. Drive the enable input $\overline{RE}$ low to enable the receiver. Drive $\overline{RE}$ logic high to disable the receiver and put receiver output RO in high impedance.

The CA-IS2082B RS-485 transceiver does not require fail-safe bias resistors because a true fail-safe feature is integrated into the device. The receiver's threshold for logic-high and logic-low are set at $V_{IT+(IN)}$ (-50mV, maximum) and $V_{IT-(IN)}$ (-200mV, minimum). If the differential receiver input voltage of V_A-V_B is greater than or equal to -50mV, RO is logic high when $\overline{RE}$ is low; RO is logic low when V_A-V_B is less than or equal to -200mV in case the receiver is enabled. Thereby eliminating the need for fail-safe bias resistors while complying fully with the RS-485 standard, as shown in Table 9-1 (the receiver truth table). Fail-safe feature is used to keep the receiver's output in a defined state when the receiver is not connected to the cable, or the cable is open or short.

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Table 9-1. CA-IS2082B Receiver Truth Table

VDDA	VDDB	DIFFERENTIAL INPUT	ENABLE	OUTPUT
		(V_A - V_B)	($\overline{RE}$)	(RO)
Powered up	Powered up	-50mV ≤ V_A - V_B	L	H
Powered up	Powered up	-200mV < V_A - V_B < -50mV	L	Indeterminate
Powered up	Powered up	V_A - V_B ≤ -200mV	L	L
Powered up	Powered up	X	H	Hi-Z
Powered up	Powered up	X	open	Hi-Z
Powered up	Powered up	Open/Short/Idle	L	H
Powered down	Powered up	X	X	Hi-Z
Powered up	Powered down	X	L	H

Notes:

1. X = don't care; H = high level; L = low level; Hi-Z = high impedance.
2. $\overline{RE}$ has an internal weak pull-up to VDDA.

9.3. Driver

The transmitter converts a single-ended input signal (DI) from the local controller to differential outputs for the bus lines A and B. The truth table for the transmitter is provided in Table 9-2. The driver outputs and receiver inputs are protected from ±8kV electrostatic discharge (ESD) to GNDB on the cable side. The driver's outputs also feature short-circuit protection and thermal shutdown function. The driver's enable pin DE has an internal weak pull-down to GNDA and driver input pin DI has an internal weak pull-up to VDDA.

Table 9-2. CA-IS2082B Transmitter Truth Table

VDDA	VDDB	INPUT	ENABLE INPUT	OUTPUTS	
		(DI)	(DE)	A	B
Powered up	Powered up	H	H	H	L
Powered up	Powered up	L	H	L	H
Powered up	Powered up	X	L	Hi-Z	Hi-Z
Powered up	Powered up	X	Open	Hi-Z	Hi-Z
Powered up	Powered up	Open	H	H	L
Powered down	Powered up	X	X	Hi-Z	Hi-Z
Powered up	Powered down	X	X	Hi-Z	Hi-Z
Powered down	Powered down	X	X	Hi-Z	Hi-Z

Notes:

1. X = don't care; H = high level; L = low level; Hi-Z = high impedance.
2. DE pin has an internal weak pull-down to GNDA. DI pin has an internal weak pull-up to VDDA.

9.4. Protection Functions

9.4.1. Signal Isolation

The CA-IS2082B device integrates digital galvanic isolators using Chipanalog's capacitive isolation technology based on the ON-OFF keying (OOK) modulation scheme, allowing data transmission between the controller side and cable side of the transceiver with different power domains.

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9.4.2. Thermal Shutdown

If the junction temperature of the CA-IS2082B device exceeds the thermal shutdown threshold $T_{J(shutdown)}$ (160°C, typ.), the driver's output is set to high-impedance state. The shutdown condition is cleared when the junction temperature drops to normal operation temperature range of the device.

9.4.3. Current-Limit

The CA-IS2082B protects the transmitter output stage against a short-circuit to a positive or negative voltage over the common mode voltage range of -7V to 12V by limiting the driver current. However, this will cause large supply current and dissipation. Thermal shutdown further protects the devices from excessive temperatures that may result from a short circuit. The transmitter returns to normal operation once the short is removed.

10. Applications Information

10.1. Typical Application

The CA-IS2082B half-duplex RS-485 transceiver commonly used for asynchronous data transmissions. It's driver and receiver enable pins allow for the configuration of different operating modes. An RS-485 bus consists of multiple transceivers connecting in parallel to a bus cable, as seen in the following typical application circuit Figure 10-1, this half-duplex network reduces overall cabling requirements.

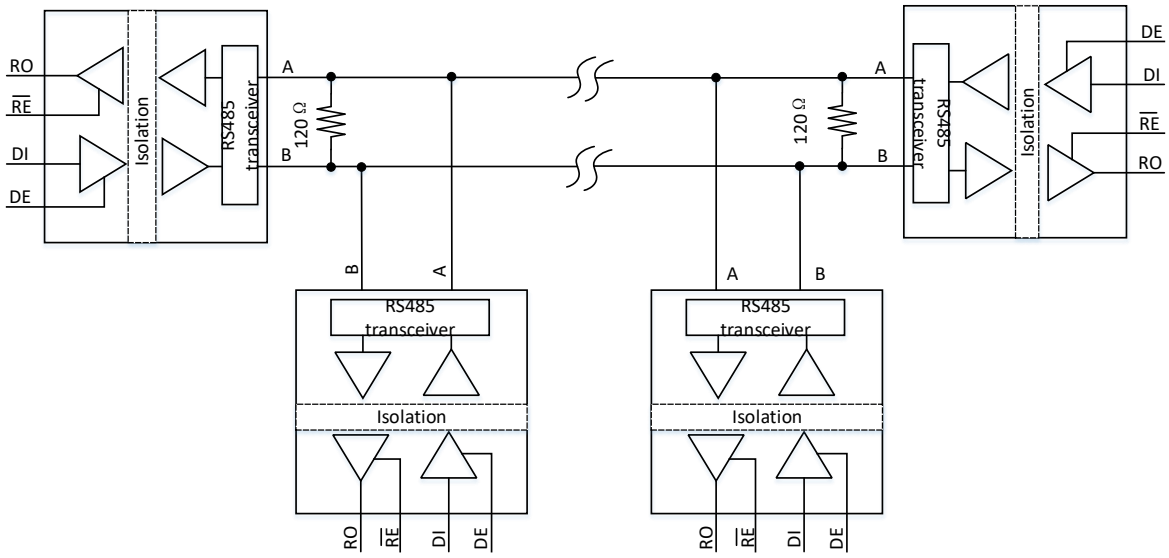

Figure 10-1. Typical isolated half-duplex RS-485 application circuit

According to RS-485 standard, the maximum recommended data rate in the RS-485 network is 20Mbps, which can be achieved at a maximum cable length of 40ft (12m). The absolute maximum distance is 4000ft (1.2km) of cable, at which point, data rate is limited to 100kbps. These were the specifications made in the original standard, new RS-485 transceivers and cables are pushing the limit of RS-485 far beyond its original definitions. However, the maximum data rate is still limited by the bus loading, number of nodes, cable length etc. factors. For RS-485 network design, margin must be given for signal loss across the system and cabling, parasitic loadings, timing, network imbalances, ground offsets and signal integrity thus a practical maximum data rate, number of nodes often lower. To minimize reflections, terminate the line at both ends with a termination resistor (120Ω in the typical application circuits), whose value matches the characteristic impedance (Z_0) of the cable, and keep stub lengths off the main line as short as possible. As a general rule moreover, termination resistors should be placed at both far ends of the cable. This method, known as parallel termination, generally allows for higher data rates over longer cable length. Note that the maximum data rate for the CA-IS2082B transceiver is 20Mbps.

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10.2. 256 transceivers on the bus

The maximum number of transceivers or receivers allowed depends on how much each device loads down the system. All devices connected to an RS-485 network should be characterized in regard to multiples or fractions of unit loads. The maximum number of unit loads allowed one twisted pair cable, assuming a properly terminated cable with a characteristic impedance of 120Ω or more, is 32 (375Ω). The CA-IS2082B transceiver has a 1/8-unit load (96kΩ) receiver, which allows up to 256 transceivers, connected in parallel, on one communication line.

10.3. PCB Layout

It is recommended to design an isolation channel underneath the isolator that is free from ground and signal planes. Any galvanic or metallic connection between the cable side and logic side will defeat the isolation. To make sure device operation is reliable at all data rates and supply voltages, the decoupling capacitors between VDDA and GNDA and between VDDB and GNDB are recommended, see Figure 10-2 the CA-IS2082B typical application circuit. The capacitors should be located as close as possible to the IC to minimize inductance.

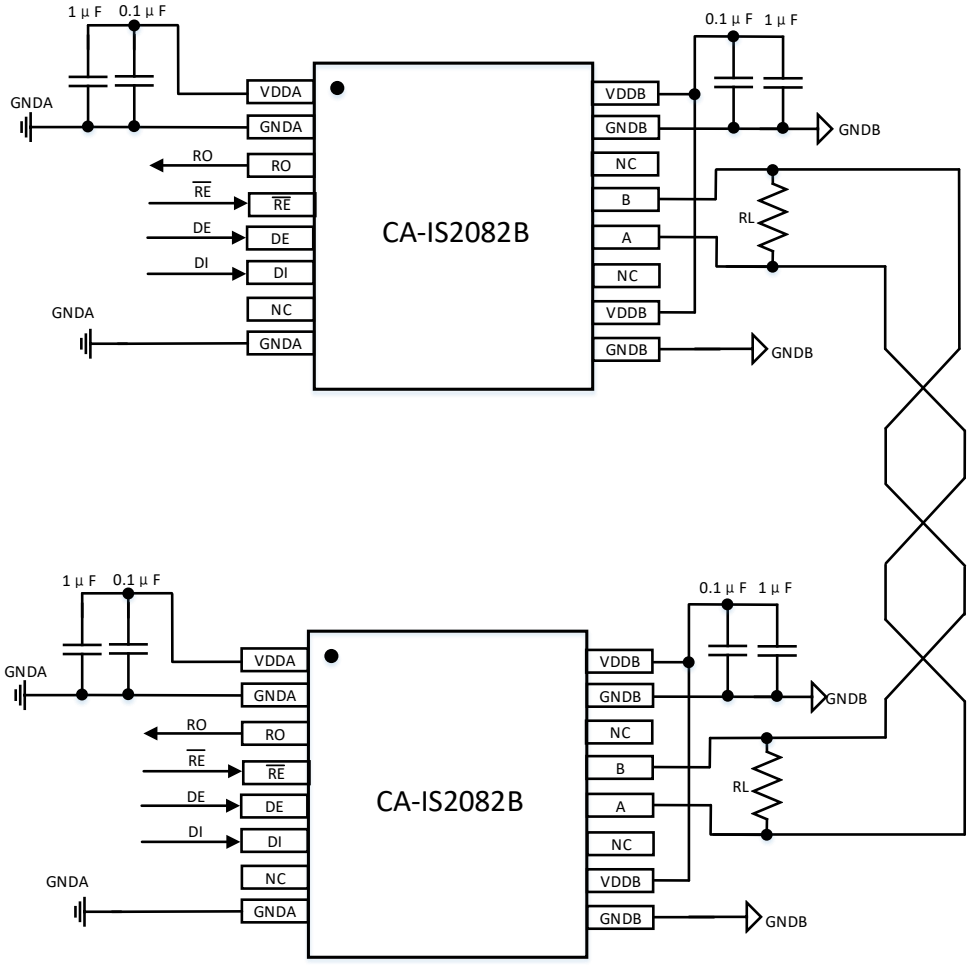

Figure 10-2. CA-IS2082B Typical application circuit

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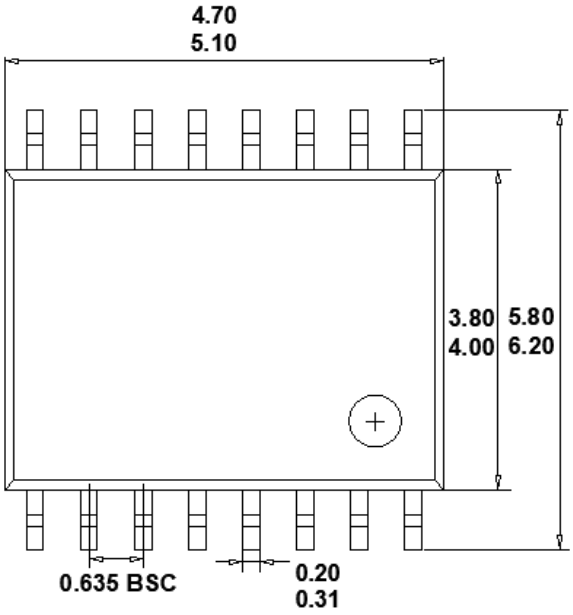
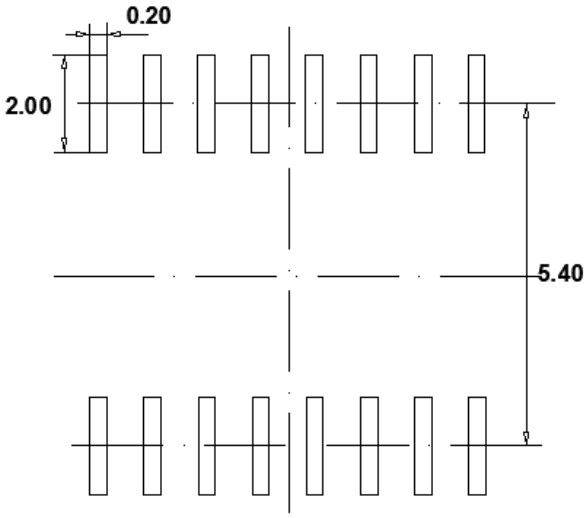
11. Package Information

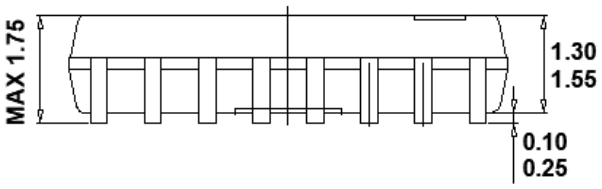
The following diagrams illustrate the dimension diagram of CA-IS2082B isolated RS-485 transceiver packaged in SSOP16(B) package and the suggested pad dimension diagram, wherein dimensions are in millimeters.



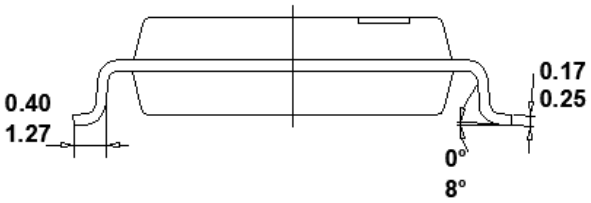
TOP VIEW



RECOMMENDED LAND PATTERN



BOTTOM VIEW



LEFT SIDE VIEW

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12. Soldering Temperature (reflow) Profile

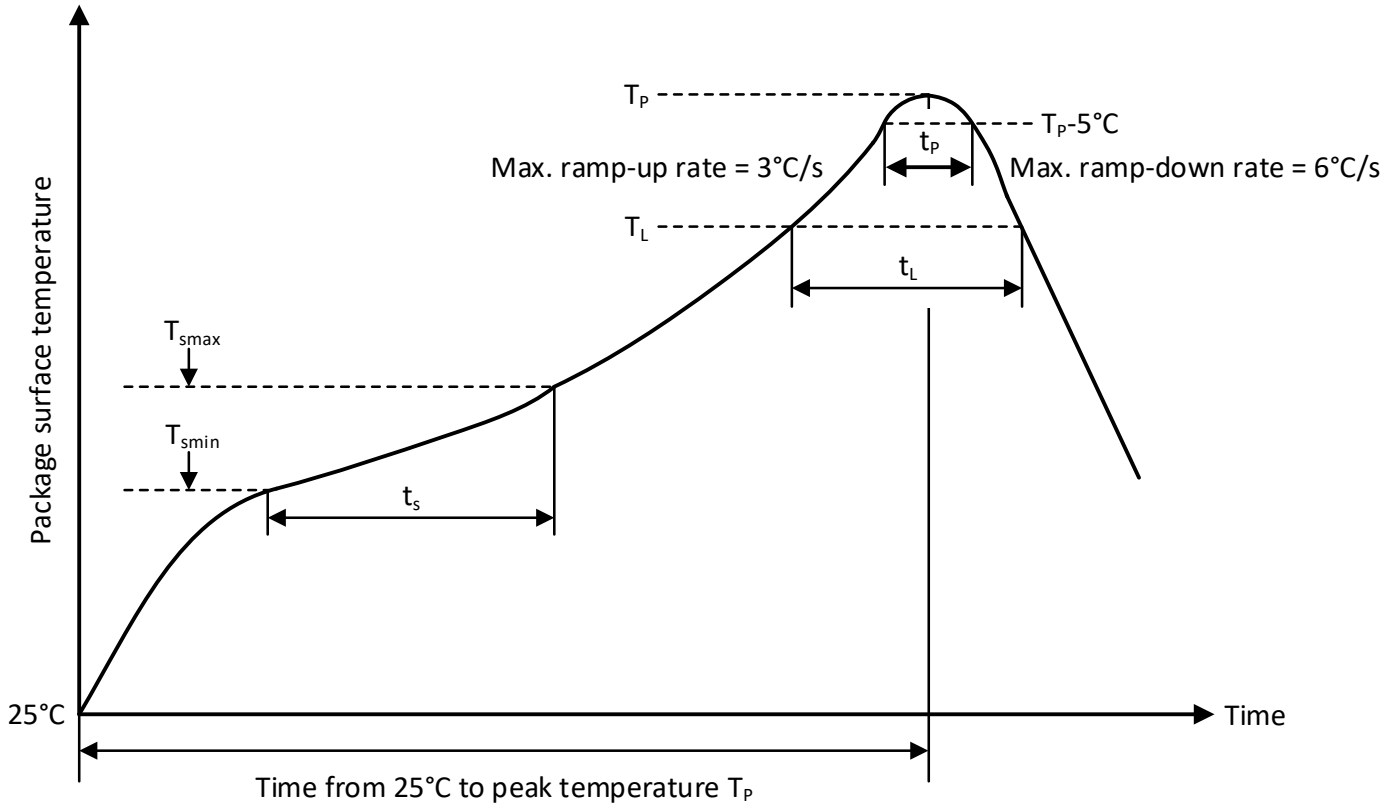

Figure. 12-1 Soldering Temperature (reflow) Profile

Table 12-1 Soldering Temperature Parameters

Profile Feature	Pb-Free Soldering
Ramp-up rate (T_L = 217°C to peak T_P)	3°C/s max
Time t_s of preheat temp (T_{smin} = 150°C to T_{smax} = 200°C)	60~120 seconds
Time t_L to be maintained above 217°C	60~150 seconds
Peak temperature T_P	260°C
Time t_P within 5°C of actual peak temp	30 seconds max
Ramp-down rate (peak T_P to T_L = 217°C)	6°C/s max
Time from 25°C to peak temperature T_P	8 minutes max

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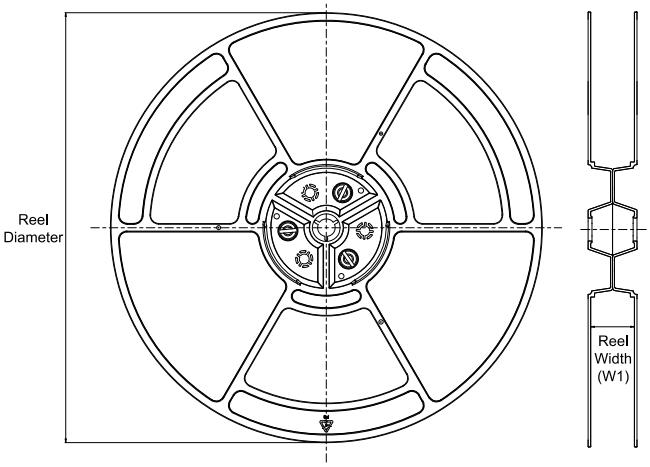
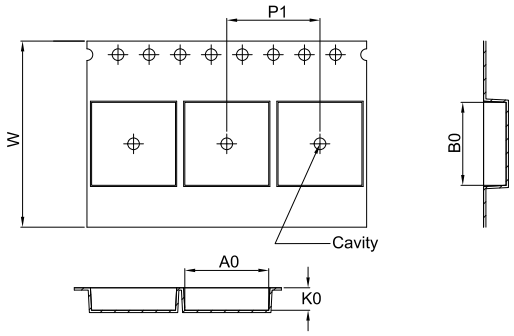
13. Tape and Reel Information

REEL DIMENSIONS

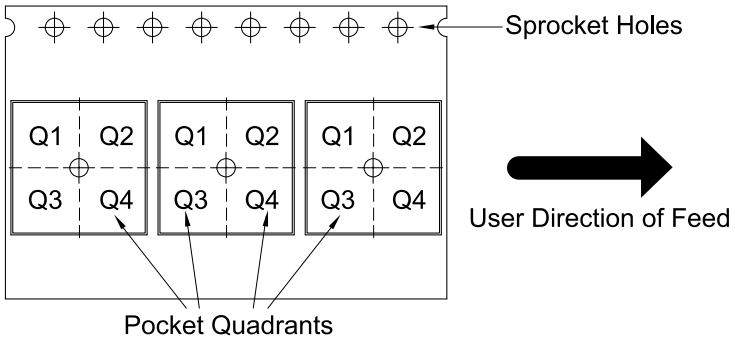


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CA-IS2080B	SSOP	B	16	2500	330	12.4	6.4	5.2	2.1	8.0	12.0	Q1

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