1.5W, 5kV$_{RMS}$ Isolated DC-DC Converter with Integrated Transformer

1 Features

- **Complete Switch Mode Power Supply**
  - High integration with internal transformer
  - Soft-start reduces input inrush current and output overshoot
  - Hiccup current-limit protection
  - Thermal shutdown
- **4.5 V to 5.5 V Input Voltage Range**
- **Selectable Output voltages**
  - 3.3V and 5V output options
  - 3.7V and 5.4V output options provide headroom voltage to power LDO
- **Delivers up to 1.5W(5V/300mA) Typical Output Power**
- **Excellent Load Transient Response**
- **Complies with CISPR32 Class B Radiated Emissions**
- **Up to ±3kV HBM and ±2kV CDM ESD protection**
- **Robust Galvanic Isolation Barrier**
  - High lifetime: > 40 years
  - Up to 5kV$_{RMS}$ isolation rating
  - ±150 kV/μs typical CMTI
- **Wide Operating Temperature Range: -40°C to 125°C**
- **Low Profile SOIC16-WB (10.30mm × 7.50) Package**
- **Safety-Related Certifications (Pending)**
  - VDE certification according to DIN EN IEC60747-17(VDE 0884-17):2021-10
  - UL certification according to UL1577
  - CQC certification according to GB4843.1-2022

2 Applications

- Tractor inverters
- Onboard chargers and DC/DC converters
- Battery management system
- Electric compressor

3 General Description

The CA-IS3115AW-Q1 is a family of complete isolated DC-DC converters with up to 5kV$_{RMS}$ isolation rating. These devices integrate most of the components needed for an isolated power supply —switching controller, power switches, transformer, soft-start, protection circuit etc. — into a single, compact SOIC package. The result is an efficient and compact fully integrated solution that is easy to comply with EMI requirements and makes power-supply isolation design as easy as possible. Operating over an input voltage range of 4.5V to 5.5V, the CA-IS3115AW-Q1 devices provide a fixed output voltage of 3.3V, 3.7V, 5V or 5.4V set by pin SEL. 3.7V and 5.4V output options provide headroom voltage to power an LDO. Only output, input bypass capacitors, and a pull-up resistor for 3.7V or 5.4V outputs are needed to finish the design.

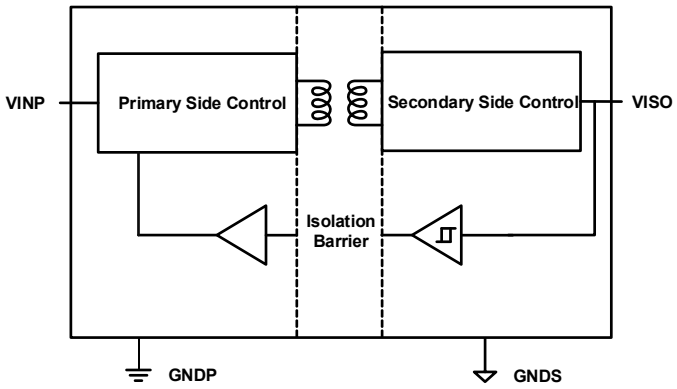
The CA-IS3115AW-Q1 devices feature a unique control scheme, which can quickly respond to load transient and accurately regulate the output voltage. The devices are capable of delivering a load up to 1.5W output power and offering soft-start, current limit, short-circuit protection and thermal shutdown protection features to better enhance the reliability of the system. The CA-IS3115AW-Q1 devices include an enable input pin (EN). Connect the EN pin to the VINP input voltage or force this pin high to turn on the DC-DC converter. Force this pin low to disable the device and enter shutdown mode. In shutdown mode, the device stops switching operation with microampere standby supply current.

The CA-IS3115AW-Q1 devices are available in wide-body SOIC16 package with creepage and clearance > 8mm, and operate over -40°C to +125°C temperature range.

Device Information

Part number	Package	Package size (NOM)
CA-IS3115AW-Q1	SOIC16-WB(W)	10.30 mm × 7.50 mm

Simplified Block Diagram



4 Ordering Information

Table 4-1. Ordering Information

Part #	Output Power (W)	Isolation Rating(kV_{RMS})	Package
CA-IS3115AW-Q1	1.5	5.0	SOIC16-WB

Table of Contents

5 Revision history

Revision Number	Description	Revised Date	Page Changed
Preliminary Version	N/A	2023/10/17	N/A
Version 1.00	Update isolation ratings	2023/12/01	6,7
Version 1.01	Adds output derating curves	2024/01/03	11,12
Version 1.02	Adds Short circuit protection function description	2024/01/09	14
Version 1.03	Update VDE,UL,CQC,TUV information Update the test conditions of V_{IOSM}	2024/04/16	1,6,7
Version 1.04	Update the test conditions of $VISO_{(LOAD)}$	2024/05/14	8

6 Pin Configuration and Description

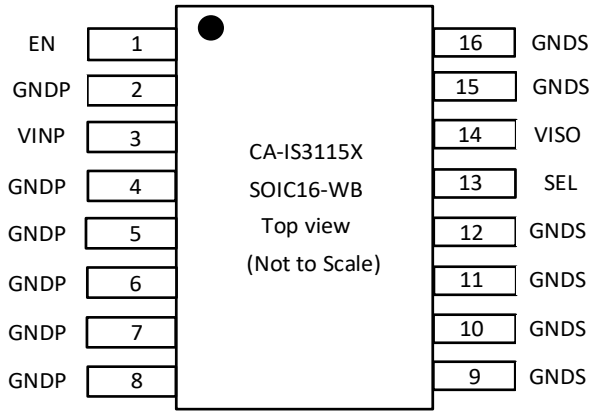


Figure 6-1. CA-IS3115AW-Q1 Top View

Table 6-1. CA-IS3115AW-Q1 Pin Description

Pin name	Pin number	Type	Description
EN	1	Input	Enable input, active-high. Force this pin high to enable the device. Force this pin low to disable the device and put the device into shutdown mode.
VINP	3	Power	Primary side supply input. Connect VINP to GNDP with both 0.1μF and 10μF capacitors as close to the device(pin 3 and pin 4) as possible.
GNDP	2, 4, 5, 6, 7, 8	GND	Primary side local ground.
GNDS	9, 10, 11, 12, 15, 16	GND	Secondary side ground return connection for V_{ISO}.
SEL	13	Input	Output voltage V_{ISO} select pin: V_{ISO} = 5.0 V when SEL is shorted to VISO; V_{ISO} = 5.4 V when SEL is connected to VISO through a 100kΩ resistor; V_{ISO} = 3.3 V when SEL is shorted to GNDS; V_{ISO} = 3.7V when SEL is connected to GNDS through a 100kΩ resistor. Don't leave SEL pin open.
VISO	14	Power	Isolated supply voltage pin. Connnect VISO to GNDS with both 0.1μF and 10μF capacitors as close to the device(pin 14 and pin 15) as possible.

7 Specifications

7.1 Absolute Maximum Ratings[1, 2]

Parameters		Minimum value	Maximum value	Unit
V_{INP}	Power supply voltage	-0.5	6.0	V
V_{ISO}	Isolated supply voltage	-0.5	6.0	V
EN	EN input voltage	-0.5	V_{INP}+0.3[3]	V
SEL	SEL input voltage	-0.5	V_{ISO}+0.3[3]	V
T_J	Junction temperature	-40	150	°C
T_{STG}	Storage temperature range	-65	150	°C

Notes:
1. The stresses listed under "Absolute Maximum Ratings" are stress ratings only, not for functional operation condition. Exposure to absolute maximum rating conditions for extended periods may cause permanent damage to the device.
2. All voltage values are with respect to the local ground (GNDP or GNDS) and are peak voltage values.
3. Maximum voltage must not be exceed 6 V.

7.2 ESD Ratings

		Value	Unit
V_{ESD} Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1]	±3000	V
	Charged device model (CDM), per JEDEC Specification JESD22-C101, all pins[2]	±2000	

Notes:
1. Per JEDEC document JEP155, 500V HBM allows safe manufacturing of standard ESD control process.
2. Per JEDEC document JEP157, 250V CDM allows safe manufacturing of standard ESD control process.

7.3 Recommended Operating Conditions

Parameters		Minimum value	Typical value	Maximum value	Unit
V_{INP}	Power supply voltage	4.5	5	5.5	V
V_{EN}	EN input voltage	0		5.5	V
V_{ISO}	Isolated supply voltage	0		5.7	V
V_{SEL}	SEL input voltage	0		5.7	V
T_A	Ambient Temperature	-40		125	°C
T_J	Junction temperature	-40		150	°C

7.4 Thermal Information

Thermal Metric		CA-IS3115AW-Q1 SOIC16-WB(W)	Unit
$R_{\theta JA}$	Junction-to-ambient thermal resistance	68	°C/W
$R_{\theta JC}$	Junction-to-case thermal resistance	18	

7.5 Power Ratings

Parameters		Test Conditions	Minimum value	Typical value	Maximum value	Unit
P_D	Power dissipation	V_{INP} = 5.5V, V_{ISO} = 5.4V, 300mA output current			3	W

7.6 Insulation Specifications

Parameters		Test Conditions	Value	Unit
CLR	External clearance	Shortest terminal-to-terminal distance through air	8	mm
CPG	External creepage	Shortest terminal-to-terminal distance across the package surface	8	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	28	μm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11)； IEC 60112	>600	V
	Material group	According to IEC 60664-1	I	
	IEC 60664-1 over-voltage category	Rated mains voltage ≤ 300 V_{RMS}	I-IV	
		Rated mains voltage ≤ 600 V_{RMS}	I-IV	
		Rated mains voltage ≤ 1000 V_{RMS}	I-III	
DIN V VDE V 0884-17:2021-10[1]				
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	2121	V_{PK}
V_{IOWM}	Maximum operating isolation voltage	AC voltage; time-dependent dielectric breakdown (TDDB) test	1500	V_{RMS}
		DC voltage	2121	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t=60 s (qualification); $V_{TEST} = 1.2 \times V_{IOTM}$, t=1 s (100% product test)	7070	V_{PK}
V_{IOSM}	Maximum surge isolation voltage[2]	Test method per IEC 62368-1, 1.2/50 μs waveform, $V_{TEST} = 1.6 \times V_{IOSM}$ (qualification)	8000	V_{PK}
q_{pd}	Apparent charge[3]	Method a, after input/output safety tests subgroup 2/3, $V_{ini} = V_{IOTM}$, t_{ini} = 60s; $V_{pd(m)} = 1.2 \times V_{IORM}$, t_m = 10s	≤5	pC
		Method a, after environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, t_{ini} = 60s; $V_{pd(m)} = 1.6 \times V_{IORM}$, t_m = 10s	≤5	
		Method b1, at routine test (100% production test) and preconditioning (sample test) $V_{ini} = 1.2 \times V_{IOTM}$, t_{ini} = 1s; $V_{pd(m)} = 1.875 \times V_{IORM}$, t_m = 1s	≤5	
C_{IO}	Barrier capacitance, input to output[4]	V_{IO} = 0.4 × sin (2πft), f = 1 MHz	3.5	pF
R_{IO}	Isolation resistance , input to output[4]	V_{IO} = 500 V, T_A = 25°C	$>10^{12}$	Ω
		V_{IO} = 500 V, 100°C ≤ T_A ≤ 125°C	$>10^{11}$	
		V_{IO} = 500 V at T_S = 150°C	$>10^{9}$	
	Pollution degree		2	
UL 1577				
V_{ISO}	Maximum isolation voltage	$V_{TEST} = V_{ISO}$, t = 60 s (certified) $V_{TEST} = 1.2 \times V_{ISO}$, t = 1 s (100% production test)	5000	V_{RMS}

Notes:

1. This coupler is suitable for “safe electrical insulation” only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
2. Devices are immersed in oil during surge characterization.
3. The characterization charge is discharging charge (pd) caused by partial discharge.
4. Capacitance and resistance are measured with all pins on field-side and logic-side tied together.

7.7 Safety-Related Certifications

VDE	UL	CQC
Certified according to DIN V VDE V 0884-17:2021-10	Certified according to UL 1577 Component Recognition Program	Certified according to GB4943.1-2011
Maximum transient isolation voltage: 7070 V_{PK} Maximum repetitive peak isolation voltage: 2121 V_{PK} Maximum surge isolation voltage: 8000 V_{PK}	Maximum isolation voltage: 5000 V_{RMS}	reinforced isolation (Altitude≤5000m)
Certificate number: 40057278 （reinforced isolation）	Certificate number: E511334	Certification number: CQC23001406424

7.8 Electrical Characteristics

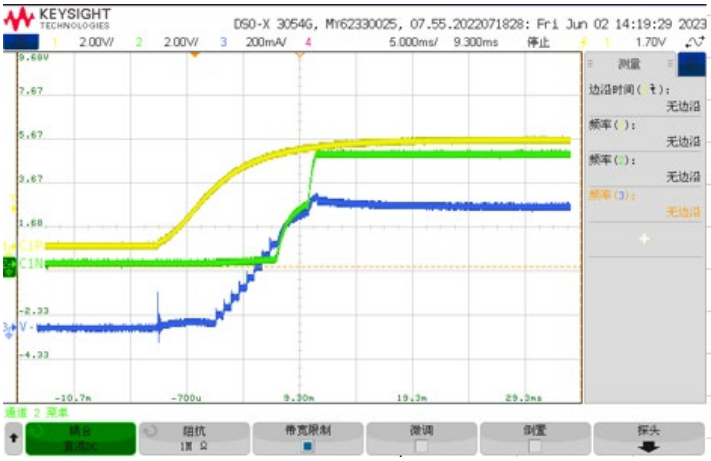
Over operating temperature range T_A = -40 to 125°C, V_{INP} = 4.5V to 5.5V, SEL connected to V_{ISO}, C_{VINP} = C_{VISO} = 10µF, unless otherwise specified. All typical specs are at T_A = 25°C and V_{INP} = 5V.

Parameters		Test Conditions	Minimum value	TYP	Maximum value	Unit
Power Supply Input						
I_{VINP_SD}	V_{INP} shutdown current	EN = LOW		0.5	30	µA
I_{VINP_O}	V_{INP} quiescent current I_{OUT} = 0% load	EN = HIGH, SEL connected to V_{ISO} (5V output)		4.9	20	mA
		EN = HIGH, SEL 100kΩ to VISO (5.4Voutput)		5.2	20	mA
		EN = HIGH, SEL connected to GNDS (3.3V output)		4.1	20	mA
		EN = HIGH, SEL 100kΩ to GNDS (3.7V output)		4.3	20	mA
I_{VINP_SC}	DC current from VINP supply under short circuit on VISO	VISO short to GNDS		77	100	mA
V_{UVLO+}	Input undervoltage lockout rising threshold			2.7	3	V
V_{UVLO-}	Input undervoltage lockout falling threshold		2.1	2.3		V
$V_{HYS(UVLO)}$	Input undervoltage lockout hysteresis			0.4	0.6	V
EN, SEL pins						
V_{IH_EN}	EN Input threshold, logic HIGH		0.7V_{INP}			V
V_{IL_EN}	EN Input threshold, logic LOW				0.3V_{INP}	V
I_{EN}	Input leakage current	V_{INP} = 5V, V_{EN} = 5V		10	20	µA
Isolated DC-DC Converter						
V_{ISO}	Isolated output voltage	SEL connected to V_{ISO} (5V output), I_{ISO} = 150mA	4.75	5.0	5.25	V
		SEL 100KΩ to VISO (5.4V output), I_{ISO} = 150mA	5.13	5.4	5.67	
		SEL connected to GNDS (3.3V output), I_{ISO} = 200mA	3.13	3.3	3.47	
		SEL 100KΩ to GNDS (3.7V output), I_{ISO} = 200mA	3.51	3.7	3.89	
I_{LOAD_MAX}	Maximum load currrent	SEL connected to V_{ISO} (5V output)	240	300		mA
		SEL 100KΩ to VISO (5.4V output)	240	300		
		SEL connected to GNDS (3.3V output)	320	400		
		SEL 100KΩ to GNDS (3.7V output)	320	400		
$VISO_{(RIP)}$	Voltage ripple on isolated supply output (pk-pk)	20MHz bandwidth, SEL short to VISO (5V input, 5V or 5.4V output),I_{ISO} = 150mA		65		mV
		20MHz bandwidth, SEL short to GNDS (5V input, 3.3V or 3.7V output), I_{ISO} = 200mA		55		
$VISO_{(LINE)}$	Line regulation	SEL short to VISO (5V or 5.4V output), I_{ISO} = 150mA, V_{INP} = 4.5V to 5.5 V		4	20	mV/V
		SEL short to GNDS (3.3V or 3.7V output), I_{ISO} = 200mA, V_{INP} = 4.5V to 5.5V		4	20	
$VISO_{(LOAD)}$	Load regulation	SEL short to VISO (5V input, 5V or 5.4V output), I_{ISO} = 0 to 240mA		0.5%	2%	
		SEL short to GNDS (5V input, 3.3V or 3.7V output), I_{ISO} = 0 to 320mA		0.5%	2%	
EFF	Efficiency@maximum load current	I_{ISO} = 300 mA, C_{LOAD} = 0.1µF || 10µF; V_{ISO}=5V, 5.4V		60%		
		I_{ISO} = 300mA, C_{LOAD} = 0.1µF || 10µF; V_{ISO}=3.3V,3.7V		50%		
CMTI	Common-mode transient immunity	Slew Rate of GNDP versus GNDS, V_{CM}=1200V_{RMS}	±150			kV/µs
t_{RISE}	V_{ISO} rise time	10% to 90%, V_{ISO} =3.3V, 3.7V, 5.0V, 5.4V		1		ms
V_{ISO} ripple voltage (peak to peak)		10% to 90% load step with 10mA/µs slew-rate; V_{ISO} ripple voltage difference at two loads		100		mV
V_{ISO} load transient response				5		µs

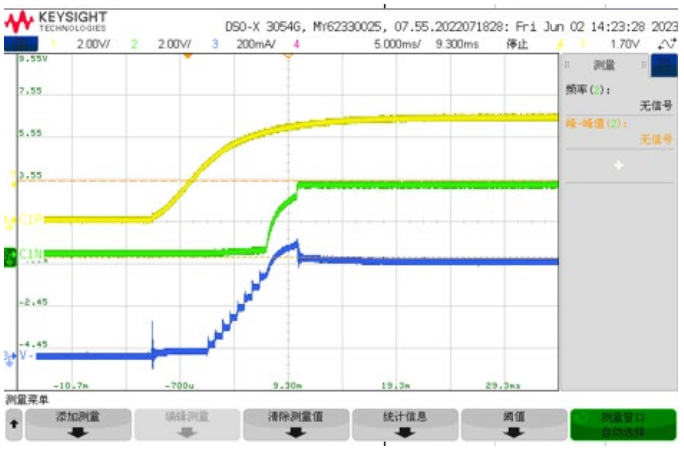
7.9 MSL

Parameters	Standard	Level
MSL	IPC/JEDEC J-STD-020D.1	MSL 3

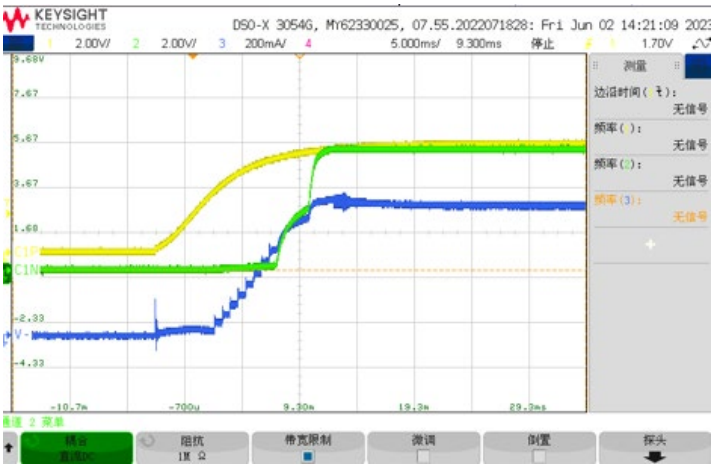
7.10 Typical Operating Characteristics



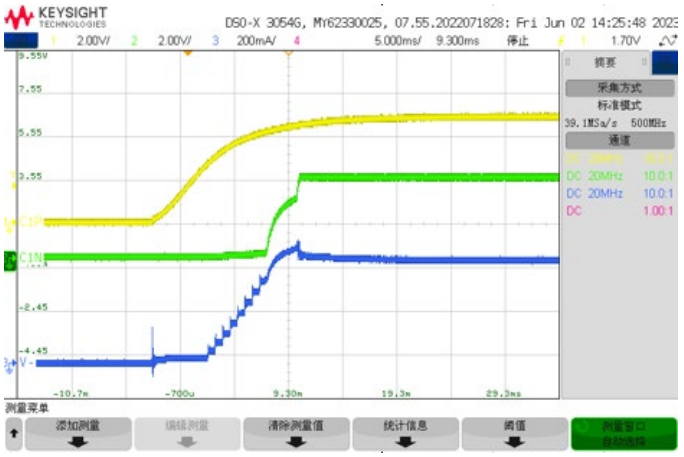
Soft-start waveform: V_{INP} =5V(yellow), V_{ISO}=5V(green), I_{ISO}=300mA(blue)



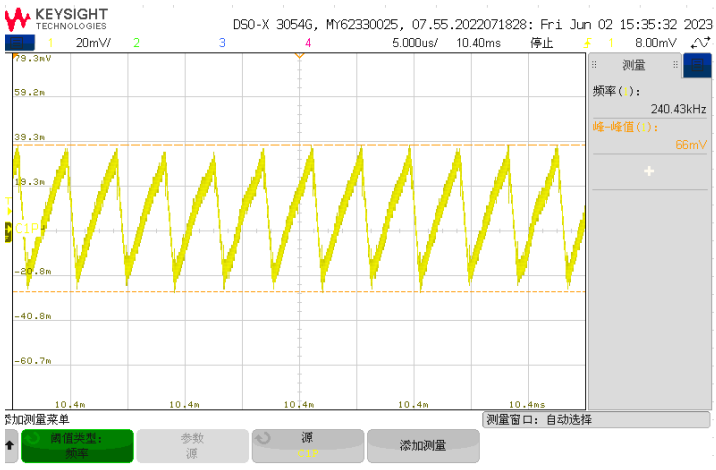
Soft-start waveform: V_{INP} =5V(yellow), V_{ISO}=3.3V(green), I_{ISO}=300mA(blue)



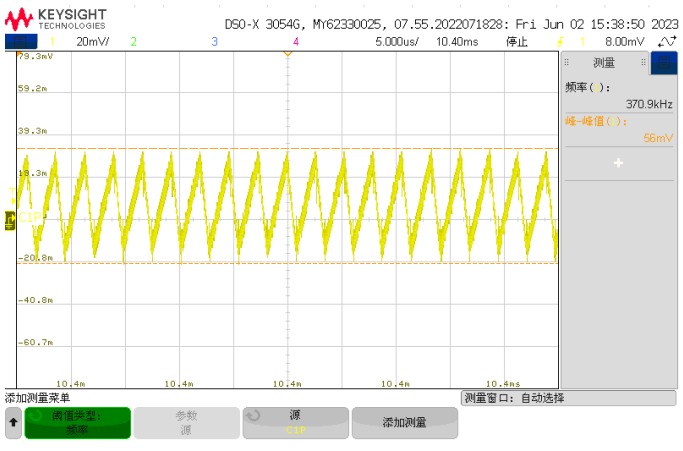
Soft-start waveform: V_{INP} =5V(yellow), V_{ISO}=5.4V(green), I_{ISO}=300mA(blue)



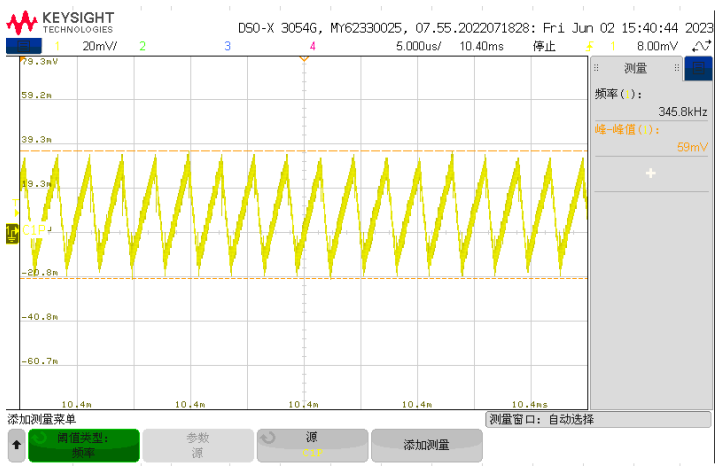
Soft-start waveform: V_{INP} =5V(yellow), V_{ISO}=3.7V(green), I_{ISO}=300mA(blue)



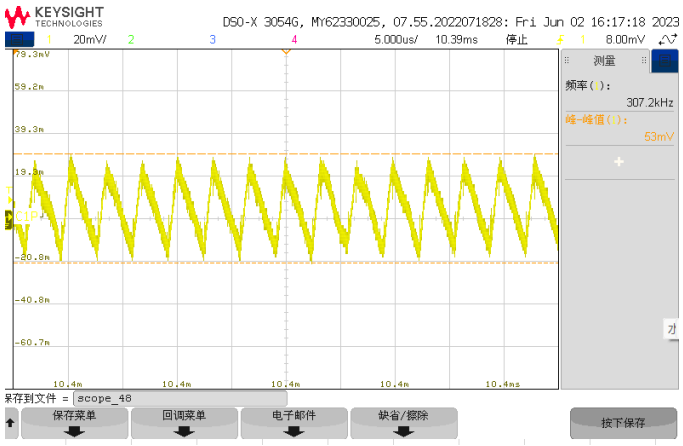
V_{ISO} ripple voltage(peak to peak): V_{INP} =5V, V_{ISO}=5V, I_{ISO}=300mA



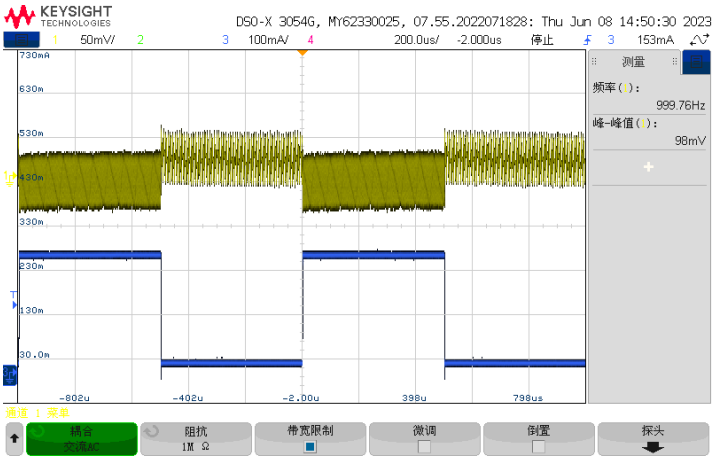
V_{ISO} ripple voltage(peak to peak): V_{INP} =5V, V_{ISO}=3.3V, I_{ISO}=300mA



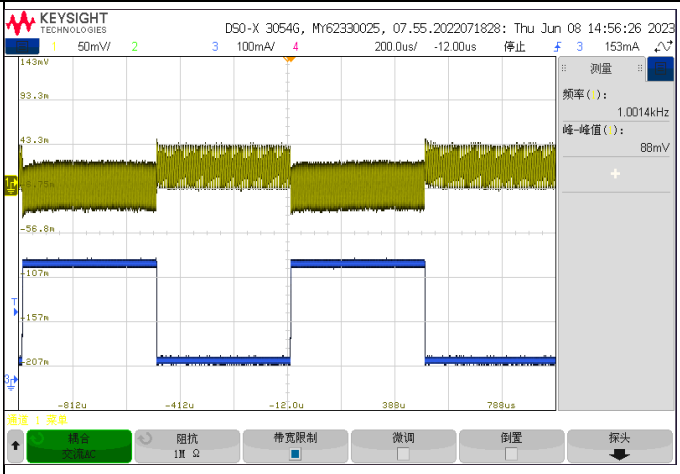
V_{ISO} ripple voltage(peak to peak): V_{INP} =5V, V_{ISO}=5.4V, I_{ISO}=300mA



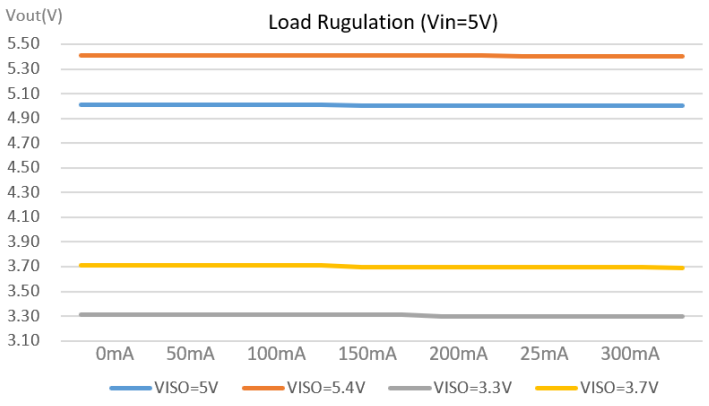
V_{ISO} ripple voltage(peak to peak): V_{INP} =5V, V_{ISO}=3.7V, I_{ISO}=300mA



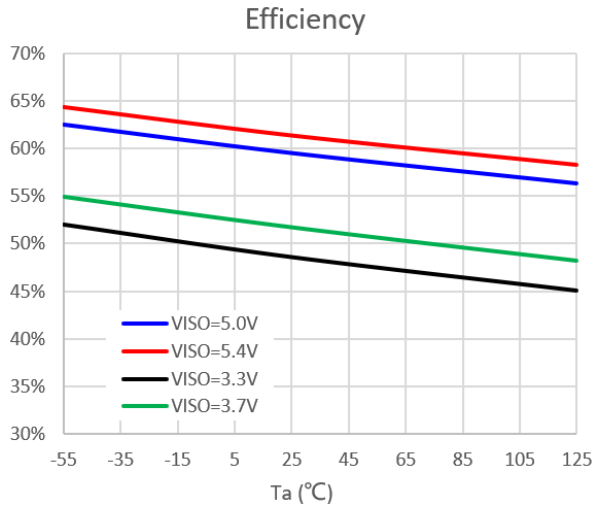
V_{ISO} Load transient response: V_{INP} =5V, V_{ISO}=5V
Load-current: 30mA/270mA



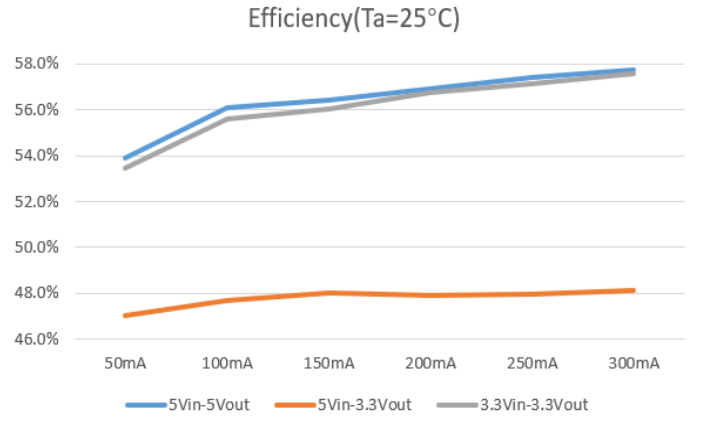
V_{ISO} Load transient response: V_{INP} =5V, V_{ISO}=3.3V
Load-current: 30mA/270mA



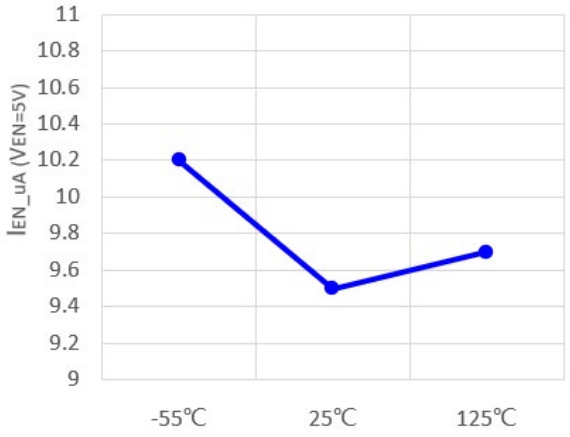
V_{ISO} load regulation: V_{INP} =5V, V_{ISO}=5V/5.4V/3.3V/3.7V
Output current: 0mA-300mA



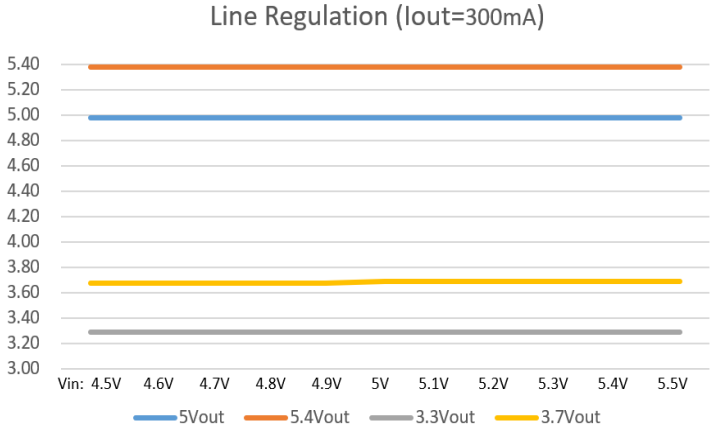
Power supply efficiency vs. temperature
V_{INP} =5V, V_{ISO}=5V/5.4V/3.3V/3.7V, output current = 300mA



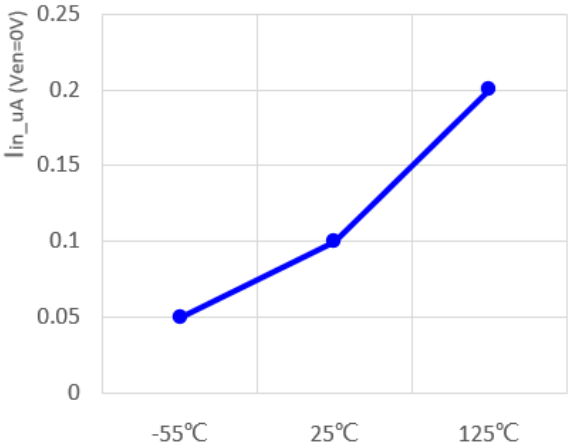
Efficiency for 5V-5V/5V-3.3V/3.3V-3.3V @25° C



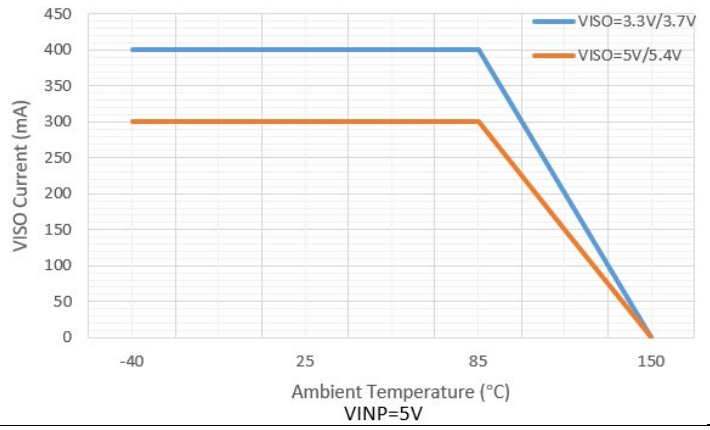
EN Pin input current vs. temperature



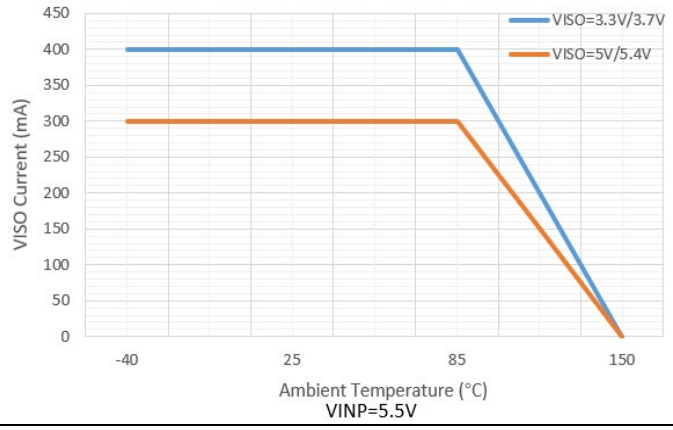
Line regulation: V_{INP} =4.5v ~ 5.5V
Output current: 300mA



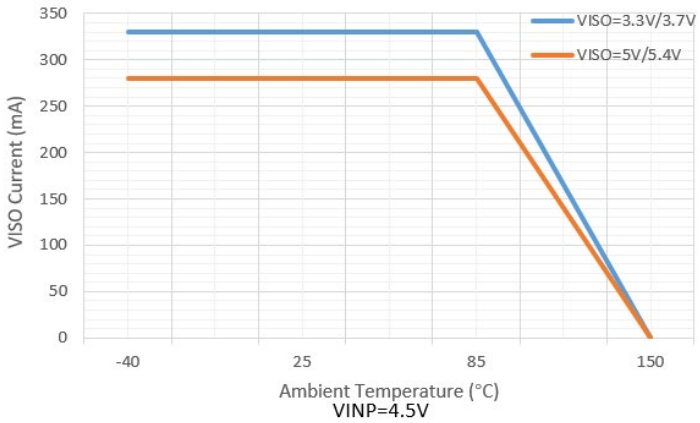
VINP Pin input current vs. temperature
(EN=0V, VINP=5V)



VINP=5V, output current derating vs. temperature



VINP=5.5V, output current derating vs. temperature

	
VINP=4.5V, output current derating vs. temperature	

8 Detailed Description

8.1 Overview

The CA-IS3115AW-Q1 is a family of complete isolated DC-DC converters designed to provide isolated power with up to 1.5W output power across a 5kV$_{RMS}$ isolation barrier. The devices operate over 4.5V to 5.5V input voltage range and use a proprietary control mechanism. The input supply V$_{INP}$ is provided to the primary power controller that switches the power stage connected to the integrated transformer. Power is transferred to the secondary side and regulated to a fixed output voltage set by the SEL pin. The soft-start feature allows to reduce input inrush current and avoid output overshoot. These devices also incorporate an output enable (EN) control and undervoltage lockout(UVLO) function that allows the user to turn on the part at the desired input-voltage level. Figure 8-1 shows the CA-IS3115AW-Q1's functional block diagram. Connect the EN pin to VINP or force this pin high to turn on the DC-DC converter. Force this pin low to disable the device and enter low-current shutdown mode. These devices offer a ready-made, reliable, easy-to-use solution and allow users save PCB space and reduce design time for the popular 5V, 3.3V power supply systems.

These devices are provided with a robust overcurrent protection scheme that protects the devices under overload and output short-circuit conditions. A cycle-by-cycle peak current limit turns off the switching operation and triggers hiccup mode. Once the hiccup timeout period expires, soft-start is attempted again. Hiccup mode operation ensures low power dissipation under output short-circuit conditions.

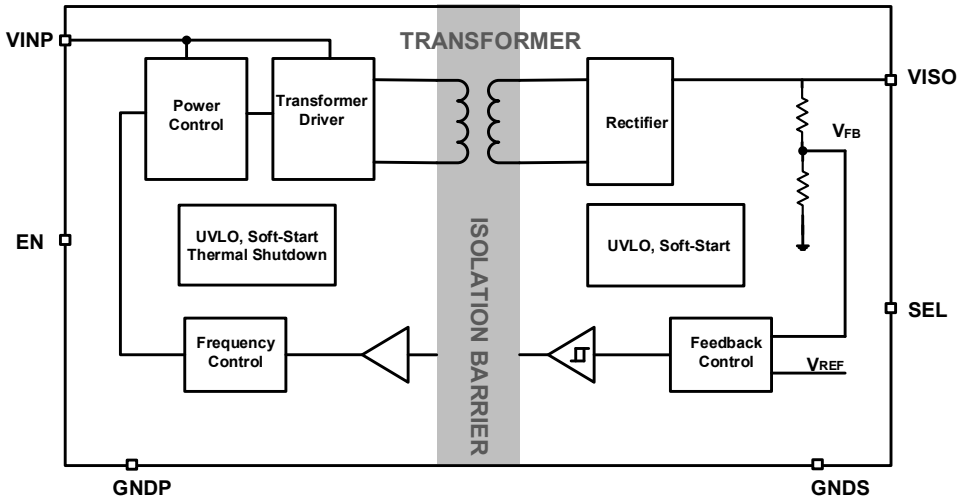


Figure 8-1. Functional Block Diagrams

8.2 Output Voltage Selection

At startup, the CA-IS3115AW-Q1 monitors the state of pin SEL after applying V$_{INP}$ supply voltage above the UVLO rising threshold or enabling via the EN pin, to build the desired regulation voltage level for the V$_{ISO}$ output. See Table 8-1 for the output voltage selection.

Table 8-1. V$_{ISO}$ Output Voltage Selection

EN	SEL	VISO
High	Sorted to VISO	5V
High	100kΩ to VISO	5.4V
High	Shorted to GNDS	3.3V
High	100KΩ to GNDS	3.7V
High	OPEN	Unsupported
Low	X	0V
Note: Don't leave SEL pin open.		

8.3 Protection Functions

8.3.1 UVLO and Soft-Start

The CA-IS3115AW-Q1 undervoltage lockout (UVLO) on both V_{INP} power supply and V_{ISO} isolated supply. Upon power-up, the primary side transformer driver is disabled while the V_{INP} voltage is below the threshold voltage V_{UVLO+}(2.7V, typ.), and V_{ISO} output is off. The output powers up once the threshold is met. This allows the user to turn on the part at stable input-voltage level.

For many applications, it is necessary to minimize the inrush current at start-up. The CA-IS3115AW-Q1 devices built-in soft-start circuit significantly reduces the start-up current spike and output voltage overshoot. Once input power supply is applied at VINP pin, the internal soft-start circuit will control the power delivered to the output gradually increase, allowing for a graceful turn-on ramp.

8.3.2 Current-limit Protection

The CA-IS3115AW-Q1 devices are provided with an over-current protection scheme that protects the device under overload and output short-circuit conditions. A cycle-by-cycle peak current limit turns off the switching operation and triggers a hiccup mode whenever the switch current exceeds the internal current limit. Once the hiccup timeout period expires, soft-start is attempted again. The hiccup condition is cleared when the over-current is removed.

8.3.3 Thermal Shutdown

Thermal-shutdown protection limits total power dissipation in the device. When the junction temperature of the device exceeds 175°C(T_{SD}), an on-chip thermal sensor shuts down the device, allowing the device to cool. The thermal sensor turns the device on again after the junction temperature cools and junction temperature drops to normal operation temperature range (< 150°C) of the device.

9 Applications Information

9.1 Typical Application Circuit

The CA-IS3115AW-Q1 devices are high-integration isolated power supply solution. Included in the package are the switching controller, power switches, transformer, and all support components. Only output and input bypass capacitors are needed to finish the design. For the applications with LDO post regulator, it needs a single 100kΩ external resistor to set the output level to 3.7V or 5.4V, see Figure 9-1 typical application circuit.

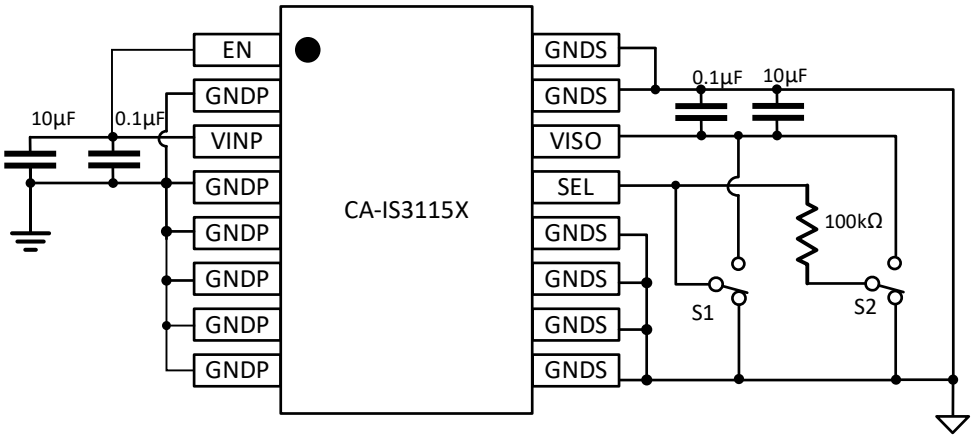


Figure 9-1. CA-IS3115AW-Q1 Typical Application Circuit

9.2 Input and Output Capacitors

The input capacitors (between VINP and GNDP) are required to reduce the peak current drawn from input power source and reduce the switching noise, increase efficiency. For the input capacitors, choose the ceramic capacitor because they have the lowest equivalent series resistance (ESR), smallest size, and lowest cost. For most applications, we recommend to use at least 0.1μF and 10μF ceramic capacitors with X5R or X7R temperature characteristic.

The output capacitors between VISO and GNDS are required as well to keep the output voltage ripple small and to ensure loop stability. These bypass capacitors must have low impedance at the switching frequency. Ceramic capacitors are recommended due to their small size and low ESR. Make sure the capacitors do not degrade their capacitance significantly over temperature and DC bias. It is recommended to have at least 10μF of effective capacitance at output.

9.3 PCB Layout Guidelines

High switching frequencies and large peak currents make PCB layout a very important part of the isolated DC-DC converter design. Good PCB design minimizes excessive electromagnetic interference (EMI) and voltage gradients in the ground plane to avoid instability and regulation errors. Even with the high level of integration, like CA-IS3115AW-Q1, users may fail to achieve specified operation with a haphazard or poor layout. So careful PCB layout is critical to achieve clean and stable operation, and ensure that the grounding and heat sinking are acceptable.

Place the input capacitors, output capacitors, and the CA-IS3115AW-Q1 IC on the same PCB layer. Place decoupling capacitors as close as possible to the CA-IS3115AW-Q1 device pins, see Figure 9-2 recommended components placement for the PCB layout. The paths must be wide and short to minimize inductance, also any via holes must be avoided on these paths. Connect all of the ground (GNDP, GNDS) connections to as large a plane area as possible for best heat-sinking. To ensure isolation performance between the primary side and secondary side, on the top layer and bottom layer keep the space under the CA-IS3115AW-Q1 device free from traces, vias, and pads to maintain maximum creepage distance (≥ 8mm).

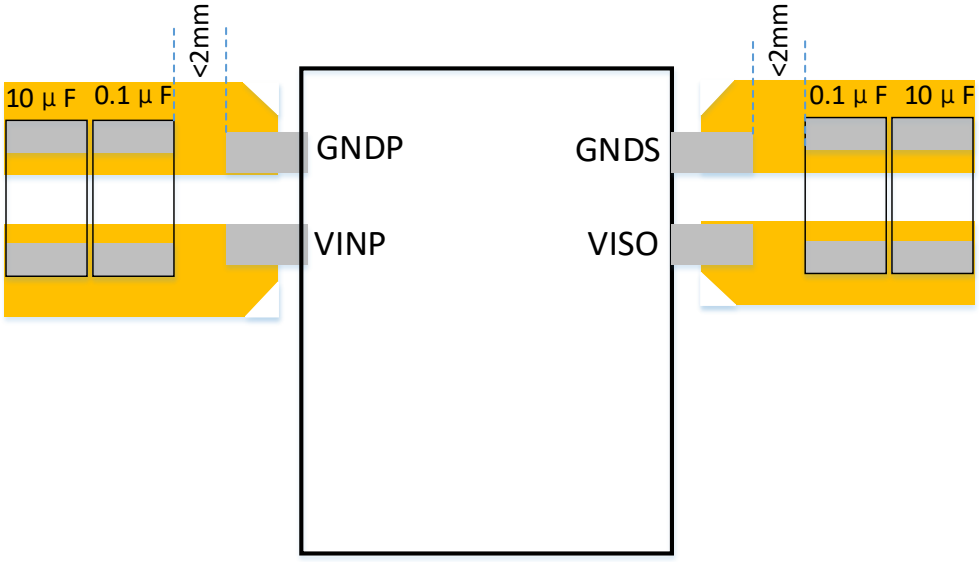
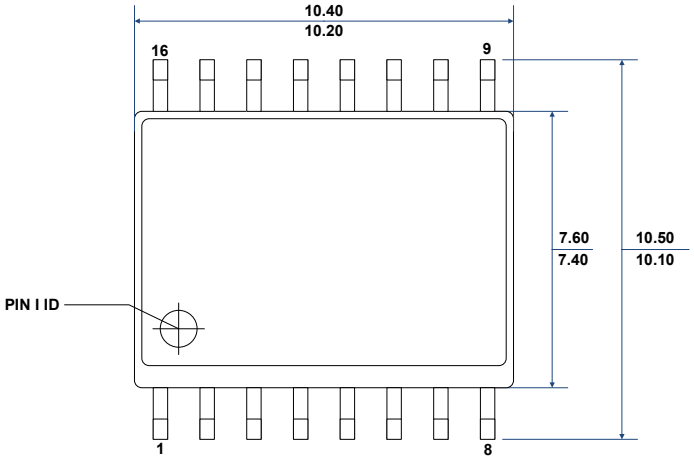


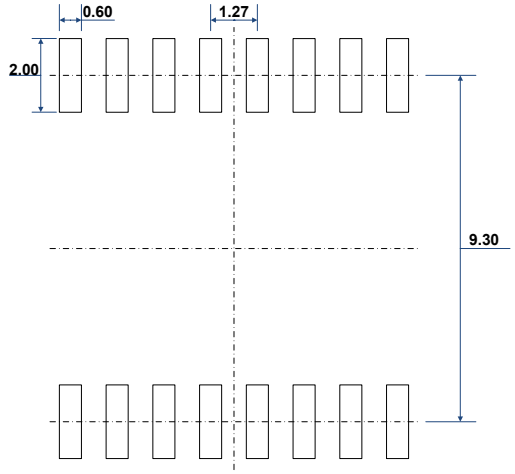
Figure 9-2. Recommended Bypass Capacitors Placement

10 Package Information

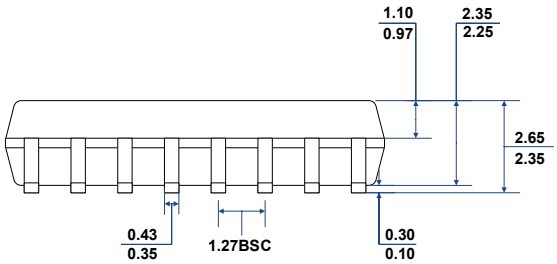
The following figure illustrates the size drawing and recommended pad size of SOIC16-WB wide-body package for the CA-IS3115AW-Q1 isolated DC-DC converter. All dimensions are in millimeters.



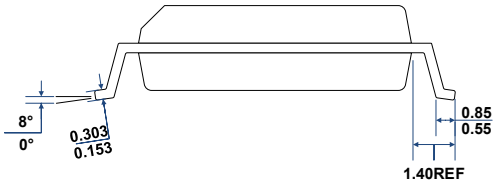
TOP VIEW



RECOMMENDED LAND PATTERN



FRONT VIEW



LEFT-SIDE VIEW

11 Soldering Temperature (reflow) Profile

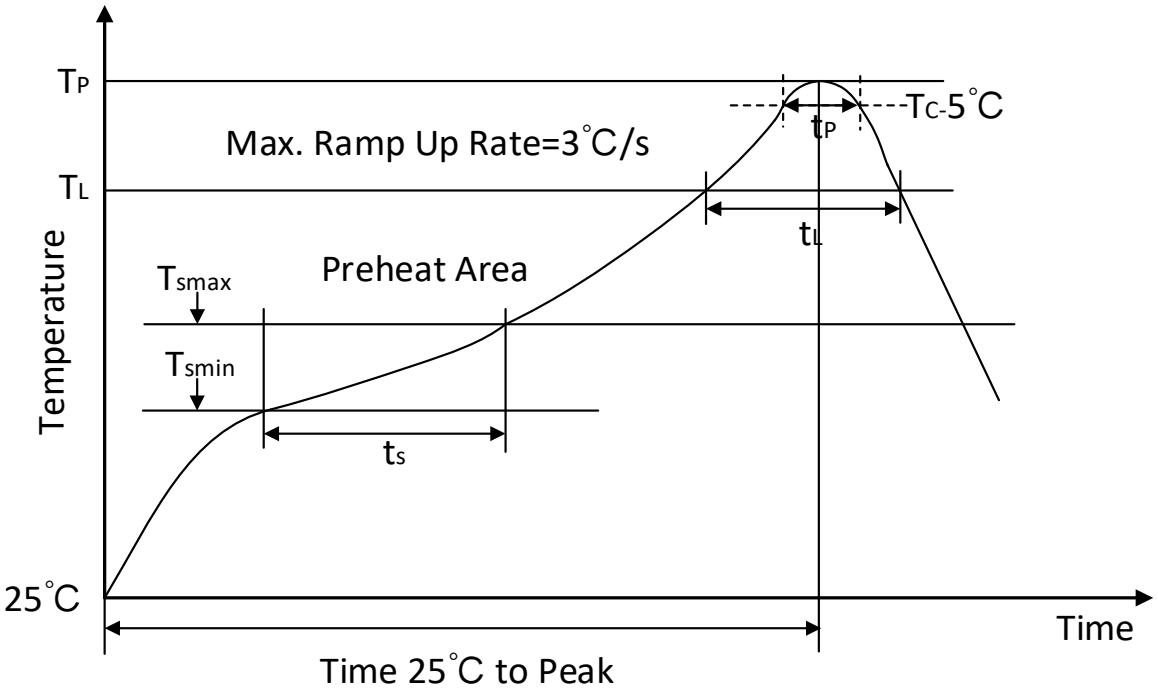


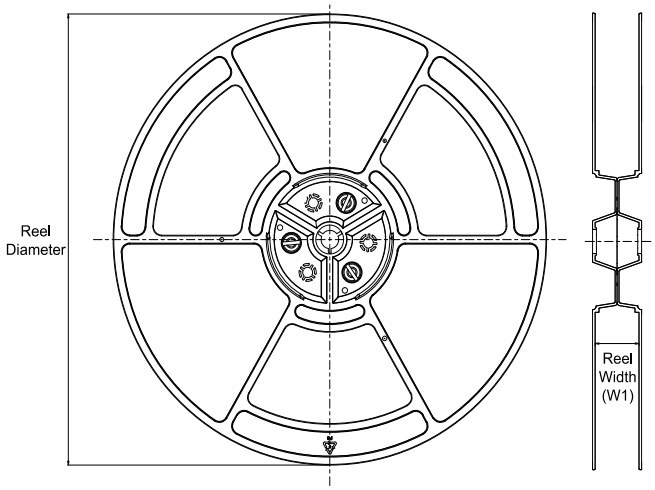
Figure 11-1. Soldering Temperature (reflow) Profile

Table 11-1. Soldering Temperature Parameter

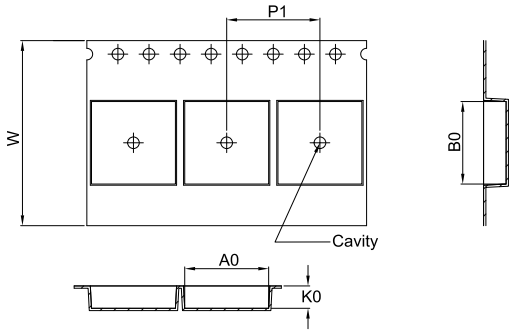
Profile Feature	**Pb-Free Assembly**
Average ramp-up rate(217 °C to Peak)	3°C /second max
Time of Preheat temp(from 150°C to 200°C	60-120 second
Time to be maintained above 217°C	60-150 second
Peak temperature	260 +5/-0 °C
Time within 5°C of actual peak temp	30 second
Ramp-down rate	6°C /second max.
Time from 25°C to peak temp	8 minutes max

12 Tape and Reel Information

REEL DIMENSIONS

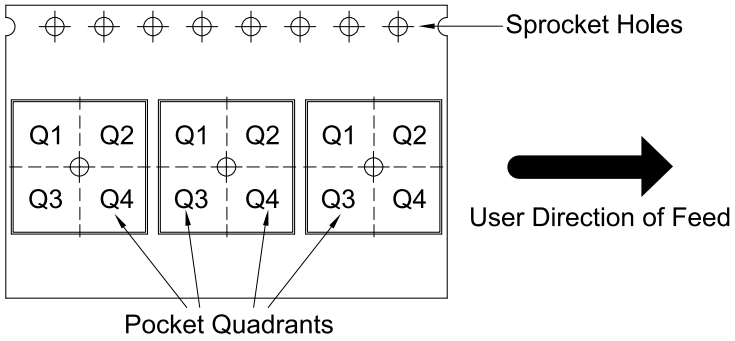


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CA-IS3115AW-Q1	SOIC	W	16	1000	330	16.4	10.8	10.7	2.9	12.0	24.0	Q1

13 Important statement

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