6A Sink/5A Source, 5.7kV$_{RMS}$ Isolated Dual-Channel Gate Driver

1. Features

- **Support Broad Range of Applications**
  - Dual low-side, dual high-side drivers
  - Half-bridge drivers
- **6A Peak Sink Current and 5A Peak Source Current**
- **Wide Supply Range:**
  - 3V to 18V Input-side V_{CCI} supply range
  - Up to 25V $V_{DD\_}$ output drive supply
  - Provide6V、8V and 12V precision UVLO options
- **Delay Characteristics**
  - 56ns Propagation delay (Typ.)
  - 5ns Propagation delay matching (Max.)
  - 7ns Pulse width distortion(Max.)
  - 20ns Minimum pulse width(Typ.)
- **Programmable Overlap and Dead-time**
- **-40°C to +125°C Operating Temperature Range**
- **Robust Galvanic Isolation**
  - High lifetime: >40 years
  - Up to 3.75kV$_{RMS}$ (narrow SOIC package) isolation rating
  - Common-mode transient immunity (CMTI) > ±100V/ns
  - Withstands up to 8kV surge
- **Package options**
  - Narrow-body SOIC16(N) package
- **Safety regulatory approvals**
  - VDE Basic isolation and Basic isolation per DIN EN IEC 60747-17 (VDE 0884-17): 2021-10
  - UL certification per UL 1577 for 1 minute
  - TUV certification per EN61010-1:2010+A1
  - AEC-Q100, Grade 1

2. Applications

- Isolated DC-DC and AC-DC Converters
- Motor Control
- LED Lighting
- Uninterruptible Power Supply (UPS)
- Isolated Gate Driver for Inverters
- HEV/EV Battery Charger

3. General Description

The CA-IS322x devices are a family of dual-channel isolated gate drivers capable of sinking 6A and sourcing 5A peak currents. These devices have very fast switching time, combined with short propagation delays (56ns, typ) and small pulse width distortion, making them ideal to drive power MOSFET, IGBT or silicon-carbide(SiC) transistors with up to 5MHz frequency in various inverter, isolated power supply or motor control applications.

All devices have integrated digital galvanic isolation using Chipanalog's proprietary capacitive isolation technology. They feature isolation for a withstand voltage rating of 3.75kV$_{RMS}$ for 60 seconds with minimum common-mode transient immunity (CMTI) of 100V/ns. The internal functional isolation between driver A and driver B on the secondary-side allows up to 1500V DC working voltage.

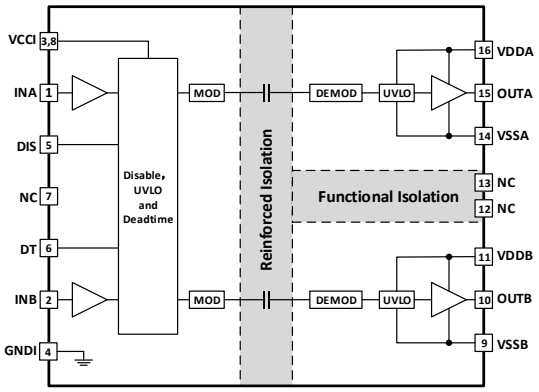
The CA-IS322x family of devices can be configured as dual low-side, dual high-side or half-bridge drivers with programmable dead-time. The enable control (EN pin for the CA-IS3222) and disable control (DIS pin for the CA-IS3221) allow both driver A and driver B outputs to be quickly set to logic-low, turning off the external power transistor. They also have a default-low output. The default is the state the output assumes when the input is either not powered or is open-circuit. Also, the driver outputs are set to logic-low when input-side or output-side supply is in UVLO, or the device is disabled.

The CA-IS322x devices accept 3V to 18V V_{CCI} supply and up to 25V $V_{DD\_}$ wide supply range. They are available in a 16-pin narrow-body SOIC package. The devices are rated for operation at ambient temperatures of -40°C to +125°C.

Device Information

Part Number	Package	Package Size (Nominal Value)
CA-IS3221-Q1 CA-IS3222-Q1	SOIC16-NB(N)	9.9 mm x 3.9 mm

Simplified Schematic



4. Ordering Information

Table 4-1. Ordering Information

Part #	DIS PIN / EN PIN	VDDA/VDDB UVLO	Isolation Rating	Package
CA-IS3221AN-Q1	DIS	6	3.75 kV_{RMS}	SOIC16-NB
CA-IS3221BN-Q1	DIS	8	3.75 kV_{RMS}	SOIC16-NB
CA-IS3221CN-Q1	DIS	12	3.75 kV_{RMS}	SOIC16-NB
CA-IS3222AN-Q1	EN	6	3.75 kV_{RMS}	SOIC16-NB
CA-IS3222BN-Q1	EN	8	3.75 kV_{RMS}	SOIC16-NB
CA-IS3222CN-Q1	EN	12	3.75 kV_{RMS}	SOIC16-NB

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5. Revision History

Revision Number	Description	Revised Date	Page Changed
Preliminary Version	N/A		N/A
Version 1.00	N/A	2023/11/02	N/A
Version 1.01	1. Update the certificate information of VDE、UL、CQC、TUV	2024/04/16	1,7,8

6. Pin Configuration and Description

6.1. CA-IS3221-Q1 Pin Configuration and Description

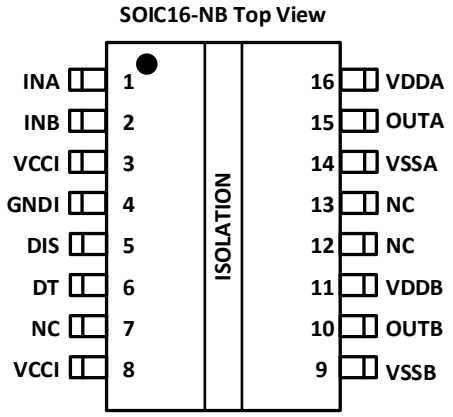


Figure 6-1. The CA-IS3221-Q1 Pin Configuration (SOIC16 Narrow Package)

Table 6-1. The CA-IS3221-Q1 Pin Description

Pin Name	Pin Number	Type	Description
INA	1	Input	Driver A input. INA is TTL/CMOS compatible and has internal pulldown to GNDI. Connect this pin to GNDI if not used.
INB	2	Input	Driver B input. INB is TTL/CMOS compatible and has internal pulldown to GNDI. Connect this pin to GNDI if not used.
VCCI	3, 8	Power Supply	3 V to 18 V power supply input for input side. Bypass VCCI to GNDI with an at least 0.1μF capacitor as close to the device as possible.
GNDI	4	Ground	Ground reference for input-side
DIS	5	Logic Input	Disable input on input-side. Drive DIS high to disable isolator and put driver output low; Drive DIS low or leave open, enable gate driver. DIS has internal pull-down to GNDI. Connect this pin to GNDI if not used.
DT	6	Input	Programmable dead-time input. Connecting DT to V_{CCI} allows the output to overlap; Placing a 500Ω to 500kΩ resistor between DT and GNDI adjusts dead time according to t_{DT}(ns)=10 x R_{DT} (kΩ). We recommended to bypass DT to GNDI with an at least 2.2nF ceramic capacitor as close to pin DT and resistor RDT as possible. This Pin cannot be floating.
NC	7, 12, 13	---	No internal connection.
VSSB	9	Ground	Ground reference for output-side (driver B).
OUTB	10	Output	Gate driver output B.
VDDB	11	Power Supply	Power supply input for output-side (driver B). Bypass VDDB to VSSB with 0.1μF||10μF capacitors as close as possible to the pin VDDB.
VSSA	14	Ground	Ground reference for output-side (driver A).
OUTA	15	Output	Gate driver output A.
VDDA	16	Power Supply	Power supply input for output-side (driver A). Bypass VDDA to VSSA with 0.1μF||10μF capacitors as close as possible to the pin VDDA.

6.2. CA-IS3222-Q1 Pin Configuration and Description

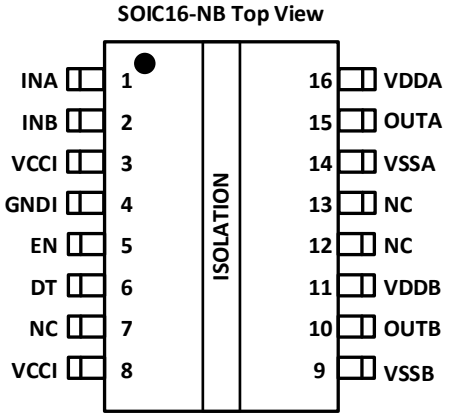


Figure 6-2. The CA-IS3222-Q1 Pin Configuration (SOIC16 Narrow Package)

Table 6-2. The CA-IS3222 Pin Description

Pin Name	Pin Number	Type	Description
INA	1	Input	Driver A input. INA is TTL/CMOS compatible and has internal pull-down to GNDI. Connect this pin to GNDI if not used.
INB	2	Input	Driver B input. INB is TTL/CMOS compatible and has internal pull-down to GNDI. Connect this pin to GNDI if not used.
VCCI	3, 8	Power Supply	3 V to 18 V power supply input for input side. Bypass V_{CCI} to GNDI with an at least 0.1µF capacitor as close to the device as possible.
GNDI	4	Ground	Ground reference for input-side.
EN	5	Logic Input	Active-high enable input on input-side. Drive EN low or connect to GNDI to disable isolator and put driver output low; Drive EN high or leave open, enable gate driver. EN has internal pull-up to VCCI. Connect this pin to V_{CCI} if not used.
DT	6	Input	Programmable dead-time input. Connecting DT to V_{CCI} allows the output to overlap; Placing a 500Ω to 500kΩ resistor between DT and GNDI adjusts dead time according to t_{DT}(ns)=10 x R_{DT} (kΩ). We recommended to bypass DT to GNDI with an at least 2.2nF ceramic capacitor as close to pin DT and resistor RDT as possible. This Pin cannot be floating.
NC	7, 12, 13	---	No internal connection.
VSSB	9	Ground	Ground reference for output-side (driver B).
OUTB	10	Output	Gate driver output B.
VDDB	11	Power Supply	Power supply input for output-side (driver B). Bypass VDDB to VSSB with 0.1µF||10µF capacitors as close as possible to the pin VDDB.
VSSA	14	Ground	Ground reference for output-side (driver A).
OUTA	15	Output	Gate driver output A.
VDDA	16	Power Supply	Power supply input for output-side (driver A). Bypass VDDA to VSSA with 0.1µF||10µF capacitors as close as possible to the pin VDDA.

7. Specifications

7.1. Absolute Maximum Ratings[1]

over operating free-air temperature range unless otherwise specified. [1]

Parameters		Minimum	Maximum	Unit
Power supply voltage on input-side	VCCI to GNDI	-0.3	20	V
Power supply voltage on output-side	VDDA-VSSA, VDDB-VSSB	-0.3	30	V
Driver output	OUTA to VSSA, OUTB to VSSB	-0.3	V_{DDA}+0.3 V_{DDB}+0.3	V
	OUTA to VSSA, OUTB to VSSB, 200ns transient.	-2	V_{DDA}+0.3 V_{DDB}+0.3	
Input signals	INA, INB, DIS, DT to GND	-0.3	V_{CCI}+0.3	V
	INA, INB, 50ns transient.	-5	V_{CCI}+0.3	
Channel to channel voltage	VSSA-VSSB, VSSB-VSSA		1500	V
Junction temperature[2]		-40	150	°C
Storage temperature		-65	150	°C

Notes:

1. The stresses listed under "Absolute Maximum Ratings" are stress ratings only, not for functional operation condition. Exposure to absolute maximum rating conditions for extended periods may cause permanent damage to the device.
2. To maintain the recommended operating junction temperature conditions, see Thermal Information.

7.2. ESD Ratings

			Value	Unit
V_{ESD}	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001.	±4000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101.	±1000	

7.3. Recommended Operating Conditions

Over operating free-air temperature range unless otherwise specified.

Parameters			Minimum	Maximum	Unit
V_{CCI}	Power supply voltage on input-side		3	18	V
V_{DDA}, V_{DDB}	Power supply voltage on output-side	6V UVLO version	8	25	V
		8V UVLO version	10	25	V
		12V UVLO version	14	25	V
T_J	Junction temperature		-40	130	°C
T_A	Ambient temperature		-40	125	°C

7.4. Thermal Information

Thermal Metric		SOIC16-NB	Unit
$R_{\theta JA}$	Junction-to-ambient thermal resistance	96.2	°C/W

7.5. Power Ratings

Parameters		Test Conditions	Typical Value	Unit
P_D	Maximum input and output power dissipation	V_{CCI}= 18V, V_{DDA}=V_{DDB}=15V, INA/INB=3.3V, 3MHz square wave with 50% duty cycle, C_L = 1nF	1.05	W
P_{D1}	Maximum input power dissipation		0.05	W
P_{D2}	Maximum output power dissipation		0.5	W

7.6. Insulation Specifications

Parameters		Test Conditions	Specifications	Unit
			N	
CLR	External clearance	Shortest terminal-to-terminal distance through air	>4	mm
CPG	External creepage	Shortest terminal-to-terminal distance across the package surface	>4	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	> 28	µm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11)；IEC 60112	> 600	V
	Material group	According to IEC 60664-1	I	
	IEC 60664-1 over-voltage category	Rated mains voltage ≤ 150 V_{RMS}	I-IV	
		Rated mains voltage ≤ 300 V_{RMS}	I-III	
		Rated mains voltage ≤ 600 V_{RMS}	/	
DIN V VDE V 0884-17: 2021-10				
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	566	V_{PK}
V_{IOWM}	Maximum operating isolation voltage	AC voltage; time-dependent dielectric breakdown (TDDB) test	400	V_{RMS}
		DC voltage	566	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t=60 s (qualification); $V_{TEST} = 1.2 \times V_{IOTM}$, t=1 s (100% product test)	5300	V_{PK}
V_{IOSM}	Maximum surge isolation voltage[2]	Test method per IEC 62368-1, 1.2/50 µs waveform, $V_{TEST} = 1.3 \times V_{IOSM}$ (qualification)	5000	V_{PK}
q_{pd}	Apparent charge[3]	Method a, after input/output safety tests subgroup 2/3, $V_{ini} = V_{IOTM}$, t_{ini} = 60s; $V_{pd(m)} = 1.2 \times V_{IORM}$, t_m = 10s	≤5	pC
		Method a, after environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, t_{ini} = 60s; $V_{pd(m)} = 1.3 \times V_{IORM}$, t_m = 10s	≤5	
		Method b1, at routine test (100% production test) and preconditioning (sample test) $V_{ini} = 1.2 \times V_{IOTM}$, t_{ini} = 1s; $V_{pd(m)} = 1.5 \times V_{IORM}$, t_m = 1s	≤5	
C_{IO}	Barrier capacitance, input to output[4]	V_{IO} = 0.4 × sin (2πft), f = 1 MHz	0.5	pF
R_{IO}	Isolation resistance , input to output[4]	V_{IO} = 500 V, T_A = 25°C	$>10^{12}$	Ω
		V_{IO} = 500 V, 100°C ≤ T_A ≤ 125°C	$>10^{11}$	
		V_{IO} = 500 V at T_S = 150°C	$>10^{9}$	
	Pollution degree		2	
	Climatic category		40/125/21	
UL 1577				
V_{ISO}	Maximum isolation voltage	$V_{TEST} = V_{ISO}$, t = 60 s (certified) $V_{TEST} = 1.2 \times V_{ISO}$, t = 1 s (100% production test)	3750	V_{RMS}

7.7. Safety-Related Certifications

VDE	UL	TUV
Certified according to DIN EN IEC 60747-17 (VDE 0884-17):2021-10; EN IEC 60747-17: 2020+AC:2021	Certified according to UL 1577 Component Recognition Program	Certified according to EN 61010-1:2010 +A1
Basic isolation (SOIC16-NB): Maximum transient isolation voltage: 5300V_{pk} Maximum repetitive-peak isolation voltage: 566 V_{pk} Maximum surge isolation voltage: 5000V_{pk}	Protection voltage: - 3750V_{RMS} for SOIC16-NB package	Basic insulation 3750 V_{RMS} for SOIC16-NB package
Certificate Number：40052786 CA-IS3221AN-Q1：Pending CA-IS3222AN-Q1：Pending	Certificate Number：E511334 CA-IS3221AN-Q1：Pending CA-IS3222AN-Q1：Pending	Certificate Number：AK 505918190001 CA-IS3221AN-Q1：Pending CA-IS3222AN-Q1：Pending

7.8. Safety Limits

Parameters		Test Conditions		Minimum	Typical	Maximum	Unit
I_S	Safety output supply current	R_{qJA} = 96.2°C/W, V_{DDA} = V_{DDB} = 15V, T_J = 150°C, T_A = 25°C	Driver A, Driver B			43	mA
		R_{qJA} = 96.2°C/W, V_{DDA} = V_{DDB} = 25V,T_J = 150°C, T_A = 25°C	Driver A, Driver B			25	
P_S	Safety power dissipation	R_{qJA} = 96.2°C/W, T_J = 150°C, T_A = 25°C	Input			50	mW
			Driver A			625	
			Driver B			625	
			Total			1300	
T_S	Maximum safety temperature[1]					150	°C

Note：

1. $T_{J(max)} = T_S = T_A + R_{\theta JA} * P_S$, where $T_{J(max)}$) is the maximum allowed junction temperature. $P_S = I_S * V_{IN}$, where V_{IN} is the maximum supply voltage.

7.9. Electrical Characteristics

T_A = -40°C to +125°C, V_{CCI} = 3.3V or 5V, connect a 0.1μF bypass capacitor between VCCI and GNDI; V_{DDA} = V_{DDB} = 12V for 6V and 8V-UVLO version, V_{DDA} = V_{DDB} = 15V for 12V-UVLO version, Connect a 1μF bypass capacitor between VDDA and VSSA, between VDDB and VSSB , respectively. Unless otherwise noted. Typical values are at T_A = +25°C, unless otherwise noted.

Parameters		Test Conditions	Minimum	Typical	Maximum	Unit
Supply Current						
I_{VCCI}	V_{CCI} quiescent current	V_{INA} = 0 V, V_{INB}= 0 V		1.5	2.0	mA
I_{VDDA},I_{VDDB}	V_{DDA}/ V_{DDB} quiescent current	V_{INA} = 0 V, V_{INB}= 0 V		1.0	1.8	mA
I_{VCCI}	V_{CCI} operating current	(f = 500 kHz) current per channel, C_{OUT} = 100 pF		2.0		mA
I_{VDDA},I_{VDDB}	V_{DDA}/V_{DDB} operating current	(f = 500 kHz) current per channel, C_{OUT} = 100 pF		3.0		mA
V_{CCI} Undervoltage-Lockout Threshold						
$V_{VCCI(UVLO+)}$	V_{CCI} rising	INA,INB,DT tied to VCCI, VCCI rising	2.60	2.75	2.95	V
$V_{VCCI(UVLO-)}$	V_{CCI} falling	INA,INB,DT tied to VCCI, VCCI falling	2.25	2.40	2.60	V
$V_{VCCI\_HYS(UVLO)}$	Undervoltage-lockout threshold hysteresis			0.35		V
VDD_ Undervoltage-Lockout Threshold (6V UVLO Version)						
$V_{VDDA(UVLO+)}$, $V_{VDDB(UVLO+)}$	V_{DDA}/V_{DDB} rising	VCCI=INA=INB=DT, VDD rising	5.4	6.0	6.6	V
$V_{VDDA(UVLO-)}$, $V_{VDDB(UVLO-)}$	V_{DDA}/V_{DDB} falling	VCCI=INA=INB=DT, VDD falling	4.9	5.5	6.1	V
V_{VDDA_HYS} V_{VDDB_HYS}	Undervoltage-lockout threshold hysteresis			0.5		V
VDD_ Undervoltage-Lockout Threshold (8V UVLO Version)						
$V_{VDDA(UVLO+)}$, $V_{VDDB(UVLO+)}$	V_{DDA}/V_{DDB} rising	VCCI=INA=INB=DT, VDD rising	7.3	8.1	8.9	V
$V_{VDDA(UVLO-)}$, $V_{VDDB(UVLO-)}$	V_{DDA}/V_{DDB} falling	VCCI=INA=INB=DT, VDD falling	6.7	7.4	8.2	V
$V_{VDDA\_HYS(UVLO)}$ $V_{VDDB\_HYS(UVLO)}$	Undervoltage-lockout threshold hysteresis			0.7		V
VDD_ Undervoltage-Lockout Threshold (12V UVLO Version)						
$V_{VDDA(UVLO+)}$, $V_{VDDB(UVLO+)}$	V_{DDA}/V_{DDB} rising	VCCI=INA=INB=DT, VDD rising	10.9	12.1	13.3	V
$V_{VDDA(UVLO-)}$, $V_{VDDB(UVLO-)}$	V_{DDA}/V_{DDB} falling	VCCI=INA=INB=DT, VDD falling	9.9	11.1	12.3	V
$V_{VDDA\_HYS(UVLO)}$ $V_{VDDB\_HYS(UVLO)}$	Undervoltage-lockout threshold hysteresis			1.0		V
Logic Input (INA, INB, EN and DIS)						
V_{INH}	Input high voltage	VIN rising	1.6	1.8	2	V
V_{INL}	Input low voltage	VIN falling	0.8	1	1.2	V
V_{HYS}	Input hysteresis			0.8		V
V_{INA}, V_{INB}	Negative transient, referenced to GND, 50 ns pulse		-5			V
Driver Output						
I_{OHA}, I_{OHB}	Peak output current	C_{VDD} = 10 μF, C_{LOAD} = 0.18 μF, f = 1 kHz,		5		A
I_{OLA}, I_{OLB}	Peak output current	C_{VDD} = 10 μF, C_{LOAD} = 0.18 μF, f = 1 kHz,		6		
R_{OHA}, R_{OHB}	Output resistance at high	I_{OUT} = -10 mA, T_A = 25°C, R_{OHA}, R_{OHB} do not represent drive pull-up performance.		5		Ω
R_{OLA}, R_{OLB}	Output resistance at low	I_{OUT} = 10 mA, T_A = 25°C		0.55		Ω
V_{OHA}, V_{OHB}	Output voltage at high	I_{OUT} = -10 mA, T_A = 25°C		VDD-0.05		V

V_{OLA}, V_{OLB}	Output voltage at low	I_{OUT} = 10 mA, T_A = 25°C		5.5		mV
Dead-time and Overlap						
Dead-time	Connect pin DT to V_{CCI}		Overlap time is up to INA and INB			
	R_{DT} = 20 kΩ, See Figure 8-4		160	200	240	ns

7.10. Switching Characteristics

T_A = -40°C to +125°C, V_{CCI} = 3.3V or 5V, connect a 0.1µF bypass capacitor between VCCI and GNDI; V_{DDA} = V_{DDB} = 12V for 8V-UVLO version, V_{DDA} = V_{DDB} = 15V for 12V-UVLO version, Connect a 1µF bypass capacitor between VDDA and VSSA, between VDDB and VSSB , respectively. Unless otherwise noted. Typical values are at T_A = +25°C.

Parameters		Test Conditions	Minimum	Typical	Maximum	Unit
t_r	Output rise time	C_{OUT} = 1.8 nF, See Figure 8-2		6	16	ns
t_f	Output fall time			8	12	ns
t_{PWmin}	Minimum pulse width	Output off if t_{PW} less than minimum value, No load		20	40	ns
t_{PLH}	Propagation delay, low to high	f_{PWM} = 100kHz, No Load, See Figure 8-1		62	100	ns
t_{PHL}	Propagation delay, high to low	f_{PWM} = 100kHz, No Load, See Figure 8-1		56	100	ns
t_{PWD}	Pulse width distortion $\lvert t_{PHL}-t_{PLH}\rvert$	$t_{PWD=}\lvert t_{PHL}-t_{PLH}\rvert$, No Load, See Figure 8-1			14	ns
t_{DM}	Channel to channel propagation delay matching	$t_{DM}=\lvert t_{PHLA}-t_{PHLB}\rvert$ or $\lvert t_{PLHA}-t_{PLHB}\rvert$ f_{PWM} = 100kHz, See Figure 8-1			5	ns
$t_{VCCI+ to OUT}$	V_{CCI} power up delay time: UVLO rise to OUTA, OUTB	INA or INB is connected to VCCI See Figure 8-5		55	100	µs
$t_{VDD\_+ to OUT}$	V_{DDA}, V_{DDB} power up delay time: UVLO rise to OUTA, OUTB	INA or INB is connected to VCCI See Figure 8-5		68	100	µs
$CMTI_H$	CMTI (output high)	INA = INB = VCCI; V_{CM} = 1500V, See Figure 8-6	100	150		V/ns
$CMTI_L$	CMTI (output low)	INA = INB = GNDI; V_{CM} = 1500V, See Figure 8-6	100	150		V/ns

7.11. Typical Characteristics

VCCI=3.3V or 5V, VDDA=VDDB=15V, T_A = 25°C, Unless otherwise noted.

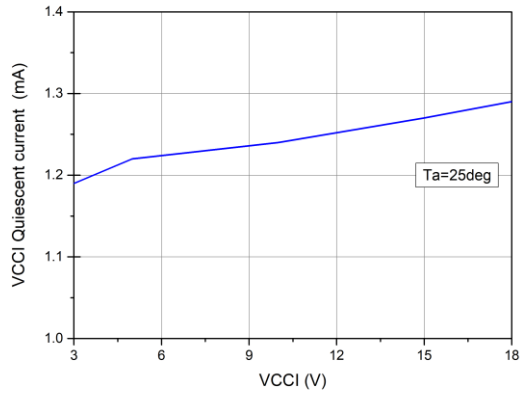


Figure 7-1 VCCI Quiescent current VS.VCCI voltage

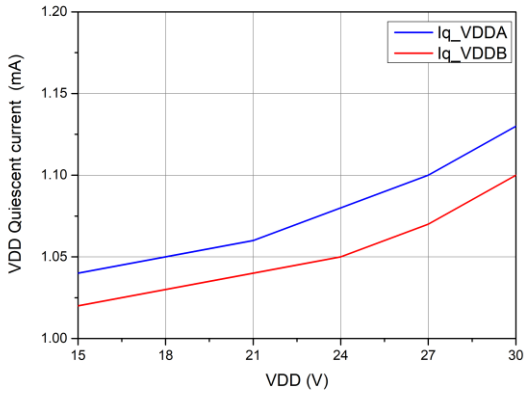


Figure 7-2 VDD Quiescent current VS. VDD voltage

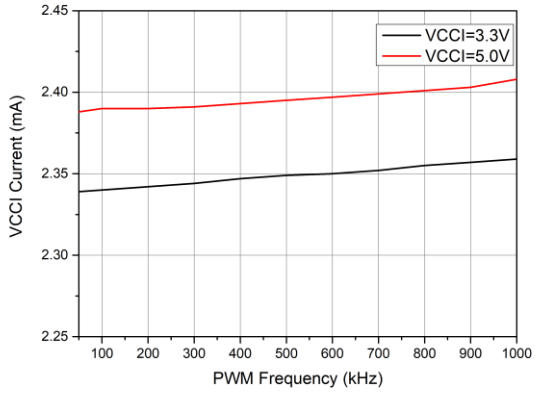


Figure 7-3 VCCI operating current VS. PWM frequency

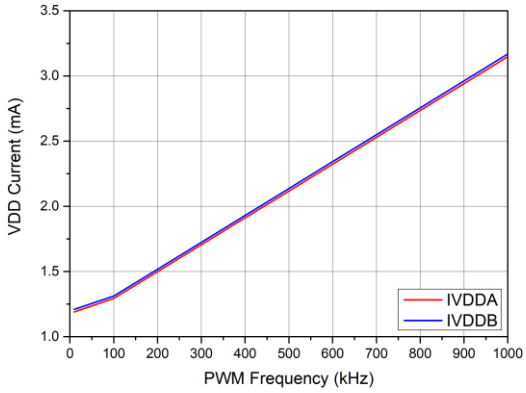


Figure 7-4 VDD operating current VS. PWM frequency （No Load）

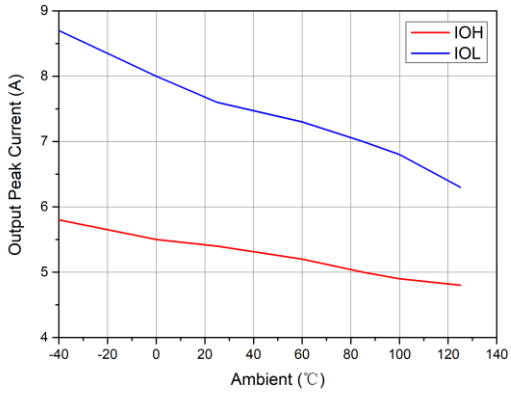


Figure 7-5 Output peak current VS. Temperature （C_{load}=180nF）

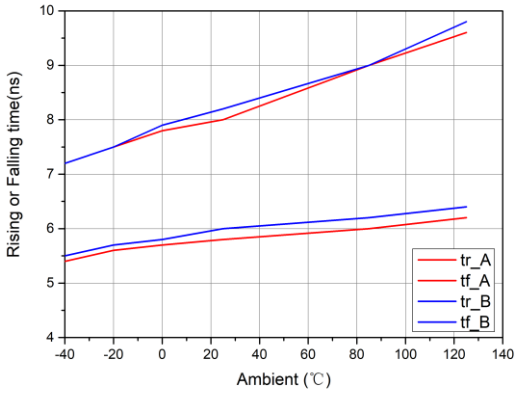


Figure 7-6 Rise time & Fall time VS. Temperature （C_{load}=1.8nF）

Continued above table：

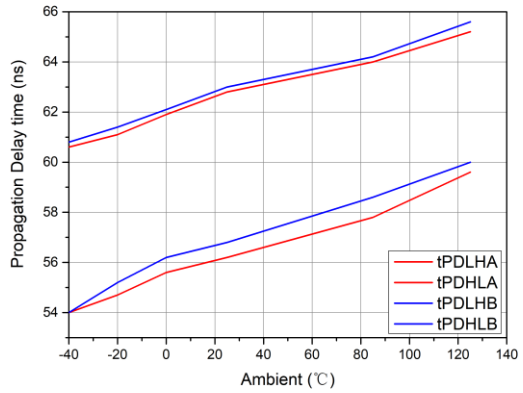


Figure 7-7 Propagation delay time VS. Temperature

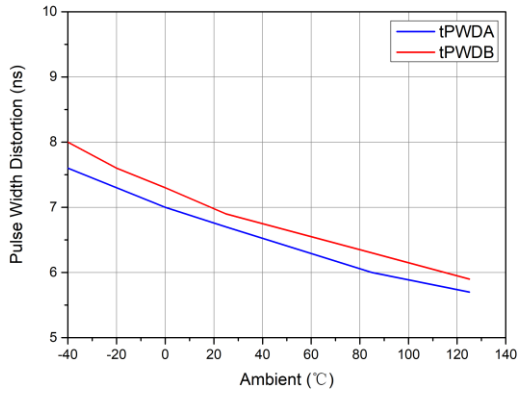


Figure 7-8 Pulse width distortion VS. Temperature

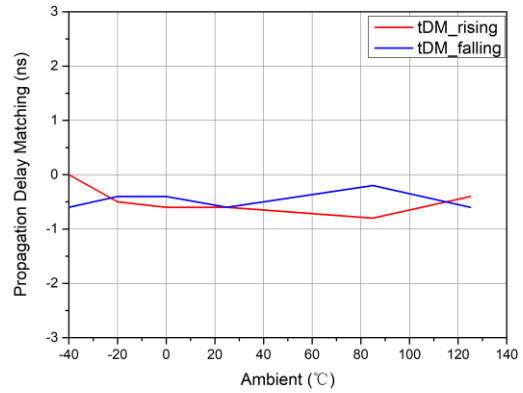


Figure 7-9 Channel delay matching VS. Temperature

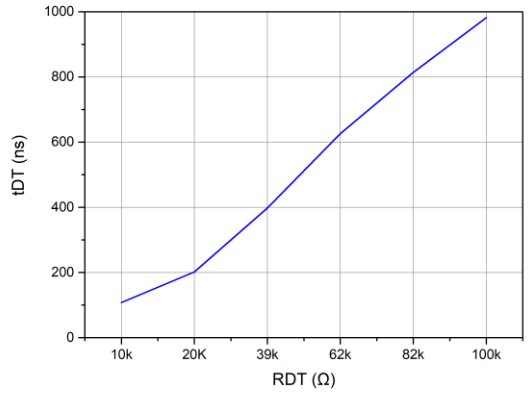


Figure 7-10 RDT VS. Dead time

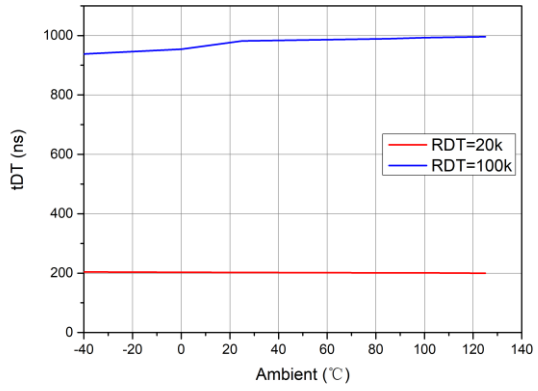


Figure 7-11 Dead time VS. Temperature

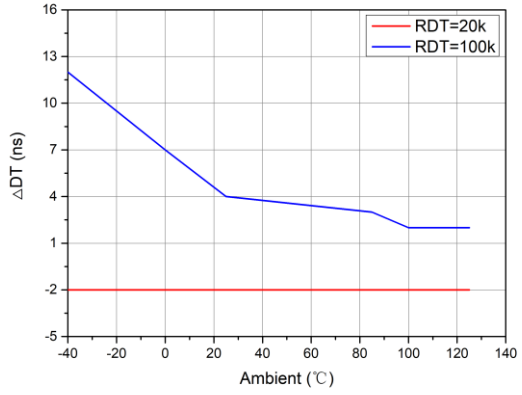


Figure 7-12 Dead time matching VS. Temperature

8. Parameter Measurement Information

8.1. Propagation Delay and Pulse Width Distortion

Figure 8-1 shows the definition and measurement for the pulse width distortion(t_{PWD}) and propagation delay matching between channel A and channel B (t_{DM}). Ensure that both inputs are in phase and disabled the dead time function by shorting the DT pin to VCCI during measurement.

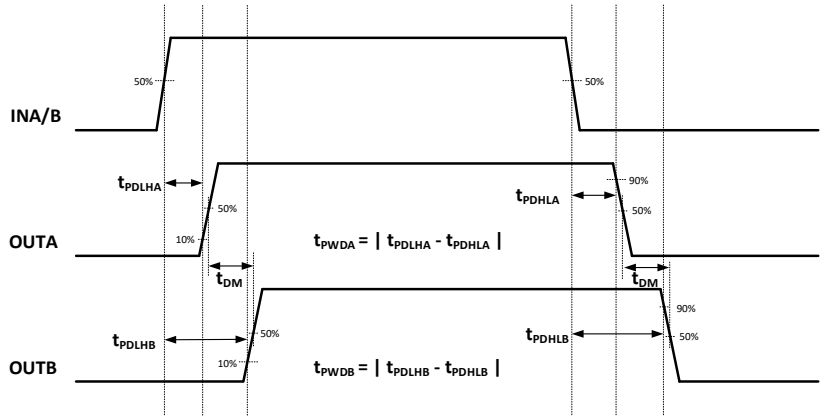


Figure 8-1. Propagation delay and pulse width distortion timing diagram (overlapping input and dead-time disabled)

8.2. Rise Time and Fall Time

Figure 8-2 shows the definition of rising time (t_r) and falling time (t_f).

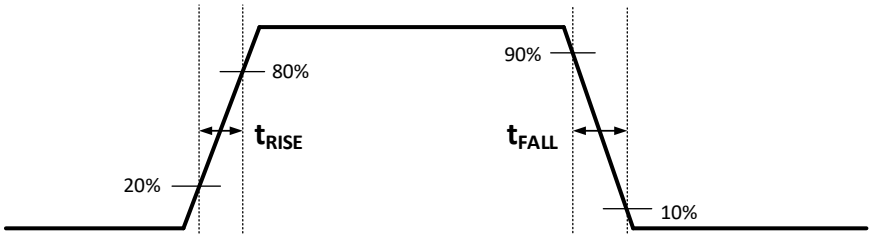


Figure 8-2. Rise time and fall time

8.3. Input and Disable Signals Response Time

Figure 8-3 shows the disable signal response timing. Bypass DIS pin to GNDI with a 1nF low-ESR/low-ESL capacitor close to DIS pin if connecting to a micro-controller with distance.

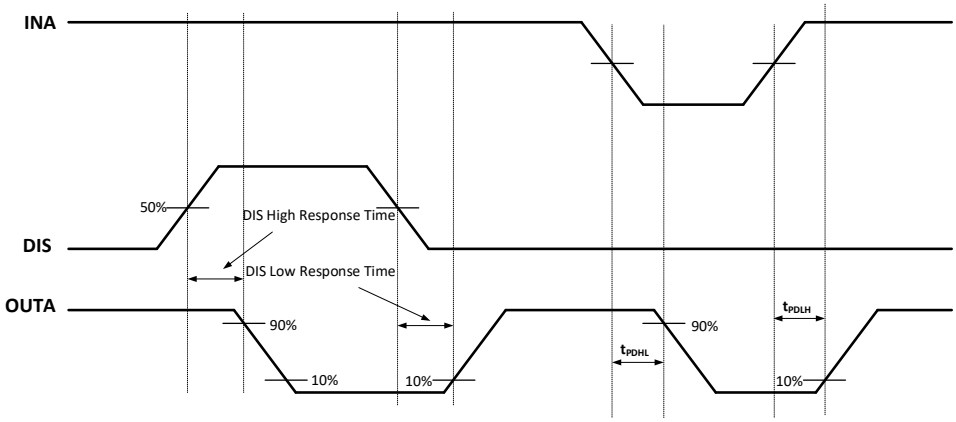


Figure 8-3. Disable timing diagram

8.4. Programmable Dead-time

Figure 8-4 shows the dead-time measurement. Leaving pin DT open or connecting an external resistor R_{DT} between DT and GNDI sets the dead-time. For more details, please see Programmable Dead-time section .

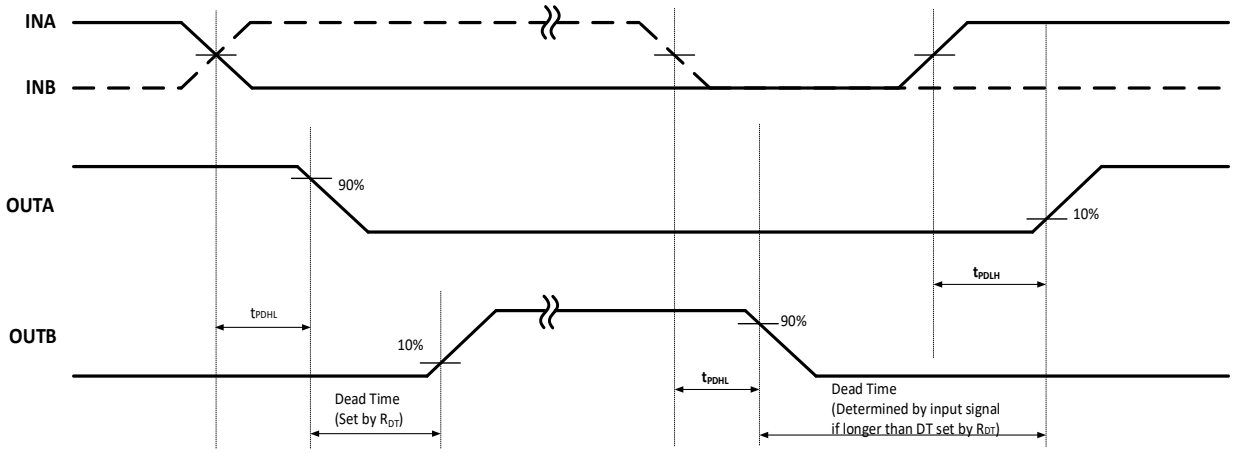


Figure 8-4. Dead-time switching parameters

8.5. Power-up UVLO Delay

Before the device enter normal operation and get ready to provide driver output correctly, there is a power-up delay from UVLO rising edge to driver output. This delay time is defined as $t_{VCCI+\ to\ OUT}$ for VCCI UVLO (55us, typ) and $t_{VDD\_+\ to\ OUT}$ for VDD_ UVLO (68us, typ), see Figure 8-5 VCCI/VDD_ power-up delay timing diagram. Designers need to leave proper margin before sending PWM signal to INA/INB after the VCCI and VDD_ supply get ready. The driver A and driver B will not respond any input signals and will keep logic low until $t_{VCCI+\ to\ OUT}$ or $t_{VDD\_+\ to\ OUT}$ after VCCI or VDD crossing its UVLO rising threshold. However, when either VCCI or VDDA/VDDB voltage are less than their respective off thresholds, there is a maximum 1µs delay (depending on the supply voltage slew rate), before the outputs are held low. This delay is designed to ensure the safe operation during VCCI or VDDA/VDDB brownouts.

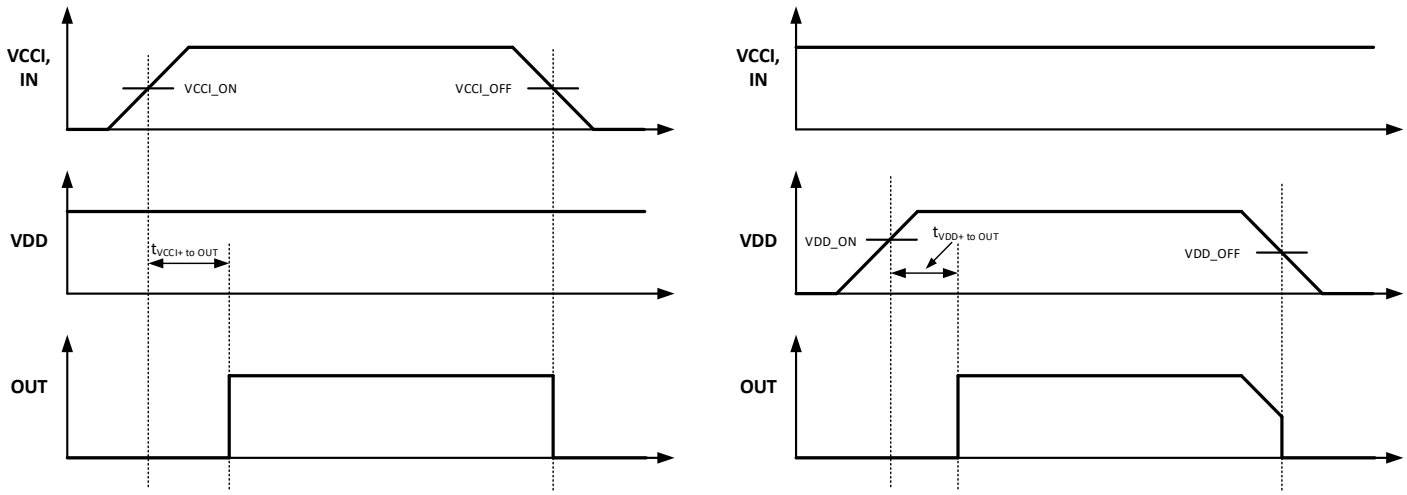


Figure 8-5. VCCI/VDD_ UVLO power-up delay

8.6. CMTI Test Circuit

Figure 8-6 is the CMTI test configuration for the CA-IS322x.

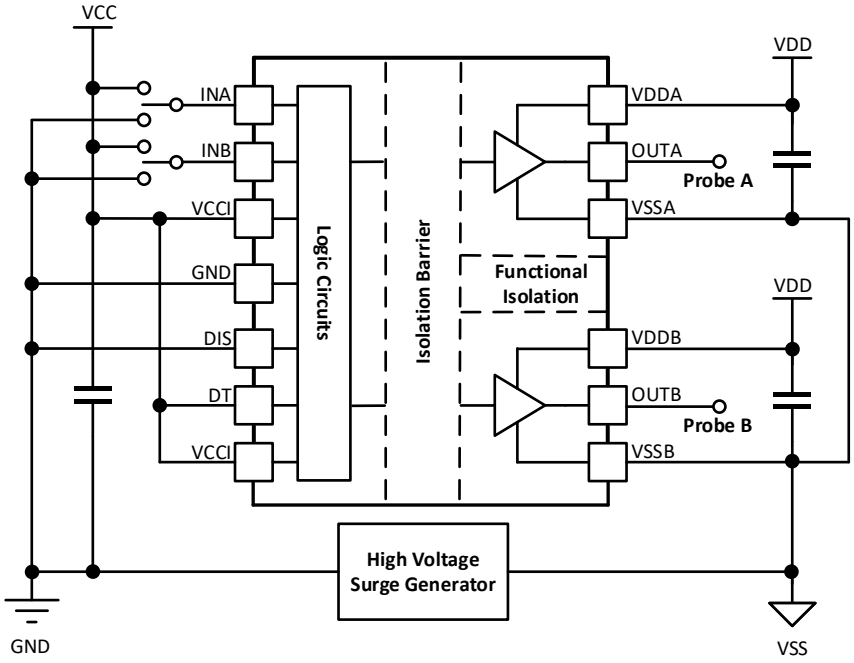


Figure 8-6. Common-mode transient immunity test circuit

9. Detailed Description

9.1. Overview

To quickly switch the power transistors to reduce switching power dissipation, a high-current, high-frequency gate driver is often placed between the controller output and the gate of power transistors, because the controllers are not capable of delivering sufficient current to drive the gates of power transistors. Also, the new power switches, such as silicon carbide (SiC) and gallium nitride (GaN) FETs are replacing traditional MOSFET and IGBT technologies in power switching applications, these new semiconductor materials can operate at higher speeds and temperatures safely, enabling smaller and more efficient designs in different applications. However, they make new demands for the gate driver, for example, high common-mode transient immunity (CMTI) and low propagation delay skew are two of the most important specifications for the new gate drivers.

The CA-IS322x family of dual-channel isolated gate drivers is designed to meet above requirements. The devices have very fast switching time, propagation delay time is minimized (56ns, typ) and matched between the dual channels within 5ns maximum. These advantages make them ideal for high-frequency, small size power system design. All devices support a minimum pulse width of 20ns with a maximum pulse width distortion of 14ns over the -40°C to +125°C operating temperature range.

These isolated gate drivers capable of sinking 6A and sourcing 5A peak currents. Programmable dead-time and internal logic circuitry prevent shoot-through during output-state changes. The devices have dual noninverting input drivers that operate from a +3V to +18V VCCI input-side power supply and up to 25V output-side supply. They also feature active-high enable control (CA-IS3222) or active-high disable control (CA-IS3221) on input-side for better control of driver operation. The default-low output is the state the output assumes when the input is either not powered or is open-circuit. Also, the driver outputs are set to logic-low when input-side or output-side supply is in UVLO, or the device is disabled. Undervoltage lockout (UVLO) with hysteresis is integrated on both $V_{DD\_}$ supply and V_{CCI} supply which ensure robust system performance under noisy conditions.

Figure 9-1 provides a simplified block diagram for the CA-IS322x isolated gate drivers. It shows the main elements of CA-IS322x, including input stage, output stage, dead-time control, V_{CCI} and $V_{DD\_}$ UVLO, digital isolator etc. functional groups. Their operations are described separately in the following sections.

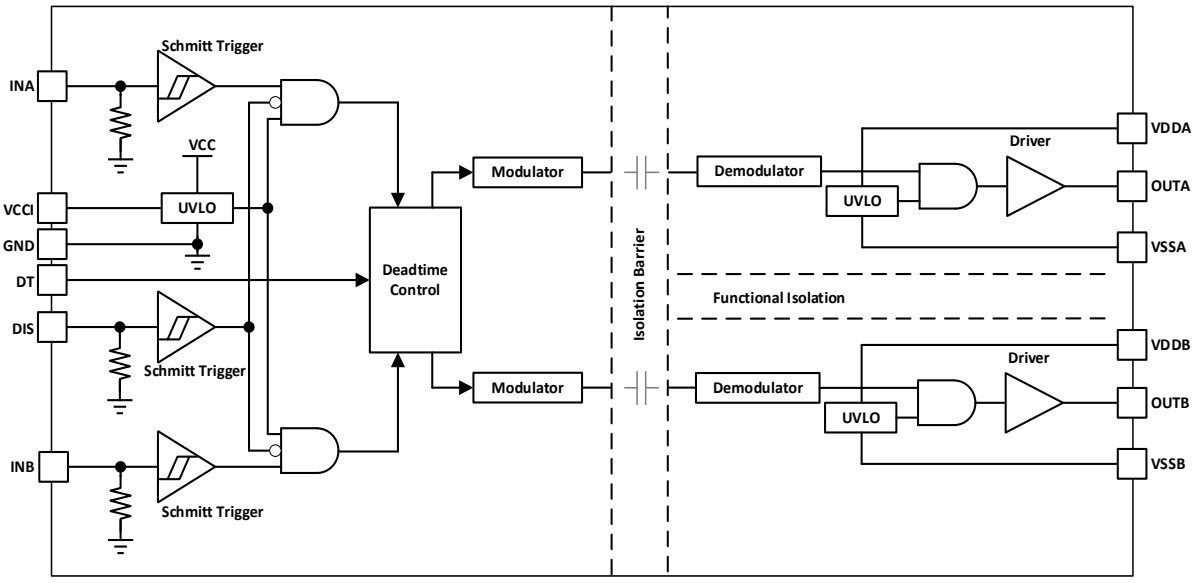


Figure 9-1. Functional block diagram

9.2. Input Stage

9.2.1. TTL and CMOS compatible inputs

The CA-IS322x devices have TTL and CMOS compatible inputs (INA, INB, DIS/EN). Their input-threshold logic (1.8V typical high threshold and 1V typical low threshold) is totally isolated from the $V_{DD\_}$ supply voltage and easy to connect with external micro-controllers. A 0.8V wide hysteresis and accurate threshold over wide-temperature range provide good noise immunity and stable operation. These devices have dual single-ended inputs (INA and INB) that reject input glitches and prevent false turn-on of the output when the input-pulses or noise transients are shorter than 20ns. The output holds the previous value when a glitch is detected on either input. Also, both INA and INB have internal pull-down resistor. If any of the inputs are left open, internal pull-down force the pin low. However, it is still recommended to connect the unused input pin to ground.

Since the input-side and output-side is separated by capacitive silicon dioxide (SiO_2) insulation barrier, the input signal amplitude of the CA-IS322x can be larger or smaller than the output-side supply voltage(V_{DDA}/V_{DDB}), however, the amplitude of any signal applied to INA or INB must never be exceed V_{CCI}, see Absolute Maximum Ratings1 table. This offers greater flexibility to choose the most efficient $V_{DD\_}$ supply rail for a given power transistors.

9.2.2. Enable and Disable Control

The CA-IS3221 features disable control (DIS) and the CA-IS3222 features enable control (EN). For the CA-IS3222 devices, drive EN low or connect to GNDI to disable isolator and put driver outputs low; Drive EN high or leave open, enable gate drivers. For the CA-IS3221 devices, drive DIS high to disable isolator and put driver output low; Drive DIS low or leave open, enable gate driver. We recommend to connect DIS pin to GNDI or connect EN pin to V_{CCI} to ensure stable operation when either disable control or enable control is not used. Also, bypass DIS pin or EN pin to GNDI with a 1nF low-ESR/low-ESL capacitor close to the pins if connecting to a micro-controller with distance. The EN pin has a weak pull-up to V_{CCI}, the DIS and INA/INB input pins have a weak pull-down to GNDI. Refer to Table 9-1 and Table 9-2 for the inputs vs. output truth tables for the CA-IS3221 and the CA-IS3222, respectively.

Table 9-1. The CA-IS3221 Inputs vs. Output Truth Table[1]

Input			Output		Description
INA	INB	Disable (DIS)	OUTA	OUTB	
L	L	L or Open	L	L	If Dead Time function is used, output transitions occur after the dead time expires. See Programmable Dead-time section for more details.
L	H	L or Open	L	H	
H	L	L or Open	H	L	
H	H	L or Open	L	L	DT is programmed with R_{DT}.
H	H	L or Open	H	H	DT is tied to VCCI.
Open	Open	L or Open	L	L	
X	X	H	L	L	

Notes:
1. X = don't care; H = high level; L = low level.
2. DIS pin has an internal weak pull-down to GNDI.

Table 9-2. The CA-IS3222 Inputs vs. Output Truth Table[1]

Input			Output		Description
INA	INB	Enable (EN)	OUTA	OUTB	
L	L	H or Open	L	L	If Dead Time function is used, output transitions occur after the dead time expires. See Programmable Dead-time section for more details.
L	H	H or Open	L	H	
H	L	H or Open	H	L	
H	H	H or Open	L	L	DT is programmed with R_{DT}.
H	H	H or Open	H	H	DT is tied to VCCI.
Open	Open	H or Open	L	L	
X	X	L	L	L	

Notes:
1. X = don't care; H = high level; L = low level.
2. EN pin has an internal weak pull-up to VCCI.

9.3. Driver Output Stage

The CA-IS322x devices provide two separate outputs. They have distinct current sourcing/sinking capabilities to control the external transistors independently. The internal functional isolation between driver A and driver B on the output-side allows up to 1500V DC working voltage. Figure 9-2 shows the output stage structure, both output channels integrate a pull-up structure and a pull-down structure. A p-channel MOSFET and an additional n-channel MOSFET in parallel combined into the pull-up structure. The n-channel MOSFET only turns on for a short period of time during the output low-to-high transition and provides a boost in the peak-sourcing current to enable the fast turn-on of the device. This is performed by briefly turning on the n-channel MOSFET during a narrow instant when the output is changing from low to high. The on-resistance of this n-channel MOSFET (R_{NMOS}) is about 0.8 Ω when activated. In Figure 9-2, $R_{OH\_}$ (5Ω, typ.) is the on-resistance of the P-channel MOSFET only. This is because the n-channel MOSFET is placed in off state in DC condition and is turned on only for a very short time. Thus, the effective on-resistance($R_{NMOS}||R_{OH\_}$) of the output pull-up stage during NMOS turn-on phase is much lower than $R_{OH\_}$. This provides a very low-impedance path to direct the Miller current.

The pull-down circuit is simply composed of an n-channel MOSFET. R_{OL} in Figure 9-2 is the on-resistance of the pull-down NMOS. Because of the very low turn-on impedance of the output stage MOSFETs, the CA-IS322x isolated gate drivers support rail-to-rail outputs (output voltage swings between VDD_ and VSS_).

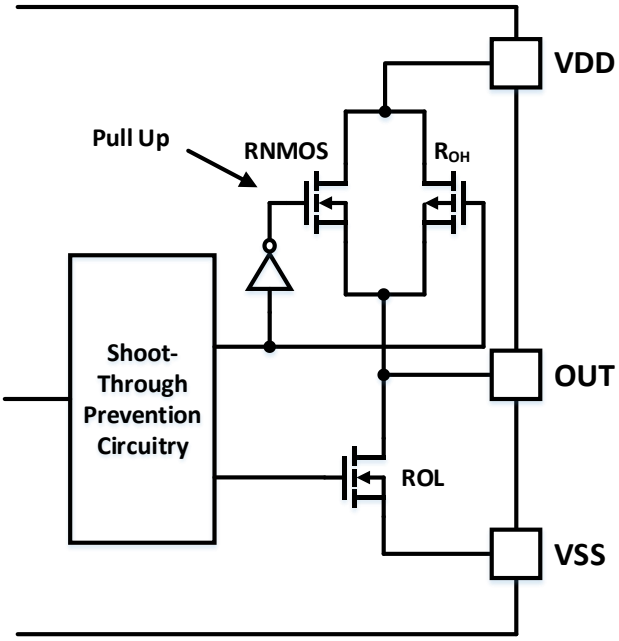


Figure 9-2. Driver output stage

9.4. Undervoltage Lockout (UVLO)

The input-side (V_{CCI}) and output-side($V_{DD\_}$) supplies are both internally monitored for undervoltage conditions. When an undervoltage condition is detected on either supply, the gate driver outputs are set to logic-low (default state) to turn off the external power transistor, regardless of the state of the inputs (INA, INB).

On the output-side, the supply terminal V_{DDA} and V_{DDB} undervoltage detection places the driver output OUTA/OUTB in logic-low during an undervoltage event on $V_{DD\_}$, $V_{DD\_} < V_{VDDA(UVLO+)}$ during power on, or $V_{DD\_} < V_{VDD\_(UVLO-)}$ during power-down or during normal operation due to a sagging supply voltage. The CA-IS322x offers 8V and 12V UVLO threshold options. See Figure 9-3, when the driver output stages are in power-off or UVLO condition, the upper p-channel MOSFET is held off by R_{Hi-Z} while the n-channel MOSFET gate is connected to the driver output through R_{CLAMP}. This active clamp circuit holds driver outputs to the threshold voltage of the lower n-channel MOSFET(typically around 1.5 V) or low state and limits the voltage rise on the driver outputs.

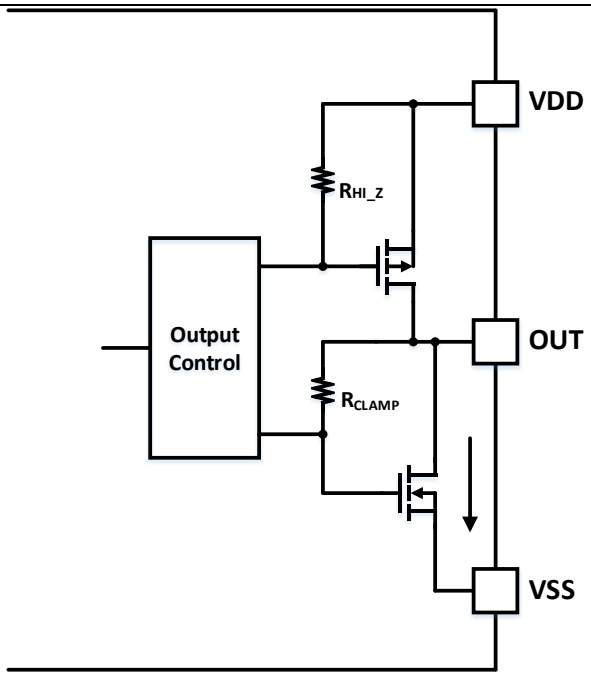


Figure 9-3. Active pull-down

On the input-side, the device isn't active unless the VCCI voltage is going to exceed $V_{VCCI(UVLO+)}$ during start up. And input signals will stop to be delivered when the supply voltage less than $V_{VCCI(UVLO-)}$.

Once an undervoltage condition is cleared and the supply voltage has returned to a valid level, the CA-IS322x gate drivers transition to normal mode after the power-up delay time ($t_{VCCI+ \text{ to } OUT}$ or $t_{VDD\_+ \text{ to } OUT}$) has expired. Both V_{CCI} UVLO and $V_{DD\_}$ UVLO have hysteresis to avoid chattering when there is ground noise from the power supply, also allows the device to accept small drops in supply voltage and ensures stable operation. Table 9-3 and Table 9-4 illustrate the V_{CCI} UVLO and $V_{DD\_}$ UVLO feature logic.

Table 9-3. The CA-IS322x output behavior during V_{CCI} undervoltage conditions

Conditions	Input		Output	
	INA	INB	OUTA	OUTB
VCCI-GNDI < $V_{VCCI(UVLO+)}$ during device start up	H	L	L	L
VCCI-GNDI < $V_{VCCI(UVLO+)}$ during device start up	L	H	L	L
VCCI-GNDI < $V_{VCCI(UVLO+)}$ during device start up	H	H	L	L
VCCI-GNDI < $V_{VCCI(UVLO+)}$ during device start up	L	L	L	L
VCCI-GNDI < $V_{VCCI(UVLO-)}$ after device start up	H	L	L	L
VCCI-GNDI < $V_{VCCI(UVLO-)}$ after device start up	L	H	L	L
VCCI-GNDI < $V_{VCCI(UVLO-)}$ after device start up	H	H	L	L
VCCI-GNDI < $V_{VCCI(UVLO-)}$ after device start up	L	L	L	L

Table 9-4. The CA-IS322x output behavior during $V_{DD\_}$ undervoltage conditions

Conditions	Input		Output	
	INA	INB	OUTA	OUTB
VDD_ - VSS_ < $V_{VDD\_(UVLO+)}$ during device start up	H	L	L	L
VDD_ - VSS_ < $V_{VDD\_(UVLO+)}$ during device start up	L	H	L	L
VDD_ - VSS_ < $V_{VDD\_(UVLO+)}$ during device start up	H	H	L	L
VDD_ - VSS_ < $V_{VDD\_(UVLO+)}$ during device start up	L	L	L	L
VDD_ - VSS_ < $V_{VDD\_(UVLO-)}$ after device start up	H	L	L	L
VDD_ - VSS_ < $V_{VDD\_(UVLO-)}$ after device start up	L	H	L	L
VDD_ - VSS_ < $V_{VDD\_(UVLO-)}$ after device start up	H	H	L	L
VDD_ - VSS_ < $V_{VDD\_(UVLO-)}$ after device start up	L	L	L	L

9.5. Digital Isolation

The CA-IS322x devices integrated digital galvanic isolators using Chipanalog's capacitive isolation technology based on the ON-OFF keying (OOK) modulation scheme, allow data transmission between the driver input-side and driver output-side with different power domains. These devices feature up to 3.75kV$_{RMS}$ (narrow-body SOIC package) of galvanic isolation and ±100V/ns minimum CMTI.

9.6. ESD Protection Structure

Figure 9-4 illustrates the enhanced ESD protection structure on the input-side and output-side. The VCCI pin and VDDA/VDDB pins are protected against voltage spikes up to +20V and 30V respectively, regardless of V_{CCI} and $V_{DD\_}$ voltages.

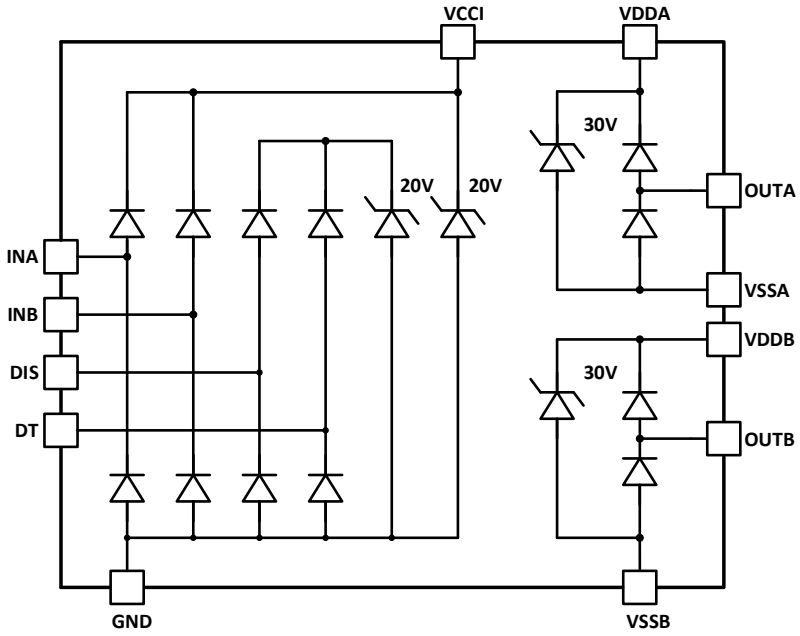


Figure 9-4. ESD protection circuit

9.7. Programmable Dead-time

The CA-IS322x isolated gate drivers have a programmable dead-time circuit to prevent shoot-through current caused by high-side and low-side power transistors overlap, as this would lead to a potentially damaging short-circuit type condition in the typical applications.

Resistor R_{DT} connected from the DT pin of the CA-IS322x to GNDI programs the amount of dead-time. This amount of dead time is applied to both leading and trailing edges of the drive signals OUTA and OUTB. The dead-time can be calculated by below equation:

$$t_{DT} \approx 10 \times R_{DT} \quad (1)$$

Where R_{DT} is in kΩ and t_{DT} is in ns. The steady state voltage at DT is approximately 0.8V. If a value of 100 kΩ is chosen for R_{DT}, the DT pin current will be less than 10uA. If R_{DT} > 5kΩ, it is recommended to parallel an at least 2.2nF ceramic capacitor as close to R_{DT} as possible to achieve better noise immunity and better dead time matching between driver A and driver B. IF DT pin be tied to V_{CCI}, this allows outputs overlap and completely match inputs. However, the DT Pin don't allow floating.

The programmed dead time is asserted by input signal's falling edge. If both INA and INB inputs are pulled high simultaneously, both outputs (OUTA, OUTB) will immediately be set low to turn-off external power transistors. This feature is used to prevent shoot-through, and it doesn't affect the programmed dead time setting for normal operation. Figure 9-5 shows various driver dead time logic and operating conditions.

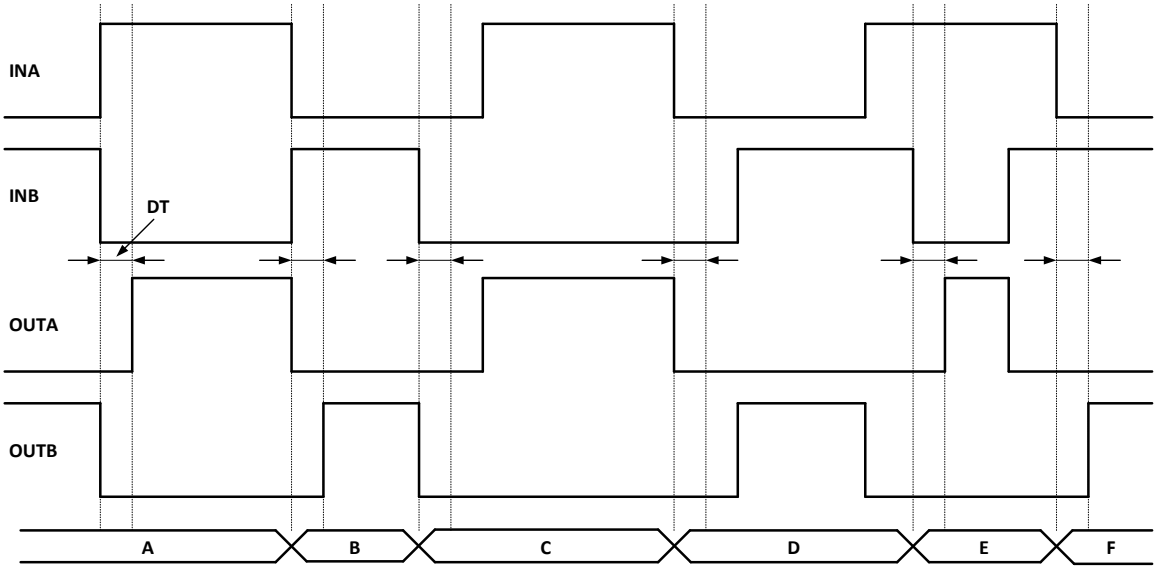


Figure 9-5. Output and input signals relationship with a programmed dead-time

In Figure 9-5 programmed dead-time timing diagram:

A: INB goes low and INA goes high; INB going low will set OUTB low immediately; The INB falling edge asserts programmed dead-time t_{DT} and applies the dead-time to OUTA. OUTA is allowed to go high after t_{DT}.

B: INB goes high and INA goes low; INA will set OUTA low immediately; The INA falling edge asserts programmed dead-time t_{DT} and applies the dead-time to OUTB. OUTB is allowed to go high after t_{DT}.

C: INB goes low, INA is still kept low; INB will set OUTB low immediately; The INB falling edge asserts programmed dead-time t_{DT} and applies the dead-time to OUTA. OUTA is allowed to go high after t_{DT}. In this case, as the INA is still kept low after t_{DT}, this means that INA input's "dead-time" is longer than t_{DT}. Thus, when INA is pulled high, OUTA will go high immediately.

D: INA goes low, INB is still kept low; INA will set OUTA low immediately; The INA falling edge asserts programmed dead-time t_{DT} and assigns the dead-time to OUTB. OUTB is allowed to go high after t_{DT}. In this case, as the INB is still kept low after t_{DT}, this means that INB input's "dead-time" is longer than t_{DT}. Thus, when INB is pulled high, OUTB will go high immediately.

E: INA goes high, both INB and OUTB are still kept high; INA will pull OUTB low immediately and keep OUTA low to avoid overshoot. After OUTB goes low, after a delay time, the device applies the programmed dead time to OUTA. OUTB is already pulled to low. After the programmed dead time, OUTA is allowed to go high.

F: INB goes high, both INA and OUTA are still kept high; INB will pull OUTA low immediately and keep OUTB low to avoid overshoot. After OUTA goes low, after a delay time, the device applies the programmed dead time to OUTB. OUTA is already pulled to low. After the programmed dead time, OUTB is allowed to go high.

10. Application and Implementation

10.1. Typical Application

The CA-IS322x isolated gate drivers are designed to drive power MOSFET, IGBT or silicon-carbide(SiC) transistors in various power supply systems to optimize system cost and efficiency. This family of devices can be configured as dual low-side, dual high-side or half-bridge drivers. The enable control (EN pin for the CA-IS3222) and disable control (DIS pin for the CA-IS3221) allow both driver A and driver B outputs to be quickly set to logic-low, turning off the external power transistor. The default-low output keeps the output in low state when input-side or output-side supply is in UVLO, or the device is disabled. The high CMTI rating of 100V/ns (min), high isolation rating, programmable dead-time, UVLO detection and the propagation delay matching of 5ns (max) between channels make the CA-IS322x devices ideal to drive high-power transistors in the industrial, automotive etc. high reliability applications.

Figure 10-1 shows the CA-IS322x typical application circuit, the CA-IS3221 is configured as a half-bridge driver which can be used in synchronous buck, synchronous boost power converters and half-bridge/full bridge isolated topologies, 3-phase motor drive applications.

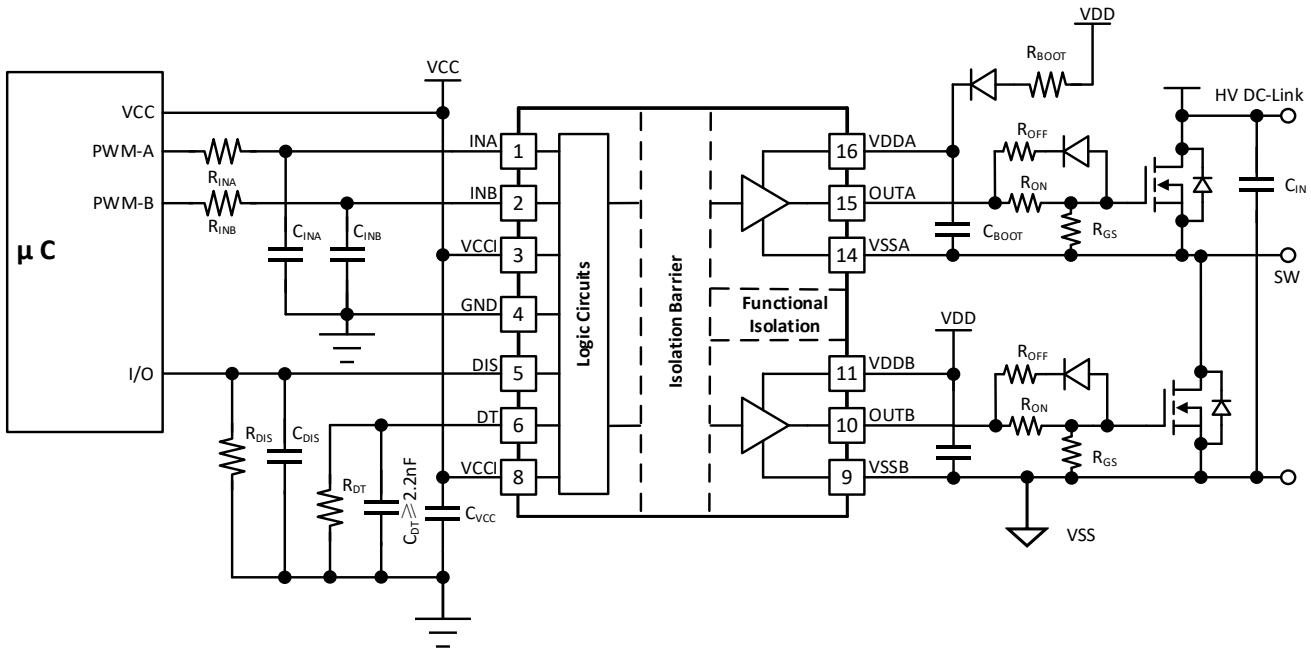


Figure 10-1. Typical application circuit for CA-IS3221-Q1

Table 10-1 lists the CA-IS322x design parameters in a typical high-side and low-side configuration, power transistor is 1200V SiC MOSFET.

Table 10-1. The CA-IS322x design requirement

Parameter	Value	Unit
Power transistor	80mΩ/31A/1200V	-
V_{CCI}	5.0	V
$V_{DD\_}$	20	V
Input amplitude	3.3	V
Switching frequency (f_s)	100	kHz
HV DC	800	V

10.2. Power Supply

The CA-IS322x devices operate in wide-supply range, V_{CCI} accepts 3V to 18V supply and $V_{DD\_}$ accepts up to 25V and as low as $V_{VDD\_(UVLO+)}$ supply voltage. They do not require special power-supply sequencing. However, suitable supply bypassing and device grounding are extremely important.

To reduce power ripple, for the input side, we recommended 100nF/25V and 1uF/25V low-ESR and low-ESL ceramic capacitors in parallel between VCCI pin and GNDI. To ensure the best performance, place the decoupling capacitor as close to the power-supply pin as possible. On the output-side, bypass VDDA and VDDB with 100nF/50V, 10μF/50V low-ESR ceramic capacitors in parallel to VSSA and VSSB, respectively. It is recommended to place the capacitors close to the VDD_ pins.

10.3. Input Filter Selection

As we know the input signal may be non-ideal when the PCB traces of MCU is too long or non-ideal layout, It is recommended that users add R_{IN}-C_{IN} low pass filter to reduce input noise. Such a filter should use an R_{IN} in the range of 0 Ω to100 Ω and a C_{IN} between 10 pF and 100 pF. When selecting these components, it is important to pay attention to the trade-off between good noise immunity and propagation delay.
In the example, an R_{IN} = 51 Ω and a C_{IN} = 33 pF are selected, with a corner frequency of approximately 95 MHz.

10.4. Gate Resistance Selection

In the typical application circuits Figure 10-1, there are two external gate driver resistors: R_{GOFF} and R_{GON}, R_{GOFF} is the external turn-off resistance; R_{GON} is the external turn-on resistance. These two resistors are chosen to limit the ringing caused by fast switching and parasitic inductances and capacitances, reduce EMI, also can be used to fine-tune gate drive strength and optimize the switching loss. Use the following equations to estimate R_{GOFF} and R_{GON} resistor values,

I_{OH} peak current calculation:

$$I_{OH} = \min\left[5A, \quad \frac{V_{DD} - V_{EE}}{\left(R_{NMOS}||R_{OH} + R_{GON} + R_{GFET_{int}}\right)}\right]$$

Where $R_{GFETint}$ is the gate resistance of the external power transistor, this number is available from power transistor data sheet. R_{NMOS} is 0.8ohm. R_{OH} is 5.5ohm.

I_{OL} peak current calculation:

$$I_{OL} = \min\left[6A, \quad \frac{V_{DD} - V_{EE}}{\left(R_{OL} + R_{GOFF} + R_{GFET_{int}}\right)}\right]$$

Where $R_{GFETint}$ is the gate resistance of the external power transistor, this number is available from power transistor data sheet. R_{OL} is 0.5ohm.

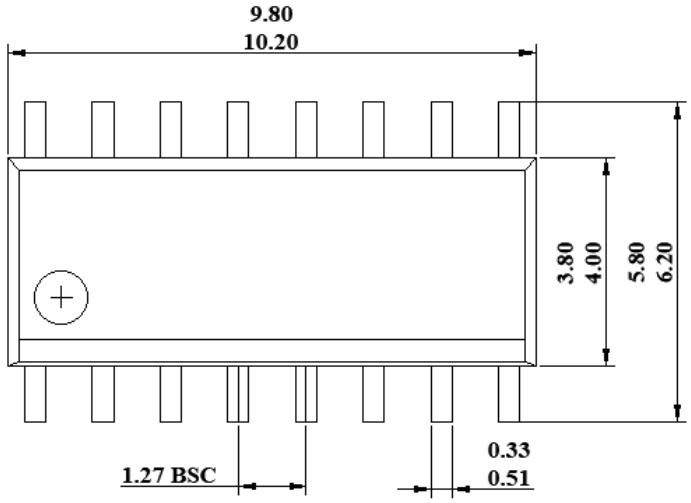
10.5. PCB Layout

Due to high current levels and fast switching(high dv/dt and di/dt) that radiate noise, proper PC board layout is essential. Follow these guidelines for good PCB layout:

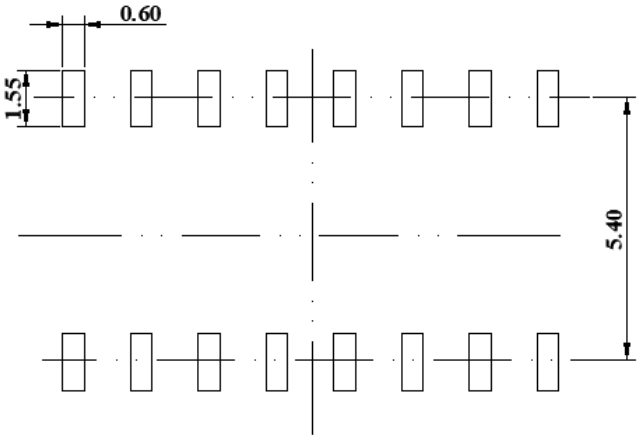
- To ensure the best performance and keep lower supply ripple, place the decoupling capacitors as close to the power-supply pin as possible. We recommend to use low ESR, low ESL MLCC capacitors in order to support more higher peak current.
- To avoid large negative transients on the switch node VSSA (HS) pin, the parasitic inductances between the source of the top transistor and the source of the bottom transistor must be minimized.
- When the MCU is far away from the driver chip, it is recommended to place the bypass capacitor as close as possible to the EN or DIS pin to reduce noise interference.
- To ensure isolation performance between the primary side and secondary side, on the top layer and bottom layer keep the space under the CA-IS322x device free from traces, vias, and pads to maintain maximum creepage distance.
- For half-bridge or high-side/low-side configurations, Channel A and Channel B drivers can operate at DC bus voltages up to 1500 VDC, and an additional PCB should be attempted creepage distance, which is the layout between the high-side and low-side PCB traces.
- OUTx connections carrying pulsed currents must be very short and as wide as possible. The inductance of these connections must be kept to an absolute minimum due to the high di/dt of the currents in high-frequency-switching operation. This implies that the OUTx loop areas should be minimized. Additionally, small current loop areas reduce radiated EMI. Place the external transistor as close to the gate driver as possible.
- When the load is heavy or the switching frequency is high, the loss of the chip also increases, it is recommended to properly increase the PCB copper cladding of the VDD and VSS pins so that it decreases the temperature of chip, the thermal can be transferred to the PCB board.
- For the multiple layers design, it is recommended to connect the VDD and VSS pins to internal ground or power planes through multiple vias. These vias should be located close to the IC pins to maximize thermal conductivity, also keep lower parasitic value.

11. Package Information

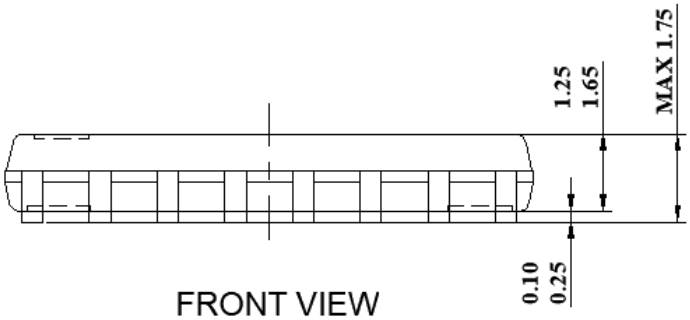
The following image show a 16-pin narrow body package.



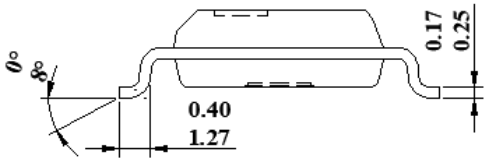
TOP VIEW



RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW

Note:

1. All dimensions are in millimeters, angles are in degrees.

12. Soldering Temperature (reflow) Profile

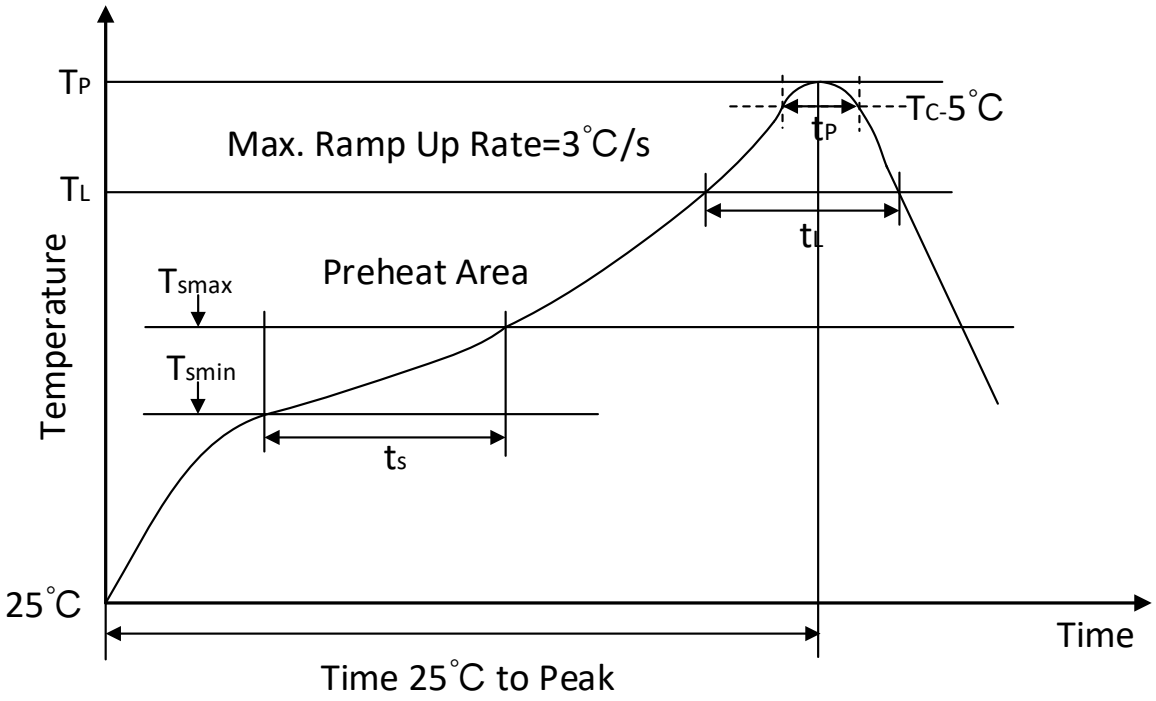


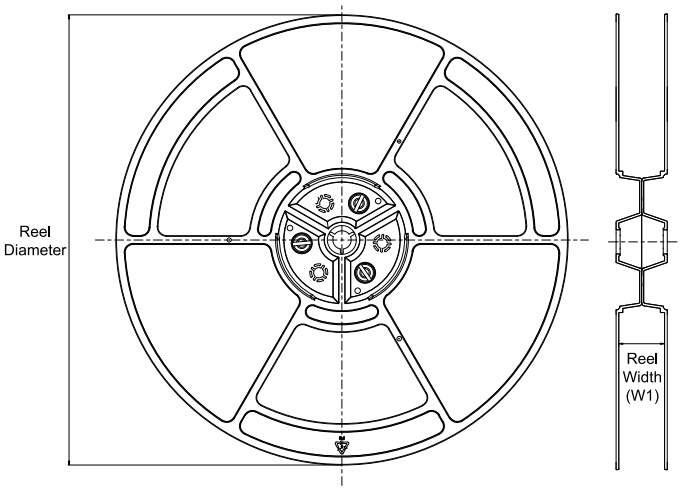
Figure 12-1. Soldering Temperature (reflow) Profile

Table 12-1. Soldering Temperature Parameter

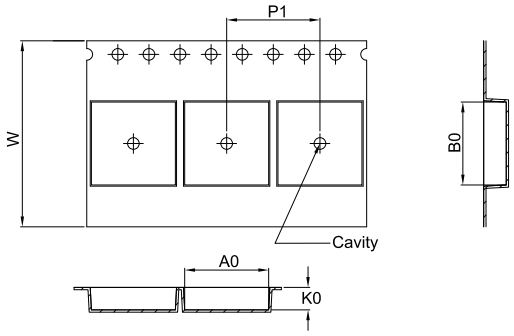
Profile Feature	Pb-Free Assembly
Average ramp-up rate(217˚C to Peak)	3˚C /second max
Time of Preheat temp(from 150 ˚C to 200 ˚C	60-120 second
Time to be maintained above 217˚C	60-150 second
Peak temperature	260 +5/-0˚C
Time within 5˚C of actual peak temp	30 second
Ramp-down rate	6 ˚C /second max.
Time from 25˚C to peak temp	8 minutes max

13. Tape and Reel Information

REEL DIMENSIONS

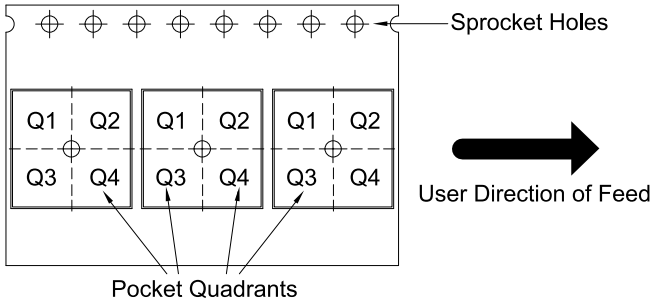


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CA-IS3221AN-Q1	SOIC16-NB	N	16	2500	330	16.4	6.40	10.30	2.10	8.00	16.00	Q1
CA-IS3221BN-Q1	SOIC16-NB	N	16	2500	330	16.4	6.40	10.30	2.10	8.00	16.00	Q1
CA-IS3221CN-Q1	SOIC16-NB	N	16	2500	330	16.4	6.40	10.30	2.10	8.00	16.00	Q1
CA-IS3222AN-Q1	SOIC16-NB	N	16	2500	330	16.4	6.40	10.30	2.10	8.00	16.00	Q1
CA-IS3222BN-Q1	SOIC16-NB	N	16	2500	330	16.4	6.40	10.30	2.10	8.00	16.00	Q1
CA-IS3222CN-Q1	SOIC16-NB	N	16	2500	330	16.4	6.40	10.30	2.10	8.00	16.00	Q1

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