CA-IS3710 High-Speed Single-Channel Digital Isolator

1. Features

- **Robust Galvanic Isolation of Digital Signals**
  - High lifetime: > 40 years
  - Up to 3750V_{RMS} isolation rating
  - ±150 kV/μs typical CMTI
  - Schmitt trigger inputs
- **Interfaces Directly with Most MCUs and FPGAs**
  - Data rate: DC to 150Mbps
  - Accepts 2.5V to 5.5V supplies
  - Default output *High* (CA-IS3710HS) and *Low* (CA-IS3710LS) Options
- **Low Power Consumption**
  - 1.5mA per channel at 1Mbps with V_{DD} = 5.0V
  - 6.6mA per channel at 100Mbps with V_{DD} = 5.0V
- **Best in class propagation delay and skew**
  - 12ns typical propagation delay
  - 1ns pulse width distortion
  - 2ns propagation delay skew (chip -to-chip)
  - 5ns minimum pulse width
- **No Start-Up Initialization Required**
- **Wide operating temperature range: -40°C to 125°C**
- **Narrow-body SOIC8(S) package**
- **Safety Regulatory Approvals**
  - VDE 0884-17 isolation certification
  - UL According to UL1577
  - IEC 62368-1, IEC 61010-1, GB 4943.1-2011 and GB 8898-2011 certifications

2. Applications

- Industrial Automation
- Motor Control
- Medical Systems
- Isolated Power Supplies
- Solar Inverters
- Isolated ADC,DAC
- Automotive

3. General Description

The CA-IS3710 devices are high-performance single-channel, unidirectional digital isolator with up to 3.75kV_{RMS} isolation rating and ultra-fast data rate. This device offers high electromagnetic immunity and low emissions at low power consumption while isolating different ground domains and block high-voltage/high-current transients from sensitive or human interface circuitry. Internal isolation channel has a logic input and output buffer separated by capacitive silicon dioxide (SiO_2) insulation barrier, the integrated Schmitt trigger on the input provides excellent noise immunity.

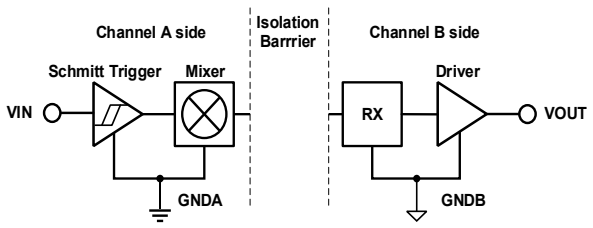
The CA-IS3710 devices feature default outputs. When the input is either not powered or is open-circuit, the default output is low for devices with suffix L and high for devices with suffix H, see the Ordering Information for suffixes associated with each option.

The CA-IS3710 series devices are specified over the -40°C to +125°C operating temperature range and are available in 8-pin SOIC narrow body package.

Device information

Part number	Package	Package size (NOM)
CA-IS3710HS-Q1	SOIC8(S)	4.90 mm × 3.90 mm
CA-IS3710LS-Q1		

Simplified Channel Structure



GNDA and GNDB are the isolated grounds for A side and B side respectively.

4. Ordering Information

Table 4-1. Ordering Information

Part Number	Number of Inputs A Side	Number of Inputs B Side	Default Output	Isolation Rating (kV_{rms})	Output Enable	Package
CA-IS3710LS-Q1	1	0	Low	3.75	No	SOIC8-NB
CA-IS3710HS-Q1	1	0	High	3.75	No	SOIC8-NB

Contents

5. Revision History

Revision Number	Description	Page Changed
Version 1.00	N/A	N/A
Version 1.01	$V_{IT+(IN)}$ Min value changed to 2V， $V_{IT-(IN)}$ max value changed to 0.8V, removed $V_{I(HYS)}$。	8,11, 12, 13
Version 1.02	Description of $V_{IT+(IN)}$ changed to rising input switching threshold and $V_{IT-(IN)}$ changed to falling input switching threshold.	8
Version 1.03	Changed POD and tape and reel information.	16,18
Version 1.04	Update VDE certification information.	6,7
Version 1.04	Update TUV and UL certification information.	7

6. Pin Configuration and Description

CA-IS3710 8-Pin SOIC Top View

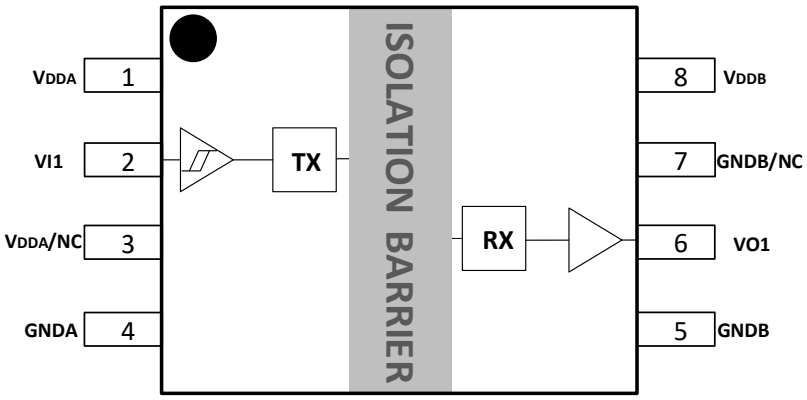


Figure 6-1. CA-IS3710 pin configuration

Table 6-1. CA-IS3710 pin description

8-Pin SOIC pin# CA-IS3710	Name	Type	Description
1	V_{DDA}	Supply	Power supply for side A.
2	VI1	Digital I/O	Digital input 1 on side A, corresponds to logic output 1 on side B.
3	V_{DDA}/NC	---	Not internally connected.
4	GNDA	Ground	Ground reference for side A.
5	GNDB	Ground	Ground reference for side B.
6	VO1	Digital I/O	Digital output 1 on side B, VO1 is the logic output for the VI1 input on side A.
7	GNDB/NC		Not internally connected.
8	VDDB	Supply	Power supply for side B.

7. Specifications

7.1. Absolute Maximum Ratings[1]

Parameters		Minimum value	Maximum value	Unit
V_{DDA}, V_{DDB}	Power supply voltage [2]	-0.5	7.0	V
V_{IN}	Voltage at VI_X, VO_X	-0.5	$V_{DD\_}$ + 0.5[3]	V
I_O	Output current	-20	20	mA
T_J	Junction temperature		150	°C
T_{STG}	Storage temperature range	-65	150	°C

Notes:
1. The stresses listed under "Absolute Maximum Ratings" are stress ratings only, not for functional operation condition. Exposure to absolute maximum rating conditions for extended periods may cause permanent damage to the device.
2. All voltage values are with respect to the local ground terminal (GNDA or GNDB) and are peak voltage values.
3. Maximum voltage must not be exceed 7 V.

7.2. ESD Ratings

		Numerical value	Unit
V_{ESD} Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins [1]	±6000	V
	Charged device model (CDM), per JEDEC Specification JESD22-C101, all pins[2]	±2000	V

Notes:
1. Per JEDEC document JEP155, 500V HBM allows safe manufacturing of standard ESD control process.
2. Per JEDEC document JEP157, 250V HBM allows safe manufacturing of standard ESD control process.

7.3. Recommended Operating Conditions

	PARAMETER		MIN	TYPE	MAX	UNIT
V_{DDA}, V_{DDB}	Supply voltage on side A, B		2.375	3.3/5.0	5.50	V
$V_{DD(UVLO+)}$	V_{DD} Undervoltage-Lockout Threshold When Supply Voltage is Rising		1.95	2.24	2.375	V
$V_{DD(UVLO-)}$	V_{DD} Undervoltage-Lockout Threshold When Supply Voltage is Falling		1.88	2.10	2.325	V
$V_{HYS(UVLO)}$	V_{DD} Undervoltage-Lockout Threshold Hysteresis		70	140	250	mV
I_{OH}	High-level Output Current	V_{DDO}[1] = 5V	-4			mA
		V_{DDO} = 3.3V	-2			
		V_{DDO} = 2.5V	-1			
I_{OL}	Low-level Output Current	V_{DDO} = 5V			4	mA
		V_{DDO} = 3.3V			2	
		V_{DDO} = 2.5V			1	
V_{IH}	High-level Input Voltage		2.0			V
V_{IL}	Low-level Input Voltage				0.8	V
DR	Data Rate		0		150	Mbps
T_A	Ambient Temperature		-40	27	125	°C

Note:
1. V_{DDO} = Output-side supply V_{DD}.

7.4. Thermal Information

Thermal Metric		CA-IS3710 SOIC8-NB(S)	Unit
$R_{\theta JA}$	Junction-to-ambient thermal resistance	109.0	°C/W

7.5. Power Rating

Parameters		Test conditions	MIN	TYPE	MAX	Unit
CA-IS3710						
P_D	Maximum Power Dissipation	V_{DDA} = V_{DDB} = 5.5 V, C_L = 15 pF, T_J = 150°C, Input a 75-MHz 50% duty cycle square wave.			60	mW
P_{DA}	Maximum Power Dissipation on Side-A				10	mW
P_{DB}	Maximum Power Dissipation on Side-B				50	mW

7.6. Insulation Specifications

Parameters		Test conditions	Value	Unit
			S	
CLR	External Clearance	Shortest terminal-to-terminal distance through air	4	mm
CPG	External Creepage	Shortest terminal-to-terminal distance across the package surface	4	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	28	μm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11)； IEC 60112	>600	V
	Material group	Per IEC 60664-1	I	
Overvoltage category per IEC 60664-1		Rated mains voltage ≤ 150 V_{RMS}	I-IV	
		Rated mains voltage ≤ 300 V_{RMS}	I-III	
		Rated mains voltage ≤ 600 V_{RMS}	N/A	
DIN V VDE V 0884-17:2021-10[1]				
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	566	V_{PK}
V_{IOWM}	Maximum operating isolation voltage	AC voltage; time-dependent dielectric breakdown (TDDB) test	400	V_{RMS}
		DC voltage	566	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t=60 s (certified); $V_{TEST} = 1.2 \times V_{IOTM}$, t=1 s (100% product test)	5300	V_{PK}
V_{IOSM}	Maximum surge isolation voltage[2]	Test method per IEC 62368-1, 1.2/50 μs waveform, $V_{TEST} = 1.3 \times V_{IOSM}$ (qualification)	4070	V_{PK}
q_{pd}	Apparent charge[3]	Method a, after input/output safety test of the subgroup 2/3, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)} = 1.2 \times V_{IORM}$, t_m = 10 s	≤5	pC
		Method a, after environmental test of the subgroup 1, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)} = 1.6 \times V_{IORM}$, t_m = 10 s	≤5	
		Method b, at routine test (100% production test) and preconditioning (type test) $V_{ini} = 1.2 \times V_{IOTM}$, t_{ini} = 1 s; $V_{pd(m)} = 1.5 \times V_{IORM}$, t_m = 1 s	≤5	
C_{IO}	Barrier capacitance, input to output[4]	V_{IO} = 0.4 × sin (2πft), f = 1 MHz	~0.5	pF
R_{IO}	Isolation resistance[4]	V_{IO} = 500 V, T_A = 25°C	$>10^{12}$	Ω
		V_{IO} = 500 V, 100°C ≤ T_A ≤ 125°C	$>10^{11}$	
		V_{IO} = 500 V at T_S = 150°C	$>10^{9}$	
	Pollution degree		2	
UL 1577				
V_{ISO}	Maximum withstanding isolation voltage	$V_{TEST} = V_{ISO}$, t = 60 s (qualification) $V_{TEST} = 1.2 \times V_{ISO}$, t = 1 s (100% production test)	3750	V_{RMS}

Notes:

1. This coupler is suitable for “safe electrical insulation” only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
2. Devices are immersed in oil during surge characterization test.
3. The characterization charge is discharging charge (pd) caused by partial discharge.
4. Capacitance and resistance are measured with all pins on field-side and logic-side tied together.

7.7. Safety-Related Certifications

VDE	UL	TUV
Certified according to DIN EN IEC 60747-17 (VDE 0884-17):2021-10; EN IEC 60747-17:2020+AC:2021	Certified according to UL 1577 Component Recognition Program	Certified according to EN 61010-1:2010+A1
Maximum transient isolation voltage：5300V_{pk}(SOIC8-NB) Maximum repetitive peak isolation voltage：566V_{pk}(SOIC8-NB) Maximum surge isolation voltage：4070V_{pk}(SOIC8-NB)	3750 V_{RMS}(SOIC8-NB)	3750 V_{RMS}(SOIC8-NB)
Certification Number：40052786	Certification Number：E511334	Certification Number：AK 505918190001

7.8. Electrical Characteristics

V_{DDA} = V_{DDB} = 5 V ± 10%, T_A = -40 to 125°C (over recommended operating conditions, unless otherwise specified)

Parameters		Test conditions	MIN	TYPE	MAX	UNIT
V_{OH}	High-level Output Voltage	I_{OH} = -4mA; See Figure 8-2	V_{DDO}[1]-0.4	4.8		V
V_{OL}	Low-level Output Voltage	I_{OL} = 4mA; See Figure 8-2		0.2	0.4	V
$V_{IT+(IN)}$	Rising input switching threshold		2			V
$V_{IT-(IN)}$	Falling input switching threshold				0.8	V
I_{IH}	High-Level Input Leakage Current	V_{IH} = V_{DDA} at INx or ENx			20	μA
I_{IL}	Low-Level Input Leakage Current	V_{IL} = 0 V at INx	-20			μA
Z_O	Output Impedance[2]			50		Ω
CMTI	Common-mode Transient Immunity	V_I = V_{DDI}[1] or 0 V, V_{CM} = 1200V; See Figure 8-3	100	150		kV/μs
C_I	Input Capacitance[3]	V_I = V_{DD}/ 2 + 0.4×sin(2πft), f = 1 MHz, V_{DD} = 5 V		2		pF

Notes:
1. V_{DDI} = Input-side supply V_{DD}, V_{DDO} = Output-side supply V_{DD}.
2. The nominal output impedance of each isolator driver is 50 Ω ± 40%.
3. Measured from pin to Ground.

V_{DDA} = V_{DDB} = 3.3 V ± 10%, T_A = -40 to 125°C (over recommended operating conditions, unless otherwise specified)

Parameters		Test conditions	MIN	TYPE	MAX	UNIT
V_{OH}	High-level Output Voltage	I_{OH} = -2mA; See Figure 8-2	V_{DDO}[1]-0.4	3.1		V
V_{OL}	Low-level Output Voltage	I_{OL} = 2mA; See Figure 8-2		0.2	0.4	V
$V_{IT+(IN)}$	Rising input switching threshold		2			V
$V_{IT-(IN)}$	Falling input switching threshold				0.8	V
I_{IH}	High-Level Input Leakage Current	V_{IH} = V_{DDA} at INx or ENx			20	μA
I_{IL}	Low-Level Input Leakage Current	V_{IL} = 0 V at INx	-20			μA
Z_O	Output Impedance[2]			50		Ω
CMTI	Common-mode Transient Immunity	V_I = V_{DDI}[1] or 0 V, V_{CM} = 1200V; See Figure 8-3	100	150		kV/μs
C_I	Input Capacitance[3]	V_I = V_{DD}/ 2 + 0.4×sin(2πft), f = 1 MHz, V_{DD} = 3.3 V		2		pF

Notes:
1. V_{DDI} = Input-side supply V_{DD}, V_{DDO} = Output-side supply V_{DD}.
2. The nominal output impedance of each isolator driver is 50 Ω ± 40%.
3. Measured from pin to Ground.

V_{DDA} = V_{DDB} = 2.5 V ± 10%, T_A = -40 to 125°C (over recommended operating conditions, unless otherwise specified)

Parameters		Test conditions	MIN	TYPE	MAX	UNIT
V_{OH}	High-level Output Voltage	I_{OH} = -1mA; See Figure 8-2	V_{DDO}[1]-0.4	2.3		V
V_{OL}	Low-level Output Voltage	I_{OL} = 1mA; See Figure 8-2		0.2	0.4	V
$V_{IT+(IN)}$	Rising input switching threshold		2			V
$V_{IT-(IN)}$	Falling input switching threshold				0.8	V
I_{IH}	High-Level Input Leakage Current	V_{IH} = V_{DDA} at INx or ENx			20	μA
I_{IL}	Low-Level Input Leakage Current	V_{IL} = 0 V at INx	-20			μA
Z_O	Output Impedance[2]			50		Ω
CMTI	Common-mode Transient Immunity	V_I = V_{DDI}[1] or 0 V, V_{CM} = 1200V; See Figure 8-3	100	150		kV/μs
C_I	Input Capacitance[3]	V_I = V_{DD}/ 2 + 0.4×sin(2πft), f = 1 MHz, V_{DD} = 2.5 V		2		pF

Notes:
1. V_{DDI} = Input-side supply V_{DD}, V_{DDO} = Output-side supply V_{DD}.
2. The nominal output impedance of each isolator driver is 50 Ω ± 40%.
3. Measured from pin to Ground.

7.9. Supply Current Characteristics

V_{DDA} = V_{DDB} = 5 V ± 10%, T_A = -40 to 125°C (over recommended operating conditions, unless otherwise specified).

Parameters	Test conditions		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
CA-IS3710							
Supply Current – DC Signal	V_{IN} = 0V (CA-IS3710LS); V_{IN} = V_{DDA} (CA-IS3710HS)		I_{DDA}		0.9	1.7	mA
			I_{DDB}		0.9	1.7	
	V_{IN} = V_{DDA} (CA-IS3710LS); V_{IN} = 0V(CA-IS3710HS)		I_{DDA}		1.7	2.6	
			I_{DDB}		0.9	1.7	
Supply Current – AC Signal	All Channels Switching with 50% Duty Cycle Square Wave Clock Input with 5V Amplitude; C_L = 15 pF for Each Channel.	1Mbps (500kHz)	I_{DDA}		1.4	2.1	
			I_{DDB}		1.5	2.2	
		10Mbps (5MHz)	I_{DDA}		1.4	2.1	
			I_{DDB}		4.4	6.6	
		100Mbps (50MHz)	I_{DDA}		1.4	2.1	
			I_{DDB}		11	16	
Note: 1. V_{DDI} = Input-side supply V_{DD}.							

V_{DDA} = V_{DDB} = 3.3 V ± 10%, T_A = -40 to 125°C (over recommended operating conditions, unless otherwise specified)

Parameters	Test conditions		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
CA-IS3710							
Supply Current – DC Signal	V_{IN} = 0V (CA-IS3710LS); V_{IN} = V_{DDA} (CA-IS3710HS)		I_{DDA}		0.9	1.7	mA
			I_{DDB}		0.9	1.7	
	V_{IN} = V_{DDA} (CA-IS3710LS); V_{IN} = 0V(CA-IS3710HS)		I_{DDA}		1.7	2.6	
			I_{DDB}		0.9	1.7	
Supply Current – AC Signal	All Channels Switching with 50% Duty Cycle Square Wave Clock Input with 3.3V Amplitude; C_L = 15 pF for Each Channel.	1Mbps (500kHz)	I_{DDA}		1.4	2.1	
			I_{DDB}		1.0	1.4	
		10Mbps (5MHz)	I_{DDA}		1.4	2.1	
			I_{DDB}		3.1	4.2	
		100Mbps (50MHz)	I_{DDA}		1.4	2.1	
			I_{DDB}		7.2	10	
Note: 1. V_{DDI} = Input-side supply V_{DD}.							

V_{DDA} = V_{DDB} = 2.5 V ± 10%, T_A = -40 to 125°C (over recommended operating conditions, unless otherwise specified)

Parameters	Test conditions		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
CA-IS3710							
Supply Current – DC Signal	V_{IN} = 0V (CA-IS3710LS); V_{IN} = V_{DDA} (CA-IS3710HS)		I_{DDA}		0.9	1.7	mA
			I_{DDB}		0.9	1.7	
	V_{IN} = V_{DDA} (CA-IS3710LS); V_{IN} = 0V(CA-IS3710HS)		I_{DDA}		1.7	2.6	
			I_{DDB}		0.9	1.7	
Supply Current – AC Signal	All Channels Switching with 50% Duty Cycle Square Wave Clock Input with 2.5V Amplitude; C_L = 15 pF for Each Channel.	1Mbps (500kHz)	I_{DDA}		1.4	2.1	
			I_{DDB}		1.0	1.5	
		10Mbps (5MHz)	I_{DDA}		1.4	2.1	
			I_{DDB}		2.5	3.6	
		100Mbps (50MHz)	I_{DDA}		1.4	2.1	
			I_{DDB}		6.0	9.0	
Note: 1. V_{DDI} = Input-side supply V_{DD}.							

7.10. Timing Characteristics

V_{DDA} = V_{DDB} = 5 V ± 10%, T_A = -40 to 125°C (over recommended operating conditions, unless otherwise specified)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DR	Data Rate		0		150	Mbps
PW_{min}	Minimum Pulse Width				5.0	ns
t_{PLH}, t_{PHL}	Propagation Delay Time	See Figure 8-1	5.0	12.0	15.0	ns
PWD	Pulse Width Distortion $\|t_{PLH} - t_{PHL}\|$			0.2	4.5	ns
$t_{sk(pp)}$	Part-to-Part Output Skew Time [1]			2.0	4.5	ns
t_r	Output Signal Rise Time	See Figure 8-1		2.5	4.0	ns
t_f	Output Signal Fall Time	See Figure 8-1		2.5	4.0	ns
t_{DO}	Default Output Delay Time from Input Power Loss	See Figure 8-2		8	12	ns
t_{SU}	Start-up Time			15	40	µs

Note:

1. tsk(pp) is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

V_{DDA} = V_{DDB} = 3.3 V ± 10%, T_A = -40 to 125°C (over recommended operating conditions, unless otherwise specified)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DR	Data Rate		0		150	Mbps
PW_{min}	Minimum Pulse Width				5.0	ns
t_{PLH}, t_{PHL}	Propagation Delay Time	See Figure 8-1	5.0	12.0	15.0	ns
PWD	Pulse Width Distortion $\|t_{PLH} - t_{PHL}\|$			0.2	4.5	ns
$t_{sk(pp)}$	Part-to-Part Output Skew Time [2]			2.0	4.5	ns
t_r	Output Signal Rise Time	See Figure 8-1		2.5	4.0	ns
t_f	Output Signal Fall Time	See Figure 8-1		2.5	4.0	ns
t_{DO}	Default Output Delay Time from Input Power Loss	See Figure 8-2		8	12	ns
t_{SU}	Start-up Time			15	40	µs

Note:

1. tsk(pp) is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

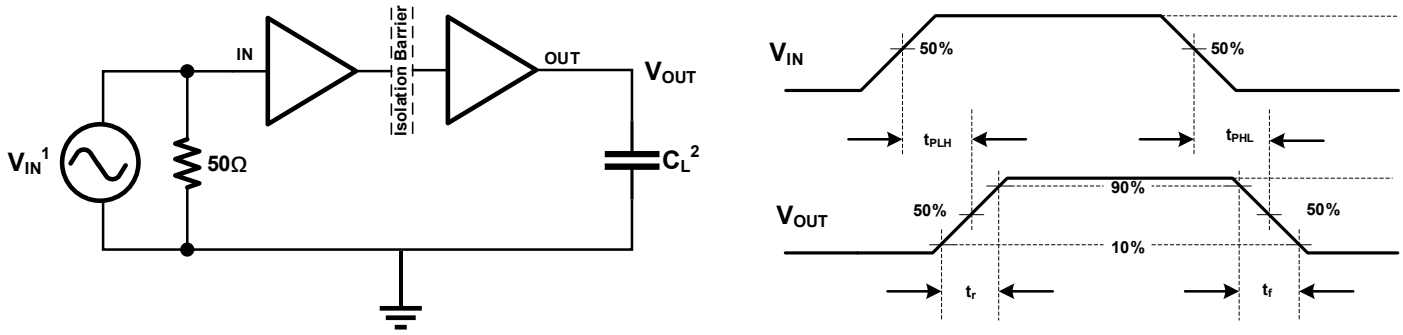
V_{DDA} = V_{DDB} = 2.5 V ± 10%, T_A = -40 to 125°C (over recommended operating conditions, unless otherwise specified)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DR	Data Rate		0		150	Mbps
PW_{min}	Minimum Pulse Width				5.0	ns
t_{PLH}, t_{PHL}	Propagation Delay Time	See Figure 8-1	5.0	12.0	15.0	ns
PWD	Pulse Width Distortion $\|t_{PLH} - t_{PHL}\|$			0.2	5.0	ns
$t_{sk(pp)}$	Part-to Part Output Skew Time [2]			2.0	5.0	ns
t_r	Output Signal Rise Time	See Figure 8-1		2.5	4.0	ns
t_f	Output Signal Fall Time	See Figure 8-1		2.5	4.0	ns
t_{DO}	Default Output Delay Time from Input Power Loss	See Figure 8-2		8	12	ns
t_{SU}	Start-up Time			15	40	µs

Note:

1. tsk(pp) is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

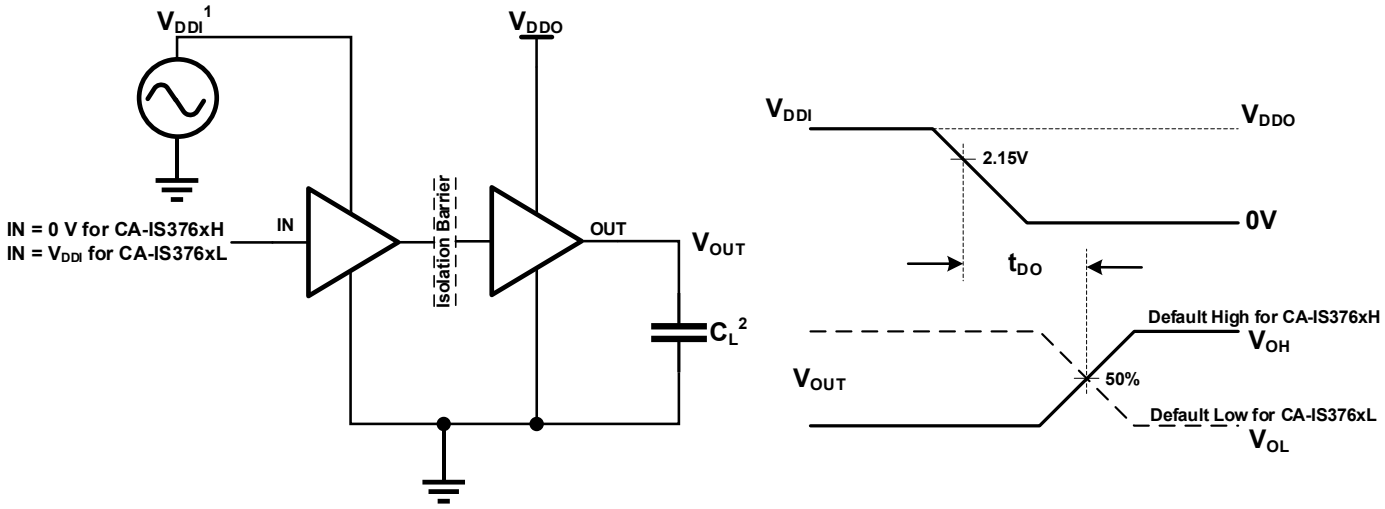
8. Parameter Measurement Information



Notes:

1. A square wave generator provide V_{IN} input signal with the following characteristics: frequency ≤100kHz, 50% duty cycle, t_r≤3ns, t_f≤3ns, Z_{out} = 50Ω. At the input, 50 Ω resistor is required to terminate input generator signal. It is not needed in actual application.
2. C_L = 15pF and includes external circuit (instrumentation and fixture etc.) capacitance. Since the load capacitance influence the output rising time, it's a key factor in the timing characteristic measurement.

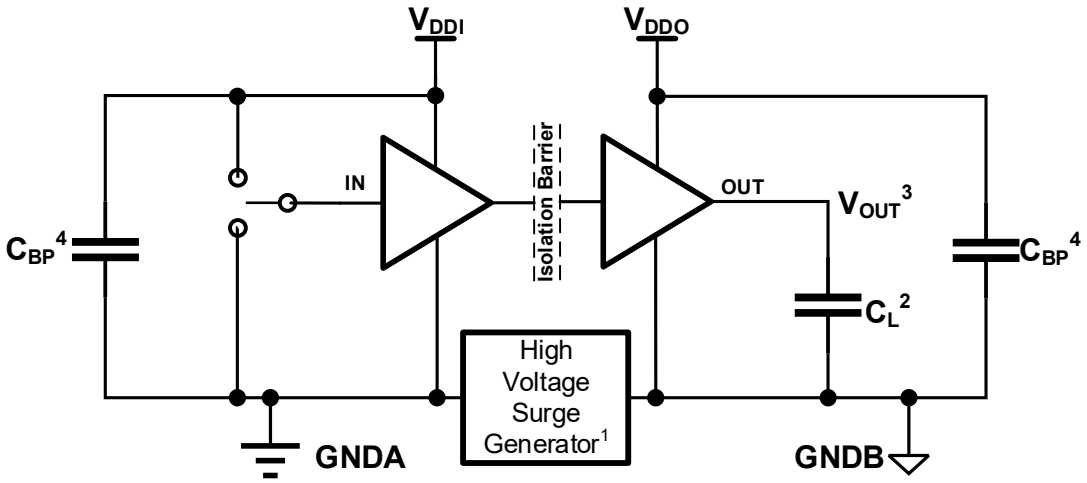
Figure 8-1. Switching Characteristics Test Circuit and Voltage Waveforms



Notes:

1. Power Supply Ramp Rate = 10 mV/ns. V_{DDI} should ramp over 2.375V, and less than 5.5V.
2. C_L = 15pF and includes external circuit (instrumentation and fixture etc.) capacitance. Since the load capacitance influence the output rising time, it's a key factor in the timing characteristic measurement.

Figure 8-2. Default Output Delay Time Test Circuit and Voltage Waveforms



Notes:

1. The High Voltage Surge Generator generates repetitive high voltage surges with > 1kV amplitude, rise time <10ns and fall time <10ns, to reach common-mode transient noise with > 150kV/μs slew rate.
2. C_L = 15pF and includes external circuit (instrumentation and fixture etc.) capacitance.
3. Pass-fail criteria: the output must remain stable.
4. C_{BP} (0.1 ~ 1uF) is bypass capacitance.

Figure 8-3. Common-Mode Transient Immunity Test Circuit

9. Detailed Description

9.1. Overview

The CA-IS3710 is a family of single-channel digital galvanic isolators using Chipanalog's full differential capacitive isolation technology. These devices have an ON-OFF keying (OOK) modulation scheme to transfer digital signals across the SiO_2 based isolation barrier between circuits with different power domains. The transmitter sends a high frequency carrier across the barrier to represent one digital state and sends no signal to represent the other digital state. The receiver demodulates the signal and recovery input signal at output through a buffer stage. With this OOK architecture, CA-IS3710 family of devices builds a robust data transmission path between different power domains without any special start-up initialization requirements. These devices also incorporate advanced full differential techniques to minimize the radiated emissions due the high frequency carrier and IO buffer switching.

9.2. Functional Block Diagram

The conceptual block diagram of a digital capacitive isolator, Figure 9-1, shows a functional block diagram of a typical channel; Figure 9-2 shows the operating waveform of a typical channel. The isolation channel of CA-IS3710 is unidirectional, only passes data in one direction with guaranteed data rates from DC up to 150Mbps as indicated in the functional diagram.

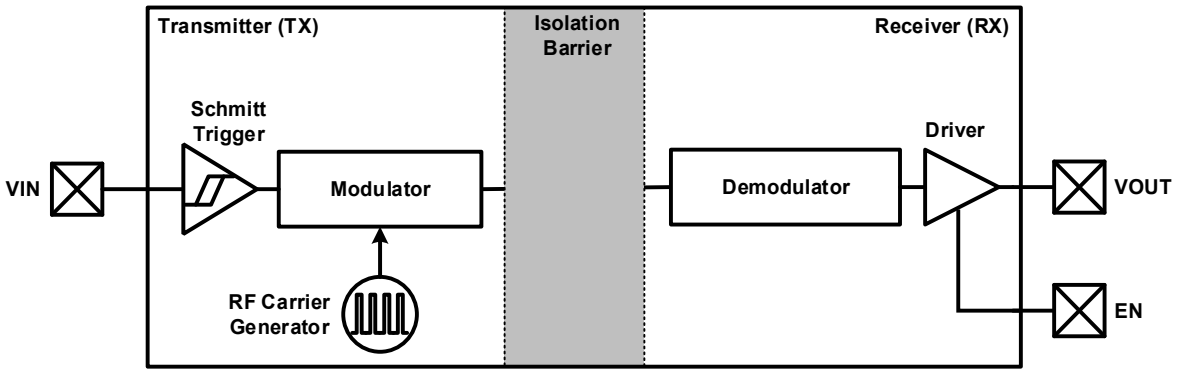


Figure 9-1. Functional Block Diagram of CA-IS3710

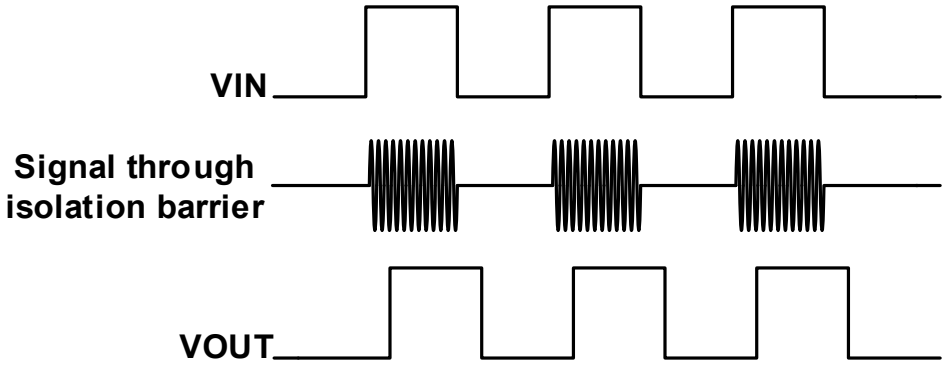


Figure 9-2. Conceptual Operation Waveforms of CA-IS3710's Single Channel

9.3. Device Operation Modes

Table 9-1 lists the operation modes for the CA-IS3710 devices.

Table 9-1. Operation Mode

V_{DDI}[1]	V_{DDO}[1]	INPUT (VIx)[2]	OUTPUT (VOx)	OPERATION
PU	PU	H	H	Normal operation mode: Each channel output follows the logic state of its input.
		L	L	
		Open	Default	Default output mode: When input VIx is open, the corresponding channel output goes to its default logic state. Default is *High* for CA-IS3710HS and Low for CA-IS3710LS.
PD	PU	X	Default	Default output mode: When V_{DDI} is unpowered, a channel output assumes the logic state based on its default option. Default is *High* for CA-IS3710HS and Low for CA-IS3710LS.
X	PD	X	Undetermined	If the output side V_{DDO} is unpowered, a channel output is undetermined.[4]

Notes:

1. V_{DDI} = Input-side supply V_{DD}; V_{DDO} = Output-side supply V_{DD}; PU = Powered up ($V_{DD} \geq V_{DD(UVLO+)}$); PD = Powered down ($V_{DD} \leq V_{DD(UVLO\_)}$); X = Irrelevant; H = High level; L = Low level; Z = High Impedance.
2. A strongly driven input signal can weakly power the floating V_{DD} through an internal protection diode and cause undetermined output.
3. The output is in undetermined state when $V_{DD(UVLO+)} < V_{DDI}$, $V_{DDO} < V_{DD(UVLO-)}$.

10. Application and Implementation

The CA-IS3710 isolation ICs provide complete galvanic isolation between two power domains, protecting circuits from high common-mode transients and faults, eliminating ground loops. In many applications, digital isolators are replacing optocouplers because they can reduce the power requirements and take up less board space while offering the same isolation capability. The CA-IS3710 devices are the high-performance, single-channel digital isolator. Unlike optocouplers, which require external components to improve performance, provide bias, or limit current, the CA-IS3710 devices only require two external bypass capacitors to operate. To reduce ripple and the chance of introducing data errors, bypass V_{DDA} and V_{DDB} pins with 0.1µF to 1µF low-ESR ceramic capacitors to GNDA and GNDB respectively. Place the bypass capacitors as close to the power supply input pins as possible. Figure 10-1 shows typical operating circuit of CA-IS3710; Figure 10-2 is the typical applications for CA-IS37xx series products.

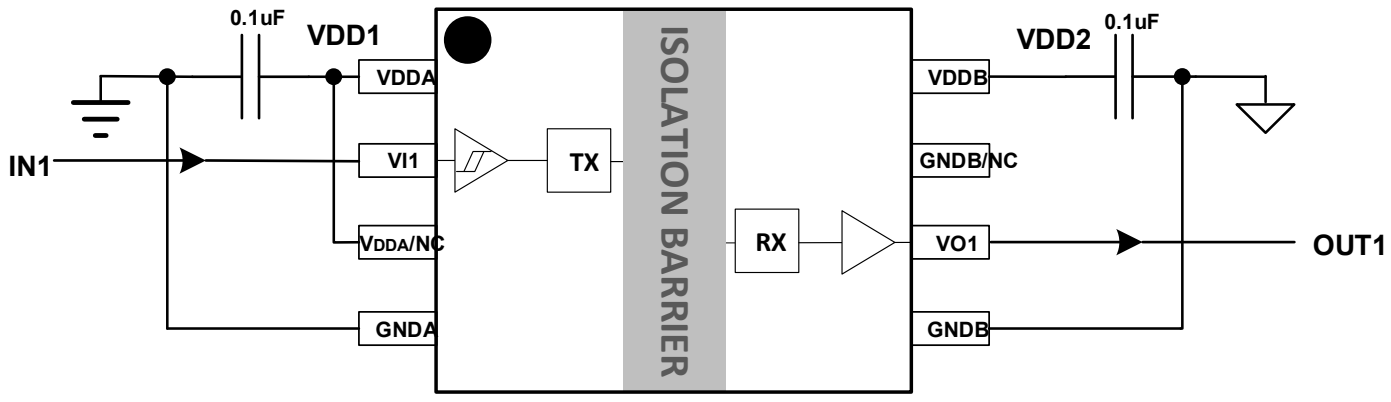


Figure 10-1. Typical Application Circuit of CA-IS3710

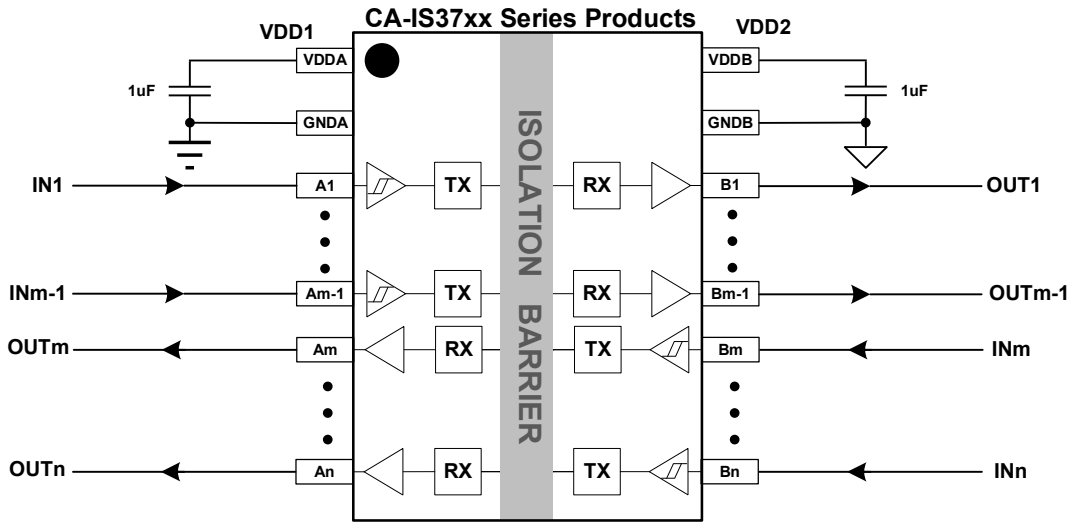
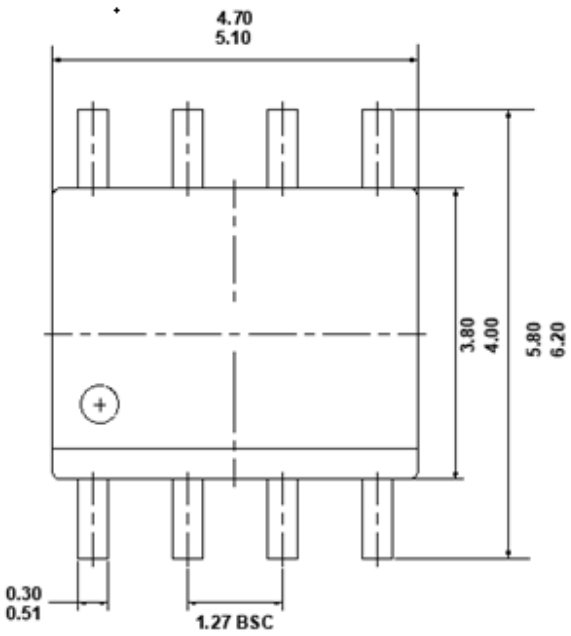


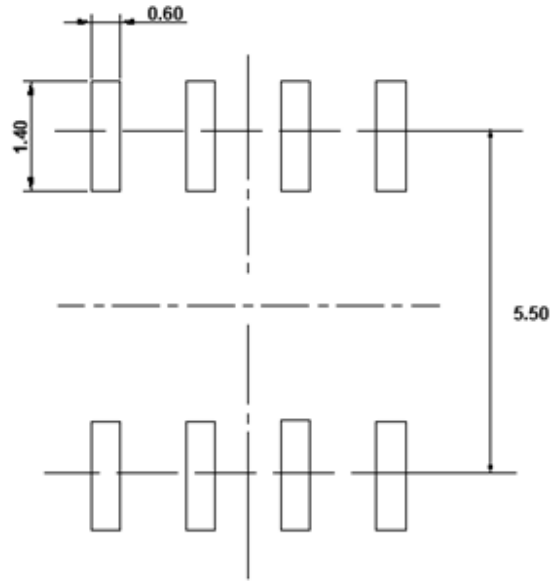
Figure 10-2. Typical Applications for the CA-IS37xx Series Digital Isolators

11. Package Information

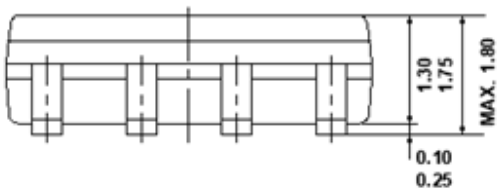
8-Pin Narrow Body SOIC Package Outline



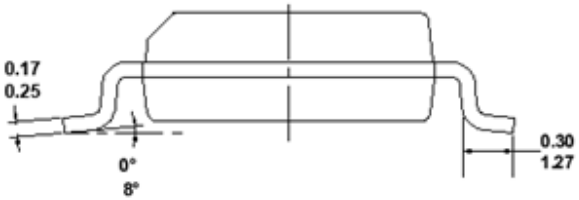
TOP VIEW



RECOMMENDED LAND PATTERN



FRONT VIEW



LEFT SIDE VIEW

Note:

1. All dimensions are in millimeters, angles are in degrees.

12. Soldering Temperature (reflow) Profile

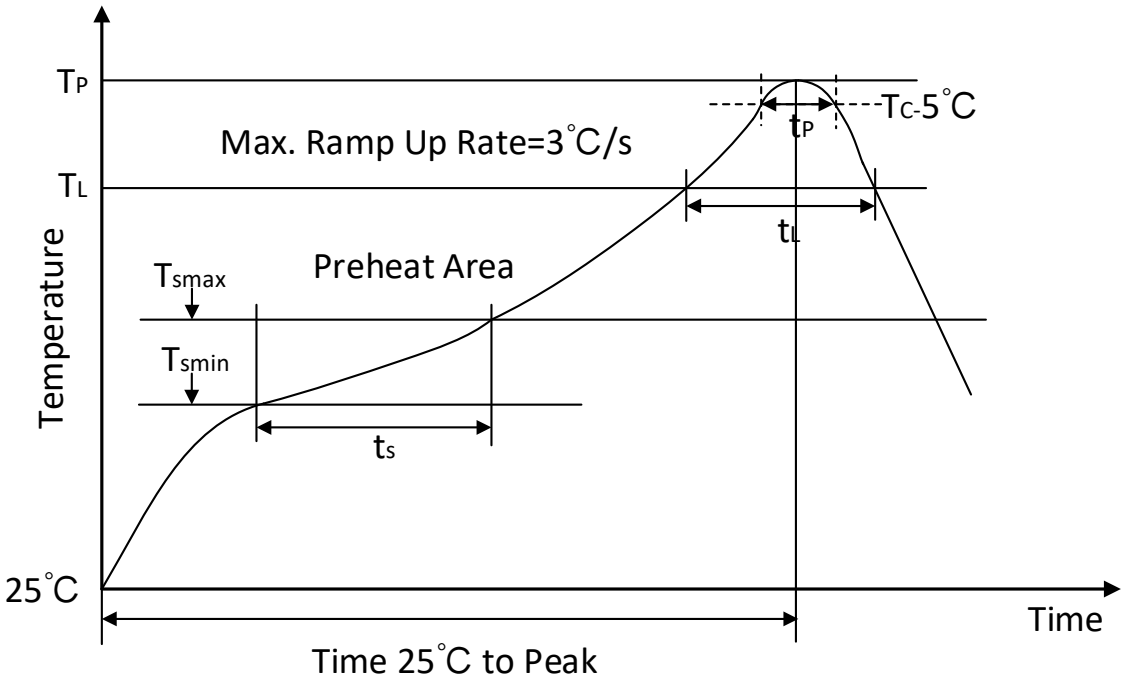


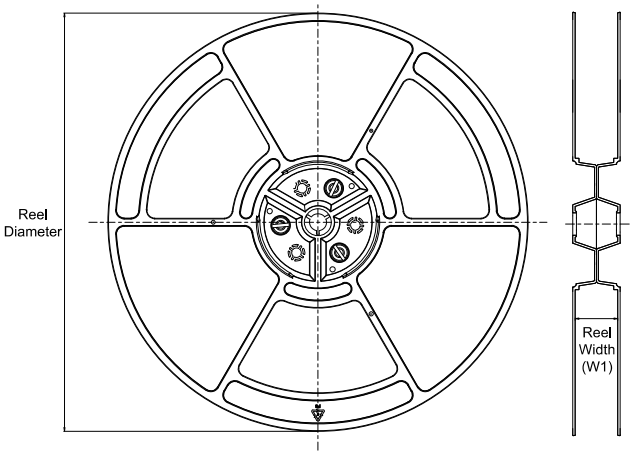
Figure. 12-1 Soldering Temperature (reflow) Profile

Table 12-1 Soldering Temperature Parameter

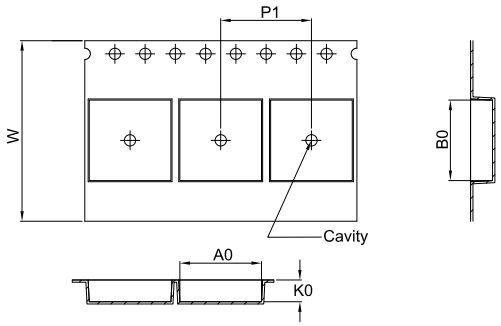
Profile Feature	**Pb-Free Assembly**
Average ramp-up rate(217 ℃ to Peak)	3℃ /second max
Time of Preheat temp(from 150 ℃ to 200 ℃	60-120 second
Time to be maintained above 217 ℃	60-150 second
Peak temperature	260 ℃
Time within 5 ℃ of actual peak temp	30 second
Ramp-down rate	6 ℃ /second max.
Time from 25℃ to peak temp	8 minutes max

13. Tape and Reel Information

REEL DIMENSIONS

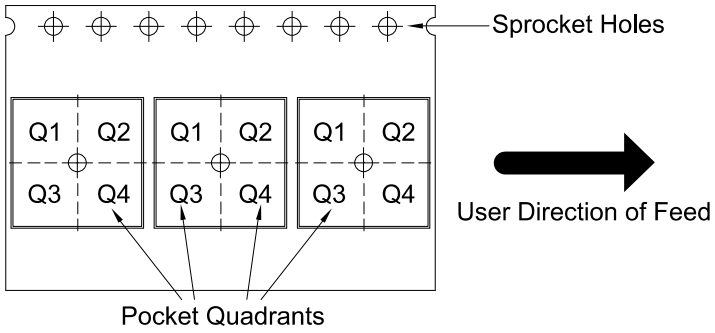


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CA-IS3710LS-Q1	SOIC	S	8	2500	330	12.4	6.4	5.4	2.1	8.0	12.0	Q1
CA-IS3710HS-Q1	SOIC	S	8	2500	330	12.4	6.4	5.4	2.1	8.0	12.0	Q1

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