CA-IS386x High-Speed Six-Channel Digital Isolators

1. Features

- **Robust Galvanic Isolation of Digital Signals**
  - High lifetime: >40 years
  - Up to 5700 V_{RMS} isolation rating (wide body packages)
  - ±150 kV/μs typical CMTI
  - Wide operating temperature range: -40°C to 125°C
  - Schmitt trigger inputs
- **Interfaces Directly with Most MCUs and FPGAs**
  - Data rate: DC to 150Mbps
  - Accepts 2.5V to 5.5V supplies
  - Default output *High* (CA-IS386xH) and *Low* (CA-IS386xL) Options
- **Low Power Consumption**
  - 1.5mA per channel at 1Mbps with VDD = 5.0V
  - 6.6mA per channel at 100Mbps with VDD = 5.0V
- **Best in class propagation delay and skew**
  - 12ns typical propagation delay
  - 1ns pulse width distortion
  - 2ns propagation delay skew (chip -to-chip)
  - 5ns minimum pulse width
- Isolation Rating up to 5.7kVrms
- ESD：±8kV HBM
- **Package Options**
  - Wide-body SOIC16-WB(W) package
- **Safety Regulatory Approvals**
  - VDE 0884-17 isolation certification
  - UL According to UL1577
  - TUV, EN 61010-1:2010+A1 certifications

2. Applications

- Solar Inverter
- Wind-Generated Electricity
- High Voltage Power Storage
- High Voltage Grid System
- EV Charging Station
- Medical Electronics

3. General Description

The CA-IS386x devices are high-performance six-channel, unidirectional digital isolators with up to 5.7kV_{RMS} (wide-body package) isolation rating and ultra-fast data rate. The CA-IS386x devices offer high electromagnetic immunity and low emissions at low power consumption while isolating different ground domains and block high-voltage/high-current transients from sensitive or human interface circuitry. Each isolation channel has a logic input and output buffer separated by capacitive silicon dioxide (SiO2) insulation barrier, the integrated Schmitt trigger on each input provide excellent noise immunity.

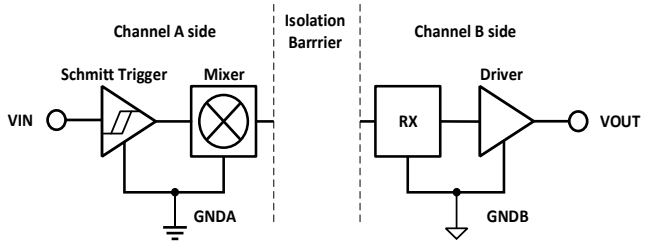
The CA-IS386x family offers all possible unidirectional channel configurations to accommodate any 6-channel design digital I/O applications, especial for the multiple SPI devices isolation. The CA-IS3860 features six channels transferring digital signals in one direction; The CA-IS3861 device has five forward and one reverse-direction channels; The CA-IS3862 device offers four forward and two reverse-direction channels isolation; The CA-IS3863 provides further design flexibility with three channels in each direction. All devices of this family features default outputs. When the input is either not powered or is open-circuit, the default output is low for devices with suffix L and high for devices with suffix H, see the *Ordering Information* for suffixes associated with each option.

The CA-IS386x series devices are specified over the -40°C to +125°C operating temperature range and are available in 16-pin SOIC wide body package.

Device information

Part number	Package	Package size (NOM)
CA-IS3860 CA-IS3861 CA-IS3862 CA-IS3863	SOIC16-WB(W)	10.30 mm × 7.50 mm

Simplified Channel Structure



GNDA and GNDB are the isolated grounds for A side and B side respectively.

4. Ordering Information

Table 4-1. Ordering Information

Part Number	Number of Inputs A Side	Number of Inputs B Side	Default Output	Isolation Rating (kV_{RMS})	Output Enable	Package
CA-IS3860LW	6	0	Low	5.7	No	SOIC16-WB
CA-IS3860HW	6	0	High	5.7	No	SOIC16-WB
CA-IS3861LW	5	1	Low	5.7	No	SOIC16-WB
CA-IS3861HW	5	1	High	5.7	No	SOIC16-WB
CA-IS3862LW	4	2	Low	5.7	No	SOIC16-WB
CA-IS3862HW	4	2	High	5.7	No	SOIC16-WB
CA-IS3863LW	3	3	Low	5.7	No	SOIC16-WB
CA-IS3863HW	3	3	High	5.7	No	SOIC16-WB

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5. Revision History

Revision Number	Description	Page Changed
Version 1.00	N/A	N/A
Version 1.01	Updated UL certification information	8
Version 1.02	Updated UL, TUV certification information	8
Version 1.03	Updated VDE certification information	8
Version 1.04	Updated insulation specifications	7
Version 1.05	Updated TUV and UL certification information	8

6. Pin Configuration and Description

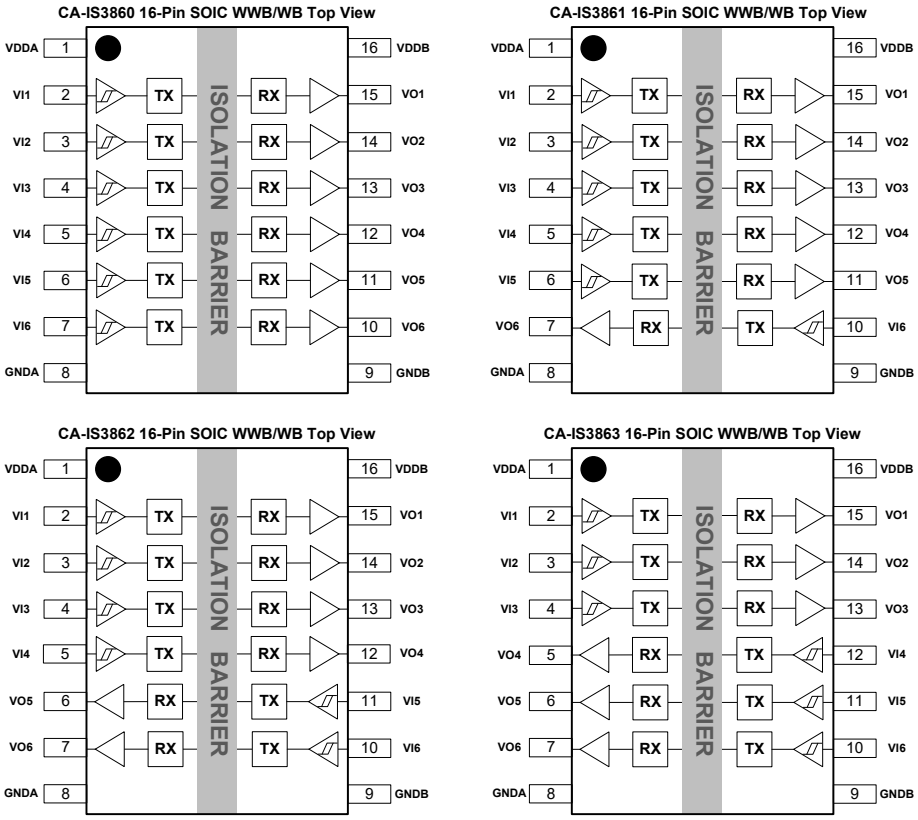


Figure 6-1. CA-IS386x pin configuration

Table 6-1. CA-IS386x pin description

16-SOIC Pin#				Name	Type	Description
CA-IS3860	CA-IS3861	CA-IS3862	CA-IS3863			
1	1	1	1	VDDA	Supply	Power supply for side A.
2	2	2	2	VI1	Digital I/O	Digital input 1 on side A, corresponds to logic output 1 on side B.
3	3	3	3	VI2	Digital I/O	Digital input 2 on side A, corresponds to logic output 2 on side B.
4	4	4	4	VI3	Digital I/O	Digital input 3 on side A, corresponds to logic output 3 on side B.
5	5	5	12	VI4	Digital I/O	Digital input 4 on side A/B, corresponds to logic output 4 on side B/A.
6	6	11	11	VI5	Digital I/O	Digital input 5 on side A/B, corresponds to logic output 5 on side B/A.
7	10	10	10	VI6	Digital I/O	Digital input 6 on side A/B, corresponds to logic output 6 on side B/A.
8	8	8	8	GNDA	Ground	Ground reference for side A.
9	9	9	9	GNDB	Ground	Ground reference for side B.
10	7	7	7	VO6	Digital I/O	Digital output 6 on side B/A, VO6 is the logic output for the VI6 input on side A/B.
11	11	6	6	VO5	Digital I/O	Digital output 5 on side B/A, VO5 is the logic output for the VI5 input on side A/B.
12	12	12	5	VO4	Digital I/O	Digital output 4 on side B/A, VO4 is the logic output for the VI4 input on side A/B.
13	13	13	13	VO3	Digital I/O	Digital output 3 on side B, VO3 is the logic output for the VI3 input on side A.
14	14	14	14	VO2	Digital I/O	Digital output 2 on side B, VO2 is the logic output for the VI2 input on side A.
15	15	15	15	VO1	Digital I/O	Digital output 1 on side B, VO1 is the logic output for the VI1 input on side A.
16	16	16	16	VDDB	Supply	Power supply for side B.

7. Specifications

7.1. Absolute Maximum Ratings[1]

Parameters		Minimum value	Maximum value	Unit
V_{DDA}, V_{DDB}	Power supply voltage [2]	-0.5	7.0	V
V_{IN}	Voltage at VI_X, VO_X, EN_X	-0.5	$V_{DD\_}$ + 0.5[3]	V
I_O	Output current	-20	20	mA
T_J	Junction temperature		150	°C
T_{STG}	Storage temperature range	-65	150	°C

Notes:
1. The stresses listed under "Absolute Maximum Ratings" are stress ratings only, not for functional operation condition. Exposure to absolute maximum rating conditions for extended periods may cause permanent damage to the device.
2. All voltage values except differential I/O bus voltages are with respect to the local ground terminal (GNDA or GNDB) and are peak voltage values.
3. Maximum voltage must not be exceed 7 V.

7.2. ESD Ratings

		Numerical value	Unit
V_{ESD} Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, to the Pins on the same side[1]	±8000	V
	Charged device model (CDM), per JEDEC Specification JESD22-C101, all pins[2]	±2000	V

Notes:
1. Per JEDEC document JEP155, 500V HBM allows safe manufacturing of standard ESD control process.
2. Per JEDEC document JEP157, 250V HBM allows safe manufacturing of standard ESD control process.

7.3. Recommended Operating Conditions

	PARAMETER		MIN	TYP	MAX	UNIT
V_{DDA}, V_{DDB}	Supply voltage on side A, B		2.375		5.50	V
$V_{DD(UVLO+)}$	V_{DD} Under-voltage-Lockout Threshold When Supply Voltage is Rising		1.95	2.24	2.375	V
$V_{DD(UVLO-)}$	V_{DD} Under-voltage-Lockout Threshold When Supply Voltage is Falling		1.88	2.10	2.325	V
$V_{HYS(UVLO)}$	V_{DD} Under-voltage-Lockout Threshold Hysteresis		70	140	250	mV
I_{OH}	High-level Output Current	V_{DDO}[1] = 5V	-4			mA
		V_{DDO} = 3.3V	-2			
		V_{DDO} = 2.5V	-1			
I_{OL}	Low-level Output Current	V_{DDO} = 5V			4	mA
		V_{DDO} = 3.3V			2	
		V_{DDO} = 2.5V			1	
V_{IH}	High-level Input Voltage		2.0			V
V_{IL}	Low-level Input Voltage				0.8	V
DR	Data Rate		0		150	Mbps
T_A	Ambient Temperature		-40	27	125	°C

Note:
1. V_{DDO} = Output-side supply V_{DD}.

7.4. Thermal Information

Thermal Metric		CA-IS386x SOIC16-WB(W)	Unit
$R_{\theta JA}$	Junction-to-ambient thermal resistance	83.4	°C/W

7.5. Power Rating

Parameters		Test conditions	MIN	TYP	MAX	Unit
CA-IS3860						
P_D	Maximum Power Dissipation	V_{DDA} = V_{DDB} = 5.5 V, C_L = 15 pF, T_J = 150°C, Input a 75-MHz 50% duty cycle square wave.			494	mW
P_{DA}	Maximum Power Dissipation on Side-A				49	mW
P_{DB}	Maximum Power Dissipation on Side-B				445	mW
CA-IS3861						
P_D	Maximum Power Dissipation	V_{DDA} = V_{DDB} = 5.5 V, C_L = 15 pF, T_J = 150°C, Input a 75-MHz 50% duty cycle square wave.			494	mW
P_{DA}	Maximum Power Dissipation on Side-A				113	mW
P_{DB}	Maximum Power Dissipation on Side-B				381	mW
CA-IS3862						
P_D	Maximum Power Dissipation	V_{DDA} = V_{DDB} = 5.5 V, C_L = 15 pF, T_J = 150°C, Input a 75-MHz 50% duty cycle square wave.			494	mW
P_{DA}	Maximum Power Dissipation on Side-A				180	mW
P_{DB}	Maximum Power Dissipation on Side-B				314	mW
CA-IS3863						
P_D	Maximum Power Dissipation	V_{DDA} = V_{DDB} = 5.5 V, C_L = 15 pF, T_J = 150°C, Input a 75-MHz 50% duty cycle square wave.			494	mW
P_{DA}	Maximum Power Dissipation on Side-A				247	mW
P_{DB}	Maximum Power Dissipation on Side-B				247	mW

7.6. Insulation Specifications

Parameters		Test conditions	Value W	Unit
CLR	External Clearance[1]	Shortest terminal-to-terminal distance through air	>8	mm
CPG	External Creepage[1]	Shortest terminal-to-terminal distance across the package surface	>8	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	28	µm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11)；IEC 60112	>600	V
	Material group	Per IEC 60664-1	I	
Overvoltage category per IEC 60664-1		Rated mains voltage ≤ 300 V_{RMS}	I-IV	
		Rated mains voltage ≤ 600 V_{RMS}	I-IV	
		Rated mains voltage ≤ 1000 V_{RMS}	I-III	
DIN V VDE V 0884-17:2021-10[2]				
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	2121	V_{PK}
V_{IOWM}	Maximum operating isolation voltage	AC voltage; time-dependent dielectric breakdown (TDDB) test	1500	V_{RMS}
		DC voltage	2121	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t=60 s (certified); $V_{TEST} = 1.2 \times V_{IOTM}$, t=1 s (100% product test)	8000	V_{PK}
V_{IOSM}	Maximum surge isolation voltage[3]	Test method per IEC 62368-1, 1.2/50 µs waveform, $V_{TEST} = 1.6 \times V_{IOSM}$ (certified)	8000	V_{PK}
q_{pd}	Apparent charge[4]	Method a, after input/output safety test of the subgroup 2/3, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)} = 1.2 \times V_{IORM}$, t_m = 10 s	≤5	pC
		Method a, after environmental test of the subgroup 1, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)} = 1.6 \times V_{IORM}$, t_m = 10 s	≤5	
		Method b, at routine test (100% production test) and preconditioning (type test) $V_{ini} = 1.2 \times V_{IOTM}$, t_{ini} = 1 s; $V_{pd(m)} = 1.875 \times V_{IORM}$, t_m = 1 s	≤5	
C_{IO}	Barrier capacitance, input to output[5]	V_{IO} = 0.4 × sin (2πft), f = 1 MHz	~0.5	pF
R_{IO}	Isolation resistance[5]	V_{IO} = 500 V, T_A = 25°C	$>10^{12}$	Ω
		V_{IO} = 500 V, 100°C ≤ T_A ≤ 125°C	$>10^{11}$	
		V_{IO} = 500 V at T_S = 150°C	$>10^{9}$	
	Pollution degree		2	
UL 1577				
V_{ISO}	Maximum withstanding isolation voltage	$V_{TEST} = V_{ISO}$, t = 60 s (qualification) $V_{TEST} = 1.2 \times V_{ISO}$, t = 1 s (100% production test)	5700	V_{RMS}

NOTE:

1. Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications.
2. This coupler is suitable for safe electrical insulation only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
3. Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
4. Apparent charge is electrical discharge caused by a partial discharge (pd).
5. All pins on each side of the barrier tied together creating a two-terminal device.

7.7. Safety-Related Certifications

VDE	UL	CQC	TUV
Certified according to DIN EN IEC 60747-17 (VDE 0884-17):2021-10; EN IEC 60747-17:2020+AC:2021	Recognized under UL 1577 Component Recognition Program	Certified according to GB 4943.1-2022	Recognized under EN 61010-1:2010+A1
Maximum transient isolation voltage：8000V_{pk}(SOIC16-WB) Maximum repetitive peak isolation voltage： 2121V_{pk}(SOIC16-WB) Maximum surge isolation voltage： 8000V_{pk}(SOIC16-WB)	Single Protection： SOIC16-WB: 5700V_{RMS}；	SOIC16-WWB: Reinforced insulation SOIC16-WB: Reinforced insulation （Altitude ≤ 5000 m）	SOIC16-WB: 5000V_{RMS}；
Certification Number：40057278	Certification Number：E511334	Certificate number: CQC23001406424	Certification Number： AK 505918190001

7.8. Electrical Characteristics

V_{DDA} = V_{DDB} = 5 V ± 10%, T_A = -40 to 125°C (over recommended operating conditions, unless otherwise specified)

Parameters		Test conditions	MIN	TYP	MAX	UNIT
V_{OH}	High-level Output Voltage	I_{OH} = -4mA; See Figure 8- 1	V_{DDO}[1]-0.4	4.8		V
V_{OL}	Low-level Output Voltage	I_{OL} = 4mA; See Figure 8- 1		0.2	0.4	V
$V_{IT+(IN)}$	Positive-going Input Logic High		2			V
$V_{IT-(IN)}$	Negative-going Input Logic Low				0.8	V
$V_{IT+(EN)}$	EN Pin input Logic High		0.7*V_{DD}			V
$V_{IT-(EN)}$	EN Pin input Logic Low				0.3*V_{DD}	V
I_{IH}	High-Level Input Leakage Current	V_{IH} = V_{DDA} at INx or ENx			20	μA
I_{IL}	Low-Level Input Leakage Current	V_{IL} = 0 V at INx	-20			μA
Z_O	Output Impedance[2]			50		Ω
CMTI	Common-mode Transient Immunity	V_I = V_{DDI}[1] or 0 V, V_{CM} = 1200V; See Figure 8- 3	100	150		kV/μs
C_I	Input Capacitance[3]	V_I = V_{DD}/ 2 + 0.4×sin(2πft), f = 1 MHz, V_{DD} = 5 V		2		pF

Notes:
1. V_{DDI} = Input-side supply V_{DD}, V_{DDO} = Output-side supply V_{DD}.
2. The nominal output impedance of each isolator driver is 50 Ω ± 40%.
3. Measured from pin to Ground.

V_{DDA} = V_{DDB} = 3.3 V ± 10%, T_A = -40 to 125°C (over recommended operating conditions, unless otherwise specified)

Parameters		Test conditions	MIN	TYP	MAX	UNIT
V_{OH}	High-level Output Voltage	I_{OH} = -2mA; See Figure 8- 1	V_{DDO}[1]-0.4	3.1		V
V_{OL}	Low-level Output Voltage	I_{OL} = 2mA; See Figure 8- 1		0.2	0.4	V
$V_{IT+(IN)}$	Positive-going Input Logic High		2			V
$V_{IT-(IN)}$	Negative-going Input Logic Low				0.8	V
$V_{IT+(EN)}$	EN Pin input Logic High		0.7*V_{DD}			V
$V_{IT-(EN)}$	EN Pin input Logic Low				0.3*V_{DD}	V
I_{IH}	High-Level Input Leakage Current	V_{IH} = V_{DDA} at INx or ENx			20	μA
I_{IL}	Low-Level Input Leakage Current	V_{IL} = 0 V at INx	-20			μA
Z_O	Output Impedance[2]			50		Ω
CMTI	Common-mode Transient Immunity	V_I = V_{DDI}[1] or 0 V, V_{CM} = 1200V; See Figure 8- 3	100	150		kV/μs
C_I	Input Capacitance[3]	V_I = V_{DD}/ 2 + 0.4×sin(2πft), f = 1 MHz, V_{DD} = 3.3 V		2		pF

Notes:
1. V_{DDI} = Input-side supply V_{DD}, V_{DDO} = Output-side supply V_{DD}.
2. The nominal output impedance of each isolator driver is 50 Ω ± 40%.
3. Measured from pin to Ground.

V_{DDA} = V_{DDB} = 2.5 V ± 10%, T_A = -40 to 125°C (over recommended operating conditions, unless otherwise specified)

Parameters		Test conditions	MIN	TYP	MAX	UNIT
V_{OH}	High-level Output Voltage	I_{OH} = -1mA; See Figure 8- 1	V_{DDO}[1]-0.4	2.3		V
V_{OL}	Low-level Output Voltage	I_{OL} = 1mA; See Figure 8- 1		0.2	0.4	V
$V_{IT+(IN)}$	Positive-going Input Logic High		2			V
$V_{IT-(IN)}$	Negative-going Input Logic Low				0.8	V
$V_{IT+(EN)}$	EN Pin input Logic High		0.7*V_{DD}			V
$V_{IT-(EN)}$	EN Pin input Logic Low				0.3*V_{DD}	V
I_{IH}	High-Level Input Leakage Current	V_{IH} = V_{DDA} at INx or ENx			20	μA
I_{IL}	Low-Level Input Leakage Current	V_{IL} = 0 V at INx	-20			μA
Z_O	Output Impedance[2]			50		Ω
CMTI	Common-mode Transient Immunity	V_I = V_{DDI}[1] or 0 V, V_{CM} = 1200V; See Figure 8- 3	100	150		kV/μs
C_I	Input Capacitance[3]	V_I = V_{DD}/ 2 + 0.4×sin(2πft), f = 1 MHz, V_{DD} = 2.5 V		2		pF

Notes:
1. V_{DDI} = Input-side supply V_{DD}, V_{DDO} = Output-side supply V_{DD}.
2. The nominal output impedance of each isolator driver is 50 Ω ± 40%.

3. Measured from pin to Ground.

7.9. Supply Current Characteristics

V_{DDA} = V_{DDB} = 5 V ± 10%, T_A = -40 to 125°C (over recommended operating conditions, unless otherwise specified).

Parameters	Test conditions		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
CA-IS3860							
Supply Current – DC Signal	V_{IN} = 0V (CA-IS3860L); V_{IN} = V_{DDA} (CA-IS3860H)		I_{DDA}		2.0	2.9	mA
			I_{DDB}		3.9	5.7	
	V_{IN} = V_{DDA} (CA-IS3860L); V_{IN} = 0V(CA-IS3860H)		I_{DDA}		7.0	10.7	
			I_{DDB}		4.1	6.1	
Supply Current – AC Signal	All Channels Switching with 50% Duty Cycle Square Wave Clock Input with 5V Amplitude; C_L = 15 pF for Each Channel.	1Mbps (500kHz)	I_{DDA}		4.5	6.8	
			I_{DDB}		6.3	9.3	
		10Mbps (5MHz)	I_{DDA}		4.8	7.2	
			I_{DDB}		26.9	40.6	
		100Mbps (50MHz)	I_{DDA}		6.4	9.5	
			I_{DDB}		59.0	80	
CA-IS3861							
Supply Current – DC Signal	V_{IN} = 0V (CA-IS3861L); V_{IN} = V_{DDI}[1] (CA-IS3861H)		I_{DDA}		2.3	3.4	mA
			I_{DDB}		3.6	5.3	
	V_{IN} = V_{DDI}[1] (CA-IS3861L); V_{IN} = 0V(CA-IS3861H)		I_{DDA}		6.5	9.9	
			I_{DDB}		4.6	6.9	
Supply Current – AC Signal	All Channels Switching with 50% Duty Cycle Square Wave Clock Input with 5V Amplitude; C_L = 15 pF for Each Channel.	1Mbps (500kHz)	I_{DDA}		4.5	6.7	
			I_{DDB}		5.7	8.4	
		10Mbps (5MHz)	I_{DDA}		5.1	7.6	
			I_{DDB}		19.8	29.9	
		100Mbps (50MHz)	I_{DDA}		10.6	16.3	
			I_{DDB}		45.6	62.1	
CA-IS3862							
Supply Current – DC Signal	V_{IN} = 0V (CA-IS3862L); V_{IN} = V_{DDI}[1] (CA-IS3862H)		I_{DDA}		2.8	4.5	mA
			I_{DDB}		3.8	5.8	
	V_{IN} = V_{DDI}[1] (CA-IS3862L); V_{IN} = 0V(CA-IS3862H)		I_{DDA}		6.2	9.9	
			I_{DDB}		5.6	8.7	
Supply Current – AC Signal	All Channels Switching with 50% Duty Cycle Square Wave Clock Input with 5V Amplitude; C_L = 15 pF for Each Channel.	1Mbps (500kHz)	I_{DDA}		5.4	8.3	
			I_{DDB}		6.3	9.5	
		10Mbps (5MHz)	I_{DDA}		13.1	18.3	
			I_{DDB}		21.0	31.5	
		100Mbps (50MHz)	I_{DDA}		26.0	36.9	
			I_{DDB}		44.7	72.2	
CA-IS3863							
Supply Current – DC Signal	V_{IN} = 0V (CA-IS3863L); V_{IN} = V_{DDI}[1] (CA-IS3863H)		I_{DDA}		2.9	4.4	mA
			I_{DDB}		2.9	4.4	
	V_{IN} = V_{DDI}[1] (CA-IS3863L); V_{IN} = 0V(CA-IS3863H)		I_{DDA}		5.5	8.4	
			I_{DDB}		5.5	8.4	
Supply Current – AC Signal	All Channels Switching with 50% Duty Cycle Square Wave Clock Input with 5V Amplitude; C_L = 15 pF for Each Channel.	1Mbps (500kHz)	I_{DDA}		4.3	6.5	
			I_{DDB}		4.3	6.5	
		10Mbps (5MHz)	I_{DDA}		5.7	8.4	
			I_{DDB}		5.7	8.4	
		100Mbps (50MHz)	I_{DDA}		19.9	30.0	
			I_{DDB}		19.9	30.0	

Note:

1. V_{DDI} = Input-side supply V_{DD}.

V_{DDA} = V_{DDB} = 3.3 V ± 10%, T_A = -40 to 125°C (over recommended operating conditions, unless otherwise specified)

Parameters	Test conditions		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
CA-IS3860							
Supply Current – DC Signal	V_{IN} = 0V (CA-IS3860L); V_{IN} = V_{DDA} (CA-IS3860H)		I_{DDA}		1.9	2.8	mA
			I_{DDB}		3.6	5.4	
	V_{IN} = V_{DDA} (CA-IS3860L); V_{IN} = 0V(CA-IS3860H)		I_{DDA}		6.8	10.5	
			I_{DDB}		3.9	5.7	
Supply Current – AC Signal	All Channels Switching with 50% Duty Cycle Square Wave Clock Input with 3.3V Amplitude; C_L = 15 pF for Each Channel.	1Mbps (500kHz)	I_{DDA}		4.4	6.7	
			I_{DDB}		5.2	7.5	
		10Mbps (5MHz)	I_{DDA}		4.6	7.0	
			I_{DDB}		18.3	24.6	
		100Mbps (50MHz)	I_{DDA}		6.1	9.0	
			I_{DDB}		38.3	51.8	
CA-IS3861							
Supply Current – DC Signal	V_{IN} = 0V (CA-IS3861L); V_{IN} = V_{DDI}[1] (CA-IS3861H)		I_{DDA}		2.2	3.2	mA
			I_{DDB}		3.4	5.0	
	V_{IN} = V_{DDI}[1] (CA-IS3861L); V_{IN} = 0V(CA-IS3861H)		I_{DDA}		6.3	9.7	
			I_{DDB}		4.4	6.5	
Supply Current – AC Signal	All Channels Switching with 50% Duty Cycle Square Wave Clock Input with 3.3V Amplitude; C_L = 15 pF for Each Channel.	1Mbps (500kHz)	I_{DDA}		4.3	6.5	
			I_{DDB}		4.8	7.1	
		10Mbps (5MHz)	I_{DDA}		4.8	7.1	
			I_{DDB}		13.9	18.9	
		100Mbps (50MHz)	I_{DDA}		8.6	12.2	
			I_{DDB}		30.1	40.8	
CA-IS3862							
Supply Current – DC Signal	V_{IN} = 0V (CA-IS3862L); V_{IN} = V_{DDI}[1] (CA-IS3862H)		I_{DDA}		2.7	4.3	mA
			I_{DDB}		3.6	5.6	
	V_{IN} = V_{DDI}[1] (CA-IS3862L); V_{IN} = 0V(CA-IS3862H)		I_{DDA}		6.0	9.7	
			I_{DDB}		5.4	8.4	
Supply Current – AC Signal	All Channels Switching with 50% Duty Cycle Square Wave Clock Input with 3.3V Amplitude; C_L = 15 pF for Each Channel.	1Mbps (500kHz)	I_{DDA}		4.9	7.7	
			I_{DDB}		5.6	8.5	
		10Mbps (5MHz)	I_{DDA}		10.0	14.3	
			I_{DDB}		15.2	22.7	
		100Mbps (50MHz)	I_{DDA}		18.5	26.2	
			I_{DDB}		30.4	48.1	
CA-IS3863							
Supply Current – DC Signal	V_{IN} = 0V (CA-IS3863L); V_{IN} = V_{DDI}[1] (CA-IS3863H)		I_{DDA}		2.7	4.1	mA
			I_{DDB}		2.7	4.1	
	V_{IN} = V_{DDI}[1] (CA-IS3863L); V_{IN} = 0V(CA-IS3863H)		I_{DDA}		5.3	8.1	
			I_{DDB}		5.3	8.1	
Supply Current – AC Signal	All Channels Switching with 50% Duty Cycle Square Wave Clock Input with 3.3V Amplitude; C_L = 15 pF for Each Channel.	1Mbps (500kHz)	I_{DDA}		4.1	6.2	
			I_{DDB}		4.1	6.2	
		10Mbps (5MHz)	I_{DDA}		5.1	7.4	
			I_{DDB}		5.1	7.4	
		100Mbps (50MHz)	I_{DDA}		13.6	18.7	
			I_{DDB}		13.6	18.7	

Note:

1. V_{DDI} = Input-side supply V_{DD}.

V_{DDA} = V_{DDB} = 2.5 V ± 10%, T_A = -40 to 125°C (over recommended operating conditions, unless otherwise specified)

Parameters	Test conditions		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
CA-IS3860							
Supply Current – DC Signal	V_{IN} = 0V (CA-IS3860L); V_{IN} = V_{DDA} (CA-IS3860H)		I_{DDA}		1.9	2.7	mA
			I_{DDB}		3.6	5.2	
	V_{IN} = V_{DDA} (CA-IS3860L); V_{IN} = 0V(CA-IS3860H)		I_{DDA}		6.8	10.4	
			I_{DDB}		3.8	5.5	
Supply Current – AC Signal	All Channels Switching with 50% Duty Cycle Square Wave Clock Input with 2.5V Amplitude; C_L = 15 pF for Each Channel.	1Mbps (500kHz)	I_{DDA}		4.3	6.6	
			I_{DDB}		4.8	6.9	
		10Mbps (5MHz)	I_{DDA}		4.6	6.9	
			I_{DDB}		14.7	19.8	
		100Mbps (50MHz)	I_{DDA}		5.7	8.5	
			I_{DDB}		28.9	39.0	
CA-IS3861							
Supply Current – DC Signal	V_{IN} = 0V (CA-IS3861L); V_{IN} = V_{DDI}[1] (CA-IS3861H)		I_{DDA}		2.1	3.2	mA
			I_{DDB}		3.3	4.8	
	V_{IN} = V_{DDI}[1] (CA-IS3861L); V_{IN} = 0V(CA-IS3861H)		I_{DDA}		6.3	9.6	
			I_{DDB}		4.3	6.4	
Supply Current – AC Signal	All Channels Switching with 50% Duty Cycle Square Wave Clock Input with 2.5V Amplitude; C_L = 15 pF for Each Channel.	1Mbps (500kHz)	I_{DDA}		4.3	6.4	
			I_{DDB}		4.5	6.6	
		10Mbps (5MHz)	I_{DDA}		4.6	6.9	
			I_{DDB}		11.4	15.5	
		100Mbps (50MHz)	I_{DDA}		7.6	10.8	
			I_{DDB}		23.1	31.2	
CA-IS3862							
Supply Current – DC Signal	V_{IN} = 0V (CA-IS3862L); V_{IN} = V_{DDI}[1] (CA-IS3862H)		I_{DDA}		2.6	4.2	mA
			I_{DDB}		3.5	5.5	
	V_{IN} = V_{DDI}[1] (CA-IS3862L); V_{IN} = 0V(CA-IS3862H)		I_{DDA}		6.0	9.6	
			I_{DDB}		5.3	8.3	
Supply Current – AC Signal	All Channels Switching with 50% Duty Cycle Square Wave Clock Input with 2.5V Amplitude; C_L = 15 pF for Each Channel.	1Mbps (500kHz)	I_{DDA}		4.8	7.4	
			I_{DDB}		5.2	8.0	
		10Mbps (5MHz)	I_{DDA}		8.6	12.4	
			I_{DDB}		12.6	18.6	
		100Mbps (50MHz)	I_{DDA}		14.8	21.2	
			I_{DDB}		23.3	36.3	
CA-IS3863							
Supply Current – DC Signal	V_{IN} = 0V (CA-IS3863L); V_{IN} = V_{DDI}[1] (CA-IS3863H)		I_{DDA}		2.7	4.0	mA
			I_{DDB}		2.7	4.0	
	V_{IN} = V_{DDI}[1] (CA-IS3863L); V_{IN} = 0V(CA-IS3863H)		I_{DDA}		5.2	8.0	
			I_{DDB}		5.2	8.0	
Supply Current – AC Signal	All Channels Switching with 50% Duty Cycle Square Wave Clock Input with 2.5V Amplitude; C_L = 15 pF for Each Channel.	1Mbps (500kHz)	I_{DDA}		4.0	6.1	
			I_{DDB}		4.0	6.1	
		10Mbps (5MHz)	I_{DDA}		4.8	7.0	
			I_{DDB}		4.8	7.0	
		100Mbps (50MHz)	I_{DDA}		11.3	16.0	
			I_{DDB}		11.3	16.0	

Note:
1. V_{DDI} = Input-side supply V_{DD}.

7.10. Timing Characteristics

V_{DDA} = V_{DDB} = 5 V ± 10%, T_A = -40 to 125°C (over recommended operating conditions, unless otherwise specified)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DR	Data Rate		0		150	Mbps
PW_{min}	Minimum Pulse Width				5.0	ns
t_{PLH}, t_{PHL}	Propagation Delay Time	See Figure 8- 1		12.0	15.0	ns
PWD	Pulse Width Distortion $\|t_{PLH} - t_{PHL}\|$			0.2	4.5	ns
$t_{sk(o)}$	Channel-to-Channel Output Skew Time[1]	Same-direction channels		0.4	2.5	ns
$t_{sk(pp)}$	Part-to-Part Output Skew Time [2]			2.0	4.5	ns
t_r	Output Signal Rise Time	See Figure 8- 1		2.5	4.0	ns
t_f	Output Signal Fall Time	See Figure 8- 1		2.5	4.0	ns
t_{DO}	Default Output Delay Time from Input Power Loss	See Figure 8- 1		8	12	µs
t_{SU}	Start-up Time			15	40	µs

Notes:

1. tsk(o) is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
2. tsk(pp) is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

V_{DDA} = V_{DDB} = 3.3 V ± 10%, T_A = -40 to 125°C (over recommended operating conditions, unless otherwise specified)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DR	Data Rate		0		150	Mbps
PW_{min}	Minimum Pulse Width				5.0	ns
t_{PLH}, t_{PHL}	Propagation Delay Time	See Figure 8- 1		12.0	17.0	ns
PWD	Pulse Width Distortion $\|t_{PLH} - t_{PHL}\|$			0.2	4.5	ns
$t_{sk(o)}$	Channel-to-Channel Output Skew Time[1]	Same-direction channels		0.4	2.5	ns
$t_{sk(pp)}$	Part-to-Part Output Skew Time [2]			2.0	4.5	ns
t_r	Output Signal Rise Time	See Figure 8- 1		2.5	4.0	ns
t_f	Output Signal Fall Time	See Figure 8- 1		2.5	4.0	ns
t_{DO}	Default Output Delay Time from Input Power Loss	See Figure 8- 1		8	12	µs
t_{SU}	Start-up Time			15	40	µs

Notes:

1. tsk(o) is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
2. tsk(pp) is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

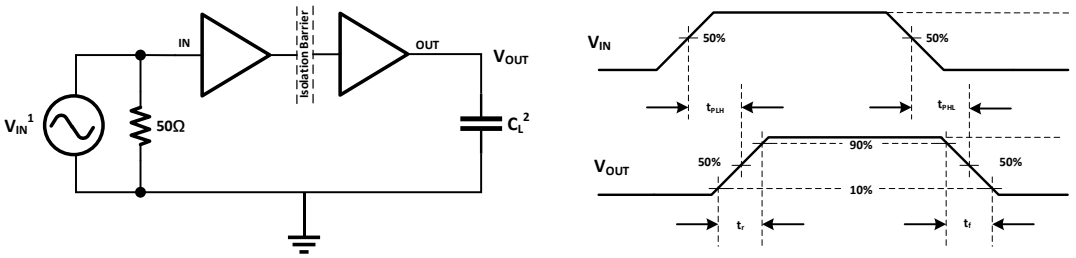
V_{DDA} = V_{DDB} = 2.5 V ± 10%, T_A = -40 to 125°C (over recommended operating conditions, unless otherwise specified)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DR	Data Rate		0		150	Mbps
PW_{min}	Minimum Pulse Width				5.0	ns
t_{PLH}, t_{PHL}	Propagation Delay Time	See Figure 8- 1		12.0	20.0	ns
PWD	Pulse Width Distortion $\|t_{PLH} - t_{PHL}\|$			0.2	4.5	ns
$t_{sk(o)}$	Channel-to-Channel Output Skew Time[1]	Same-direction channels		0.4	2.5	ns
$t_{sk(pp)}$	Part-to Part Output Skew Time [2]			2.0	5.0	ns
t_r	Output Signal Rise Time	See Figure 8- 1		2.5	4.0	ns
t_f	Output Signal Fall Time	See Figure 8- 1		2.5	4.0	ns
t_{DO}	Default Output Delay Time from Input Power Loss	See Figure 8- 1		8	12	µs
t_{SU}	Start-up Time			15	40	µs

Notes:

1. tsk(o) is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
2. tsk(pp) is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

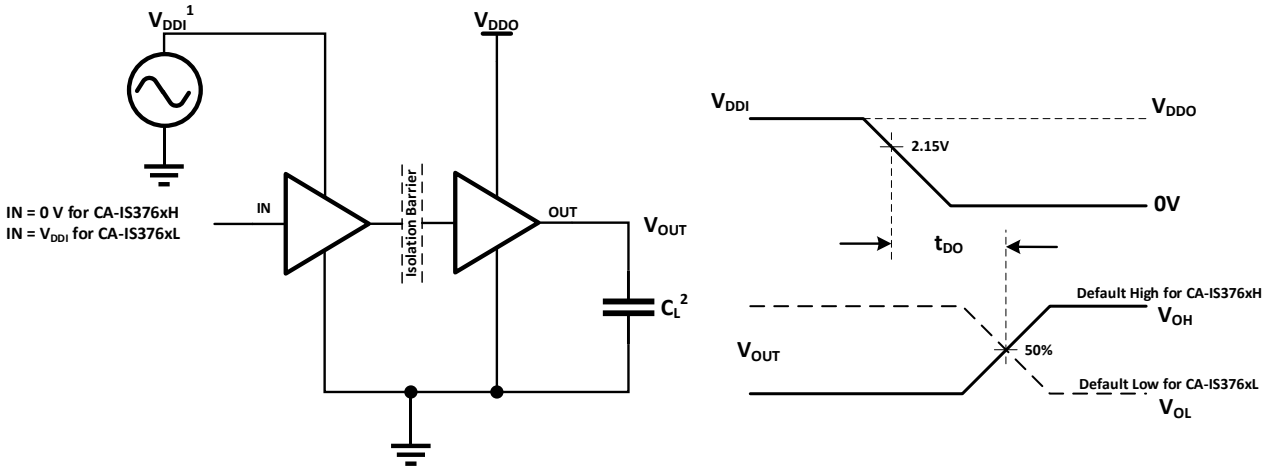
8. Parameter Measurement Information



Notes:

1. A square wave generator provide V_{IN} input signal with the following characteristics: frequency ≤100kHz, 50% duty cycle, t_r≤3ns, t_f≤3ns, Z_{out} = 50Ω. At the input, 50 Ω resistor is required to terminate input generator signal. It is not needed in actual application.
2. C_L = 15pF and includes external circuit (instrumentation and fixture etc.) capacitance. Since the load capacitance influence the output rising time, it's a key factor in the timing characteristic measurement.

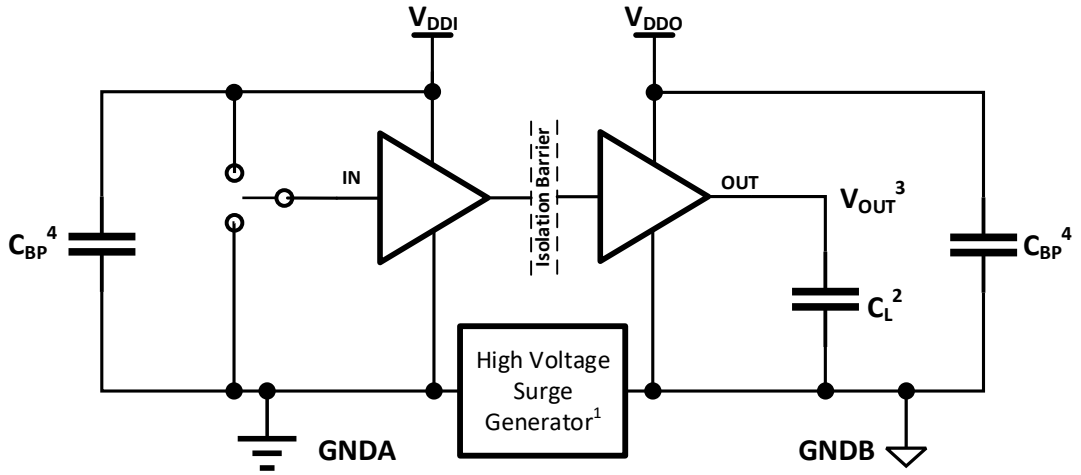
Figure 8- 1 Switching Characteristics Test Circuit and Voltage Waveforms



Notes:

1. Power Supply Ramp Rate = 10 mV/ns. V_{DDI} should ramp over 2.375V, and less than 5.5V.
2. C_L = 15pF and includes external circuit (instrumentation and fixture etc.) capacitance. Since the load capacitance influence the output rising time, it's a key factor in the timing characteristic measurement.

Figure 8- 2 Default Output Delay Time Test Circuit and Voltage Waveforms



Notes:

1. The High Voltage Surge Generator generates repetitive high voltage surges with > 1kV amplitude, rise time <10ns and fall time <10ns, to reach common-mode transient noise with > 150kV/μs slew rate.
2. C_L = 15pF and includes external circuit (instrumentation and fixture etc.) capacitance.
3. Pass-fail criteria: the output must remain stable.
4. C_{BP} (0.1 ~ 1uF) is bypass capacitance.

Figure 8- 3 Common-Mode Transient Immunity Test Circuit

9. Detailed Description

9.1. Overview

The CA-IS386x are a family of six-channel digital galvanic isolators using Chipanalog's full differential capacitive isolation technology. These devices have an ON-OFF keying (OOK) modulation scheme to transfer digital signals across the SiO2 based isolation barrier between circuits with different power domains. The transmitter sends a high frequency carrier across the barrier to represent one digital state and sends no signal to represent the other digital state. The receiver demodulates the signal and recovery input signal at output through a buffer stage. With this OOK architecture, CA-IS386x family of devices build a robust data transmission path between different power domains without any special start-up initialization requirements. These devices also incorporate advanced full differential techniques to maximize the CMTI performance and minimize the radiated emissions due the high frequency carrier and IO buffer switching.

9.2. Functional Block Diagram

The conceptual block diagram of a digital capacitive isolator, Figure 9- 1, shows a functional block diagram of a typical channel; Figure 9- 2shows the operating waveform of a typical channel. Each channel of the CA-IS386x is unidirectional, only passes data in one direction as indicated in the functional diagram. Each device of this family features six unidirectional channels that operate independently with guaranteed data rates from DC up to 150Mbps.

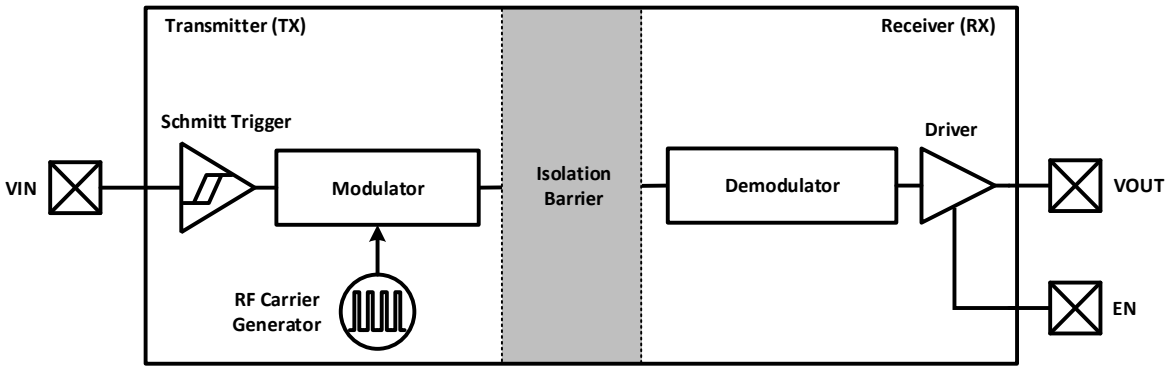


Figure 9- 1 Functional Block Diagram of a Single Channel

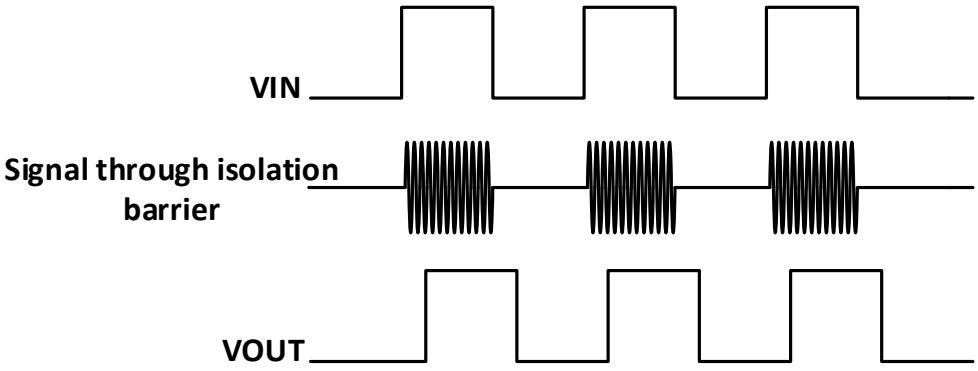


Figure 9- 2 Conceptual Operation Waveforms of a Single Channel

9.3. Device Operation Modes

Table 9-1 lists the operation modes for the CA-IS386x devices.

Table 9-1. Operation Mode

V_{DDI}[1]	V_{DDO}[1]	INPUT (VIx)[2]	OUTPUT (VOx)	OPERATION
PU	PU	H	H	Normal operation mode: A channel output follows the logic state of its input.
		L	L	
		Open	Default	Default output mode: When input VIx is open, the corresponding channel output goes to its default logic state. Default is *High* for CA-IS386xH and Low for CA-IS386xL.
PD	PU	X	Default	Default output mode: When V_{DDI} is unpowered, a channel output assumes the logic state based on its default option. Default is *High* for CA-IS386xH and Low for CA-IS386xL.
X	PD	X	Undetermined	If the output side V_{DDO} is unpowered, a channel output is undetermined.[3]

Notes:

1. V_{DDI} = Input-side supply V_{DD}; V_{DDO} = Output-side supply V_{DD}; PU = Powered up ($V_{DD} \geq V_{DD(UVLO+)}$); PD = Powered down ($V_{DD} \leq V_{DD(UVLO\_)}$); X = Irrelevant; H = High level; L = Low level; Z = High Impedance.
2. A strongly driven input signal can weakly power the floating V_{DD} through an internal protection diode and cause undetermined output.
3. The outputs are in undetermined state when $V_{DD(UVLO\_)} < V_{DDI}$, $V_{DDO} < V_{DD(UVLO+)}$.

10. Application and Implementation

The CA-IS386x isolation ICs provide complete galvanic isolation between two power domains, protecting circuits from high common-mode transients and faults, eliminating ground loops. In many applications, digital isolators are replacing optocouplers because they can reduce the power requirements and take up less board space while offering the same isolation capability. The CA-IS386x devices are the high-performance, six-channel digital isolators. Unlike optocouplers, which require external components to improve performance, provide bias, or limit current, the CA-IS386x devices only require two external bypass capacitors to operate. To reduce ripple and the chance of introducing data errors, bypass VDDA and VDDB pins with 0.1µF to 1µF low-ESR ceramic capacitors to GNDA and GNDB respectively. Place the bypass capacitors as close to the power supply input pins as possible. Figure 10- 1 shows typical operating circuit of the CA-IS3863; Figure 10- 2 is the typical applications for CA-IS37xx series products.

The CA-IS386x family devices do not require special power supply sequencing. The logic levels are set independently on either side by V_{DDA} and V_{DDB} supply voltage. When designing with digital isolators, keep in mind that because of the single-ended design structure, digital isolators do not conform to any specific interface standard and are only intended for isolating single-ended CMOS or TTL digital signal lines. The isolator is typically placed between the data controller (that is, MCU or FPGA), and a data converter or a line transceiver, regardless of the interface type or standard. The PCB designer should follow some critical recommendations in order to get the best performance from the design. For the high-speed digital signal circuit boards, we recommend to use the standard FR4 PCB material and a minimum of four layers is required to accomplish a low EMI PCB design. Layer order from top-to-bottom is: high-speed signal layer, ground plane, power plane, and low-frequency signal layer. Also, keep the input/output traces as short as possible, avoid using vias to make low-inductance paths for the signals. Keep the area underneath the digital isolator ICs free from ground and signal planes.

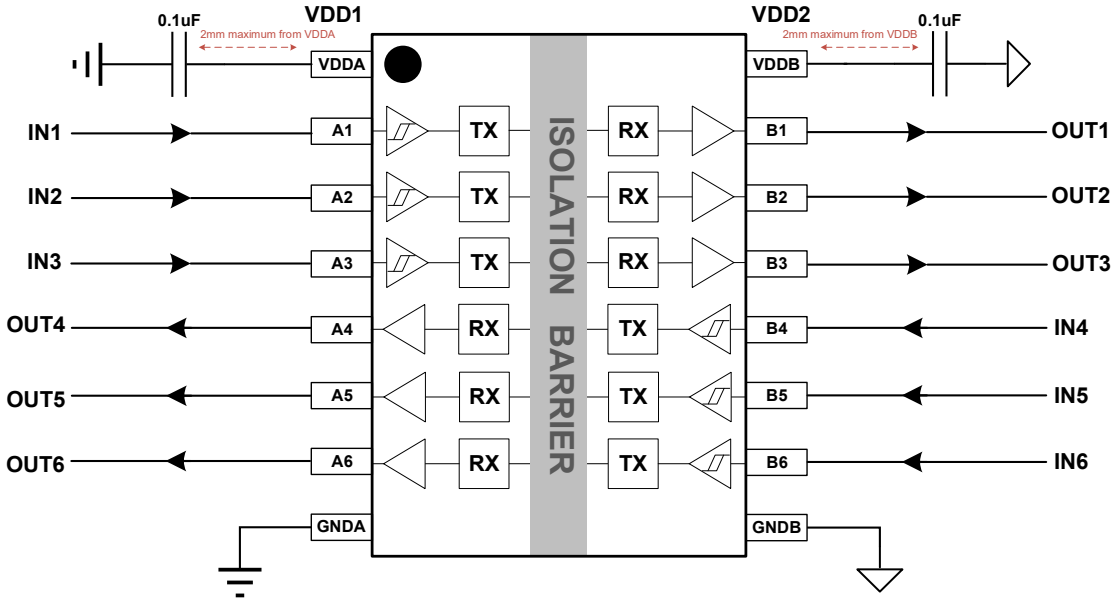


Figure 10- 1 Typical Application Circuit of CA-IS3863

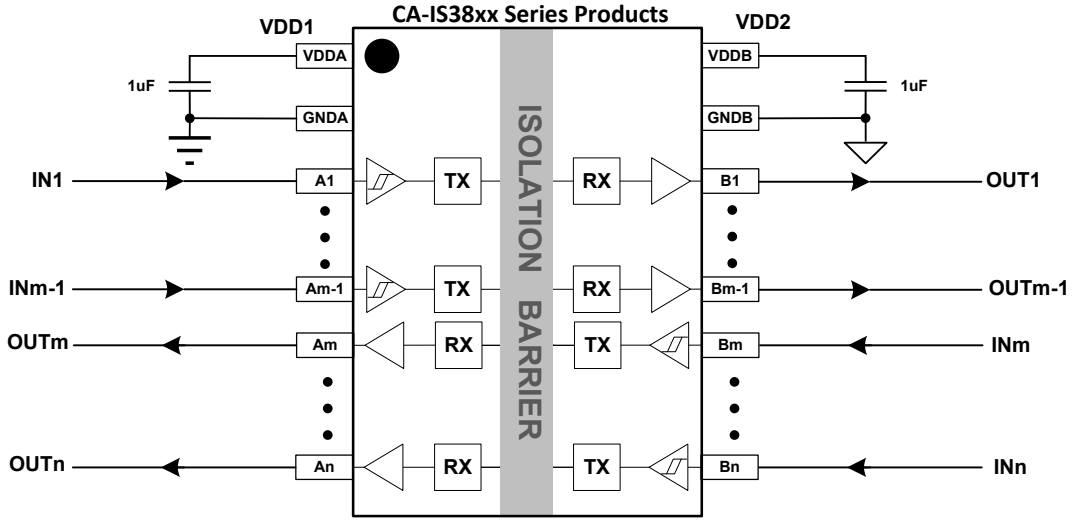
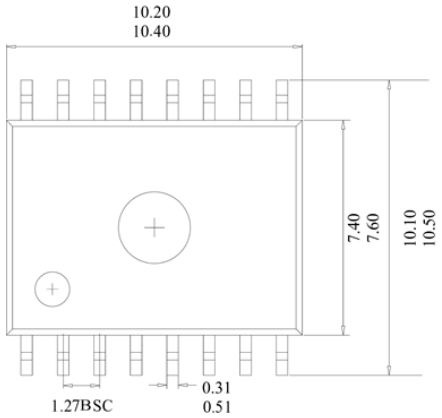


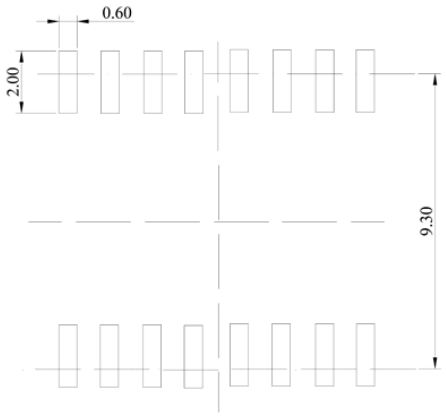
Figure 10- 2 Typical Applications for the CA-IS38xx Series Digital Isolators

11. Package Information

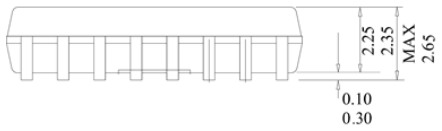
11.1. 16-Pin Wide Body SOIC Package Outline



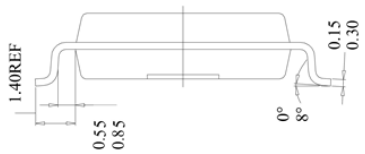
TOP VIEW



RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW

Note:

1. All dimensions are in millimeters, angles are in degrees.

12. Soldering Temperature (reflow) Profile

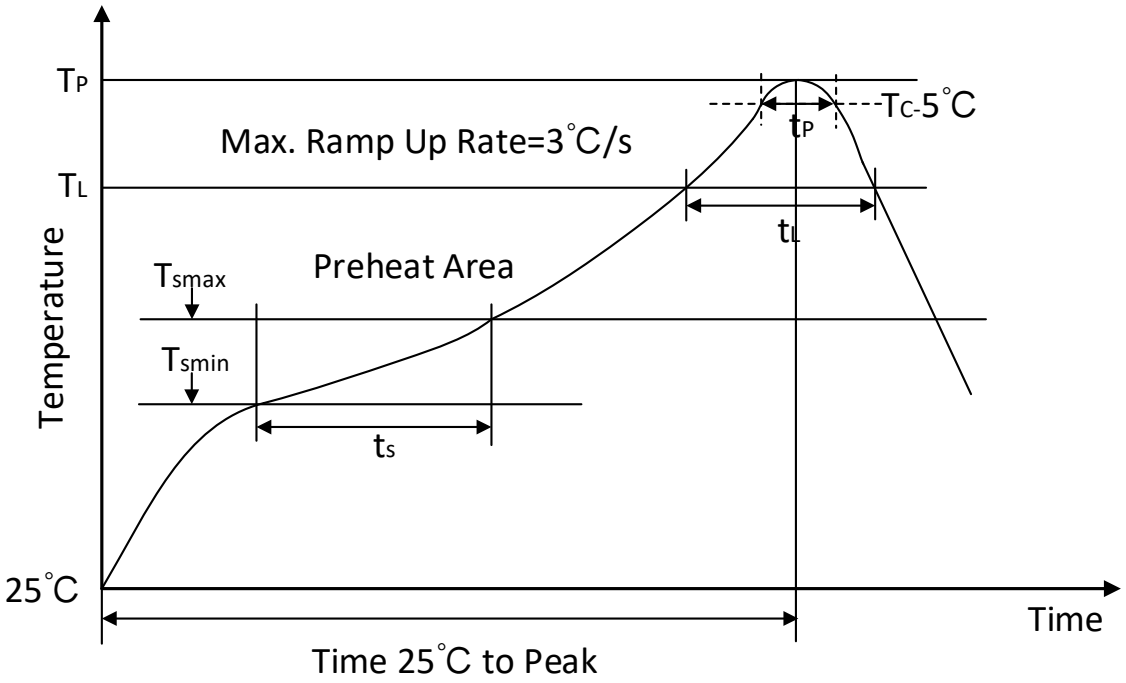


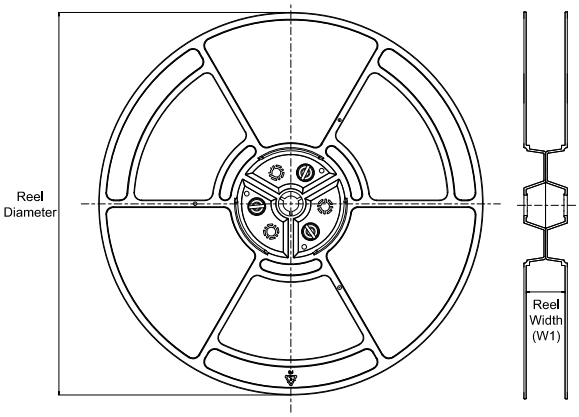
Figure 12- 1 Soldering Temperature (reflow) Profile

Table 12- 1 Soldering Temperature Parameter

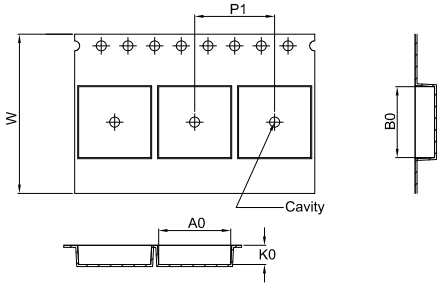
Profile Feature	Pb-Free Assembly
Average ramp-up rate(217 ℃ to Peak)	3℃ /second max
Time of Preheat temp(from 150 ℃ to 200 ℃)	60-120 second
Peak temperature	260 ℃
Time to be maintained above 217 ℃	60-150 second
Time within 5 ℃ of actual peak temp	30 second
Ramp-down rate	6 ℃/second max.
Time from 25℃ to peak temp	8 minutes max

13. Tape and Reel Information

REEL DIMENSIONS

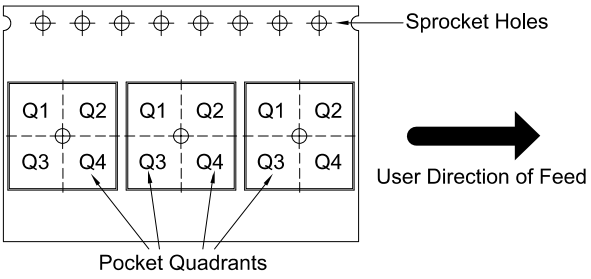


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CA-IS3860LW	SOIC	W	16	1000	330	16.4	10.9	10.7	3.2	12.0	16.0	Q1
CA-IS3860HW	SOIC	W	16	1000	330	16.4	10.9	10.7	3.2	12.0	16.0	Q1
CA-IS3861LW	SOIC	W	16	1000	330	16.4	10.9	10.7	3.2	12.0	16.0	Q1
CA-IS3861HW	SOIC	W	16	1000	330	16.4	10.9	10.7	3.2	12.0	16.0	Q1
CA-IS3862LW	SOIC	W	16	1000	330	16.4	10.9	10.7	3.2	12.0	16.0	Q1
CA-IS3862HW	SOIC	W	16	1000	330	16.4	10.9	10.7	3.2	12.0	16.0	Q1
CA-IS3863LW	SOIC	W	16	1000	330	16.4	10.9	10.7	3.2	12.0	16.0	Q1
CA-IS3863HW	SOIC	W	16	1000	330	16.4	10.9	10.7	3.2	12.0	16.0	Q1

14. Important statement

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