AEC-Q100 Qualification Report

Product Series： CA-IF1042LX-Q1

Report Version： V1.0

Reference Doc.： AEC- Q100- REV-H

Contents

1. Overview

Reliability testing of microelectronic products is a risk mitigation process designed to ensure the service life of device in customer applications. Semiconductor wafer manufacturing process and package-level reliability can be assessed in a variety of ways and may include accelerated environmental test conditions. Chipanalog evaluates manufacturability of the device to verify a robust silicon and assembly flow to ensure continuity of supply to customers. Chipanalog qualifies new devices, significant changes, and product families based on AEC-Q100.

2. Part Number List

Package Type	**Part Number**
SOIC8	CA-IF1042LS-Q1/CA-IF1042LVS-Q1

Note：AEC-Q100 provides the guideline for the use of generic data to accelerate and streamline the qualification process. Products sharing the same major product, process and materials elements may be categorized in a product qualification family.

3. Production Information

3.1. Wafer information

Wafer	DARKNESS
Fab site	SMIC
Fab Process	18BCDA

3.2. Package information

Assembly site	JCET-D8
FT site	JCET-D8
Package	SOIC8
Lead Frame	Cu
Bond wire	20um Au
MSL level	MSL1
Operation Temp.	Grade 1：-40℃~125℃

4. Reliability Qualification Plan

Test Group A–Accelerated Environment Stress Tests					
Group	**Item**	**Refer.**	**Test condition**	**QTY**	**Remark**
A1	PC	J-STD-020 JESD22-A113	Test @ Rm, Moisture Preconditioning MSL1 Before THB/BHAST, AC/UHAST, TC, and PTC stress,	231 pcs*3 lots	
A2	BHAST	JESD22-A110	BHAST: 130℃, 85% RH, 96 hrs (Test @ Rm/Hot)	77 pcs*3 lots	
A3	UHAST	JESD22-A101	UHAST: 130℃, 85% RH, 96 hrs (Test @ Rm)	77 pcs*3 lots	
A4	TC	JESD22-A104	-65℃-150℃, 500 cycles (Test @Rm/ Hot)	77 pcs*3 lots	
A5	PTC	JESD22-A105	-40℃-125℃, 1000 cycles (Test @ Rm/Hot)	NA	P<1W; ΔT<40℃;
A6	HTSL	JESD22-A103	T_a = 150℃, 1000 hrs (Test @ Rm/Hot)	45 pcs*1 lot	
Test Group B–Accelerated Lifetime Simulation Tests					
Group	**Item**	**Refer.**	**Test condition**	**QTY**	**Remark**
B1	HTOL	JESD22-A108	T_a = 125℃, V_{cc} = 5.5V, 1000 hrs (Test @ Rm/Cold/Hot)	77 pcs*3 lots	
B2	ELFR	AEC-Q100-008	T_a = 125℃, V_{cc} = 5.5V, 48 hrs (Test @ Rm/Hot)	800 pcs*3 lots	
B3	EDR	AEC-Q100-005	Test @ Rm/Hot	NA	Not NVM
Group C–Package Assembly Integrity Tests					
Group	**Item**	**Refer.**	**Test condition**	**QTY**	**Remark**
C1	WBS	AEC-Q100-001 AEC-Q003	Cpk > 1.67, Each bonder used T0 samples	30 bonds from 5 pcs	
C1	WBS	AEC-Q100-001 AEC-Q003	Cpk > 1.67, Each bonder used samples after TC	30 bonds from 5 pcs	
C2	WBP	MIL-STD883 AEC-Q003	Cpk > 1.67, Each bonder used T0	30 bonds from 5 pcs	
C2	WBP	MIL-STD883 AEC-Q003	Cpk > 1.67, Each bonder used samples after TC	30 bonds from 5 pcs	
C3	SD	JESD22-B102 JSTD-002D	> 95% coverage, 8hr steam aging prior to testing	15 pcs*1 lot	
C4	PD	JESD22-B100 JESD22-B108 AEC-Q003	Cpk > 1.67	10 pcs*3 lots	
C5	SBS	AEC-Q100-010 AEC-Q003	Cpk > 1.67, 5 balls from min. of 10 devices	NA	No solder ball
C6	LI	JESD22 B105	10 leads from each of 5 devices	NA	

Test Group D–Die Fabrication Reliability Tests					
Group	**Item**	**Refer.**	**Test condition**	**QTY**	**Remark**
D1	EM	JESD61	---	---	Done by Fab
D2	TDDB	JESD35	---	---	Done by Fab
D3	HCI	JESD60 & 28	---	---	Done by Fab
D4	NBTI	JESD90	---	---	Done by Fab
D5	SM	JESD61, 87, & 202	---	---	Done by Fab
Group E-Electrical Verification Tests					
Group	**Item**	**Refer.**	**Test condition**	**QTY**	**Remark**
E1	TEST	per datasheet	Pre and Post Stress Electrical Test	all	
E2	HBM	AEC Q100-002	500V, 1KV, 2KV, 6KV (Test @ Rm/Hot)	3 pcs/voltage level	
E3	CDM	AEC-Q100-011	250V, 500V, 750V, 2KV (Test @ Rm/Hot)	3 pcs/voltage level	
E4	LU	AEC-Q100-004	Test @ Rm/Hot	6 pcs*1 lot	
E9	EMC	SAE J1752/3	Electromagnetic Compatibility (Radiated Emissions)	1 pcs*1 lot	
E10	SC	AEC Q100-012	Applicable to all smart power devices.	NA	Not smart power device
E11	SER	JESD89-2 & JESD89-3	Applicable to devices with memory sizes≥1Mbit SRAM or DRAM based cells.	NA	Memory sizes<1Mbit
E12	LF	AEC Q005	Applicable to ALL Pb-free devices.	-	

5. Reliability Test Results

Test Group A–Accelerated Environment Stress Test					
Group	**Item**	**Test Condition**	**QTY**	**Lot NO.**	**Result**
A1	PC	Test @ Rm, Moisture Preconditioning before BHAST, UHAST, TC stress, MSL = 1, Peak Reflow Temp = 260℃	240 pcs*3 lots	2315A	Pass
				2316A	Pass
				2317A	Pass
A2	BHAST	130℃, 85% RH, 96 hrs, V_{cc} = 5.5 V	80 pcs*3 lots	2315A	Pass
				2316A	Pass
				2317A	Pass
A3	UHAST	130℃, 85% RH, 96 hrs	80 pcs*3 lots	2315A	Pass
				2316A	Pass
				2317A	Pass
A4	TC	-65℃-150℃, 500 cycles	80 pcs*3 lots	2315A	Pass
				2316A	Pass
				2317A	Pass
	TC-WBP	Bond pull after TC500cyc	30 bonds from 5 pcs	2316A	Pass
A6	HTSL	T_a = 150℃, 1000 hrs	45 pcs*1 lot	2316A	Pass
Test Group B–Accelerated Lifetime Simulation Tests					
Group	**Item**	**Test Condition**	**QTY**	**Lot NO.**	**Result**
B1	HTOL	T_a = 125℃, 1000 hrs, V_{cc} = 5.5 V, TTL input, F = 10 kHz	80 pcs*3 lots	2315A	Pass
				2316A	Pass
				2317A	Pass
B2	ELFR	T_a = 125℃, V_{cc} = 5.5 V, 48 hrs	800 pcs*3 lots	2315A	Pass
				2316A	Pass
				2317A	Pass
Group C–Package Assembly Integrity Tests					
Group	**Item**	**Test Condition**	**QTY**	**Lot NO.**	**Result**
C1	WBS	Cpk > 1.67， Each bonder used T0 samples	30 bonds from 5 pcs	2316A	Pass, CPK=2.48
C2	WBP	Cpk > 1.67, each bonder used T0	30 bonds from 5 pcs	2316A	Pass, CPK=2.21
C3	SD	>95% coverage, 8 hrs steam aging prior to testing	15 pcs*1 lot	2316A	Pass
C4	PD	Cpk > 1.67	10 pcs*3 lots	2315A	Pass
				2316A	
				2317A	

TEST GROUP D–Die Fabrication Reliability Tests			
Group	**Item**	**Test Condition**	**ADDITIONAL REQUIREMENTS**
D1	EM	---	The Die Fabrication Reliability Tests are carried out by every fabrication site. The data, test method, calculations and internal criteria are available to the customer upon request.
D2	TDDB	---	
D3	HCI	---	
D4	NBTI	---	
D5	SM	---	

Group E-Electrical Verification Tests					
Group	**Item**	**Test Condition**	**QTY**	**Lot NO.**	**Result**
E1	TEST	Pre and Post Stress Electrical Test	all	/	All pass
E2	HBM	500V, 1KV, 2KV, 6KV (Test @ Rm/Hot)	3 pcs/voltage level	2315A	Pass 6KV
E3	CDM	250V, 500V, 750V, 2KV (Test @ Rm/Hot)	3 pcs/voltage level	2315A	Pass 2KV
E4	LU	Test @ Rm/Hot	6 pcs*1 lot	2315A	Pass
E9	EMC	Electromagnetic Compatibility (Radiated Emissions)	1 pcs*1 lot	2315A	Level N11
E12	LF	Per AEC-Q005	/	SOP8	Pass

6. MTBF&FIT

Supporting Data (Ea = 0.7 eV, Confidence Level = 60%)							MTBF (hrs)	FIT
Test Temp.	**Test Voltage**	**Duration**	**QTY**	**Fail QTY**	**Operation Temp.**	**Operation Voltage**		
125℃	5.5V	1000hrs	240	0	55℃	5V	4.98E+07	20.1
125℃	5.5V	48hrs	2400	0	55℃	5V		

7. Conclusion

CA-IF1042LX-Q1 series products are qualified by AEC-Q100 standard.

Disclaimer

This information is provided to assist customers in design and development. It could change for technology innovation without notice.

The devices are shipped after passing final test. Customers are responsible to conduct sufficient engineering and additional qualification testing to determine whether a device is suitable for use in their applications.

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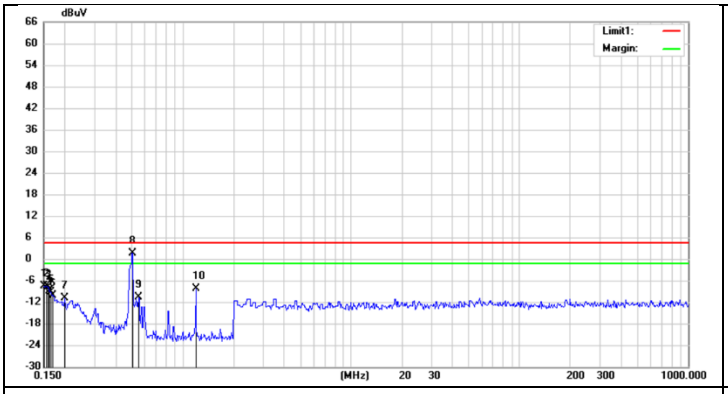
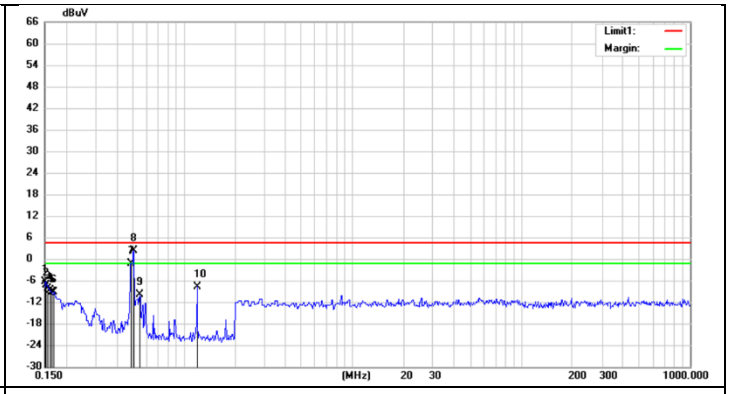
Revision History

Revision	Change Log	Date
V1.0	Initial release	2023.08.28

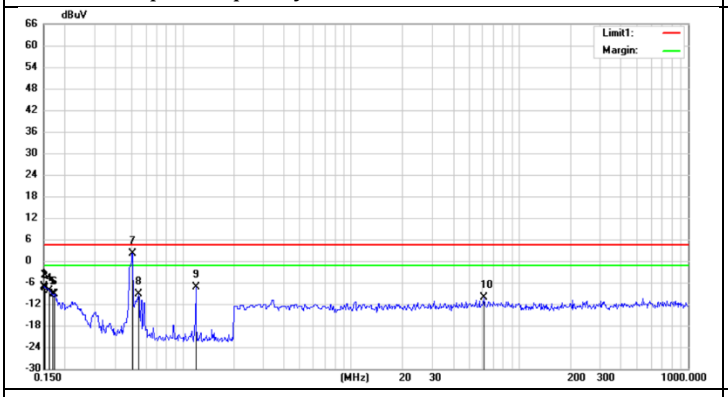
Appendix 1: EMC Test Results



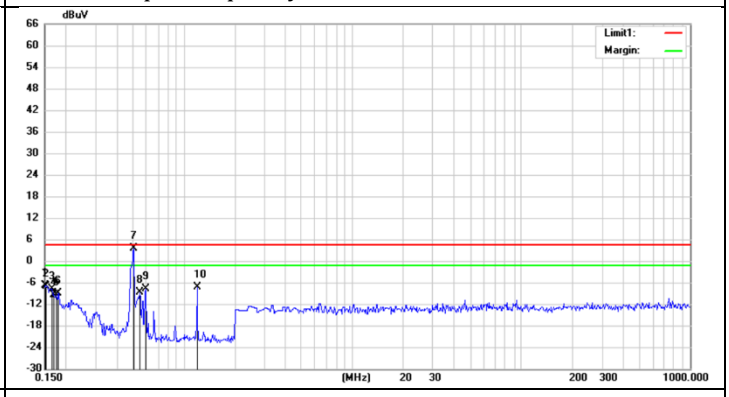
Input frequency = 5KHz， Polarization=0°



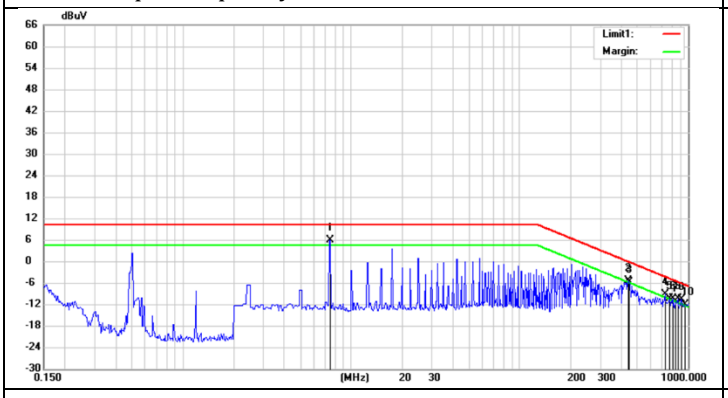
Input frequency = 5KHz， Polarization=90°



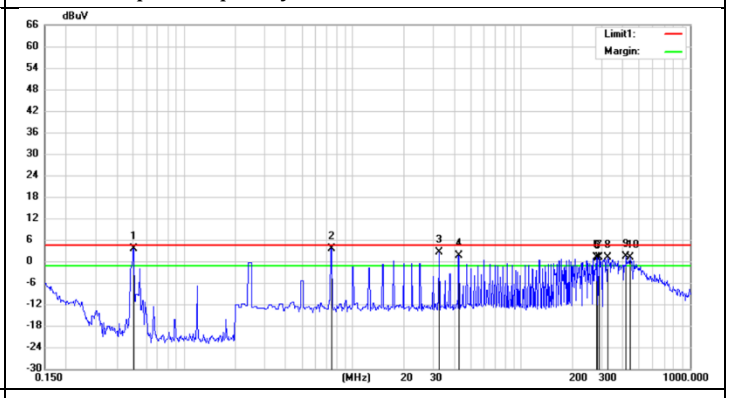
Input frequency = 5KHz， Polarization=180°



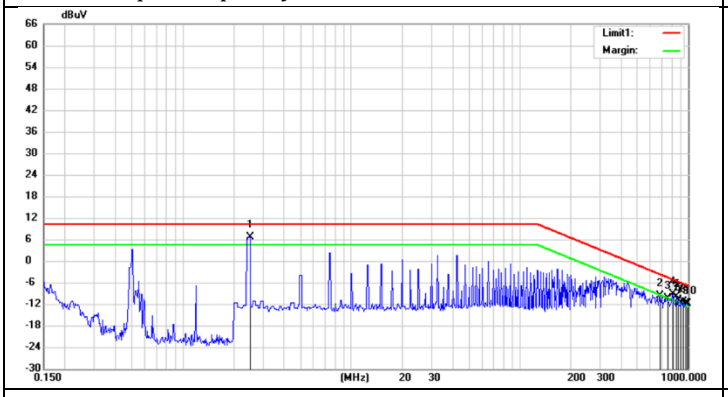
Input frequency = 5KHz， Polarization=270°



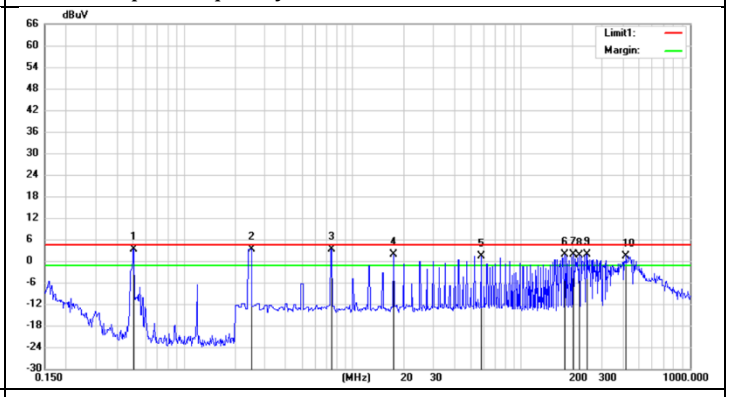
Input frequency = 2.5MHz， Polarization=0°



Input frequency = 2.5MHz， Polarization=90°

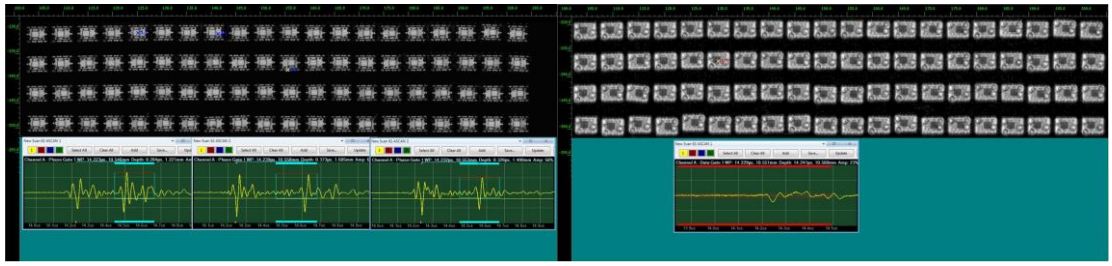
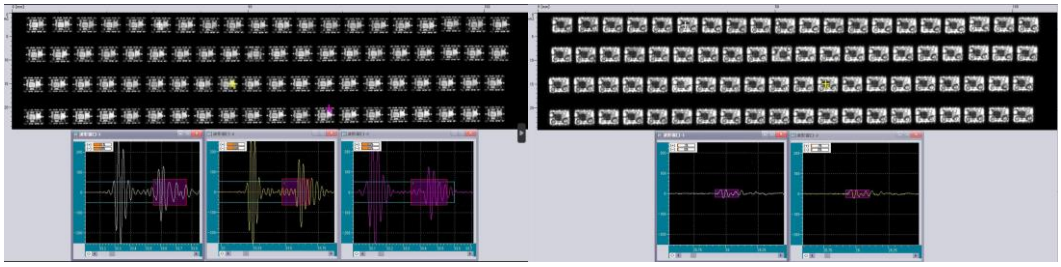
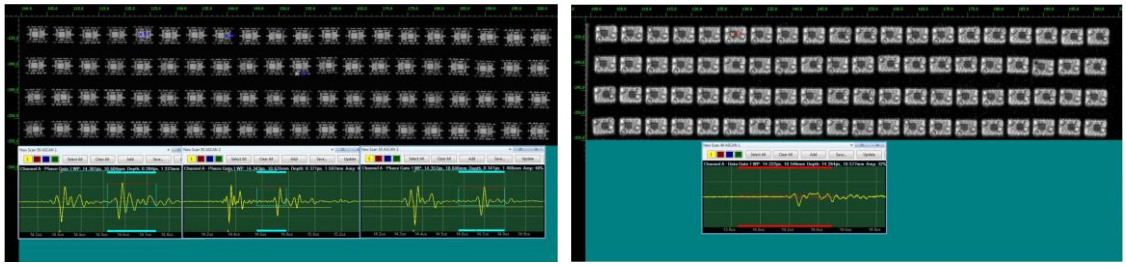
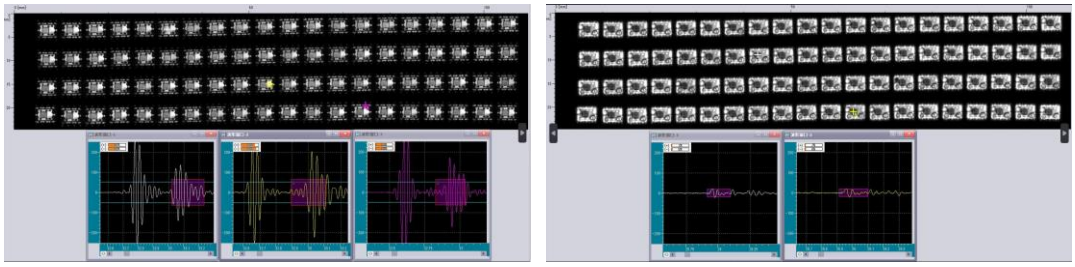
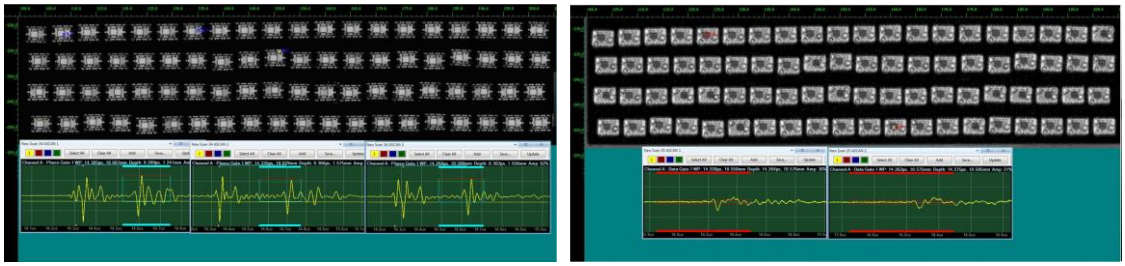


Input frequency = 2.5MHz， Polarization=180°



Input frequency = 2.5MHz， Polarization=270°

Appendix 2: SAT Test Results

Lot 1 pre-MSL	
Lot 1 post-MSL	
Lot 2 pre-MSL	
Lot 2 post-MSL	
Lot 3 pre-MSL	
Lot 3 post-MSL