# Four-channel Local Interconnect Network (LIN) transceiver

## 1. Features

- **AEC-Q100 Qualified for Automotive Application**
- **Meets LIN2.0、LIN2.1、LIN2.2、LIN2.2A and ISO 17987-4:2016(12V) Physical-layer (EPL) Standards**
- **Compliant to SAE J2602-1 and SAE J2602-2 LIN Physical-layer Specification**
- **Designed to Support 12V Applications with Wide Operating Supply Range:**
  - 5V to 28V supply range ($V_{BAT}$)
- **Support up to 20kbps LIN Transmission Data Rate**
- **Operating Mode:**
  - Normal operation
  - Low-power Standby
  - Low-power Sleep
  - Power-off
- **Wake-up from Low-power Mode:**
  - Remote wake-up via LINx bus
  - wake-up via SLPx_N pins
- **Integrated 30kΩ LIN pull-up Resistor**
- **Power-up/down Glitch-free Operation on LIN bus and RXD output**
- **Integrated Protection Increases Robustness**
  - ±42V fault-tolerant LIN bus
  - 42V load dump protection
  - ±14kV Human Body Model ESD Protection (LINx, $V_{BAT}$)
  - ±10kV IEC 61000-4-2 ESD Protection (LINx and $V_{BAT}$ to GAN)
  - Undervoltage protection on $V_{BAT}$
  - Transmitter dominant timeout prevents lockup
  - LIN bus short circuit protection functions.
  - TXD dominant time-out function
  - Initial TXD dominant check when switching to Normal mode
  - Thermal shutdown
  - System level fail-safe protection for the unpowered node or ground disconnection
- **–40°C to 150°C Junction Temperatures Range**
- **Available in QFN24 Packages**

## 2. Applications

- Body electronics
- Automotive gateway
- Infotainment and cluster
- Hybrid electric vehicles and powertrain systems

## 3. General Description

The CA-IF1024F-Q1 is a Local Interconnect Network (LIN) four channel transceiver, which is a low speed Universal Asynchronous Transceiver (UART) communication protocol that supports automotive in vehicle networks.

The CA-IF1024F-Q1 transceiver controls the LIN bus state via the TXDx input and reports the bus state on output RXD between the protocol controller and physical LIN networks. These device features slew-rate control and wave-shaping to reach a very low level of electromagnetic emission (EME) within a broad frequency range.

The CA-IF1024F-Q1 devices are designed to support 12V automotive applications with 5V to 18V wide $V_{BAT}$ input voltage operating range and have up to ±42V fault protection on LIN bus, with integrated ESD protection, these devices help to reduce external components in the design. In addition, CA-IF1024F-Q1 also supports low-power sleep mode. This device supports the use of LINx and SLPx_ N-pin wake-up function

**Table 3-1. Device Information**

| Part number | Package | Package size(NOM) |
|---|---|---|
| CA-IF1024F-Q1 | QFN24(F) | 3.5mm x 5.5mm |

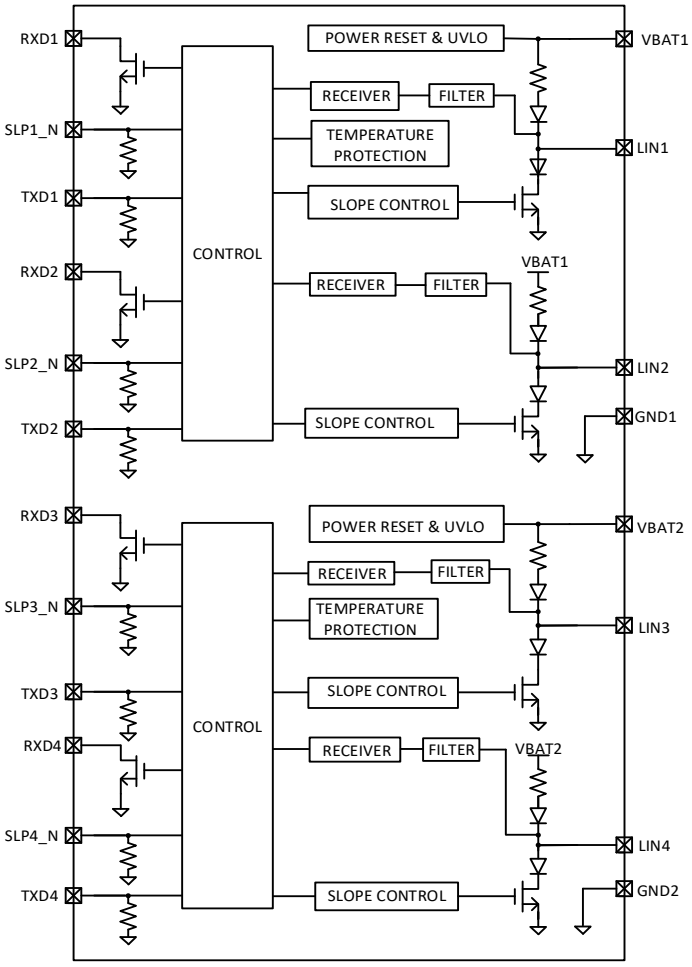



**Figure3- 1. Simplified Block Diagram**

## 4. Ordering Information

**Table 4-1. Ordering Information**

| Part Number | Features | Package |
|---|---|---|
| CA-IF1024F-Q1 | Automotive qualified part | QFN24(F) |

# Table of contents



## 5. Revision History

| Revision Number | Description | Page Changed |
|---|---|---|
| V1.0 | Initial Version | NA |

## 6. Pin Configuration and Functions

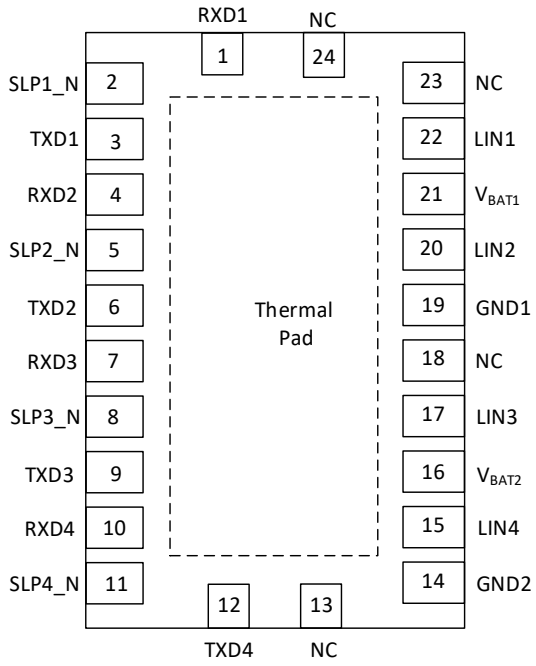



**Figure6- 1. CA-IF1024F-Q1 Pin Configuration**

**Table 6-1. CA-IF1024F-Q1 Pin Configuration and Description**

| Pin Name | Pin # | Type | Description |
|---|---|---|---|
| RXD1 | 1 | Output | Receive data output 1 (open-drain); active LOW after a wake-up event. |
| SLP1_N | 2 | Input | Enable input 1, high level enables devices into Normal mode, low level enables devices Sleep mode, reset the wake-up request on RXD1. |
| TXD1 | 3 | Input | Transmit data input 1. |
| RXD2 | 4 | Output | Receive data output 2 (open-drain); active LOW after a wake-up event. |
| SLP2_N | 5 | Input | Enable input 2, high level enables devices into Normal mode, low level enables devices Sleep mode, reset the wake-up request on RXD2. |
| TXD2 | 6 | Input | Transmit data input 2. |
| RXD3 | 7 | Output | Receive data output 3 (open-drain); active LOW after a wake-up event. |
| SLP3_N | 8 | Input | Enable input 3, high level enables devices into Normal mode, low level enables devices Sleep mode, reset the wake-up request on RXD3. |
| TXD3 | 9 | Input | Transmit data input 3. |
| RXD4 | 10 | Output | Receive data output 4 (open-drain); active LOW after a wake-up event. |
| SLP4_N | 11 | Input | Enable input 4, high level enables devices into Normal mode, low level enables devices Sleep mode, reset the wake-up request on RXD4. |
| TXD4 | 12 | Input | Transmit data input 4. |
| NC | 13 | | No internal connection. |
| GND2[1] | 14 | GND | Ground |
| LIN4 | 15 | Bus I/O | LIN4 bus input/output. |
| $V_{BAT2}$ | 16 | Power | Battery supply for LIN3 and LIN4. |
| LIN3 | 17 | Bus I/O | LIN3 bus input/output. |
| NC | 18 | | No internal connection. |
| GND1[1] | 19 | GND | Ground |
| LIN2 | 20 | Bus I/O | LIN2 bus input/output. |
| $V_{BAT1}$ | 21 | Power | Battery supply for LIN1 and LIN2. |
| LIN1 | 22 | Bus I/O | LIN1 bus input/output. |
| NC | 23 | | No internal connection. |
| NC | 24 | | No internal connection. |

**Note：**

1.For enhanced thermal and electrical performance, the exposed center pad of the QFN24 package should be soldered to board ground.

# 7. Specifications

## 7.1. Absolute Maximum Ratings[1]

| Symbol | PARAMETER | TEST CONDITIONS | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{BAT}$ | Supply voltage range | To GND, To LIN | -0.3 | 42 | V |
| $V_{TXDx}$ | TXDx voltage range | Pins TXD1 ~TXD4 to GND | -0.3 | 7 | V |
| $V_{RXDx}$ | RXDx voltage range | Pins RXD1 ~RXD4 to GND | -0.3 | 7 | V |
| $V_{SLPx\_N}$ | SLPx_N voltage range | Pins SLP1_N ~ SLP4_N to GND | -0.3 | 7 | V |
| $V_{LINx}$ | LINx voltage range | Pins LIN1 ~ LIN4 to GND<br>Pins LIN1 ~ LIN2 to $V_{BAT1}$<br>Pins LIN3 ~ LIN4 to $V_{BAT2}$ | -42 | 42 | V |
| $\triangle V_{(LIN1-LIN2)}$ | LINx voltage range | Pin LIN1 and pin LIN2 | -42 | 42 | V |
| $\triangle V_{(LIN3-LIN4)}$ | LINx voltage range | Pin LIN3 and pin LIN4 | -42 | 42 | V |
| $T_{vJ}$ | Virtual junction temperature range | | -40 | 150 | ℃ |
| $T_{STG}$ | Storage temperature range | | -55 | 150 | ℃ |

**Note:**

1. The stresses listed under “Absolute Maximum Ratings” are stress ratings only, not for functional operation condition. Exposure to absolute maximum rating conditions for extended periods may cause permanent damage to the device.

## 7.2. ESD Ratings

| PARAMETER | TEST CONDITIONS | | Value | 单位 |
|---|---|---|---|---|
| HBM ESD | LIN, $V_{BAT}$ pins | | ±14 | kV |
| | RXDx, SLPx_N, TXDx pins | | ±8 | |
| CDM ESD | Other pins to GND | | ±2 | kV |
| System Level ESD | LINx and $V_{BAT}$ to GND | IEC 61000-4-2: contact discharge, without power-up | ±10 | kV |

## 7.3. Recommended Operating Conditions

| PARAMETER | | Min. | Max. | Unit |
|---|---|---|---|---|
| $V_{BAT}$ | Battery voltage range | 5 | 18 | V |
| $V_{LINx}$ | LIN bus voltage range | 0 | 18 | V |
| $V_{LOGIC}$ | Logic voltage range (RXDx、SLPx_N 和 TXDx) | 0 | 5.5 | V |
| $T_A$ | Operation Temperature Range | -40 | 125 | °C |

## 7.4. Recommended Operating Conditions

| PARAMETER | | SOIC8 | Unit |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 41 | °C/W |

## 7.5. Electrical Characteristics

Over recommended operating conditions, $T_A$ = –40°C to 125°C, $V_{BAT}$=12V (unless otherwise noted).

### 7.5.1. Power consumption

| PARAMETER | | TEST CONDITIONS | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $V_{BAT}$ | Battery supply voltage | $V_{BAT1}$ and $V_{BAT2}$ | | 5 | | 18 | V |
| $I_{BAT}$ | $V_{BAT}$ Current | Sleep mode (both channels) | bus recessive：$V_{LINx}$=$V_{BAT}$， $V_{SLPx\_N}$=0V，$V_{BAT}$=12V | 3 | 20 | 30 | μA |
| $I_{BAT}$ | $V_{BAT}$ Current | | bus dominant：$V_{LINx}$=0V， $V_{SLPx\_N}$=0V，$V_{BAT}$=12V | 300 | 880 | 1600 | μA |
| $I_{BAT}$ | $V_{BAT}$ Current | Standby mode (both channels) | bus recessive：$V_{LINx}$=$V_{BAT}$， $V_{SLPx\_N}$=0V，$V_{BAT}$=12V | 3 | 20 | 30 | μA |
| $I_{BAT}$ | $V_{BAT}$ Current | | bus dominant：$V_{BAT}$ =12V， $V_{LINx}$=0V ，$V_{SLPx\_N}$=0V | 300 | 880 | 1600 | μA |
| $I_{BAT}$ | $V_{BAT}$ Current | Normal mode (both channels) | bus recessive：$V_{LINx}$=$V_{BAT}$， $V_{TXDx}$=5V ，$V_{SLPx\_N}$=5V | 80 | 260 | 600 | μA |
| $I_{BAT}$ | $V_{BAT}$ Current | | bus dominant：$V_{BAT}$ =12V， $V_{TXDx}$=0V，$V_{SLPx\_N}$=5V | 1 | 2.3 | 5 | mA |

### 7.5.2. Power on reset($V_{BAT}$)

| PARAMETER | | TEST CONDITIONS | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{th(POR)L}$ | Low-level power-on reset threshold voltage | | 1.6 | 3.1 | 3.9 | V |
| $V_{th(POR)H}$ | High-level power-on reset threshold voltage | | 2.3 | 3.4 | 4.3 | V |
| $V_{hys(POR)}$ | Power-on reset hysteresis voltage | | 0.05 | 0.3 | 1 | V |
| $V_{th(VBATL)L}$ | Power-on reset hysteresis voltage | | 3.9 | 4.4 | 4.7 | V |
| $V_{th(VBATL)H}$ | High-level $V_{BAT}$ LOW threshold voltage | | 4.2 | 4.7 | 4.9 | V |
| $V_{hys(VBATL)}$ | $V_{BAT}$ LOW hysteresis voltage | | 0.15 | 0.3 | 0.6 | V |

### 7.5.3. TXDx[1] Pin

| PARAMETER | | TEST CONDITIONS | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{IH}$ | High-level input voltage | | 2 | | 7 | V |
| $V_{IL}$ | Low-level input voltage | | -0.3 | | 0.8 | V |
| $V_{hys}$ | hysteresis voltage | | 50 | 200 | 400 | mV |
| $R_{PD(TXD)}$ | TXDx pull-up resistor | $V_{TXDx}$=5V | 50 | 125 | 325 | kΩ |
| $I_{IL}$ | High-level leakage current | $V_{TXDx}$=0V | -5 | 0 | 5 | μA |

**Note：**
1.TXDx Refers to TXD1/ TXD2/ TXD3/TXD4.

### 7.5.1. SLPx_N[1] Pin

| PARAMETER | | TEST CONDITIONS | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{IH}$ | High-level input voltage | | 2 | | 7 | V |
| $V_{IL}$ | Low-level input voltage | | -0.3 | | 0.8 | V |
| $V_{hys}$ | hysteresis voltage | | 50 | 200 | 400 | mV |
| $R_{PD(SLP\_N)}$ | SLPx_N pull-up resistor | $V_{TXDx}$=5V | 100 | 250 | 650 | kΩ |
| $I_{IL}$ | High-level leakage current | $V_{TXDx}$=0V | -5 | 0 | 5 | μA |

**Note：**
1.SLPx_N Refers to SLP1_N / SLP2_N / SLP3_N /SLP4_N.

### 7.5.2. RXDx[1] Pin

| PARAMETER | | TEST CONDITIONS | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $I_{OL}$ | Low-level output current | $V_{RXDx}$=0.4V | 2 | | | mA |
| $I_{LH}$ | High-level leakage current | | -5 | 0 | 5 | μA |

**Note：**

1.RXDx Refers to RXD1/RXD2/ RXD3/RXD4.

### 7.5.3. LINx[1] Pin

| PARAMETER | | TEST CONDITIONS | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $I_{BUS\_LIM}$ | Driver output current limitation @dominant | $V_{TXDx}$=0V;$V_{LINx}$=$V_{BAT}$=18V | 40 | | 150 | mA |
| $I_{BUS\_PAS\_rec}$ | Receiver input leakage current@ recessive | $V_{TXDx}$=5V;$V_{LINx}$= 18V;$V_{BAT}$=5V | | | 20 | μA |
| $I_{BUS\_PAS\_dom}$ | Receiver input leakage current@ dominant | Normal mode; $V_{TXD}$=$V_{CC}$;$V_{LIN}$= 0V;$V_{BAT}$=12V | -600 | | | μA |
| $V_{SerDiode}$[2] | Voltage drop on the serial diode | in pull-up path with $R_{slave}$， $I_{SerDiode}$=10μA | 0.4 | 0.7 | 1 | V |
| $I_{BUS\_NO\_GND}$ | Bus current @ loss ground | $V_{BAT}$=18V; $V_{LINx}$= 0V | -750 | | 10 | μA |
| $I_{BUS\_NO\_BAT}$ | Bus current @ loss battery | $V_{BAT}$=0V; $V_{LINx}$= 18V | | | 8 | μA |
| $V_{BUSdom}$ | LIN receiver dominant state | $V_{BAT}$=5V to 18V | | | 0.4$V_{BAT}$ | V |
| $V_{BUSrec}$ | LIN receiver recessive state | $V_{BAT}$=5V to 18V | 0.6$V_{BAT}$ | | | V |
| $V_{BUS\_CNT}$ | LIN receiver center threshold | $V_{BAT}$=5V to 18V;$V_{BUS\_CNT}$=( $V_{BUSdom}$+ $V_{BUSrec}$)/2 | 0.45$V_{BAT}$ | 0.5$V_{BAT}$ | 0.55$V_{BAT}$ | V |
| $V_{HYS}$ | LIN receiver hysteresis voltage | $V_{BAT}$=5V to 18V;$V_{HYS}$=$V_{BUSrec}$ -$V_{BUSdom}$ | | | 0.175 $V_{BAT}$ | V |
| $R_{slave}$ | | Resistance between LIN and $V_{BAT}$， VLIN=0V;$V_{BAT}$=12V | 20 | 30 | 60 | kΩ |
| $C_{LINx}$[2] | Slave resistance | | | | 20 | pF |
| $V_{O(DOM)}$ | LIN dominant output | Normal mode;$V_{TXD}$=0V;$V_{BAT}$= 7V | | | 1.4 | V |
| | | Normal mode;$V_{TXD}$=0V;$V_{BAT}$= 18V | | | 2.0 | V |

**Note：**

1. LINx Refers to LIN1/LIN2/LIN3/LIN4.
2. The test data is based on bench test and design simulation.

### 7.5.4. Duty cycle

| PARAMETER | | TEST CONDITIONS | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $\delta1^{1,2}$ | Duty cycle 1 | $V_{th(rec)(max)}$=0.744x$V_{BAT}$; $V_{th(dom)(max)}$=0.581x$V_{BAT}$; $t_{bit}$=50μs; $V_{BAT}$=7V~18V，see Figure8- 1 | 0.396 | | | |
| | | $V_{th(rec)(max)}$=0.76x$V_{BAT}$; $V_{th(dom)(max)}$=0.593x$V_{BAT}$; $t_{bit}$=50μs; $V_{BAT}$=5V~7V，see Figure8- 1 | 0.396 | | | |
| $\delta2^{2,3}$ | Duty cycle 2 | $V_{th(rec)(min)}$=0.422x$V_{BAT}$; $V_{th(dom)(min)}$=0.284x$V_{BAT}$; $t_{bit}$=50μs; $V_{BAT}$=7.6V~18V，see Figure8- 1 | | | 0.581 | |
| | | $V_{th(rec)(min)}$=0.41x$V_{BAT}$; $V_{th(dom)(min)}$=0.275x$V_{BAT}$; $t_{bit}$=50μs; $V_{BAT}$=6.1V~7.6V，see Figure8- 1 | | | 0.581 | |
| $\delta3^{1,2}$ | Duty cycle 3 | $V_{th(rec)(max)}$=0.778x$V_{BAT}$; $V_{th(dom)(max)}$=0.616x$V_{BAT}$; $t_{bit}$=96μs; $V_{BAT}$=7V~18V，see Figure8- 1 | 0.417 | | | |
| | | $V_{th(rec)(max)}$=0.797x$V_{BAT}$; $V_{th(dom)(max)}$=0.630x$V_{BAT}$; $t_{bit}$=96μs; $V_{BAT}$=5V~7V，see Figure8- 1 | 0.417 | | | |
| $\delta4^{2,3}$ | Duty cycle 14 | $V_{th(rec)(min)}$=0.389x$V_{BAT}$; $V_{th(dom)(min)}$=0.251x$V_{BAT}$; $t_{bit}$=96μs; $V_{BAT}$=7.6V~18V，see Figure8- 1 | | | 0.590 | |
| | | $V_{th(rec)(min)}$=0.378x$V_{BAT}$; $V_{th(dom)(min)}$=0.242x$V_{BAT}$; $t_{bit}$=96μs; $V_{BAT}$=6.1V~7.6V，see Figure8- 1 | | | 0.590 | |

**Note：**

1. δ1, δ3=$\frac{t_{bus(rec)(\min)}}{2\times t_{bit}}$
2. LIN bus load condition：(1) $C_{BUS}$=1nF, $R_{BUS}$=1kΩ；(2) $C_{BUS}$=6.8nF, $R_{BUS}$=660Ω；(3) $C_{BUS}$=10nF, $R_{BUS}$=500Ω
3. δ2, δ4=$\frac{t_{bus(rec)(\max)}}{2\times t_{bit}}$

### 7.5.5. Thermal Shutdown

| PARAMETER | | TEST CONDITIONS | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $T_{th(act)otp}$ [1] | Thermal shutdown temperature | | 150 | 175 | 200 | ℃ |
| $T_{th(rel)otp}$ [1] | Thermal shutdown temperature recovery | | | 20 | | ℃ |

**Note：**

1. The test data is based on bench test and design simulation.

### 7.5.6. Switching Characteristics

| PARAMETER | | TEST CONDITIONS | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_{rx\_pd}$ | Receiver propagation delay | Riseand fall, $C_{RXDx}$=20pF, $R_{RXDx}$=2.4kΩ | | | 6 | μs |
| $t_{rx\_sym}$ | Receiver propagation delay symmetry | | -2 | | 2 | μs |
| $t_{wake(dom)LIN}$ | LIN dominant wake-up time | Sleep mode | 30 | 80 | 150 | μs |
| $t_{gotonorm}$ | Go to normal time | | 2 | 6 | 10 | μs |
| $t_{init(norm)}$ [1] | Normal mode initialization time | | | 12 | | μs |
| $t_{gotosleep}$ | Go to sleep time | | 2 | 6 | 10 | μs |
| $t_{to(dom)TXD}$ | TXD-dominant timeout | $V_{TXDx}$=0V | 6 | 12 | 50 | ms |

**Note：**

1. The test data is based on bench test and design simulation.

## 8. Parameter Measurement Information

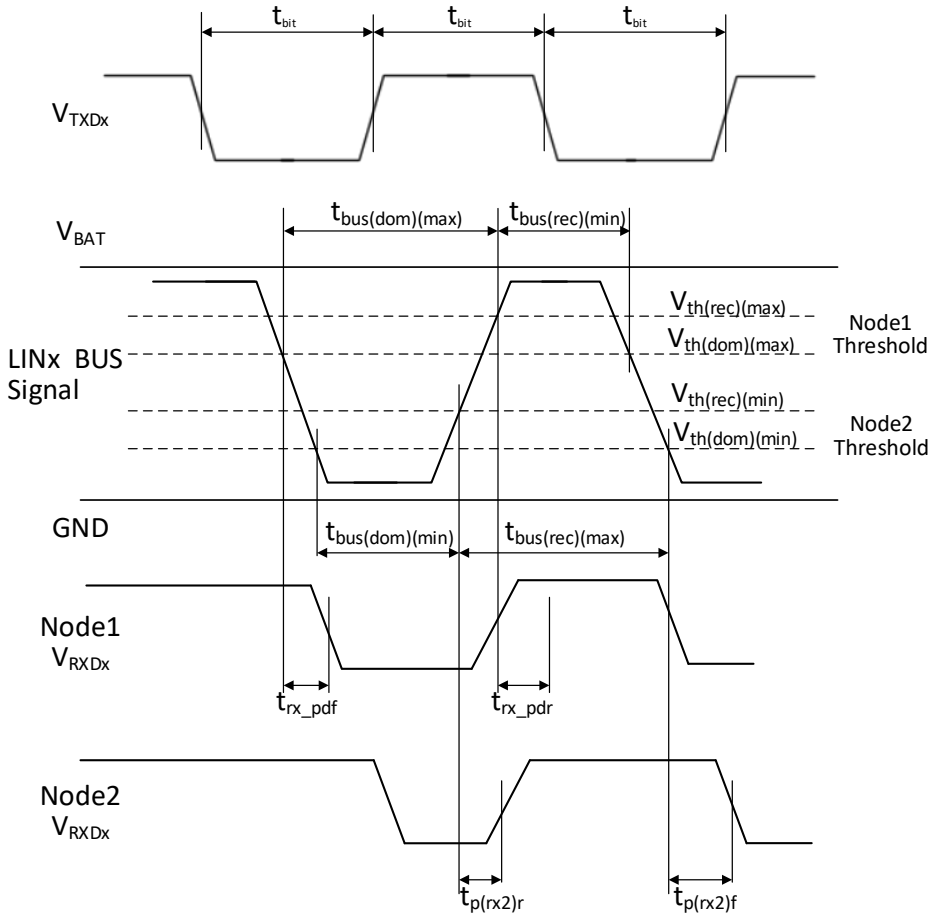



**Figure8- 1. LIN Bus Transmission Timing Diagram**

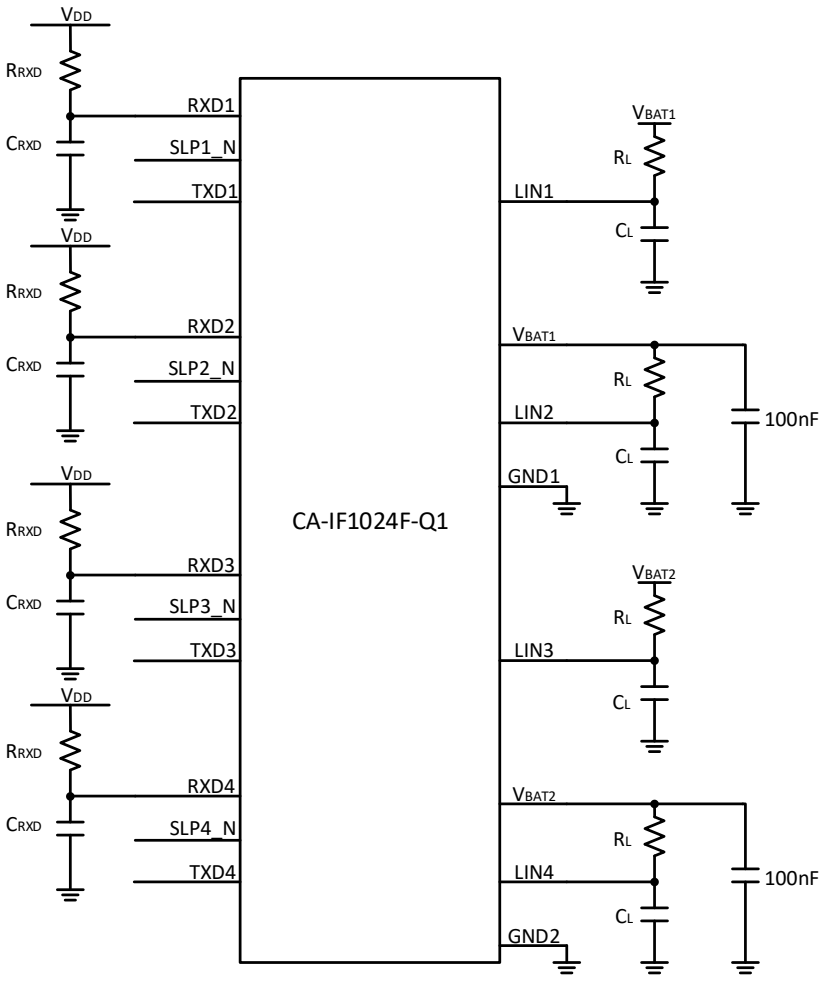



**Figure8- 2. Switch characteristic testing circuit**

# 9. Detailed Description

## 9.1. Overview

CA-IF1024F-Q1 is a four channel erface chip used between LIN protocol controllers and physical buses. It can be applied in fields such as trucks, buses, cars, and industrial control, with a transmission rate of up to 20kbps. CA-IF1024F-Q1 is divided into two independently controlled dual channel LIN transceiver modules based on LIN1/LIN2 and LIN3/LIN4. It is powered by two power sources, $V_{BAT1}$ and $V_{BAT2}$, and has independent logic control circuits, power on detection circuits, and over temperature protection circuits, respectively.

CA-IF1024F-Q1 receives the sending data stream from the protocol controller at the sending data input (TXDx) end and converts it into a bus signal with the best swing rate and waveform shaping; The input data on the LINx bus is output from the RXDx port of the receiver to an external microcontroller. This device is compatible with the "LIN 2. x/ISO 17987-4:2016/SAE J2602" standard.

The internal of the TXDx pin is pulled down to the ground to prevent the undefined floating state of the TXDx pin.

The internal of the SLPx_N pin is pulled down to the ground, and the corresponding LIN transceiver will enter the sleep mode when the SLPx_N pin is floating.

Pins RXD1 and RXD2 are set floating if $V_{BAT1}$ is disconnected. Pins RXD3 and RXD4 are set floating if $V_{BAT2}$ is disconnected.

The loss-of-ground condition has no effect on the bus port, and the bus port has no reverse current.

To avoid the effects caused by TXDx pins being forced to permanently low due to hardware and/or software application failures, after switching to normal mode, the LINx driver will be enabled only if a high TXDx level is detected.

## 9.2. Short-circuit Protection

When the LINx bus output of the driver is short circuited to VBATx or GNDx, the current is limited. When the LINx bus is short circuited to VBATx, the short-circuit current will be limited to $I_{BUS\_LIM}$; When the LINx bus is short circuited to GNDx, the short-circuit current will be limited to VBATx/Slave.

## 9.3. Thermal Shutdown

CA-IF1024F-Q1 has an over temperature protection function. When a dual channel module inside the device exceeds the shutdown protection temperature Tj (sd), the over temperature protection circuit will turn off the output driver (LIN1/LIN2 or LIN3/LIN4) of the corresponding module. The drivers are enabled again when the junction temperature falls below $T_{jd(sd)}$-$T_{jd(hys)}$ and pin TXDx is HIGH.

## 9.4. Dominant timeout

The CA-IF1024F-Q1 family of devices features a transmitter-dominant timeout($t_{to(dom)TXD}$) that prevents erroneous LIN controllers from clamping the bus to a dominant level by maintaining a permanently low TXD signal. When TXD remains in the dominant state (low) for longer than $t_{to(dom)TXD}$, the transmitter is disabled, releasing the bus to a recessive state. After a dominant timeout fault, the transmitter is re-enabled when receiving a rising edge driving TXD. The transmitter-dominant timeout limits the minimum possible data rate.

## 9.5. Operate modes

The CA-IF1024F-Q1 supports four operating modes: Normal, Standby, Sleep and Reset ,See Figure9- 1 for more details about the CA-IF1024F-Q1 operating modes.

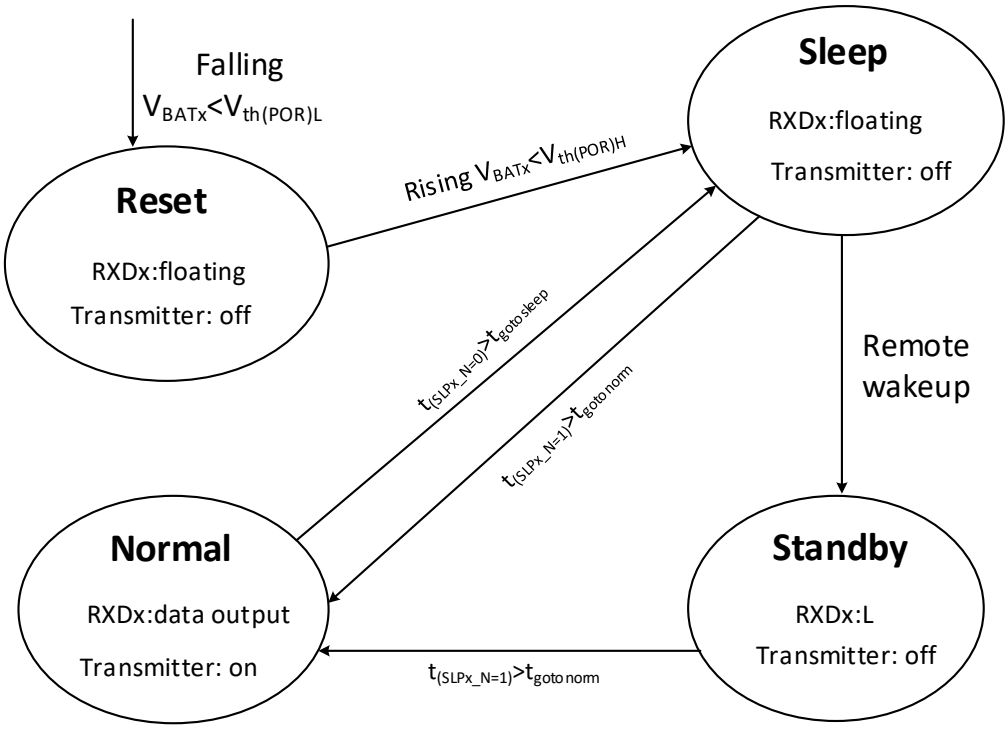



**Figure9- 1. State Diagram**

**Sleep mode:**

CA-IF1024F-Q1 has very low static power consumption when all LIN transceivers of four channels enter sleep mode, but it can still remotely wake up the corresponding channel to enter standby mode through LINx pin, or directly switch to normal mode by pulling up SLPx_N pin.

In order to prevent the CA-IF1024F-Q1 from waking up due to unexpected wake up events caused by car transient or EMI, filters are designed at the inputs LINx pin and SLPx_N pin of the receiver.

In normal mode, when SLPx_N pin has a falling edge and SLPx_N remains low for longer than $t_{gotosleep}$, the LIN transceiver of the corresponding channel of CA-IF1024F-Q1 enters the sleep mode.

The necessary conditions for CA-IF1024F-Q1 to be woken up in sleep mode are as follows: the remote wake-up time through LINx pin must be longer than twake(dom)LIN (dominant wake time of bus); The direct wake-up time through the SLPx_N pin must be longer than the $t_{gotonorm}$.

**Standby mode:**

Standby mode is also a low-power mode of CA-IF1024F-Q1 and is a transitional mode between sleep mode and normal mode. When CA-IF1024F-Q1 is in sleep mode, if a remote wake-up event is detected, the device will immediately enter standby mode, and the low level on the RXDx pin will indicate that the wake-up event has occurred.

**Normal mode:**

In Normal mode, the TJA1024 can transmit and receive data via the LIN bus lines. The transceivers operate independently, so one can be active while the others are off.

The receiver detects the data stream on the LIN bus and outputs it to the microcontroller via pin RXDx, and the high level of bus represents recessive and low level represents dominant. TXDx is the output of the driver, the data stream from protocol controller sent by TXDx to LINx pin output and waveform shaping to minimize electromagnetic radiation emission (EME).

In sleep or standby mode, as long as the high level hold time on the SLPx_N pin is longer than the $t_{gotonorm,}$ the LIN transceiver of the corresponding channel will enter the normal mode. If the low level hold time on the SLPx_N pin is longer than $t_{gotosleep}$, the LIN transceiver on the corresponding channel switches to sleep mode.

**Reset mode:**

If the voltage on $V_{BAT}$ is less than the low-level reset threshold $V_{th(VBATL)L}$ when powering on, the CA-IF1024F-Q1 is in reset mode and all input and output functions are disabled; when the voltage on VBATx is longer than the high-level reset threshold $V_{th(VBATL)H}$, CA-IF1024F-Q1 enters sleep mode.

### 9.6. Remote Wake-up

The bus wake-up, also called remote wake-up, changes the transceiver's operation mode from Sleep mode to Standby mode. A falling edge on the LIN Bus, followed by a valid dominant bus signal for $t > t_{wake(dom)LIN}$, bus results in a bus wake-up event. A transition to Standby mode is performed with the subsequent rising edge on the LIN bus(the change from dominant to recessive), see Figure9- 2.

When an effective remote wake-up event occurs, the chip enters Standby mode and RXD is continuously low to send an interrupt request to the microcontroller.

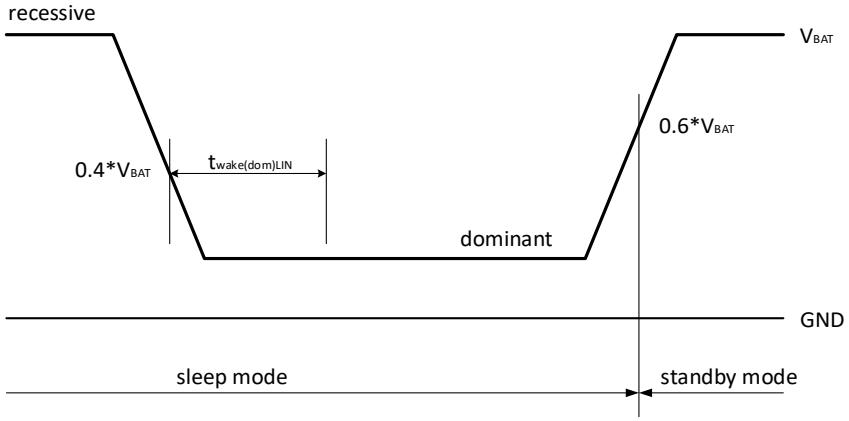



**Figure9- 2. Remote Wake-up**

## 10. Application Information

In multi-point LIN networking applications, the master node needs to use blocking diodes and 1k Ω resistors in series to pull up the bus. The slave node does not need these two devices, but can rely on internal chip pull-up. Usually, the main node bus is connected to ground with a 1nF capacitor, while the node bus is connected to ground with a 220pF capacitor.

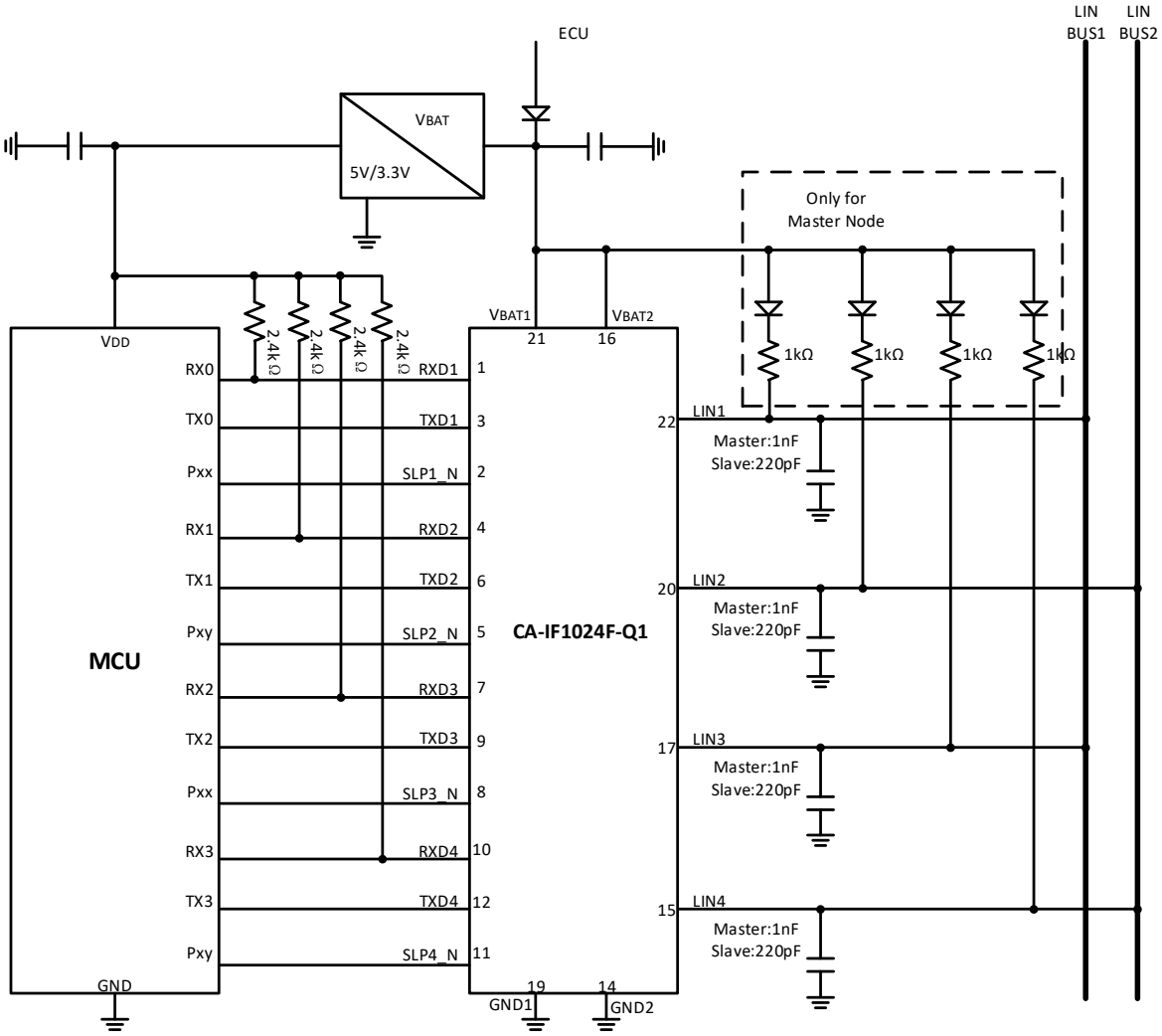



**Figure 10- 1. Typical Application Circuit in LIN Bus**

## 11. Package Information

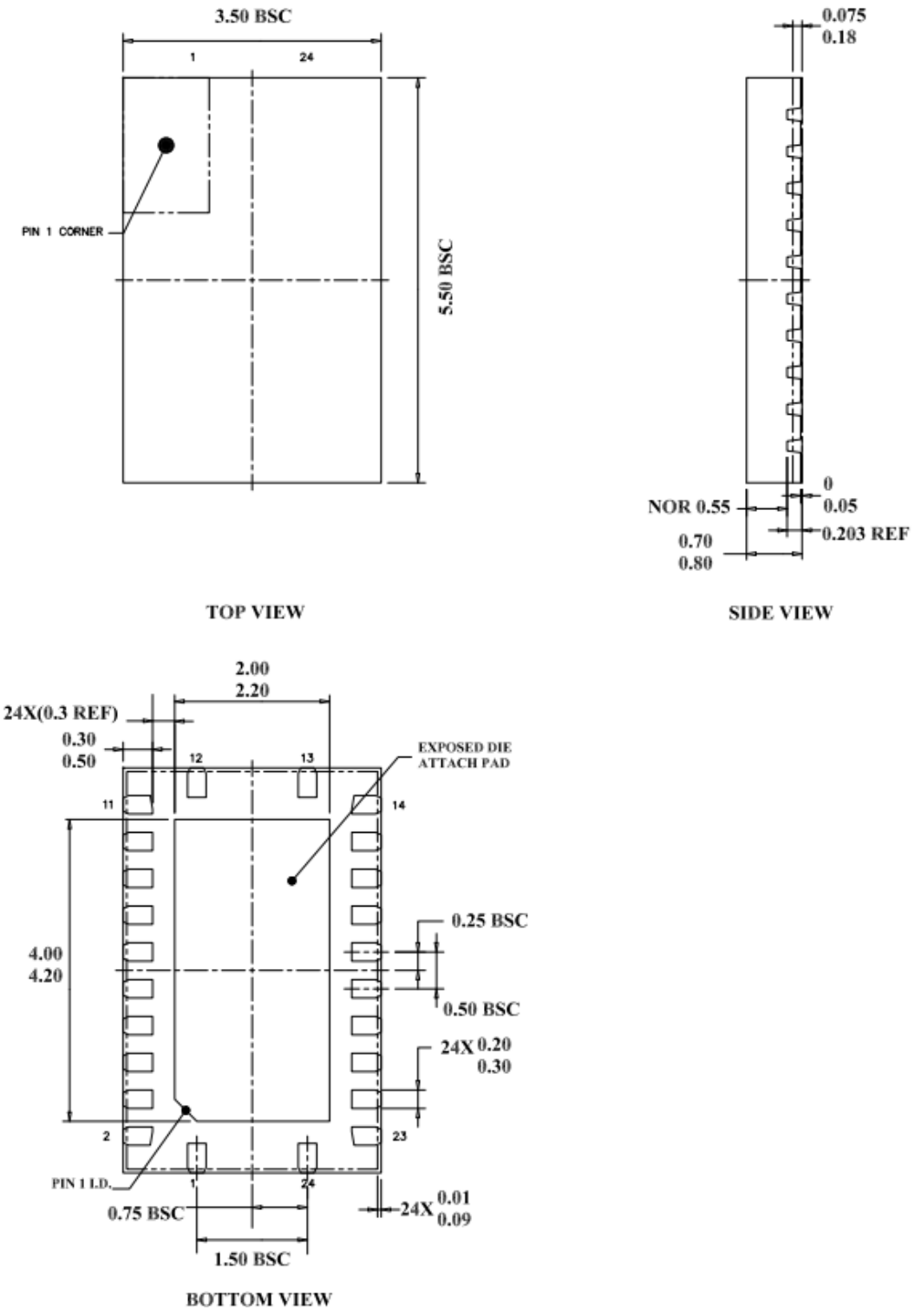



**Figure 11.QFN24 Package Outline**

## 12. Soldering Temperature (reflow) Profile

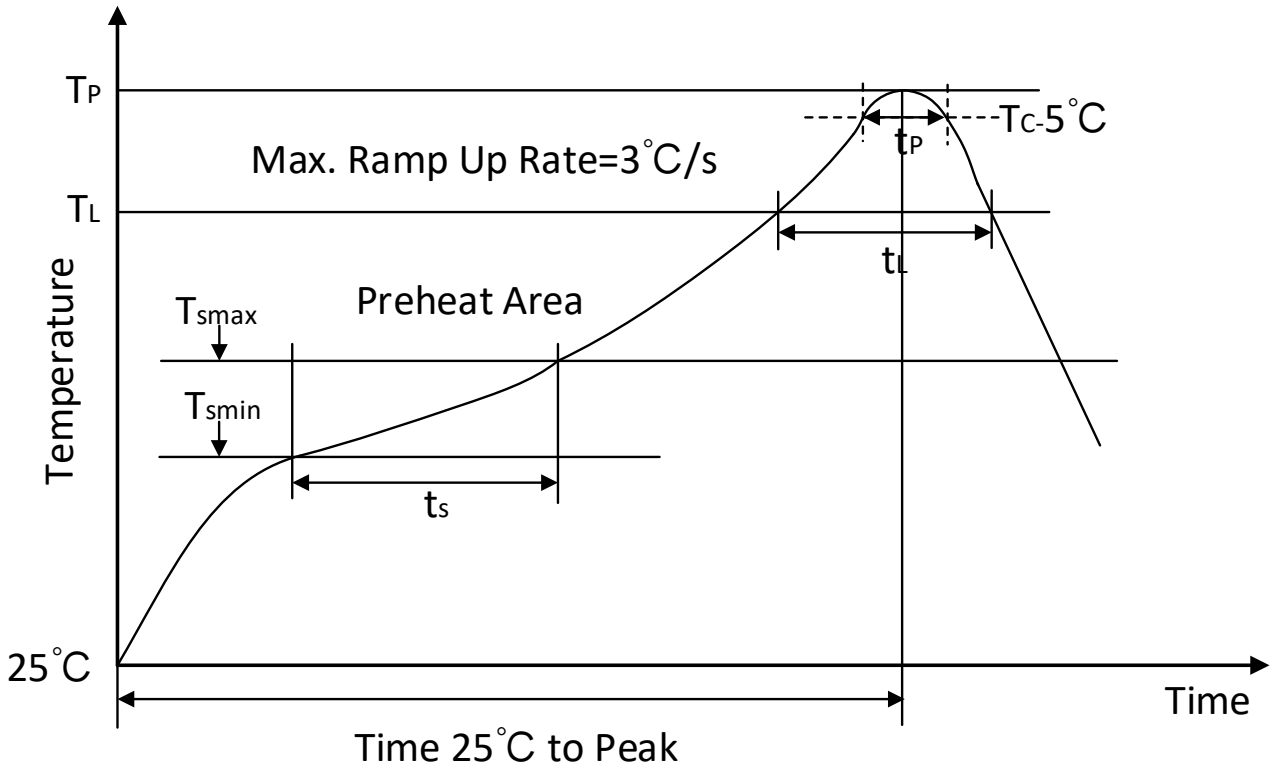


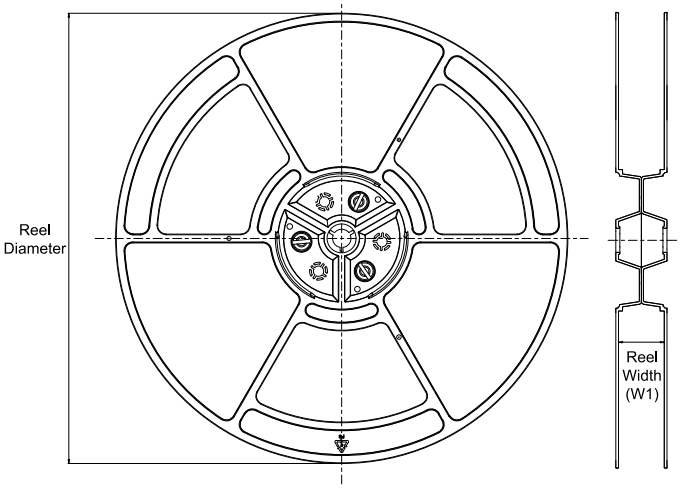

**Figure12- 1.** Soldering Temperature (reflow) Profile

**Table 12-1. Soldering Temperature Parameter**

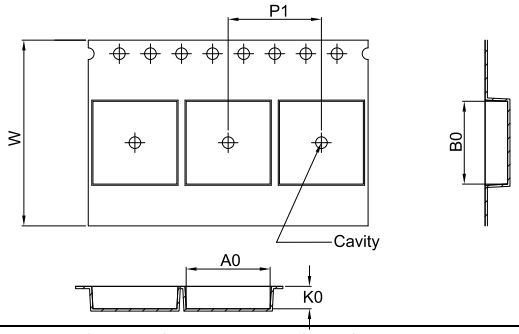
| Profile Feature | Pb-Free Assembly |
|---|---|
| Average ramp-up rate(217 ℃ to Peak) | 3℃/second max |
| Time of Preheat temp(from 150 ℃ to 200 ℃ | 60-120 second |
| Time to be maintained above 217 ℃ | 60-150 second |
| Peak temperature | 260 +5/-0 ℃ |
| Time within 5 ℃of actual peak temp | 30 second |
| Ramp-down rate | 6 ℃/second max. |
| Time from 25℃ to peak temp | 8 minutes max |

## 13. Tape and Reel Information

**REEL DIMENSIONS**

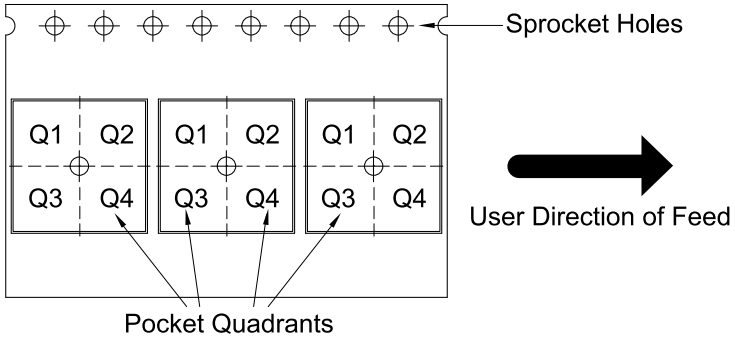



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **CA-IF1024F-Q1** | QFN | F | 24 | 3000 | 330 | 12.4 | 3.80 | 5.80 | 1.00 | 8.00 | 12.00 | Q1 |

## 14. Important Statement

The above information is for reference only and used for helping Chipanalog customers with design, research and development. Chipanalog reserves the rights to change the above information due to technological innovation without advance notice.

All Chipanalog products pass ex-factory test. As for specific practical applications, customers need to be responsible for evaluating and determining whether the products are applicable or not by themselves. Chipanalog's authorization for customers to use the resources are only limited to development of the related applications of the Chipanalog products. In addition to this, the resources cannot be copied or shown, and Chipanalog is not responsible for any claims, compensations, costs, losses, liabilities and the like arising from the use of the resources.

**Trademark information**

Chipanalog Inc.® and Chipanalog® are registered trademarks of Chipanalog.

**http://www.chipanalog.com**