CA-IF1043 Low-power, ±58V Fault Protected CAN Transceiver

1. Features

- **Meets the ISO 11898-2:2016 and ISO 11898-5:2007 physical layer standards**
- Support classic CAN and 5 Mbps CAN FD (flexible data rate)
- Short and fast loop propagation time
- Support high data rate in loaded CAN networks
- **Operation modes**
  - High-speed normal mode
  - Silent mode disables driver
  - Low-current standby mode
  - Low-power sleep mode
  - Support remote wake-up and local wake-up
- **Ideal passive behavior when unpowered**
  - Bus and logic terminals are high impedance (no load)
  - Power up/down with glitch free operation on bus and RXD output
- **Integrated protection increases robustness**
  - ±58V fault-tolerant CANH and CANL
  - ±30V extended common-mode input range (CMR)
  - Undervoltage protection on V_{CC}, V_{SUP} and V_{IO} supply terminals
  - Transmitter dominant timeout prevents lockup, data rates down to 5 kbps
  - Thermal shutdown protection(TSD)
  - CAN bus short-circuit detection and TXD to RXD short detection
  - Cold start-up detection (battery power-up first)
- 1.7 to 5.5V Logic-supply (V_{IO}) range, battery supply accepts up to 45V voltage
- –55°C to 150°C junction temperature range
- Available in SOIC14 and DFN14 packages
- AEC-Q100 Grade 1

2. Applications

- Industrial equipment
- Motor control
- Building automation
- Automotive gateway
- Advanced driver assistance systems (ADAS)

3. General Description

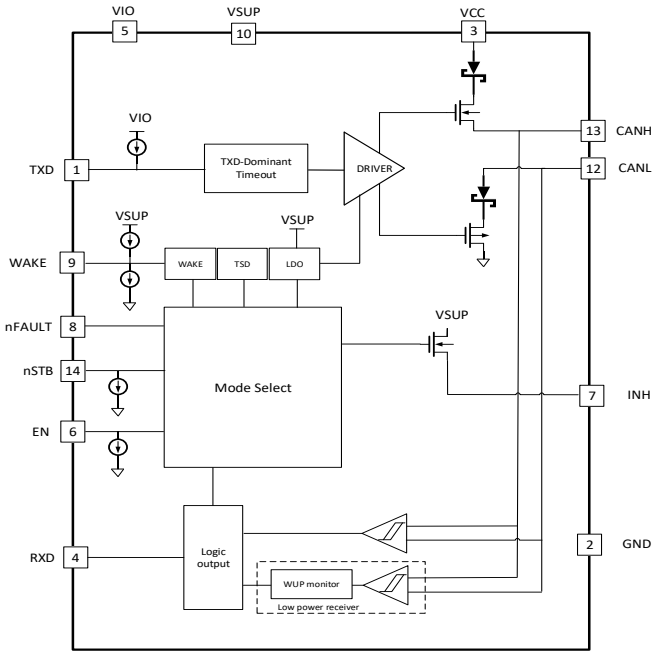
The CA-IF1043x devices are control area network (CAN) transceivers with integrated protection for industrial and automotive applications. These devices are designed for using in CAN FD networks up to 5 Mbps and feature ±58V extended fault protection on the CAN bus for equipment where overvoltage protection is required. This family of CAN transceivers also incorporate an input common-mode range(CMR) of ±30V, exceeding the ISO 11898 specification, well suited for applications where ground planes from different systems are shifting relative to each other.

The CA-IF1043x series devices include a dominant timeout to prevent bus lockup caused by controller error or by a fault on the TXD input. When the TXD remains in the dominant state (low) for longer than t_{DOM}, the driver is switched to the recessive state, releasing the bus and allowing other nodes to communicate. The transceivers feature standby (nSTB) and enable (EN) control pins for different modes of operation: normal operation and standby mode, silent mode, sleep mode for low current consumption, as well as wake-up capability over CAN bus or via the WAKE pin. Inhibit output (INH) can be used to control one or more external voltage regulators presented on a node to reduce the battery power consumption at system level. Also, the CA-IF1043x devices provide low level translation to simplify the interface with low voltage CAN controllers.

The CA-IF1043x family of devices is available in a standard 14-pin narrow-body SOIC package and 14-pin DFN package, operates over the -55°C to +150°C junction temperature range.

Device Information

Part number	Package	Package size(NOM)
CA-IF1043NF-Q1	SOIC14	3.9mm x 8.65mm
CA-IF1043DF-Q1	DFN14	3.0mm x 4.5mm



Simplified Block Diagram

4. Ordering Information

Table 4-1. Ordering Information

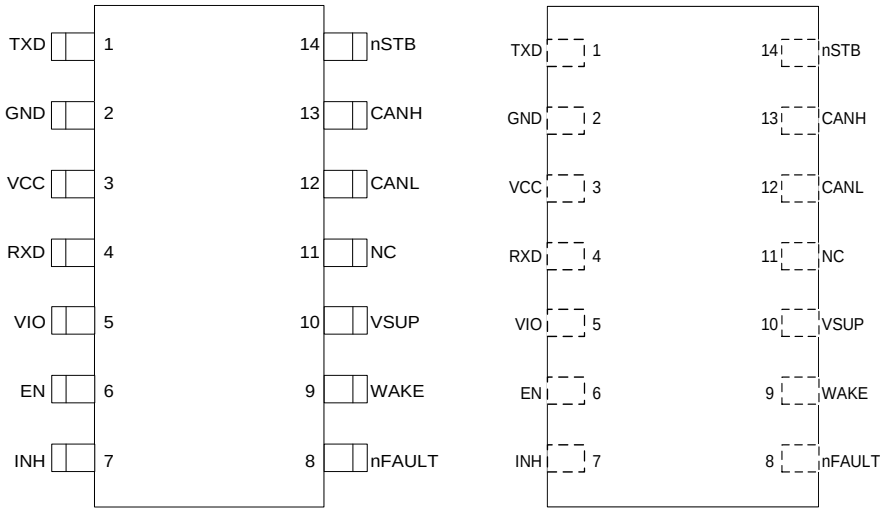
Part Number	Features	Package
CA-IF1043NF-Q1	With low level translation, automotive qualified	SOIC14
CA-IF1043DF-Q1	With low level translation, automotive qualified	DFN14

Contents

5. Revision History

Revision Number	Description	Page Changed
V1.0	N/A	N/A
V1.1	Add annotations to the mode state diagram	P21
V1.2	Updata the Unit of I_{SUP}	P6

6. Pin Configuration and Functions



SOIC14 DFN14

Figure6-1. CA-IF1043 Pin Configuration

Table 6-1. CA-IF1043 Pin Configuration and Description

Pin Name	Pin#	Type	Description
TXD	1	Digital I/O	Transmit Data Input. In normal operation, drive TXD high to set the driver in the recessive state; drive TXD low to set the driver in the dominant state； Internal pull-up resistance.
GND	2	GND	Ground.
VCC	3	Power	5V Supply Voltage. Bypass VCC to GND with an at least 0.1μF capacitor.
RXD	4	Digital I/O	Receive Data Output. In normal operation, RXD is low for dominant bus state and high for recessive bus state. The reference power supply for RXD is VIO
VIO	5	Power	Logic Supply Input. VIO input is the logic supply voltage for the logic input/output between the CAN transceiver and controller. V_{IO} allows full compatibility from +1.8V to +5.5V logic on all digital lines. Bypass VIO to GND with a 0.1μF capacitor. Connect VIO to VCC for +5V logic compatibility.
EN	6	Digital I/O	Enable control input with internal pull-down to GND. This is active-high input used with nSTB input to define the operation status of the transceiver in normal or low-power modes.
INH	7	High-voltage I/O	Inhibit Output. INH can be used to control external voltage regulators or/and microcontroller to reduce system power consumption.
nFAULT	8	Digital I/O	Fault Detected Indication. Stays high when fault is not detected.
WAKE	9	High-voltage I/O	Local Wake-up Input. Either a low-to-high (rising edge), or a high-to-low (falling edge) transition will generate a local wake-up event. Pull WAKE to ground or V_{SUP} to avoid unwanted wake-up events if not used.
VSUP	10	Power	Battery Supply Input.
NC	11	---	No internal connection.
CANL	12	Bus I/O	CAN bus line low.
CANH	13	Bus I/O	CAN bus line high.
nSTB	14	Digital I/O	Standby Mode Control with internal pull-down to GND. This is active-low input used with EN input to define the status of the transceiver in normal or low-power modes.

7. Specifications

7.1. Absolute Maximum Ratings

PARAMETER		MIN	MAX	UNIT
V_{SUP}	Battery supply voltage range	-0.3	+58	V
V_{CC}	5V bus supply voltage range	-0.3	+7	V
V_{IO}	Logic supply voltage range	-0.3	+7	V
V_{BUS}	CAN Bus I/O voltage range (CANH,CANL)	-58	+58	V
$V_{(DIFF)}$	Max differential voltage between CANH and CANL	-58	+58	V
$V_{(Logic\_Input)}$	Logic input terminal voltage range (TXD, nSTB, EN)	-0.3	+7	V
$V_{(Logic\_Output)}$	Logic output terminal voltage range (RXD)	-0.3	+7	V
V_{INH}	INH Output voltage range	-0.3	58 and ≤ V_{SUP}+0.3	V
$V_{(wake)}$	WAKE input voltage range	-58	+58	V
$I_{O(Logic)}$	Logic output current (RXD, nFAULT)		8	mA
$I_{O(INH)}$	INH output current		4	mA
$I_{O(WAKE)}$	WAKE input current		3	mA
T_J	Virtual junction temperature range	-55	150	℃

Note:

1. The stresses listed under “Absolute Maximum Ratings” are stress ratings only, not for functional operation condition. Exposure to absolute maximum rating conditions for extended periods may cause permanent damage to the device.

7.2. ESD Ratings

Parameters	TEST CONDITIONS		VALUE	UNIT
CA-IF1043NF-Q1，CA-IF1043DF-Q1				
HBM[1] ESD	Other pins		±4000	V
	CAN bus terminals (CANH, CANL) to GND		±8000	
CDM ESD	All pins		±1500	V
System Level ESD	CAN bus terminals (CANH, CANL) to GNaD	IEC 61000-4-2: unpowered contact discharge.	±6000[2]	V

Note:

1. Per JEDEC document JEP155, 500V HBM allows safe manufacturing of standard ESD control process.
2. The system CANH and CANL need to add TVS to GND.

7.3. Recommended Operating Conditions

PARAMETER		MIN	TYP	MAX	UNIT
V_{SUP}	Battery supply voltage range	4.5		45	V
V_{CC}	Supply voltage range	4.5		5.5	V
V_{IO}	Logic supply voltage range	1.8		5.5	V
$I_{OH(RXD)}$	RXD terminal high level output current	-2			mA
$I_{OL(RXD)}$	RXD terminal low level output current			2	mA
$I_{O(INH)}$	INH output current			2	mA
T_A	Ambient temperature	-40		125	℃

7.4. Thermal Information

Thermal Metric		SOIC14	DFN14	UNIT
$R_{\theta JA}$	Junction to Ambient	76.6	35.1	℃/W

7.5. Electrical Characteristics

Over recommended operating conditions, T_A = –40°C to 125°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER						
I_{SUP}	Battery Supply Current	Normal operation, silent mode, go to sleep		45	80	μA
		Standby mode, $V_{INH} = V_{(WAKE)} = V_{SUP}$		40	80	
		Sleep mode, $V_{CC} = V_{IO} = V_{INH} = 0V$, $V_{(WAKE)} = V_{SUP}$		35	70	
I_{cc}	5V Supply Current	TXD=0V, R_L = 60 Ω (dominant), see Figure 8- 1		48	70	mA
		TXD=0V, RL=50 Ohm(dominant), see Figure 8- 1		50	80	
		TXD=0V, CANH =-25V (dominant), see Figure 8- 1		84	110	
		TXD=V_{IO}, RL=50 Ohm (recessive), see Figure 8- 1		1.8	5	
		TXD = V_{IO}, R_L = 50 Ohm, silent mode, go to sleep.		1	2.5	μA
		Standby mode, EN=L[1], nSTB=L[1]		1.2	5	
		Sleep mode, EN=H[1] or L, nSTB =L[1]		2	5	
I_{IO}	I/O Supply Current	Normal operation(dominant), TXD=0V, nSTB=EN=V_{IO}		110	450	μA
		Normal operation(recessive), silent mode or go to sleep mode, TXD=V_{IO}		3.5	5	
		Sleep mode, nSTB = L[1]		3	5	
V_{uv_SUP}	V_{SUP} UVLO Threshold	Rising	2.5	3.65	4.2	V
$V_{HYS(UVSUP)}$	VSUP UVLO Threshold	Hysteresis		50		mV
V_{uv_vcc}	V_{CC} UVLO Threshold	Rising		4.1	4.45	V
$V_{HYS(vcc)}$	V_{CC} UVLO Threshold	Hysteresis		200		mV
V_{UV_IO}	V_{IO} UVLO Threshold	Rising	1.4	1.56	1.7	V
$V_{HYS(UVIO)}$	V_{IO} UVLO Threshold	Hysteresis		80		mV
LOGIC INTERFACE (Mode select input, nSTB, EN)						
V_{IH}	High-level input voltage		0.7xV_{IO}			V
V_{IL}	Low-level input voltage				0.3xV_{Io}	V
I_{IH}	High-level input leakage current	nSTB = EN = V_{CC} = V_{IO} = 5.5V	20		200	μA
I_{IL}	Low-level input leakage current	nSTB = EN = 0V, V_{CC} = V_{IO} = 5.5V	-1		1	μA
$I_{lek(off)}$	Unpowered leakage current	nSTB = EN = 5.5V, V_{CC} = V_{IO} = 0V	-1		1	μA
LOGIC INTERFACE (CAN transmit data input, TXD)						
V_{IH}	High-level input voltage		0.7xV_{Io}			V
V_{IL}	Low-level input voltage				0.3xV_{Io}	V
I_{IH}	High-level input leakage current	TXD = V_{CC} = V_{IO} = 5.5V	-2.5	0	1	μA
I_{IL}	Low-level input leakage current	TXD = 0V, V_{CC} = V_{IO} = 5.5V	-200		20	μA
$I_{lek(off)}$	Unpowered leakage current	TXD = 5.5V, V_{CC} = V_{IO} = 0V	-1	0	1	μA
C_i[2]	Input capacitance			5		pF
LOGIC INTERFACE (CAN receive data output, RXD)						
V_{OH}	High-level output voltage	Io = -2mA, see Figure 8- 2	0.8xV_{Io}			V
V_{OL}	Low-level output voltage	Io = +2mA, see Figure 8- 2		0.22	0.2xV_{Io}	V
$I_{lek(off)}$	Unpowered leakage current	RXD = 5.5V, V_{CC} = 0V, V_{IO}=0V	-1	0	1	μA

LOGIC INTERFACE (nFAULT output)						
V_{OH}	High-level output voltage	Io = -2mA, see Figure 8- 2	$0.8xV_{Io}$			V
V_{OL}	Low-level output voltage	Io = +2mA, see Figure 8- 2			$0.2xV_{Io}$	V
$I_{lek(off)}$	Unpowered leakage current	nSTB = 5.5V, V_{CC} = 0V, V_{IO}=0V	-1	0	1	μA
INH INTERFACE (INH output)						
ΔV_H	High level voltage drop, INH to V_{SUP}	I_{INH}=-1mA,			2	V
$V_{LKG(INH)}$	Leakage current	INH = 0V, sleep mode	-2		2	μA
Io(sc)	Short-circuit current	V_{INH} = 0V	-26			mA
WAKE INTERFACE (WAKE input)						
V_{IH}	High-level input	Standby mode and sleep mode	V_{SUP}-1.4			V
V_{IL}	Low-level input	Standby mode and sleep mode			V_{SUP}-3.2	V
I_{IH}	High-level input leakage current	WAKE=V_{SUP}-1V	-25	-15		μA
I_{IL}	Low-level input leakage current	WAKE = 1V		15	25	μA
CAN BUS DRIVER						
$V_{O(DOM)}$	Bus output voltage (dominant)	Normal operation, TXD = L[1], R_L=50 -65 Ω, C_L=open, R_{CM}=open, CANH, see Figure 8- 1	2.75		4.5	V
		Normal operation, TXD = L[1], R_L = 50 -65 Ω, C_L=open, R_{CM}=open, CANL, see Figure 8- 1	0.5		2.25	V
$V_{OD(DOM)}$	Bus output differential voltage (dominant)	TXD = L[1], R_L=60 Ohm , R_{CM} =165 Ohm, -5V≤V_{CM} ≤+10V, see Figure 8- 1	1.5		3.0	V
		TXD = L[1], R_L=45-70 Ohm , R_{CM} open, see Figure 8- 1	1.4		3.3	
		TXD = L[1], R_L=50-65 Ohm , R_{CM} open, see Figure 8- 1	1.5		3.0	
		TXD = L[1], R_L=2240 Ohm , R_{CM} open, see Figure 8- 1	1.5		5.0	
$V_{O(REC)}$	Bus output voltage (recessive)	TXD = H[1], R_L=open, R_{CM}=open, CANH, CANL, see Figure 8- 1	2		3	V
$V_{OD(REC)}$	Bus output differential voltage (recessive)	TXD = H[1], R_L=60 Ω, see Figure 8- 1	-120		12	mV
		TXD = H[1], no load, see Figure 8- 1	-50		50	mV
$V_{O(STB)}$	Bus output at standby mode	EN=L[1], nSTB=L, R_L open, R_{CM} open, CANH	-0.1		0.1	V
		EN=L[1], nSTB=L[1], R_L open, R_{CM} open, CANL	-0.1		0.1	V
		EN=L[1], nSTB=L[1], R_L open, R_{CM} open, CANH-CANL	-0.2		0.2	V
$I_{OS(SS\_DOM)}$	Short-circuit current (dominant)	TXD = L[1], CANL open, V_{CANH}= -5V to 40V, see Figure 8- 7	-100			mA
		TXD = L[1], CANH open, V_{CANL} = -5V to 40V, see Figure 8- 7			100	
$I_{OS(SS\_rec)}$	Short-circuit current (recessive)	TXD = H[1], V_{BSU} = CANH = CANL = -27V to 32V, see Figure 8- 7	-6		6	mA
V_{SYM} [2]	Transient symmetry (dominant or recessive)	R_L = 60 Ω, R_{CM} open, C_{split}=4.7nF, R_{CM} open , TXD = 250kHz, 1MHz, 2.5M Hz, see Figure 8- 1	0.9		1.1	V/V
V_{SYM_DC}	DC Output symmetry (dominant or recessive)	RL =60 Ω, R_{CM} open, see Figure 8- 1	-0.4		0.4	V
CAN RECEIVER						
V_{CM}	Common-mode input range	CANH or CANL to GND, RXD output valid, see Figure 8- 2	-30		+30	V
V_{IT}	Input differential threshold voltage	Normal mode, V_{CM} from -20V to 20V, see Figure 8- 2	0.5		0.9	V
		Normal mode, V_{CM} from -30V to 30V, see Figure 8- 2	0.4		1.0	V
$V_{IT(STB)}$	Input differential threshold @	EN=L[1], nSTB=L[1], V_{CM} = -20V to 20V,	0.4		1.15	V

	standby	see Figure 8- 2			
V_{DIFF_D}	Differential input threshold (dominant)	Normal operation, V_{CM} = -20V to 20V, see Figure 8- 2	0.9	9	V
V_{DIFF_R}	Differential input threshold (recessive)	Normal operation, V_{CM} = -20V to 20V, see Figure 8- 2	-4	0.5	V
$V_{DIFF\_D(STB)}$	Differential input threshold (dominant)	Standby mode, EN= nSTB=L[1], V_{CM} = -20V to 20V, see Figure 8- 2	1.15	9	V
$V_{DIFF\_R(STB)}$	Differential input threshold (recessive)	Standby mode, EN=nSTB=L[1], V_{CM} = -20V to 20V, see Figure 8- 2	-4	0.4	V
$V_{DIFF\_(HYST)}$	Differential input threshold hysteresis	Normal operation	100		mV
R_{IN}	CANH/CANL input resistance	TXD = H[1], V_{CM} = -30V to 30V	10	45	kΩ
R_{DIFF}	Differential input resistance	TXD = H[1], V_{CM} = -30V to 30V	20	90	kΩ
$R_{DIFF\ (M)}$	Input resistance matching	V_{CANH} = V_{CANL} =5V	-2	2	%
I_{LKG}	Input Leakage Current	V_{IO} = V_{CC} = 0V, V_{CANH} = V_{CANL} =5V		5	μA
C_{IN} [2]	Input capacitance	CANH or CANL to GND, TXD=V_{CC}, V_{IO} = V_{CC}	20		pF
C_{IN_DIFF} [2]	Differential input capacitance	CANH to CANL, TXD = H[1]	10		pF
Devices					
T_{TSD} [2]	Thermal shutdown temperature		190		℃
T_{TSD_HYS} [2]	Thermal shutdown temperature threshold hysteresis		10		℃

Notes:
1. L = Low-level, H = High-level.
2. The test data is based on bench test and design simulation.

7.6. Switching Characteristics

Over recommended operating conditions, T_A = –40°C to 125°C (unless otherwise noted).

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DRIVER						
t_R	Differential output rise time	R_L=60 Ohm,C_L=100pF, see Figure 8- 1		45		ns
t_F	Differential output fall time	R_L=60 Ohm,C_L=100pF, see Figure 8- 1		45		ns
t_{ONTXD}	TXD propagation delay (recessive to dominant)	R_L=60Ω, C_L=100pF, see Figure 8- 1		50		ns
t_{OFFTXD}	TXD propagation delay (dominant to recessive)	R_L=60Ω, C_L=100pF, see Figure 8- 1		40		ns
Tsk(p)	Pulse skew	R_L=60ohm,C_L=100pF, see Figure 8- 1		10		ns
T_{TXD_DTO}	TXD dominant Timeout	R_L=60 Ω, C_L open, see Figure 8- 5	2	5	8	ms
RECEIVER						
t_{ONRXD}	RXD propagation delay (recessive to dominant)	nSTB=VIO, C_L=15pF, see Figure 8- 2		80		ns
t_{OFFRXD}	RXD Propagation delay (dominant to recessive)	nSTB=VIO, C_L=15pF, see Figure 8- 2		80		ns
t_R	RXD output rise time	nSTB=VIO ,C_L=15pF, see Figure 8- 2		8		ns
t_F	RXD output fall time	nSTB=VIO ,C_L=15pF, see Figure 8- 2		8		ns
t_{BUS_DOM}	BUS Dominant time-out time	R_L=60 Ohm, C_L open	2	5	8	ms
t_{CBF}	Bus fault detection time	45 Ohm < R_{CM} <70 Ohm	1.9			μs
WAKE INPUT						
t_{wake_HT}	WAKE hold time	R_L=60 Ohm, C_L =100pF, C_L (RXD)=15pF, see Figure 8- 10	5		50	μs
DEVICE						
t_{loop1}	Total loop delay, driver input (TXD) to receiver output (RXD), recessive to dominant	R_L=60 Ω,C_{LD}=100pF, C_L=15pF, see Figure 8- 3		155	210	ns

t_{loop2}	Total loop delay, driver input (TXD) to receiver output (RXD), dominant to recessive	R_L=60 Ω,C_{LD}=100pF, C_L=15pF, see Figure 8- 3		155	210	ns
T_{mode1}	Mode change time, from sleep to normal or silent	see Figure 8- 4			50	µs
T_{mode2}	Mode change time, from normal to silent	see Figure 8- 8			20	µ s
t_{UV_VCC}	V_{CC} UVLO detection time	From UVLO to standby mode			30	µs
t_{UV_VIO}	V_{IO} UVLO detection time	From UVLO to standby mode			60	µs
t_{UV_VSUP}	V_{SUP} UVLO detection time	From UVLO to protection mode			120	µs
$t_{UV\_long(VCC\&VIO)}$ [2]	V_{CC}&V_{IO} UVLO timeout detection	From UVLO to sleep mode	150		350	ms
t_{POWER_UP}	V_{SUP} power-up	See Figure 8- 9		250	1000	µs
t_{rec_VCC}	V_{CC} UVLO recovery time				100	µs
t_{rec_VIO}	V_{IO} UVLO recovery time				50	µs
t_{wk_FILTER}	Filter time for a valid wake-up pattern	See Figure 10- 4.	0.5		1.8	µs
$t_{WK\_TIMEOUT}$	Bus wake-up timeout	See Figure 10- 4.	0.5		6	ms
t_{start_RXD}	RXD start-up time	RXD start-up time after remote wake-up	2		50	µs
t_{start_INH}	INH start-up time	INH start-up time after remote wake-up	2		50	µs
$t_{H(go-to-sleep)}$	Minimum hold time for transition to sleep mode	nSTB=L[1], EN=H[1]	20		50	µs
$t_{mode-nFAULT}$	nFAULT response time	nFAUlT response time after mode changing			20	µs
FD TIMING						
$t_{bit(bus)}$	Bit time on CAN bus output pins with $t_{BIT(TXD)}$ = 500 ns	nSTB = VIO, R_L = 60 Ω, C_L=100pF, C_{LRXD}=15pF, see Figure 8- 6	450		530	ns
$t_{bit(bus)}$	Bit time on CAN bus output pins with $t_{BIT(TXD)}$ = 200 ns	nSTB=VIO, R_L = 60 Ω, C_L=100pF, C_{LRXD}=15pF, see Figure 8- 6	155		210	ns
$t_{bit(rxd)}$	Bit time on RXD output pins with $t_{BIT(TXD)}$ = 500 ns	nSTB=VIO, R_L = 60 Ω, C_L=100pF, C_{LRXD}=15pF, see Figure 8- 6	400		550	ns
$t_{bit(rxd)}$	Bit time on RXD output pins with $t_{BIT(TXD)}$ = 200 ns	nSTB=VIO, R_L = 60 Ω, C_L=100pF, C_{LRXD}=15pF, see Figure 8- 6	120		220	ns
t_{rec}	Receiver timing symmetry with $t_{BIT(TXD)}$ = 500ns	nSTB=VIO, R_L = 60 Ω, C_L=100pF, C_{LRXD}=15pF, see Figure 8- 6	-50		20	ns
t_{rec}	Receiver timing symmetry with $t_{BIT(TXD)}$ = 200ns	nSTB=VIO, R_L = 60 Ω, C_L=100pF, C_{LRXD}=15pF, see Figure 8- 6	-45		15	ns

Notes:

1. L = Low-level, H = High-level.
2. The test data is based on bench test and design simulation.

8. Parameter Measurement Information

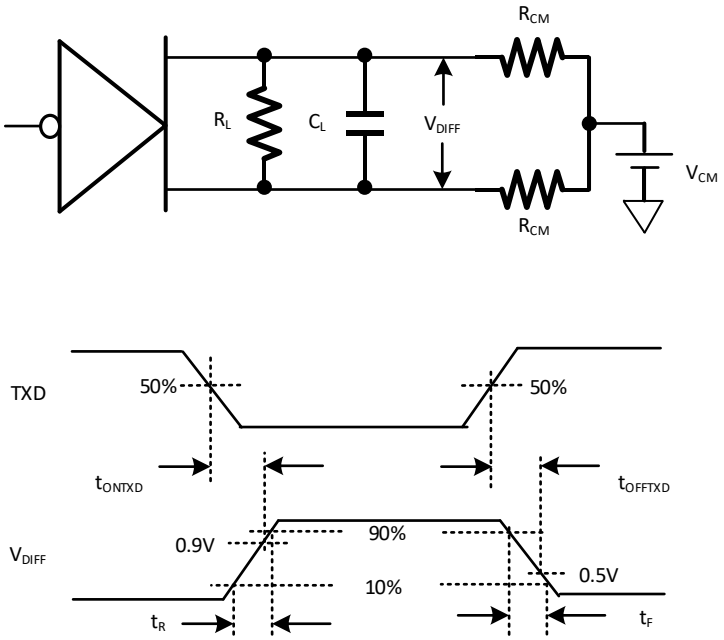


Figure 8- 1. Driver Test Circuit and Timing Diagram

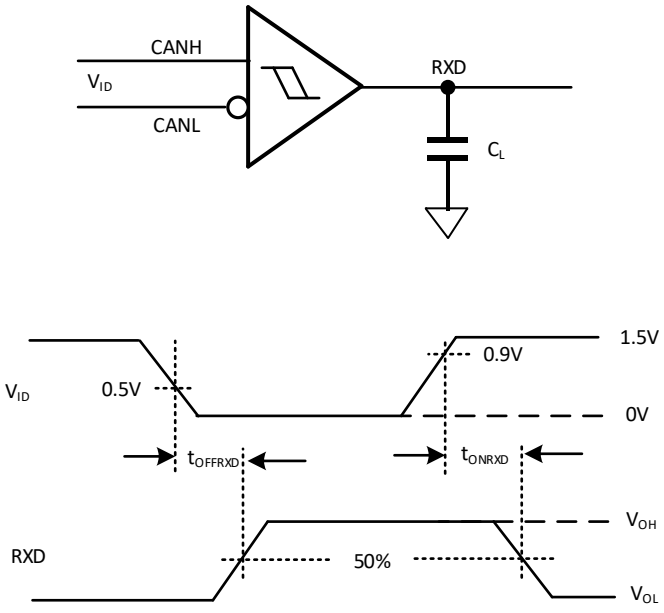


Figure 8- 2. Receiver Test Circuit and Measurement

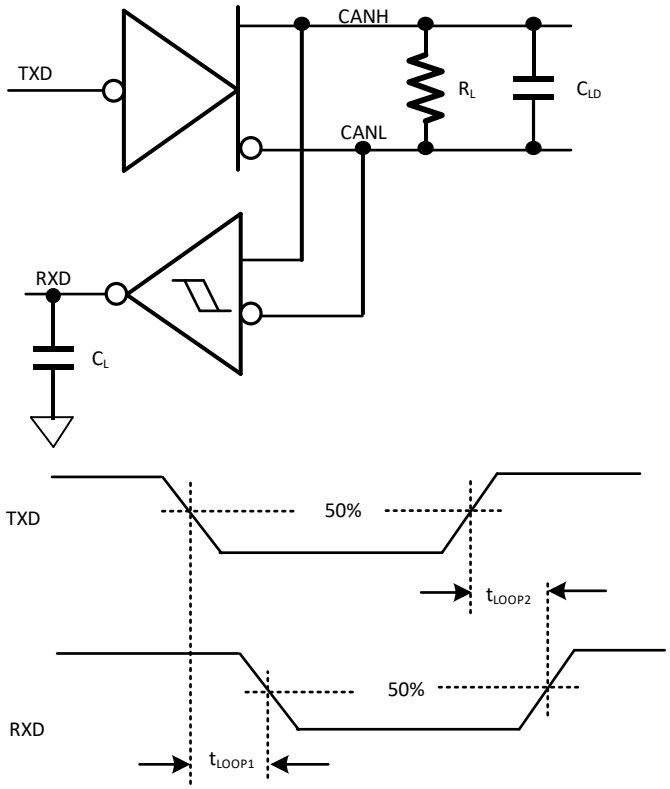


Figure 8- 3. TXD to RXD Loop Delay

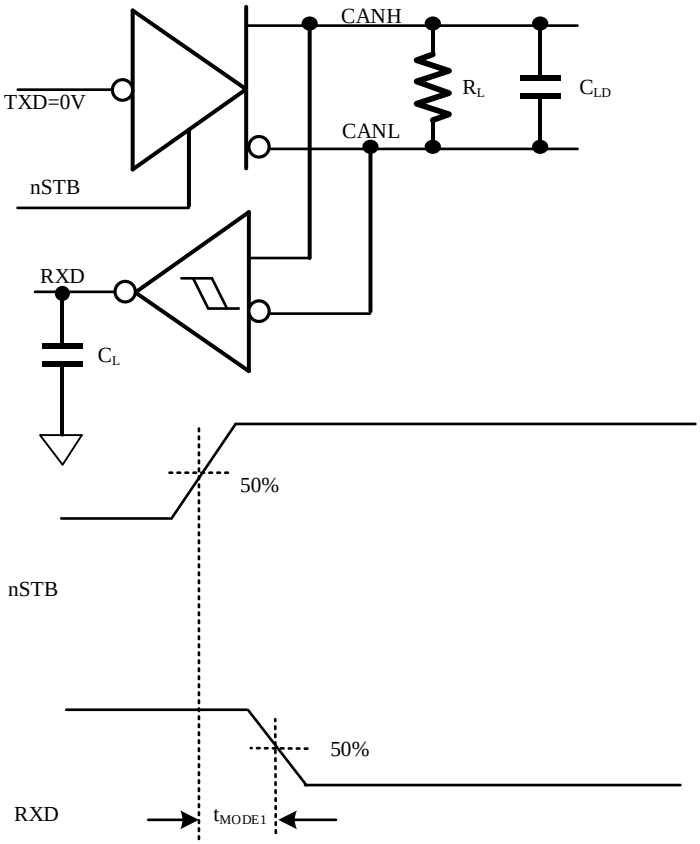


Figure 8- 4. Silent Mode to Normal Mode Test Circuit and Measurement

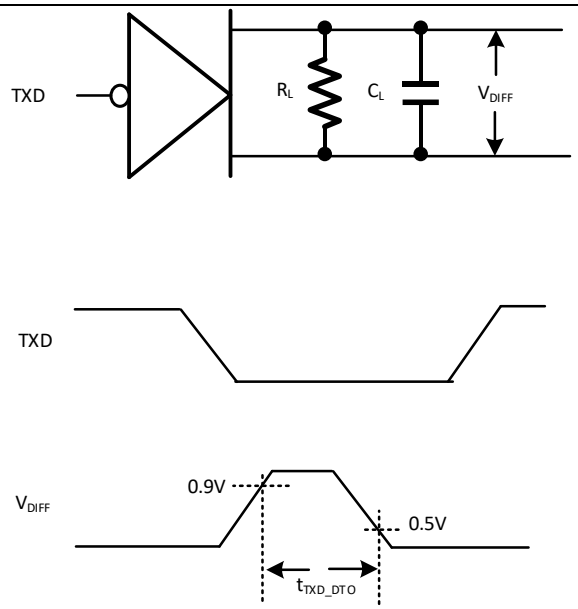


Figure 8- 5. TXD Dominant Timeout Test Circuit and Measurement

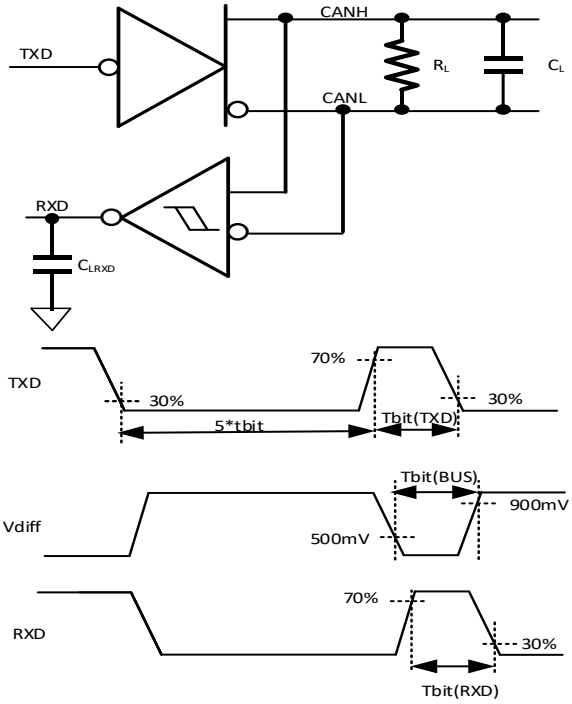


Figure 8- 6. CAN FD Timing Parameter Measurement

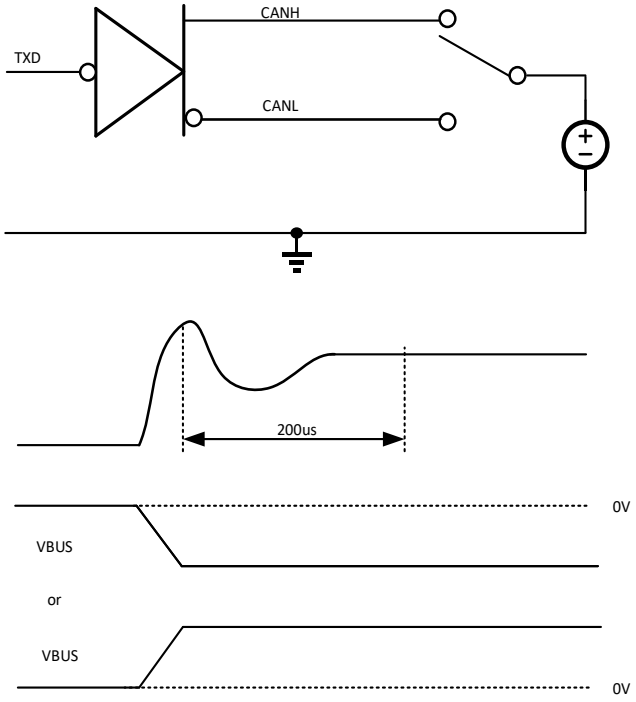


Figure 8- 7. Driver Short Circuit Current Test Circuit and Measurement

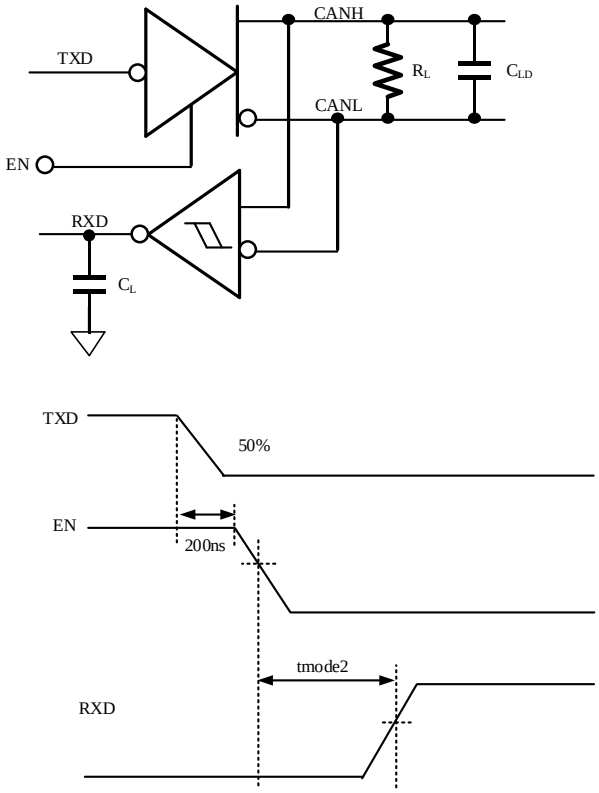


Figure 8- 8. Normal Mode to Silent Mode Test Circuit and Measurement

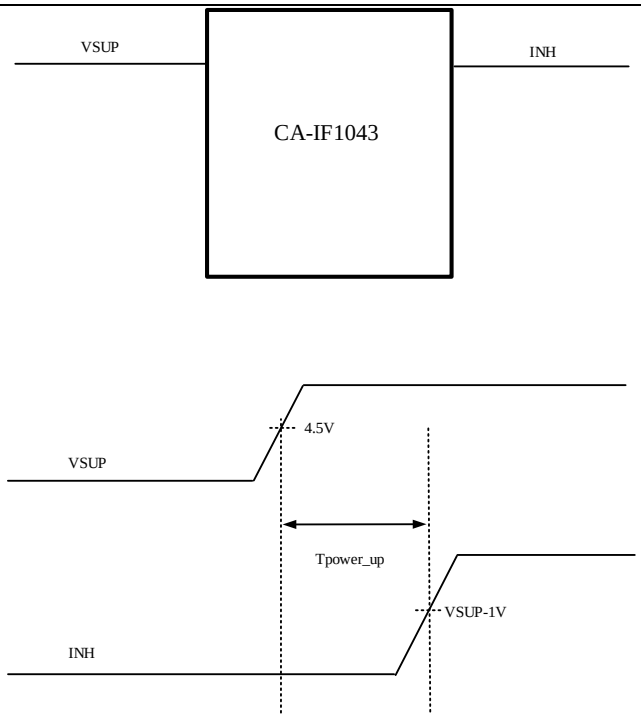


Figure 8- 9. Power-up Timing Diagram

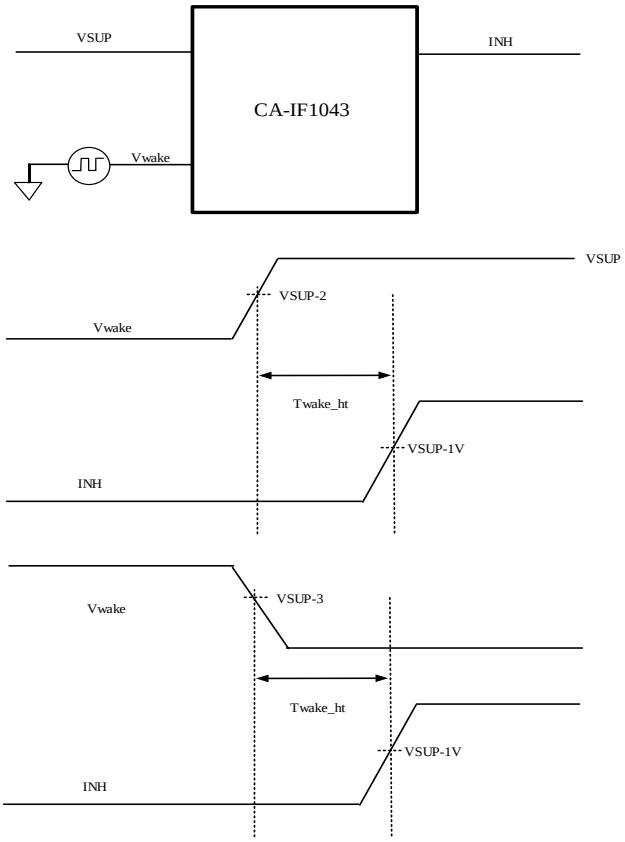


Figure 8- 10. INH Response

9. Typical Operating Characteristics and Waveforms

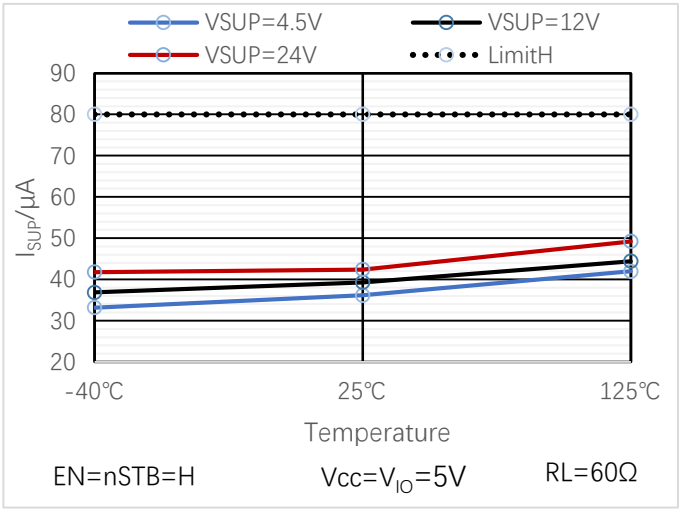


Figure 9-1 ISUP Normal mode, Dominant

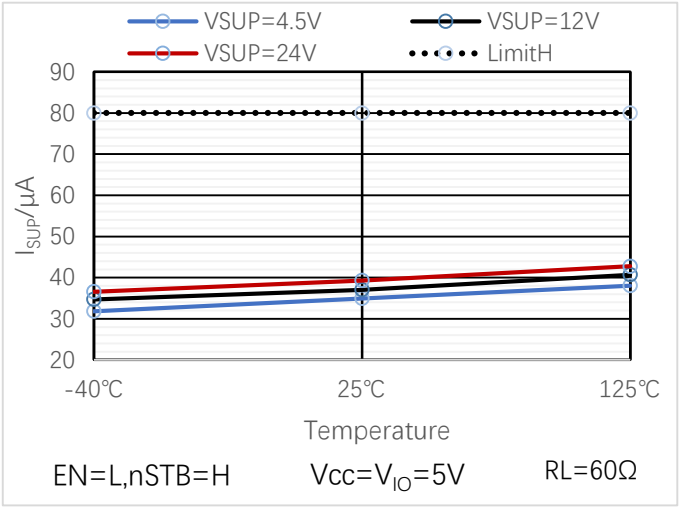


Figure 9-2 ISUP, silent mode

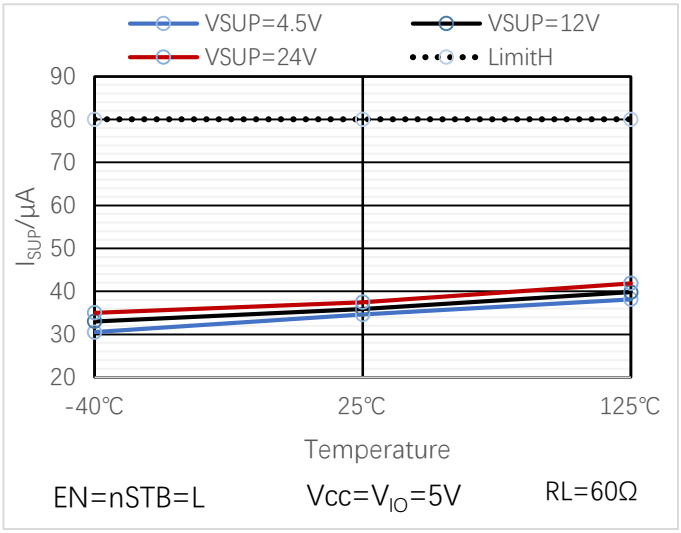


Figure 9-3 I_{SUP}, Standby mode

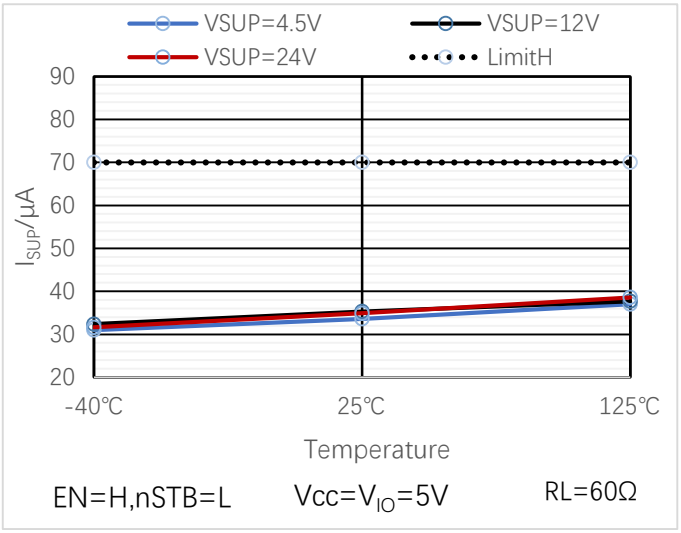


Figure 9-4 I_{SUP}, Sleep mode

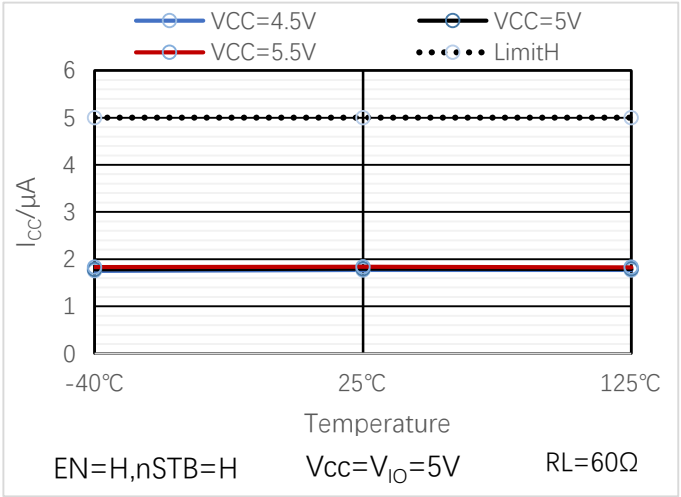


Figure 9-5 I_{CC} , Normal mode , Recessive

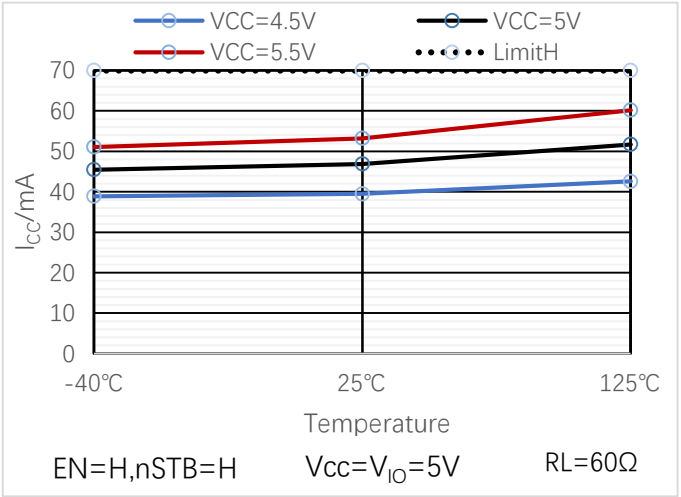


Figure 9-6 I_{CC} , Normal mode, Dominant

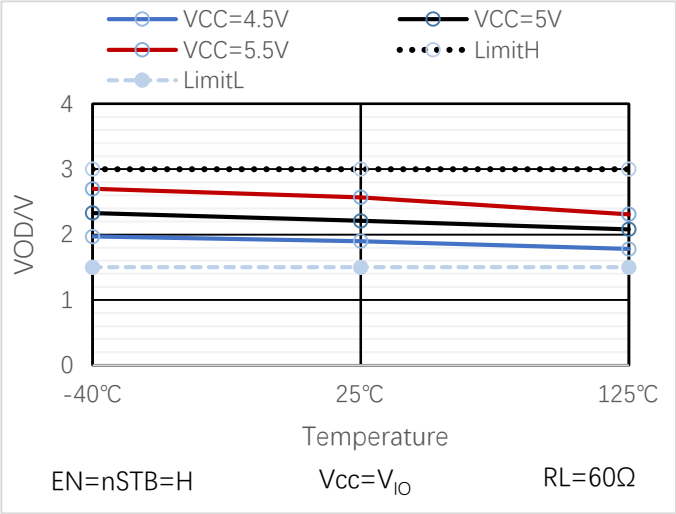


Figure 9-7 VOD, Normal mode

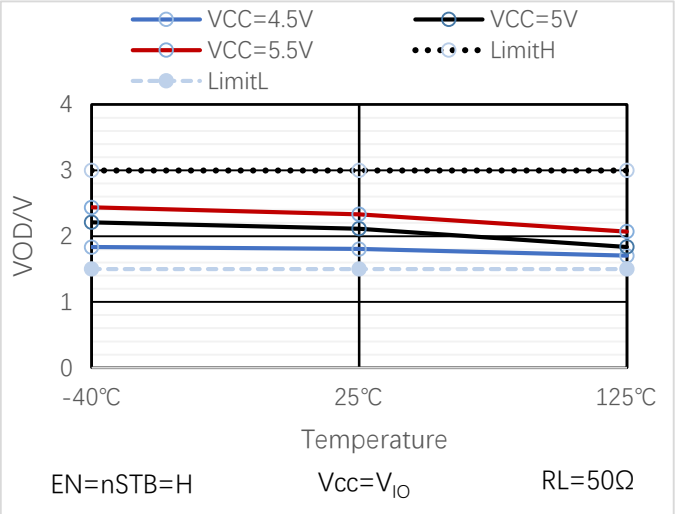


Figure 9-8 VOD, Normal mode

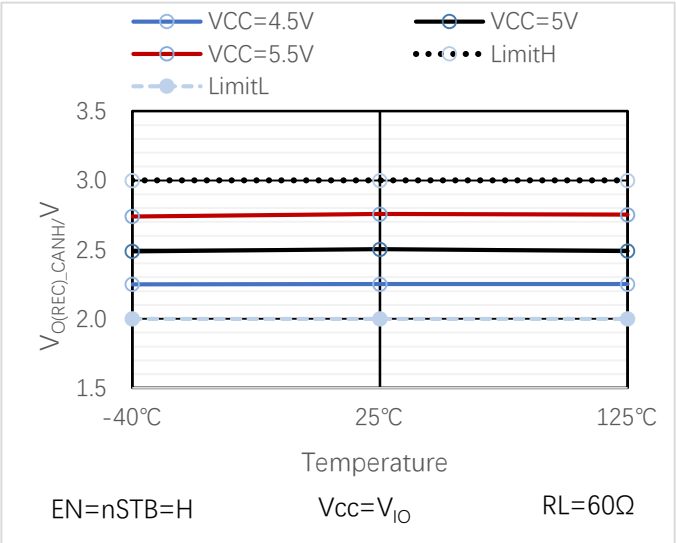


Figure 9-9 $V_{O(REC)\_CANH,}$, Normal mode

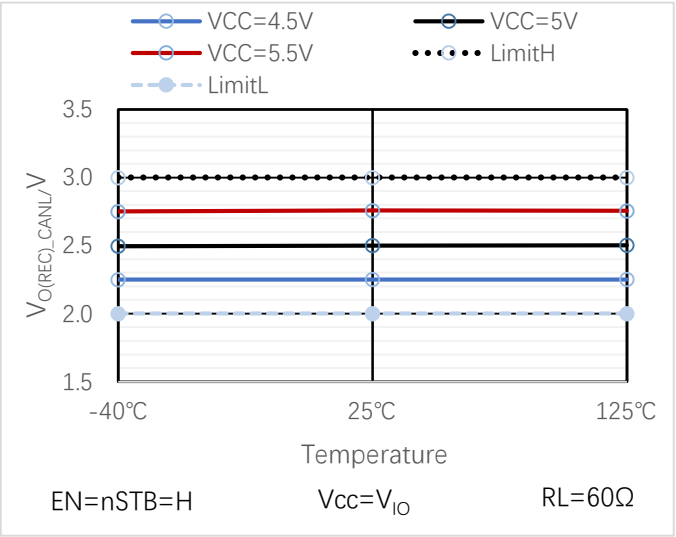


Figure 9-10 $V_{O(REC)\_CANL,}$, Normal mode

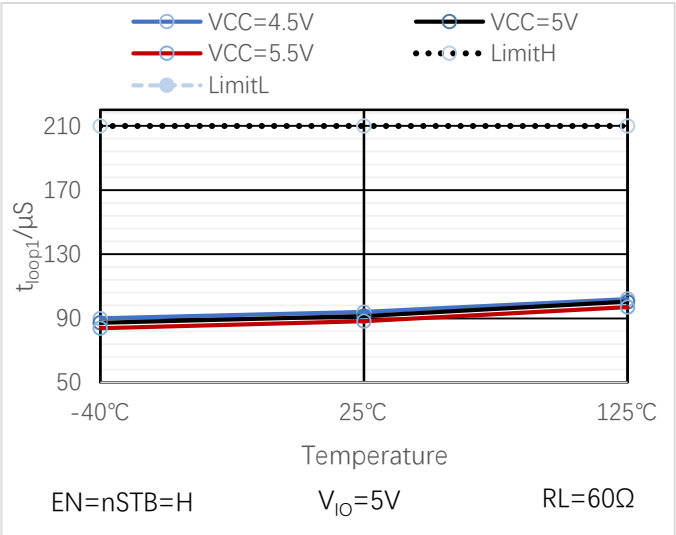


Figure 9-11 t_{loop1}

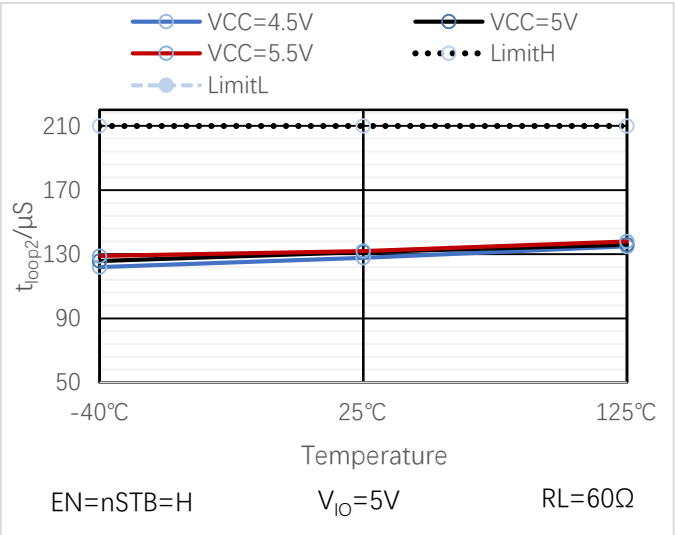


Figure 9-12 t_{loop2}

10. Detailed Description

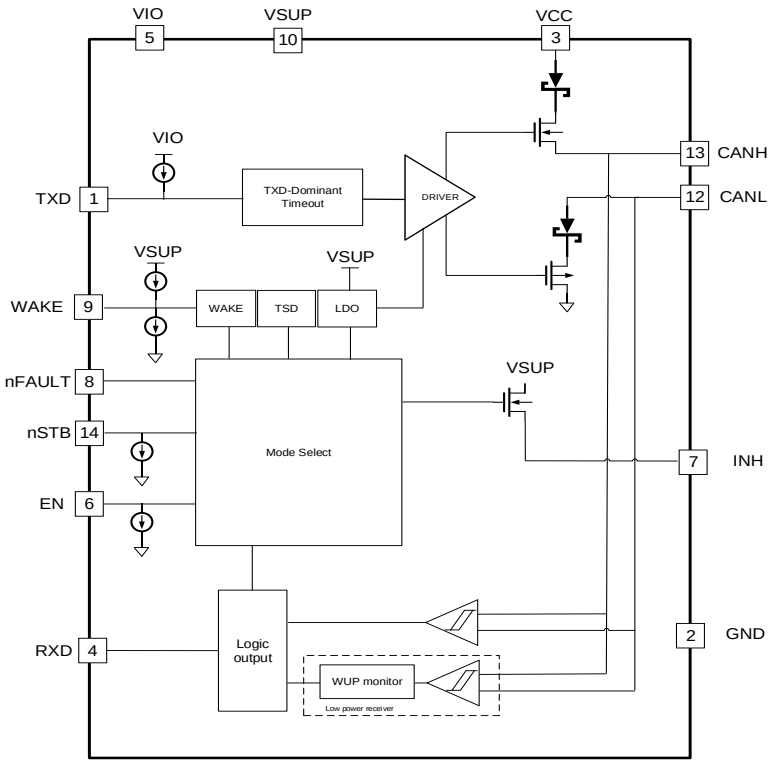
10.1. Overview

The CA-IF1043x family of devices is fault-protected Controller Area Network (CAN) transceiver, meets the ISO11898-2 (2016) high speed CAN physical layer standard. These devices are designed for harsh industrial and automotive applications with a number of integrated robust protection features set that improve the reliability of end equipment. All devices are fault protected up to ±58V for the bus pins, making them ideal for applications where overvoltage protection is required. A common-mode voltage ranges of ±30V enables communication in noisy environments where there are ground plane differences between different systems. Dominant timeout prevents the bus from being blocked by a hung-up microcontroller, and the outputs CANH and CANL are short-circuit current-limited and protected against excessive power dissipation by thermal shutdown circuitry that places the driver outputs in a high-impedance state.

A separate input V_{IO} allows the CA-IF1043x devices to communicate with logic systems down to 1.8V while operating up to a +5.5V bus supply. This provides a reduced input voltage threshold to the TXD, EN and nSTB inputs, and provides a logic-high output at RXD and nFAULT compatible with the microcontroller's supply rail. The logic compatibility eliminates external logic level translator and longer propagation delay due to level shifting. Connect VIO to VCC to operate with +5V logic systems. Also, the CA-IF1043x provides individual battery supply input that accepts up to +45V supply voltage, allowing for use in high-voltage system, for example, +12V or +24V industrial and automotive applications. The transceiver provides three low-power modes(silent, standby and sleep) that can be entered and exited through pins nSTB and EN. An output INH pin can be used to control external voltage regulator to reduce system power consumption.

The CA-IF1043x devices can operate up to 5Mbps data rate and support CAN FD. However, the maximum data rate is limited by the bus loading, number of nodes, cable length etc. factors, for CAN network design, margin must be given for signal loss across the system and cabling, parasitic loadings, timing, network imbalances, ground offsets and signal integrity thus a practical maximum data rate, number of nodes often lower than the theoretical value.

10.2. Functional and Block Diagram



10.3. CAN Bus Status

The CAN bus has two states: dominant and recessive. In the dominant state (a zero bit, used to determine message priority), CANH-CANL are defined to be logic '0' when the voltage across them is between +1.5V and +3V (higher than 0.9V). In the recessive state (a "1" bit and the state of the idle bus), the driver is defined to be logic '1' when differential voltage is between -120mV and +12mV, or when it is near zero(lower than 0.5V), see Figure 10- 1 for the bus logic state voltage definition.

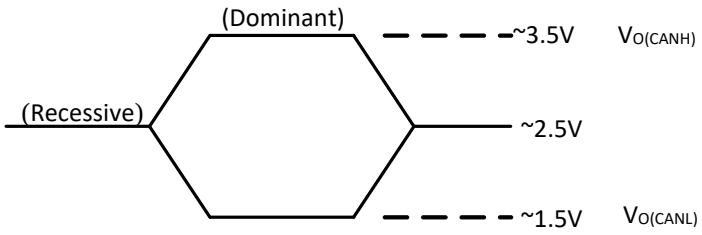


Figure 10- 1. Bus Logic State Voltage Definition

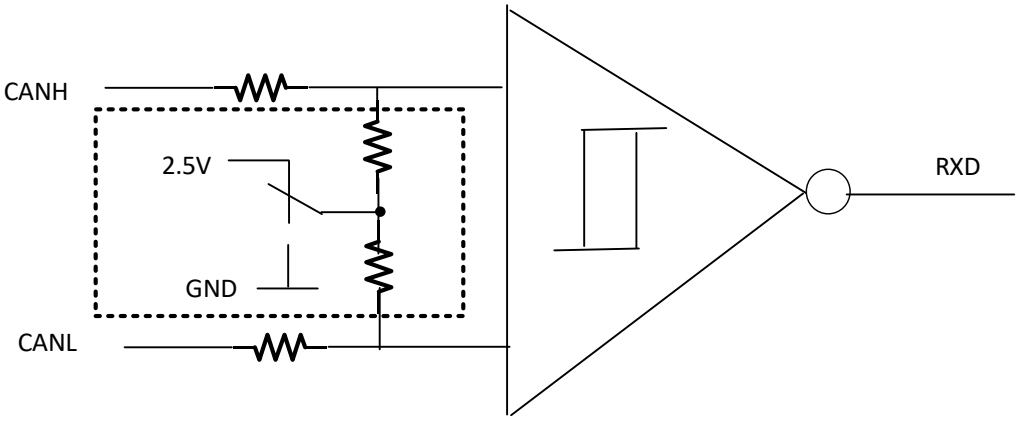


Figure 10- 2. Receiver Input/Transmitter Output Bias Circuit

10.3.1. CAN Driver

In normal operation, the driver converts a single-ended input signal (TXD) from the local CAN controller to differential outputs for the bus lines CANH and CANL. The truth table for the driver is provided in Table 10- 1. The CA-IF1043x family of devices protects the driver output stage against a short-circuit to a positive or negative voltage by limiting the driver current. Thermal shutdown further protects the devices from excessive temperatures that may result from a short circuit. The driver returns to normal operation once the junction temperature drops at least the thermal shutdown hysteresis temperature below the thermal shutdown temperature(190°C, typ.). In standby and sleep modes, the driver is disabled and put the bus in high-impedance with internal weak pull-down to ground, see Table 10- 1.

Table 10- 1. Driver FunctionTable

DEVICE MODE	TXD INPUT	TXD LOW TIME	OUTPUT		BUS STATE
			CANH	CANL	
Normal nSTB = High EN = High	Low	< t_{TXD_DTO}	High	Low	Dominant
	Low	> t_{TXD_DTO}	$V_{CC}/2$	$V_{CC}/2$	Recessive
	High or Open	X	$V_{CC}/2$	$V_{CC}/2$	Recessive
Silent	X	X	$V_{CC}/2$	$V_{CC}/2$	Recessive
Standby	X	X	High-Z	High-Z	Biased to GND
Go to sleep	X	X	High-Z	High-Z	Biased to GND
Sleep	X	X	High-Z	High-Z	Biased to GND

X = Don't care

10.3.2. CAN Receiver

The receiver of CA-IF1043x family of devices includes a main receiver to support normal bi-directional communication and a low-power receive channel to monitor the bus line and detect the wakeup event on the bus line during sleep mode. Drive the both nSTB and EN pins high for normal operation. In normal operation, the main receiver reads the differential input from the bus line (CANH and CANL) and transfers this data as a single-ended output RXD to the CAN controller. The internal comparator senses the difference voltage V_{DIFF} = (V_{CANH}-V_{CANL}), with respect to an internal threshold of 0.7V. If V_{DIFF} > 0.9V, a logic-low is present on RXD; If V_{DIFF} < 0.5V, a logic-high is present. The CANH and CANL common-mode range is ±30V in normal mode. Table 10- 2 shows the receiver input bias circuit.

The CA-IF1043 features low-power operation modes that include standby mode, sleep mode and silent mode. In standby and sleep modes, both CAN driver and the main receiver are disabled and bidirectional CAN communication is not possible. But the INH control is valid in standby mode and INH is turned off (High-Z) in sleep mode. As the low-power receiver is enabled in standby or sleep modes, this switches the receiver to a low current and low-speed state. The bus line is monitored by a low-power differential comparator to detect and recognize a wakeup event on the bus line. RXD is logic High until a valid remote wakeup or local wakeup signal is received. In silent mode, the CAN driver is disabled but the receiver is fully operational. See Table 10- 2 for more details about the receiver truth table.

Table 10- 2. Receiver Truth Table

DEVICE MODE	$V_{ID} = V_{CANH}-V_{CANL}$	BUS STATE	RXD
Normal Silent	$V_{ID} \geq 0.9V$	Dominant	Low
	$0.5V < V_{ID} < 0.9V$	Indeterminate	Indeterminate
	$V_{ID} \leq 0.5V$	Recessive	High
	Open ($V_{ID} \approx 0V$)	Open	High
Standby	$V_{ID} > 1.15V$	Dominant	Low if a remote wake event occurred, otherwise output High.
	$0.4V < V_{ID} < 1.15V$	Indeterminate	
	$V_{ID} \leq 0.4V$	Recessive	
	Open ($V_{ID} \approx 0V$)	Open	
Go to Sleep Sleep	$V_{ID} > 1.15V$	Dominant	Low if a remote wake event occurred and V_{IO} power-on, otherwise output High. Indeterminate if V_{IO} or V_{SUP} power-off.
	$0.4V < V_{ID} < 1.15V$	Indeterminate	
	$V_{ID} \leq 0.4V$	Recessive	
	Open ($V_{ID} \approx 0V$)	Open	

10.4. Operating Mode

The CA-IF1043x devices have five operating modes: protected mode, normal operation mode, silent mode, low-power standby mode and very low-power sleep mode. The operating mode is determined by an internal state machine controlled by EN and nSTB, as well as several internal flags, see Table 10- 3 and Figure 10- 3 for more details about the CA-IF1043x operating modes.

Table 10- 3. Operating Modes[1]

V_{CC}/V_{IO}	V_{SUP}	EN	nSTB	WAKERQ	MODE	Driver	Receiver	RXD	BUS OUTPUT	INH
$>V_{UV\_VCC}$ $>V_{UV\_VIO}$	$>V_{UV\_VSUP}$	H	H	X	Normal	Enabled	Enabled	Mirrors Bus	Per TXD	High
		L	H	X	Silent	Disabled	Enabled	Mirrors Bus	Biased to $V_{CC}/2$	High
		H	L	Cleared	Go to sleep[2]	Disabled	Low-power receive channel enabled	H	Weak pull-down to GND	High[2]
				Cleared	Sleep[3]	Disabled	Low-power receive channel enabled	H	Weak pull-down to GND	Floating
				SET	Standby	Disabled	Low-power receive channel enabled	Low if wakeup occurred.	Weak pull-down to GND	High
		L	L	X	Standby	Disabled	Low-power receive channel enabled	Low if wakeup occurred.	Weak pull-down to GND	High
$<V_{UV\_VCC}$ $<V_{UV\_VIO}$	$>V_{UV\_VSUP}$	X	X	X	Sleep	Disabled	Low-power receive channel enabled	H	Weak pull-down to GND	Floating
X	$<V_{UV\_VSUP}$	X	X	X	Protected	Disabled	Disabled	High-Z	High-Z	Floating

Notes:

1. L = Low-level, H = High-level, High-Z = High impedance, X = Don't care.
2. Go-to-sleep mode is transitional mode for EN = H, nSTB = L until $t_{H(go\text{-}to\text{-}sleep)}$ timer has expired and the INH transitions to high impedance (floating) after $t_{H(go\text{-}to\text{-}sleep)}$ timer has expired.
3. Mode switches from go-to-sleep to sleep once $t_{H(go\text{-}to\text{-}sleep)}$ timer has expired.

10.5. State Diagram

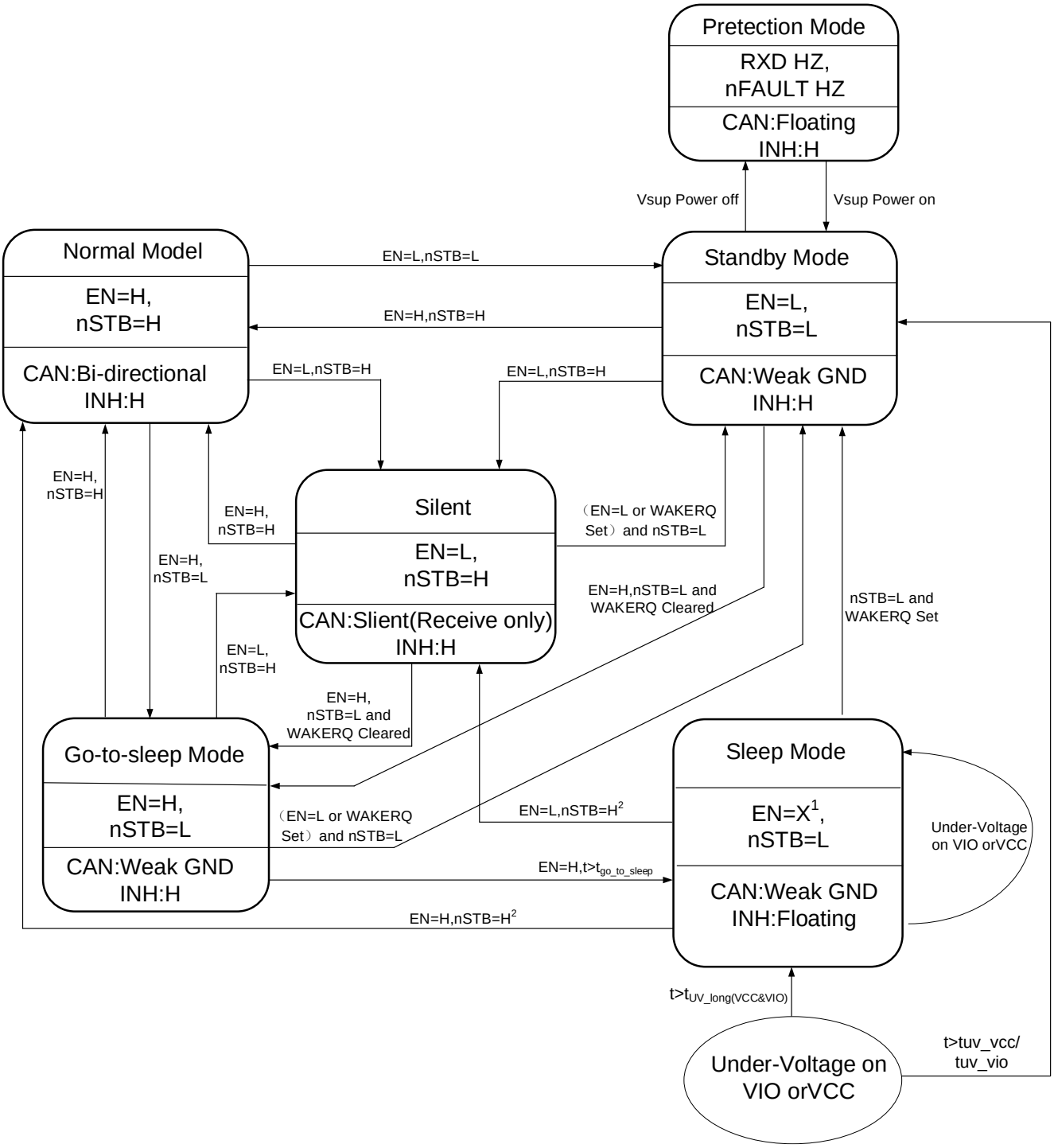


Figure 10- 3. State Diagram

Note：

1. The enable pin can be in a logical high or low state while in sleep mode but since it has an internal pull-down, the lowest possible power consumption occurs when the pin is left either floating or pulled low externally.
2. Mode transitions when valid VCC, VIO and VBAT voltages are present

10.5.1. Protected Mode

When the voltage on VSUP drops below V_{UN_VSUP} for longer than t_{UV_VSUP}, the UVSUP flag is set and put the device into protected mode. Both CAN driver and receiver are disabled, leave the bus and RXD in high-impedance. nFAULT goes high impedance and INH goes high impedance disabling external voltage regulators.

10.5.2. Normal Mode

Select the normal mode of the CA-IF1043x devices operation by setting nSTB and EN terminals to logic-high. The CAN driver and receiver are fully operational and CAN communication is bi-directional. See the CAN Receiver and CAN sections for more details. INH is logic-high during normal operation, can be used to enable external voltage regulators and microcontroller.

During normal operation, the CA-IF1043x switches to sleep mode in case of a low-level on pin nSTB and maintained at least $t_{H(go\text{-}to\text{-}sleep)}$.

10.5.3. Silent Mode

In silent mode (listen-only mode), the CAN driver is disabled, but the receiver remains active and the CAN bus state is presented on RXD. INH is logic-high enabling external voltage regulator.

10.5.4. Standby Mode

Standby mode is low-power operating mode. The CAN driver and main receiver are disabled and no communication with the CAN bus is possible in standby mode.

In standby mode, once a wakeup request (WAKERQ) is detected, RXD is placed at low-level that can be used as an interrupt for the microcontroller. INH output is switched on and remains logic-high to enable external voltage regulators. The wakeup source can be identified by the nFAULT status after the device is returned to normal mode.

10.5.5. Go-to-Sleep Mode

Go-to-sleep mode is a transitional mode for entering sleep mode. The CA-IF1043x devices remains in go-to-sleep mode for a hold time of $t_{H(go\text{-}to\text{-}sleep)}$ (5µs, max), and subsequently enters sleep mode if no wakeup events are detected, places the INH in high impedance. During $t_{H(go\text{-}to\text{-}sleep)}$, if the state of EN or nSTB changes, or if the UVSUP, PWRON, or WAKERQ flags are set, the go-to-sleep sequence is aborted.

10.5.6. Sleep Mode

Sleep mode is the lowest-power operating mode. In sleep mode, the CAN driver and receiver are disabled; INH is turn-off (high impedance), disabling external regulators to reduce V_{SUP} power consumption.

Either or both the V_{CC} or V_{IO} supplies have an undervoltage condition will place the device into sleep mode. If V_{IO} remains valid, it is recommended to drive the EN pin low once the device has transitioned into sleep mode to reduce the current consumption due to the internal pull-down on the EN terminal.

In sleep mode, the CAN bus and WAKE pin are continuously monitored for a valid wakeup signal, so that transceiver is able to wakeup by a message on the CAN bus or local wakeup event through WAKE pin. Also, EN and nSTB pins can be used to change operation modes as well if both V_{CC} and V_{IO} are powered-up.

Whenever a local or remote wake-up occurs, WAKERQ flag is set and the transceiver will enter standby mode automatically which in turn sets the INH output high. The WAKESR flag is set either high or low to identify which wake event occurred. This flag can be polled via the nFAULT terminal after the device is returned to normal mode and only until there have been four recessives to dominant transitions on the TXD pin. The wake source (WAKESR) flag has two states:

- nFAULT = Low: means that the wakeup source was through the WAKE pin.
- nFAULT = High: means that a remote wakeup occurred.

If both a local wakeup and a remote wakeup events occur, the WAKESR flag indicates whichever event was completed first.

10.6. Wake-up Events

Advanced power management and wake-up capability make the CA-IF1043x family of CAN transceivers ideal for the battery power applications. For CA-IF1043x devices, there are two different ways to exit sleep mode:

- **Remote wake-up:** the transceiver waked-up via a valid wakeup signals on the CAN bus.
- **Local wake-up:** the transceiver waked-up by state change on WAKE terminal.

10.6.1. Remote Wake-up

The bus wakeup, also called remote wakeup, changes the transceiver's operation mode from sleep mode to standby mode. To improve the system operation reliability and prevent false wake-up, the CA-IF1043x devices' receiver features wakeup timeout detection and filtered CAN bus status wakeup detection according to the ISO 11898-2:2016 standard. This means, for a valid dominant or recessive status to be considered, the bus must be kept in that state for more than the t_{WK_FILTER} time. For a remote wake-up event to successfully occur, a dominant bus level greater than t_{WK_FILTER} must be detected and received by the low-power receive channel first to initiate a wake-up event. Then the low-power monitor will wait for a valid recessive state from CAN bus. Once a valid recessive pulse is received, the low-power bus monitor is waiting for the 2nd valid dominant state, other bus traffic does not reset the bus monitor. Once the low-power receive channel detects a successful wake-up event (a series of valid dominant - recessive - dominant pulses) within the timeout value $t \le t_{WK\_TIMEOUT}$, RXD pulls low and INH pulls high. CAN controller can drive the nSTB and EN high based on this wakeup signal from RXD for normal operation. RXD is high until a valid wakeup is received during sleep mode, see Figure 10- 4 for more details.

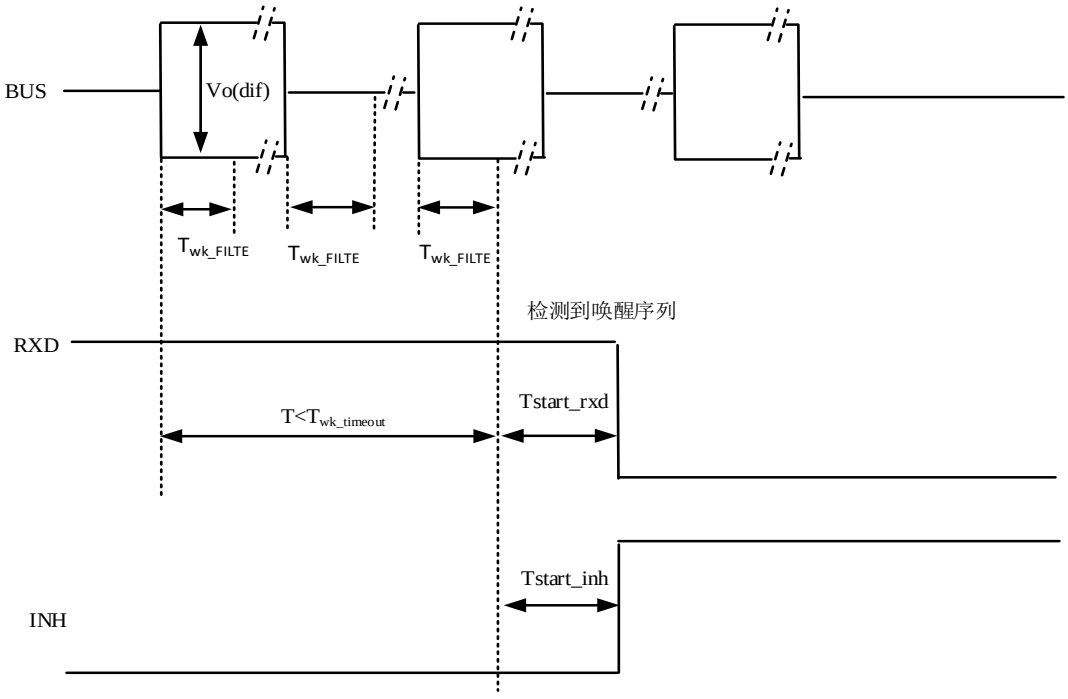


Figure 10- 4. Remote Wake-up

10.6.2. Local Wake-Up

A valid local wake-up request is generated either a low-to-high(rising edge), or a high-to-low(falling edge) transition on WAKE terminal, see Figure 10- 5 and Figure 10- 6. The WAKE is a high voltage input terminal. Once a valid local wakeup event occurs, the device trhansitions to standby mode. The local wakeup request is not active in normal mode or silent mode. To minimize system level current consumption, the internal WAKE bias voltage follows the state on the WAKE pin after a delay of t_{WAKE_min}. A constant high level on WAKE has internal pull-up towards pin VSUP and a constant low level on WAKE has internal pull-down to GND. This minimizes the current into the WAKE pin under these steady-state conditions so that it does not need to be factored into calculations of the total draw from V_{SUP}. However, for the unused local wakeup (WAKE pin), it is recommended to connect pin WAKE to V_{SUP} or GND to prevent EMI issues.

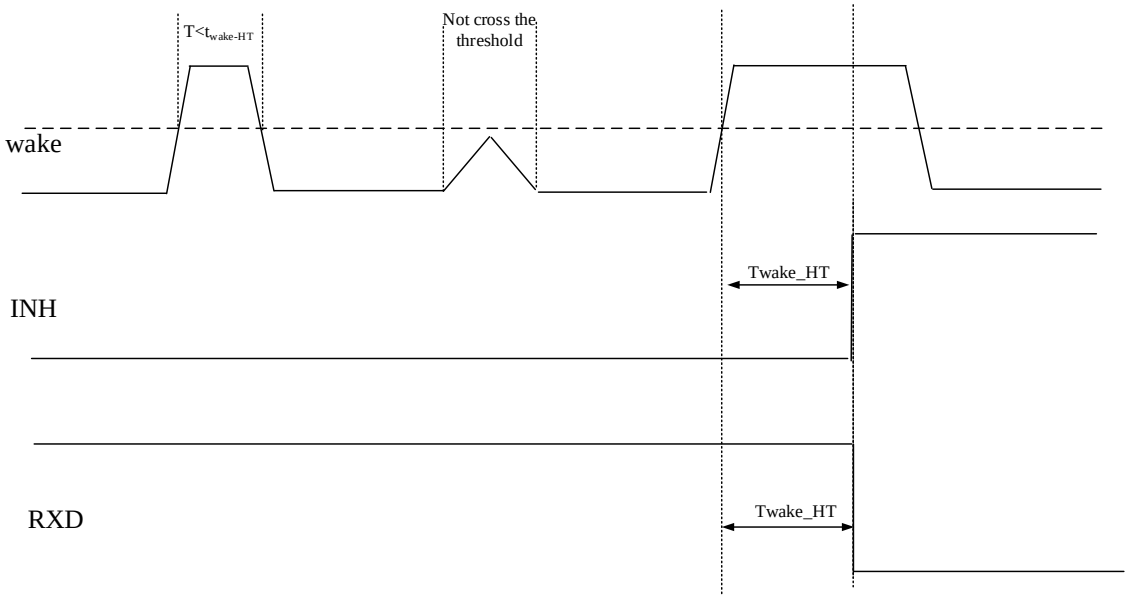


Figure 10- 5. Local Wake Up – Rising Edge

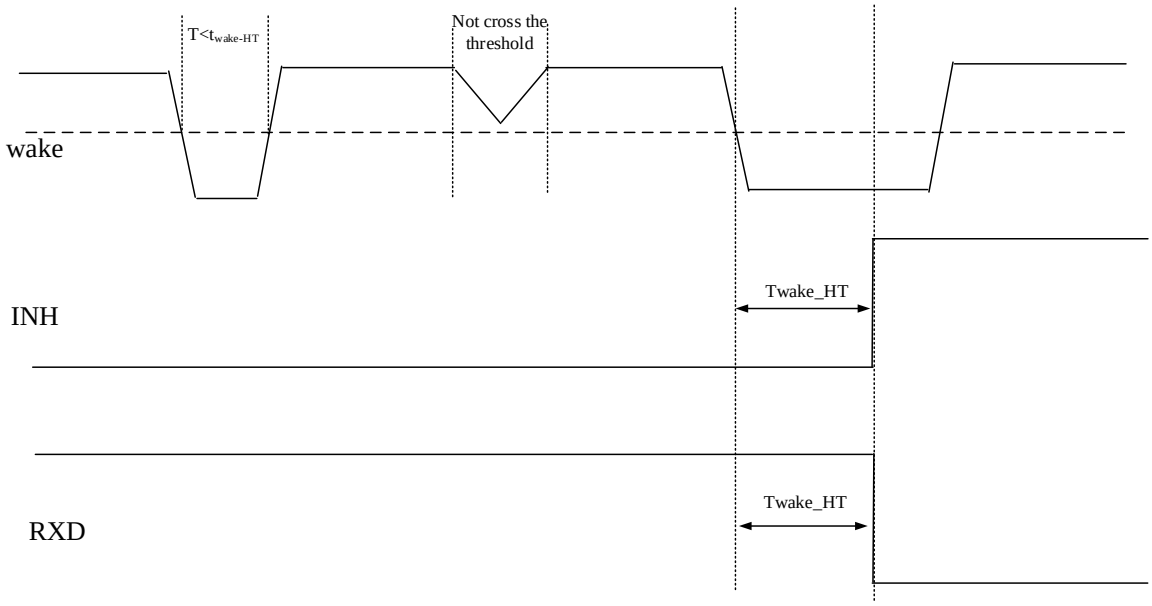


Figure 10- 6. Local Wake Up – Falling Edge

10.7. Flag Signaling

The CA-IF1043x failure detector is fully active in normal operation mode. It uses a set of six internal flags for system diagnosis and to indicate faults and five of the flags are available at different conditions to the CAN protocol controller on nFAULT pin, see Table 10- 4. A logic-low on nFAULT indicates a set flag or a fault. After the detection of a single failure, the detector switches to an appropriate state.

Table 10- 4. Flag Signaling[1]

EVENT	FLAG NAME	nFAULT [2]	CONDITIONS TO CLEAR FLAG	NOTE
Power-on	PWRON	nFAULT = L in silent mode changing from standby, go-to-sleep, or sleep mode.	Entering normal mode.	Power up on VSUP and any return of V_{SUP} after it has been below V_{UV_VSUP} set PWRON flag.
Wake-up	WAKERQ[3]	nFAULT = RXD = L after wakeup event occurs in standby, go-to-sleep, and sleep modes.	Entering normal mode or setting PWRON or under-voltage flag (UVVIO or UVVCC).	Remote wakeup on CAN bus, state transition on WAKE pin set wake-up flag. Wake up request can only be set in standby, go-to-sleep, or sleep mode.
Supply Under Voltage	UVVCC	Not available on nFAULT	Recovery of V_{CC} or wakeup event occurs.	V_{CC} undervoltage set UVVCC..
	UVVIO	Not available on nFAULT	Recovery of V_{IO} or wakeup event occurs.	V_{IO} undervoltage set UVVIO.
	UVVSUP	Not available on nFAULT	Recovery of V_{SUP}.	V_{SUP} undervoltage, triggers the PWRON and WAKERQ flags upon return of V_{SUP}.
Wake-up Resources[4]	WAKESR	nFAULT is available in normal mode before the fourth recessive to dominant edge on TXD.[5] nFAULT= L indicates wake from WAKE pin. nFAULT= H indicates wake from CAN bus.	After four recessive to dominant edges on TXD in normal mode, leaving normal mode, or either a UVVCC or UVVIO event.	Wake up event on CAN bus, state transition on WAKE pin, initial power up can set wake-up resources flag.
Bus Failures	CBF	nFAULT= L in normal mode, after the fourth dominant-to-recessive transition on TXD.	Leaving normal mode.	Either CANH of CANL terminal shorted to GND, V_{CC}, V_{SUP} set CBF flag. Failure must persist for four consecutive dominant to recessive transitions.
Local Failure	TXDDTO	nFAULT = L when device is placed into silent mode from normal mode.	RXD= L and TXD= H, or device enters normal, standby, go-to-sleep, or sleep modes.	CAN driver remains disabled until TXDDTO flag is cleared.
	TXDRXD			CAN driver remains disabled until TXDRXD flag is cleared
	CANDOM		RXD= H or device enters normal, standby, go-to-sleep, or sleep modes.	CAN driver remains enabled.
	TSD		T_J drops below T_{TSD}-T_{TSD_HYS} , and either RXD = L and TXD = H, or device enters normal, standby, go-to-sleep, or sleep modes.	CAN driver remains disabled until TSD flag is cleared.

Notes:
1. L = Low-level, H = High-level.
2. When nFAULT is active, V_{IO} and V_{SUP} must be powered up.
3. Transitions to go-to-sleep mode is blocked until WAKERQ flag is cleared.
4. Wake-up source recognition is the first wake up source. If additional wake-up events occurred, WAKESR flag still indicates the original wakeup source.
5. Indicator is only available in normal mode until the flag is cleared.

10.7.1. Power-On Flag: PWRON

PWRON flag indicates that the CA-IF1043x is in a power-on state. This is an internal and external flag. PWRON is set when V_{SUP} has dropped below V_{UV_SUP} and recovered subsequently. This condition occurs when battery voltage is first applied to VSUP pin. The primary function of the PWRON flag is to prevent the CA-IF1043x from entering sleep mode and thereby disabling external voltage regulators before the protocol controller establishes control through EN and nSTB. The PWRON flag is externally indicated as a logic-low on nFAULT when the CA-IF1043x is placed into PWRON mode. The PWON flag is cleared when the CA-IF1043x enters normal mode.

10.7.2. Wake-Up Flag: WAKERQ

The wake-up flag is set when a valid local or remote wake-up request is detected. This flag is immediately available as a logic-low on nFAULT and RXD. Setting the wake-up flag clears $t_{UV\_}$ timer for the UVVCC or UVVIO. The wake-up flag can only be set when the device is in standby mode, go-to-sleep mode, or sleep mode. This flag is cleared upon entering normal mode or during an under voltage event on VCC or VIO.

10.7.3. Wake-Up Source Flag: WAKESR

The wake-up source flag is set high or low after a local wakeup request is detected, or a remote wakeup request occurs. This flag is an internal and external flag that is only available in normal mode prior to four recessives to dominant transitions on TXD. If the nFAULT pin is high after entering normal mode, this indicates that a remote wakeup even was detected. If the nFAULT output is low after entering normal mode, this indicates that a local wakeup event occurred. The flag is cleared after four recessives to dominant edges on TXD in normal mode, or leaving normal mode, or either a UVVCC or UVVIO event.

10.7.4. Supply Undervoltage: UVVCC, UVVIO, UVVSUP

The CA-IF1043x features undervoltage detection circuits on all three supply terminals: VSUP, VCC and VIO. These undervoltage flags are internal flags and are not indicated on the nFAULT pin. The internal flag UVVCC is set when supply voltage on VCC drops below V_{UV_VCC} for longer than t_{UV_VCC}; UVVIO is set when voltage on VIO drops below V_{UV_VIO} for longer than t_{UV_VIO}, and UVVSUP flag is set when supply voltage on VSUP drops below V_{UV_VSUP} for longer than t_{UV_VSUP}.

These internal flags are cleared when the voltage on the corresponding supply pin is restored and exceeds UVLO threshold, or a local wakeup request triggered by a level change on WAKE pin or a remote wakeup event. See Table 10- 3. Upon clearing the undervoltage condition and the supplies have returned to valid levels, the CA-IF1043x returns to the operating mode determined by EN and nSTB after UVLO recovery delay time.

10.7.5. CAN Bus Failure: CBF

The bus failure flag is set when the CA-IF1043x detects a CAN bus, either CANH terminal or CANL terminal, short-circuit to V_{SUP}, V_{CC}, or GND for four consecutive dominant-recessive cycles on TXD. CAN bus failures are only detected in normal mode and are only indicated via the nFAULT terminal by driving nFAULT low while the device is in normal mode. The CAN bus driver remains active during bus failure. The bus fault detector is able to detect bus faults for any time greater than t_{CBF} (1.9µs, minimum). The flag is cleared when the CA-IF1043x leaves normal mode.

10.7.6. Local Failure

The local failure flag indicates four separate local failure conditions:

- TXD dominant timeout (TXDDTO): dominant (low) signal presents for t ≥ t_{TXD_DTO};
- TXD shorted to RXD fault (TXDRXD): TXD and RXD pins are shorted together for t ≥ t_{TXD_DTO};
- CAN bus dominant fault (CANDOM): dominant bus signal received for t ≥ t_{BUS_DOM};
- Thermal shutdown (TSD): junction temperature ≥ T_{TSD}.

When one or more local failure conditions have occurred, the local failure flag is set and indicated as a logic-low on nFAULT pin when the CA-IF1043x is placed into silent mode from normal mode. Local faults are detected in both normal mode and silent mode. All other mode transitions clear the local fault flag indicators.

Transmitter-Dominant Timeout (TXD DTO)

The CA-IF1043x family of devices features a driver-dominant timeout (t_{TXD_DTO}) that prevents erroneous CAN controllers from clamping the bus to a dominant level by maintaining a continuous low TXD signal. When TXD remains in the dominant state (low) for greater than t t_{TXD_DTO}, the driver is disabled, releasing the bus to a recessive state (see Figure 10- 7). After a dominant timeout fault, the driver is re-enabled when receiving a rising edge at TXD. The driver-dominant timeout limits the minimum possible data rate to 5kbps.

This fault is indicated via the TXDDTO flag shown on the nFAULT terminal.

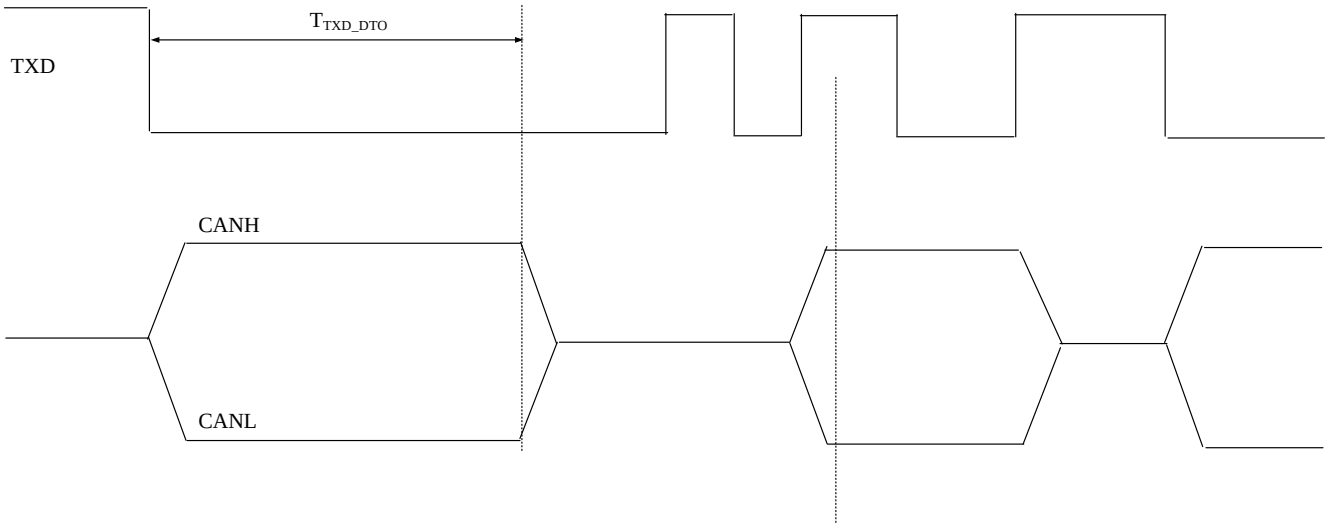


Figure 10- 7. Transmitter-Dominant Timeout Protection

TXD-to-RXD Short-Circuit Detection(TXDRXD)

The TXDRXD flag is set if the device detects a short-circuit between TXD and RXD for t ≥ t_{TXD_DTO}. This fault is then indicated via the nFAULT pin. The CA-IF1043x detects this condition and prevents the resulting bus failure by disabling the driver until the TXDRXD fault is cleared.

When switching from silent mode to another mode, the flag will be cleared to zero. When RXD=L and TXD=H, the flag will also be cleared to zero.

CAN Bus Dominant Clamping(CANDOM)

This identifier is used to detect that the bus is in an explicit state for more than t BUS_ DOM can be displayed through the nFAULT pin or through the RXD pin.

After switching from silent mode to another mode, the identifier is cleared to zero. When RXD=H, the identifier will also be cleared to zero. This fault is only indicated on the nFAULT pin in Silent mode.

Thermal Shutdown(TSD)

If the junction temperature of the devices exceeds the thermal shutdown threshold T_{TSD} (190°C), the device turns off the CAN driver thus blocking the TXD-to-bus transmission path. The shutdown condition is cleared when the junction temperature of the device drops below the thermal shutdown temperature of the device. If the fault condition that caused the thermal shutdown is still present, the temperature may rise again causing the device to reenter thermal shut down. Prolonged operation with TSD fault conditions may affect device reliability.

This fault is indicated via the TSD flag shown on the nFAULT terminal.

11. Application Information

The CA-IF1043x CAN transceivers are typically used in applications with a host microprocessor or FPGA that includes the data link layer portion of the CAN protocol. Figure 13-1. Soldering Temperature (reflow) ProfileFigure 11- 1 and Figure 11- 2 show the typical application circuit for the CA-IF1043x. In Figure 11- 1, connect VCC and VIO pins to the MCU logic-supply (+5V). In Figure 11- 2, VIO is connected with +3.3V MCU logic-supply.

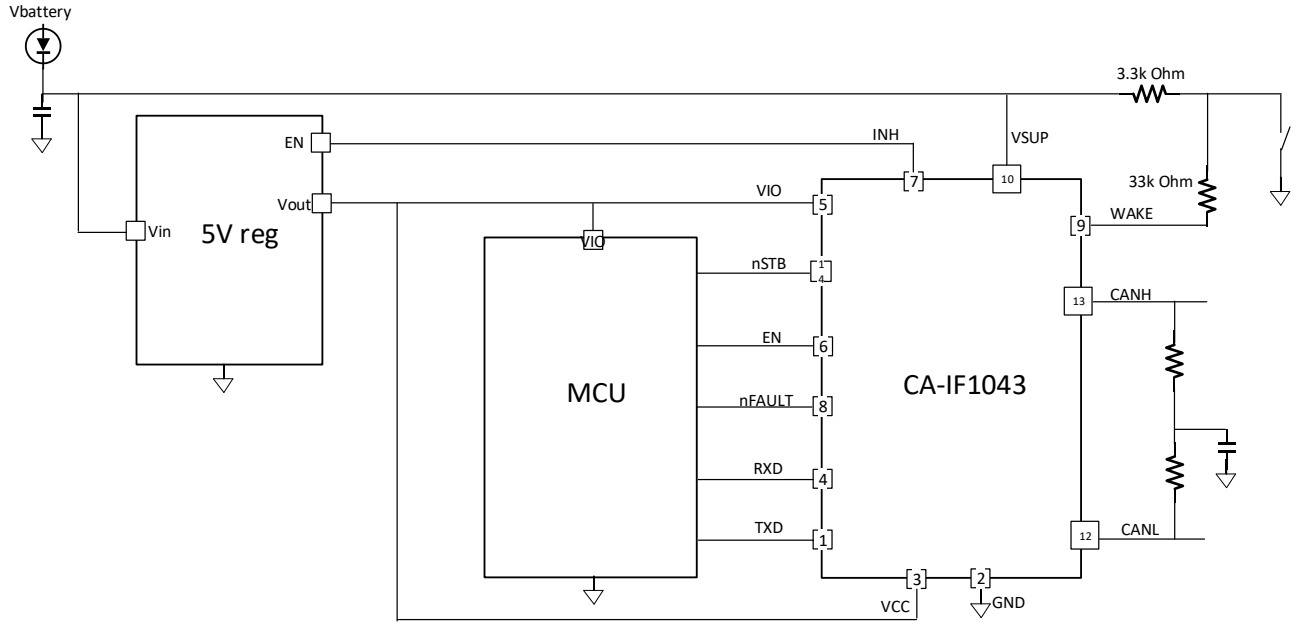


Figure 11- 1. Typical Application Circuit for the CA-IF1043x with +5V supply

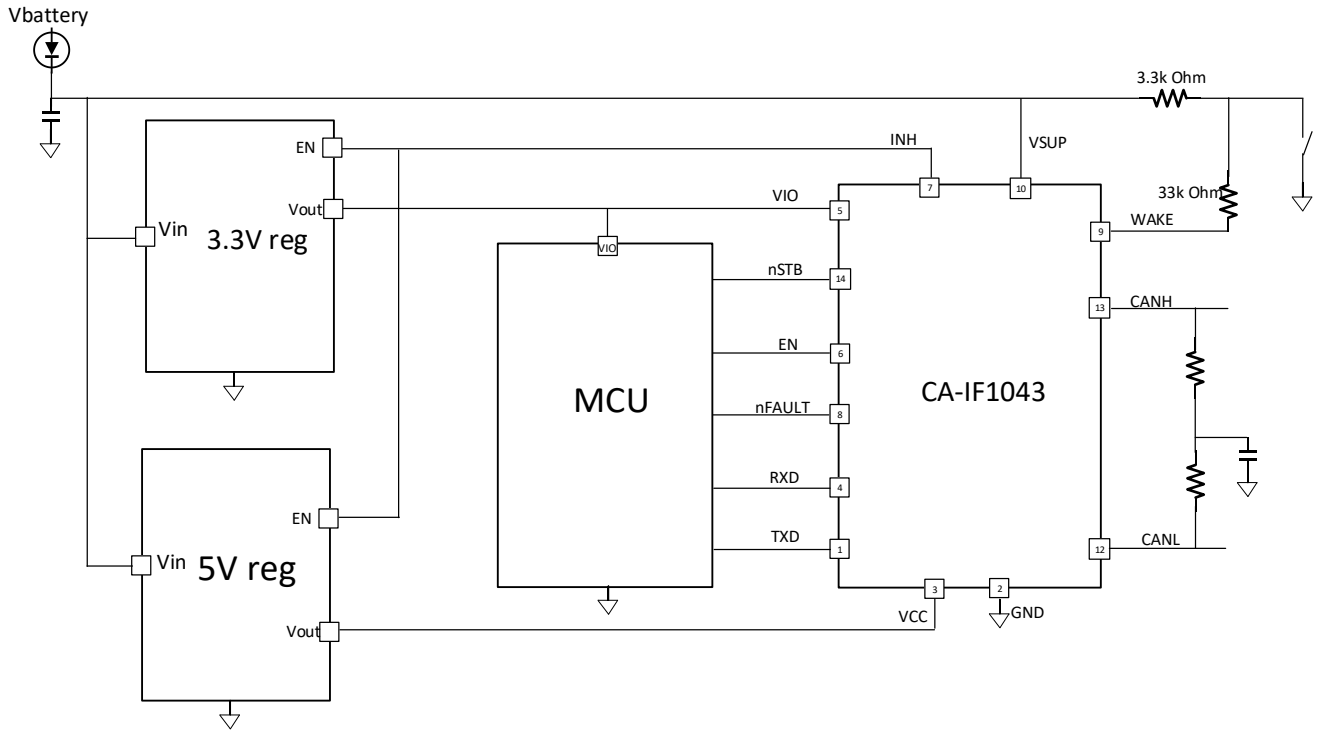


Figure 11- 2. Typical Application Circuit for the CA-IF1043x with +3.3V supplies

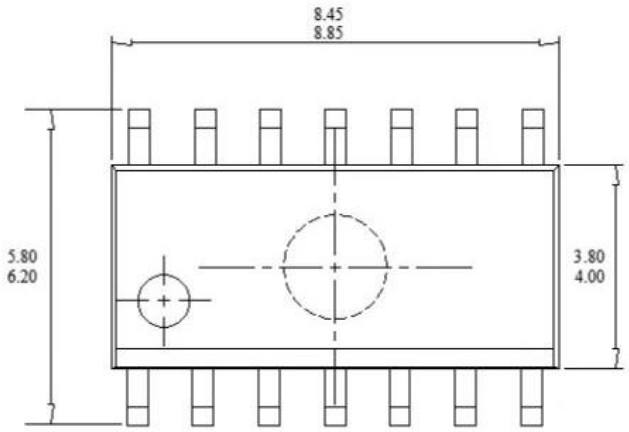
All of the CA-IF1043x devices can operate up to 5Mbps data rate. However, the maximum data rate is limited by the bus loading, number of nodes, cable length etc. For CAN network design, margin must be given for signal loss across the system and cabling, parasitic loadings, timing, network imbalances, ground offsets and signal integrity thus a practical maximum data rate, number of nodes often lower.

In multi-drop CAN applications, it is important to maintain a single linear bus of uniform impedance that is properly terminated at each end. A star, ring, or tree configuration should never be used. Any deviation from the end-to-end wiring scheme creates a stub. High-speed data edges on a stub can create reflections back down to the bus. These reflections can cause data errors by eroding the noise margin of the system. Although stubs are unavoidable in a multi-drop system, care should be taken to keep these stubs as short as possible, especially when operating with high data rates. Termination can be used to absorb reflections. Termination may be a single 120Ω resistor at the end of the bus, either on the cable or in a terminating node; or split termination, the two 60Ω termination resistors in series may be used if filtering and stabilization of the common mode voltage of the bus is desired.

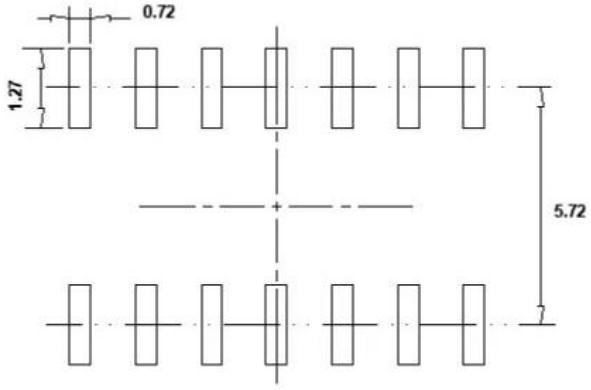
12. Package Information

SOIC14 Package Outline

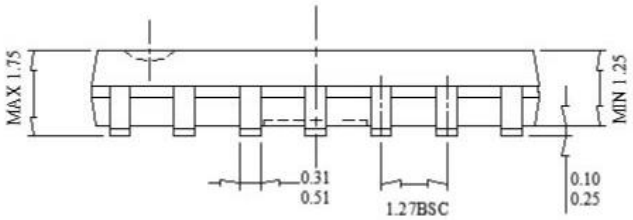
SOIC14 package size drawing and recommended pad size drawing. Dimensions in millimeters



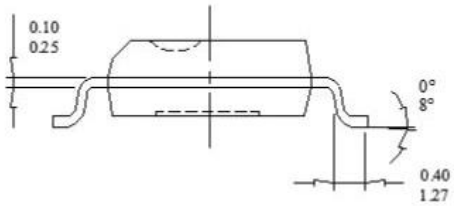
TOP VIEW



RECOMMENDED LAND PATTERN



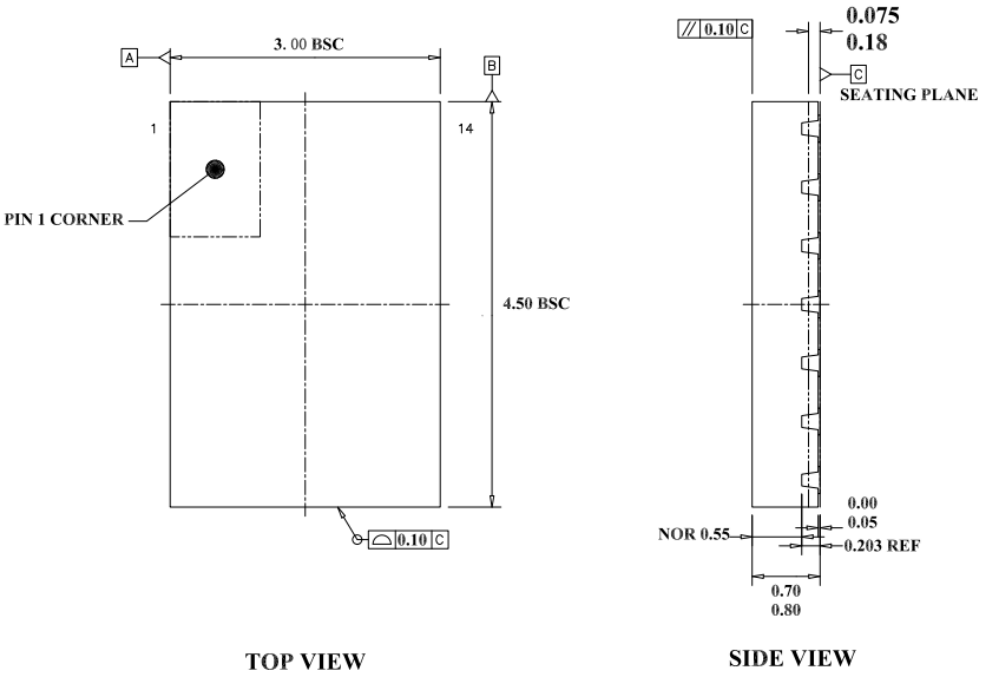
BOTTOM VIEW



LEFT SIDE VIEW

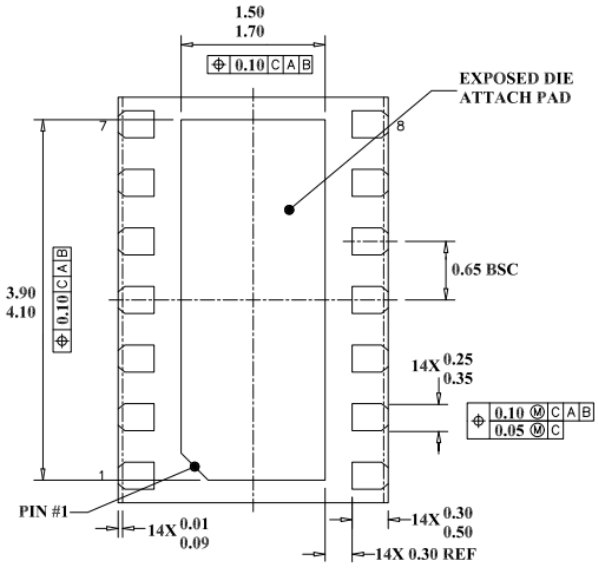
DFN14 Package Outline

DFN14 package size drawing and recommended pad size drawing. Dimensions in millimeters



TOP VIEW

SIDE VIEW



BOTTOM VIEW

13. Soldering Temperature (reflow) Profile

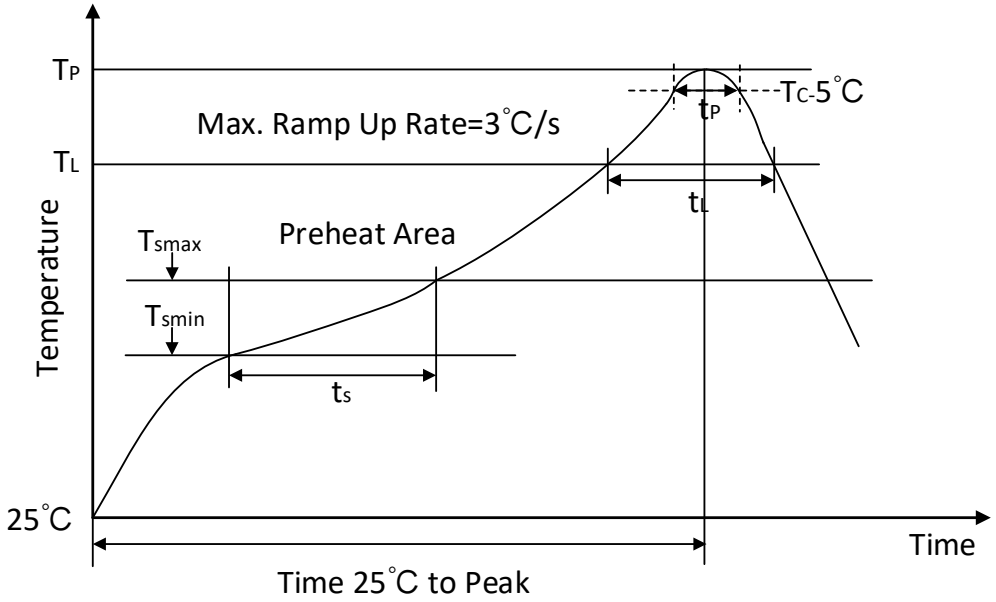


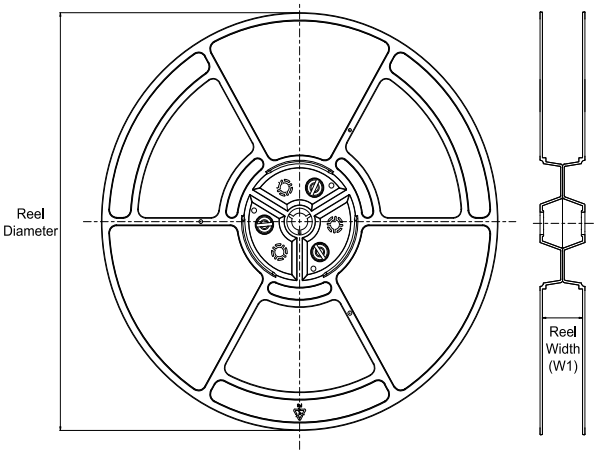
Figure 13-1. Soldering Temperature (reflow) Profile

Table 13-1. Soldering Temperature Parameter

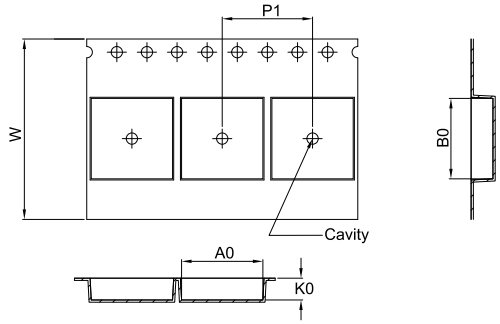
Profile Feature	**Pb-Free Assembly**
Average ramp-up rate(217°C to Peak)	3°C /second max
Time of Preheat temp(from 150 ℃ to 200°C	60-120 second
Time to be maintained above 217 °C	60-150 second
Peak temperature	260 +5/-0 °C
Time within 5°C of actual peak temp	30 second
Ramp-down rate	6 °C /second max.
Time from 25°C to peak temp	8 minutes maximum

14. Tape and Reel Information

REEL DIMENSIONS

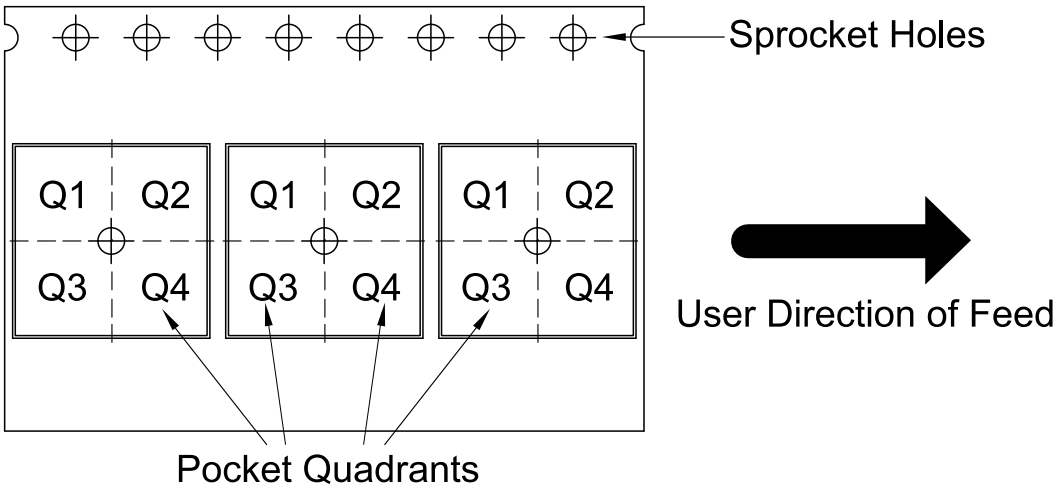


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CA-IF1043NF-Q1	SOIC14	NF	14	2500	330	16.4	6.50	9.00	2.10	8.00	16.00	Q1
CA-IF1043DF-Q1	DFN14	DF	14	3000	330	12.4	3.30	4.80	1.10	8.00	12.00	Q1

15. Appendix

Table. 14-1 Comparison Table of Parameter Symbols in ISO11898-2:2016 Standard and CA-IF1043 Datasheet

ISO 11898-2:2016		**CA-IF1043 Datasheet**	
Parameter	**Note**	**Symbol**	**Parameter**
HS-PMA dominant output characteristics			
Single ended voltage on CAN_H	V_{CAN_H}	$V_{O(DOM)}$	dominant output voltage
Single ended voltage on CAN_L	V_{CAN_L}		
Differential voltage on normal bus load	V_{Diff}	$V_{OD(DOM)}$	dominant differential output voltage
Differential voltage on effective resistance during arbitration			
Optional: Differential voltage on extended bus load range			
HS-PMA driver symmetry			
Driver symmetry	V_{sym}	V_{sym}	driver voltage symmetry
Maximum HS-PMA driver output current			
Absolute current on CAN_H	I_{CAN_H}	$I_{OS(SS\_DOM)}$	dominant short-circuit output current
Absolute current on CAN_L	I_{CAN_L}		
HS-PMA recessive output characteristics, bus biasing active/inactive			
Single ended output voltage on CAN_H	V_{CAN_H}	$V_{O(REC)}$	recessive output voltage
Single ended output voltage on CAN_L	V_{CAN_L}		
Differential output voltage	V_{Diff}	$V_{OD(REC)}$	recessive differential output voltage
Optional HS-PMA transmit dominant timeout			
Transmit dominant timeout, long	t_{dom}	t_{DOM}	TXD dominant time-out time
Transmit dominant timeout, short			
HS-PMA static receiver input characteristics, bus biasing active/inactive			
Recessive state differential input voltage range Dominant state differential input voltage range	V_{Diff}	V_{DIFF_D} V_{DIFF_R} $V_{DIFF\_D(STB)}$ $V_{DIFF\_R(STB)}$	Receiver dominant/recessive state differential input voltage range in normal /standby mode
HS-PMA receiver input resistance (matching)			
Differential internal resistance	R_{Diff}	R_{DIFF}	differential input resistance
Single ended internal resistance	R_{CAN_H} R_{CAN_L}	R_{IN}	input resistance
Matching of internal resistance	m_R	$R_{DIFF(M)}$	input resistance deviation
HS-PMA implementation loop delay requirement			
Loop delay	t_{Loop}	t_{loop2}	delay time from TXD HIGH to RXD HIGH
		t_{loop1}	delay time from TXD LOW to RXD LOW
Optional HS-PMA implementation data signal timing requirements for use with bit rates above 1 Mbit/s up to 2 Mbit/s and above 2 Mbit/s up to 5 Mbit/s			
Transmitted recessive bit width @ 2 Mbit/s / @ 5 Mbit/s, intended	$t_{Bit(Bus)}$	$t_{bit(bit)}$	transmitted recessive bit width
Received recessive bit width @ 2 Mbit/s / @ 5 Mbit/s	$t_{Bit(RXD)}$	$t_{bit(rxd)}$	bit time on pin RXD
Receiver timing symmetry @ 2 Mbit/s / @ 5 Mbit/s	Δt_{Rec}	t_{rec}	receiver timing symmetry
HS-PMA maximum ratings of V_{CAN_H}, V_{CAN_L} and V_{Diff}			
Maximum rating V_{Diff}	V_{Diff}	V(DIFF)	voltage between pin CANH and pin CANL
General maximum rating V_{CAN_H} and V_{CAN_L}		VBUS	voltage on CANH, CANL pin

Optional: Extended maximum rating VCAN_H and VCAN_L	V_{CAN_H} V_{CAN_L}		

Table. 14-1 Comparison Table of Parameter Symbols in ISO11898-2:2016 Standard and CA-IF1043 Datasheet (continued)

ISO 11898-2:2016		**CA-IF1043 Datasheet**	
Parameter	**Symbol**	**Symbol**	**Parameter**
HS-PMA maximum leakage currents on CAN_H and CAN_L, unpowered			
Leakage current on CAN_H, CAN_L	I_{CAN_H} I_{CAN_L}	I_{LKG}	leakage current
HS-PMA bus biasing control timings			
CAN activity filter time, long	t_{Filter}	t_{WK_FILTER}	bus dominant wake-up time bus recessive wake-up time
CAN activity filter time, short			
Wake-up timeout, short	t_{Wake}	$t_{WK\_TIMEOUT}$	bus wake-up time-out time
Wake-up timeout, long			
Transmit dominant time out	t_{dom}	t_{DOM}	TXD dominant Timeout
Bus Bias reaction time	t_{Bias}	t_{ONTXD}	delay time from bus active to bias or from bias to active

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