CA-IF4023 AISG On and Off Keying Coax Modem Transceiver

1. Features

- **Wide Receiver Input Dynamic Range**
  - -15dBm to +5dBm in 50Ω
- **Adjustable Output Power (5.4dBm to 12dBm) Allows Compensation for Losses in External Circuitry and Cabling**
- **AISG V3.0-compliant Output Emission Profile**
- **Autodirection Output Simplifies Bus Arbitration in Tower-mounted Equipment**
- **Supports 9.6kbps、38.4kbps and 115.2kbps AISG Signaling**
- **Integrated Active Bandpass Filter with Center Frequency at 2.176MHz**
- **3.0V to 5.5V Supply Voltage**
- **1.6V to 5.5V Independent Logic Supply Voltage**
- **Low-Power Standby Mode**
- **Small, 3mm x 3mm, 16-pin QFN Package**
- **-40°C to +125°C Operating Temperature Range**

2. Applications

- Base Stations
- Tower Equipment
- General Modem Interfaces

3. General Description

The CA-IF4023 is an integrated AISG transceiver which is compliant with the Antenna Interface Standards Group v3.0 specification. Integrated on the chip are the transmitter, receiver, and active filters. This device reduces the hassle and expense of working with discrete solutions and drastically reduces the time needed to implement the AISG protocol.

The receive channel offers a typical dynamic range of 20dB and integrates an active bandpass filter to enable demodulation of signals even in the presence of spurious frequency components. The filter has a 2.176MHz center frequency.

The transmitter integrates an narrow bandwidth bandpass filter with 2.176MHz center frequency as well, compliant with the spectrum emission requirement provided by the AISG standard. It supports adjustable output power levels varying from +5.4dBm to +12dBm in order to compensate for loss in the external circuitry and cabling.

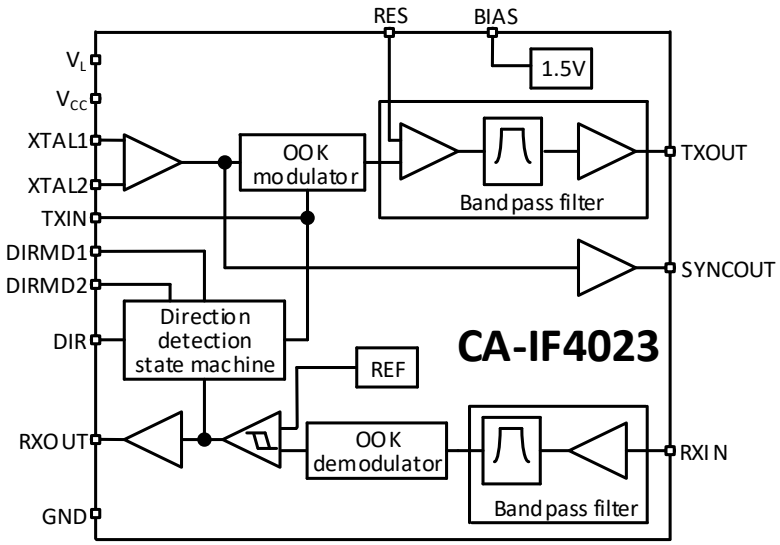
A direction output is provided which facilitates bus arbitration for the RS-485 communication interface. Also, the CA-IF4023 device integrates an oscillator input for a crystal and accepts standard clock input to the oscillator.

The CA-IF4023 is packaged in a small, 3mm x 3mm, 16-pin QFN and is fully specified for operation over -40°C to +125°C extended industrial temperature range。

Device Information

PART NUMBER	PACKAGE	BODY SIZE (NOM)
CA-IF4023	QFN16	3mm × 3mm

CA-IF4023 Function Diagram



4. Ordering Information

Table 4-1. Ordering Information

Part Number	Package	# of pins	Qty	Eco Plan	MSL	Temperature Range
CA-IF4023	QFN16	16	3000	Green (RoHS & no Sb/Br)	Level-1-260C-1 YEAR	–40°C~125°C

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5. Revision History

Revision Number	Description	Page Changed	Revision Date
Version A	N/A	N/A	2020-10-29
Version 1.00	N/A	N/A	2022-04-21
Version 1.01	Update the Package ,Tape and Reel Information	19,21	2022-11-08

6. Pin Configuration and Functions

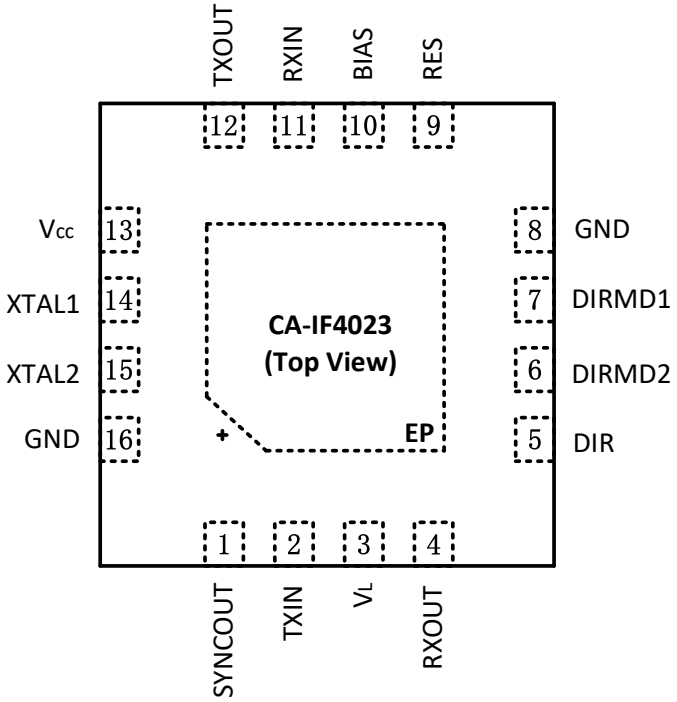


Figure 6-1. CA-IF4023 Pin Configuration

Table 6-1. CA-IF4023 Pin Configuration and Description

PIN #	PIN NAME	DESCRIPTION
1	SYNCOUT	Sync Output. Open-drain output to synchronize other devices to the 4x-carrier oscillator at XTAL1 and XTAL2. Connect 1kΩ pull-up resistor to V_{CC}.
2	TXIN	Tx input. Digital data bit stream to driver.
3	V_L	Logic supply voltage for the device.
4	RXOUT	Rx output. Digital data bit stream from receiver.
5	DIR	Direction Output. DIR is asserted high when the data stream is seen at the receiver.
6	DIRMD2	DIRSET1 and DIRSET2: Bits to set the duration of DIR.
7	DIRMD1	DIRSET[2:1]: [L:L] = 9.6 kbps; [L:H] = 38.4 kbps; [H:L] = 115 kbps; [H:H] = standby mode
8, 16	GND	Ground.
9	RES	Input voltage to adjust driver output power that is set by external resistors from BIAS pin to GND.
10	BIAS	Bias voltage output for setting driver output power by external resistors.
11	RXIN	Modulated input signal to the receiver.
12	TXOUT	Modulated output signal from the driver.
13	V_{CC}	3.0V to 5.5V analog supply voltage for the device.
14	XTAL1	I/O pins of the crystal oscillator. Connect a 4 × f_C crystal between these pins or connect XTAL1 to an 8.704MHz clock and connect XTAL2 to GND.
15	XTAL2	
-	EP	Exposed pad. Connect to ground plane for best thermal conduction.

7. Specifications

7.1. Absolute Maximum Ratings [1]

	PARAMETER	MIN	MAX	UNIT
V_{CC}, V_L	Supply voltage	–0.3	6.0	V
TXOUT, BIAS, RXIN, XTAL1, XTAL2, SYNCOUT, RES to GND.	Voltage range at coax pins	–0.3	V_{CC} + 0.3	V
TXIN, RXOUT, DIR, DIRMD1,DIRMD2 to GND	Voltage at logic pins	–0.3	V_L + 0.3	V
TXOUT to V_{CC} or GND	TXOUT output current	Internally limited		mA
SYNCOUT to V_{CC} or GND	SYNCOUT output current	Internally limited		mA
All Other Pins	Max in/out current	–20	20	mA
T_J	Junction temperature		150	°C
T_{STG}	Storage temperature	–65	150	°C

Note:

1. The stresses listed under “Absolute Maximum Ratings” are stress ratings only, not for functional operation condition. Exposure to absolute maximum rating conditions for extended periods may cause permanent damage to the device.

7.2. ESD Ratings

		VALUE	UNIT
V_{ESD} Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, RXIN and TXOUT to GND.	±8000	V
	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001，all other pins[1]	±2000	
	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[2]	±1000	

Notes:

1. Per JEDEC document JEP155, 500V HBM allows safe manufacturing of standard ESD control process.
1. Per JEDEC document JEP157, 250V CDM allows safe manufacturing of standard ESD control process.

7.3. Thermal Information

THERMAL METRIC		QFN16	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	51.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	69.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	24.2	°C/W
$R_{\theta JC(bottom)}$	Junction-to-case (bottom) thermal resistance	26.1	°C/W

7.4. Recommended Operating Conditions

PARAMETER			MIN	NOM	MAX	UNIT
V_{CC}	Analog supply voltage		3	5	5.5	V
V_L	Logic supply voltage		1.6	3.3	5.5	V
V_{IN}	Input signal amplitude at RXIN				1.12	Vpp
$1/t_{UI}$	Data signaling rate		9.6		115.2	kbps
V_{IH}	High-level input voltage	TXIN, DIRMD1, DIRMD2	0.7 x V_L		V_L	V
		XTAL1, XTAL2	0.7 x V_{CC}		V_{CC}	
V_{IL}	Low-level input voltage	TXIN, DIRMD1, DIRMD2	0		0.3 x V_L	V
		XTAL1, XTAL2	0		0.3 x V_{CC}	
R1	Bias resistor between BIAS and RES			4.1		kΩ
R2	Bias resistor between RES and GND			10		kΩ
R_{SYNC}	Pullup resistor between SYNCOUT and V_{CC}			1		kΩ
V_{RES}	Voltage at RES pin		0.7		1.5	V
f_{OSC}	Oscillator frequency		–30ppm	8.704	30ppm	MHz
C_C	Coupling capacitance between RXIN and coax (channel)			100		nF
C_{BIAS}	Capacitance between BIAS and GND			1		µF
T_A	Operating free-air temperature		–40		125	°C
T_J	Junction temperature		-40		150	°C

7.5. Electrical Characteristics

7.5.1. DC Characteristics

Over recommended operating conditions (unless otherwise noted).

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{CC}	Supply current	TXIN = L (active)	DIRMD1 = L DIRMD2 = H		30.5	44	mA
		TXIN = H (quiescent)			30	43	mA
		TXIN = 115.2kbps, 50% duty cycle			30.3	44	mA
		DIRMD1 = DIRMD2 = H (standby)			13.5	25	mA
I_L	Logic supply current	TXIN = H, RXIN = DC input				50	µA
PSRR_RX[1]	Receiver power supply rejection ratio	3.0V ≤ VCC ≤ 5.5V, $V_{TXIN} = V_L$		45			dB
PSRR_TX[2]	Output power supply rejection ratio	3.0V ≤ VCC ≤ 5.5V, $V_{TXIN} = 0$		45			dB
T_{JSD_RISE}	Thermal shutdown, temperature rise				180		°C
T_{JSD_FALL}	Thermal shutdown, temperature fall				150		°C
T_{JSD_HYS}	Thermal shutdown hysteresis				30		°C

Notes:
1. PSRR_RX is defined as $\Delta V_{RXIN}/\Delta V_{CC}$ at DC.
2. PSRR_TX is defined as $\Delta V_{TXOUT}/\Delta V_{CC}$ at DC.

7.5.2. Logic I/O

Over recommended operating conditions (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	Logic-output high threshold voltage (RXOUT, DIR)	RXOUT, DIR source 3.3mA	0.9 x V_L			V
V_{OL}	Logic-output low threshold voltage (RXOUT, DIR)	RXOUT, DIR sink 3.3mA			0.1 x V_L	V
I_{TXIN_IH}	Input high leakage current	$V_{TXIN} = V_L$			1	µA
I_{TXIN_IL}	Input low leakage current	$V_{TXIN} = 0V$	–1			µA
I_{IH}	Input leakage Current	DIRMD1, DIRMD2 shorted to V_L			50	µA
I_{IL}		DIRMD1, DIRMD2 shorted to GND	–1			µA

7.5.3. XTAL Input and SYNCOUT Output

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{XTAL_IH}	Input high leakage current	$V_{XTAL} = V_{CC}$			10	µA
I_{XTAL_IL}	Input low leakage current	$V_{XTAL} = 0V$	–1			µA
V_{SYNC_OL}	Output low voltage	SYNCOUT source 3.3mA			0.4	V

7.5.4. Receiver Filter

Over recommended operating conditions (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{PB}	Passband	$V_{RXIN} = 1.12V_{P-P}$	1.1		4.17	MHz
f_{REJ}	Receiver rejection range	2.176MHz carrier amplitude of 112.4 mV_{PP}, Frequency band of spurious components with 800mV_{PP} allowed.	1.1		4.17	MHz
t_{noise_filter}	Receiver noise filter time	DIRMD1/2 set for 9.6kbps data rate.		4		µs
		DIRMD1/2 set for >9.6kbps data rate		2		µs

7.5.5. Receiver

Over recommended operating conditions (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IT}	Threshold voltage range	f_{RXIN} = 2.176MHz	–18	–15	–12	dBm
			79.6	112.4	158.8	mV_{P-P}
Z_{IN}	Input impedance	$f = f_O$	11	18		kΩ

7.5.6. Transmitter

Over recommended operating conditions (unless otherwise noted).

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OUT}	TXOUT output on level	V_{RES} = 1.5V (maximum		10.5	12		dBm
				2.12	2.52		V_{P-P}
		V_{RES} = 0.7V (minimum)			5.38	6.28	dBm
					1.17	1.3	V_{P-P}
f_O	TXOUT Output frequency				2.176		MHz
Δf_O[1]	TXOUT Output frequency variation					±100	ppm
P_{OZ}	Output off power level at TXOUT	TXIN = V_L	At TXOUT			1	mV_{P-P}
			At coax out			–60	dBm
	Output Emission Profile [2]			Conforms to AISG spectrum emissions mask 3GPP TS 37.461, see Figure 10-1.			
Z_O	TXOUT Output impedance	DC			0.03		Ω
		f_{SW} = 10MHz			3.5		
I_{SC}	TXOUT short-circuit protection	Short to GND or V_{CC}				±200	mA

Notes:

1. Output frequency variation determined by external crystal tolerance.
2. Guaranteed by design with a recommended 470pF capacitor between RXIN and ground. Measurements above 150MHz are determined by setup.

7.5.7. Switching Characteristics

Over recommended operating conditions (unless otherwise noted).

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{RX}	Receiver propagation delay	RXIN to RXOUT, DIRMD1 = DIRMD2 = 0V			7	10	µs
		RXIN to RXOUT, DIRMD1 = V_L, DIRMD2 = 0V (38.4kbps), or DIRMD1 = 0V, DIRMD2 = V_L (115.2kbps)			5	10	µs
t_R, t_F	Receiver output rise and fall time	t_R: 10% to 90%; t_F: 90% to 10%; R_L = 1kΩ, C_L = 10pF			8	20	ns
t_{TX}	Transmitter propagation delay	TXIN to TXOUT				3	µs
t_{DIR_SKEW}[1]	Direction control skew (DIR to RXOUT)			270	670		ns
t_{DIR}	Direction control active duration	DIRMD1 = DIRMD2 = 0V (9.6kbps)			1667		µs
		DIRMD1 = V_L, DIRMD2 = 0V (38.4kbps)			417		
		DIRMD1 = 0V, DIRMD2 = V_L (115.2kbps)			137		
ΔDC	Coax receiver output duty cycle	RXIN fed by an OOK 2.176MHz sinusoidal signal with 50% duty cycle [2]	RXIN = 0dBm			±10	%
			RXIN = –10dBm			±10	

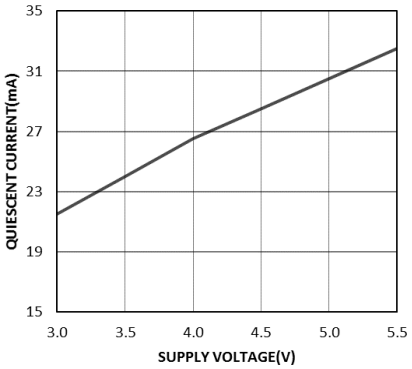
Notes:

1. See Figure Figure 8-2.
2. ±2µs envelope rise/fall.

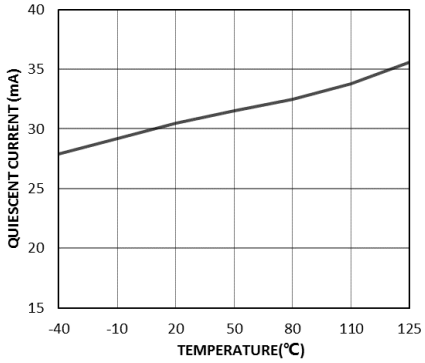
7.6. Typical Operating Characteristics and Waveform

Over recommended operating conditions, unless otherwise noted.

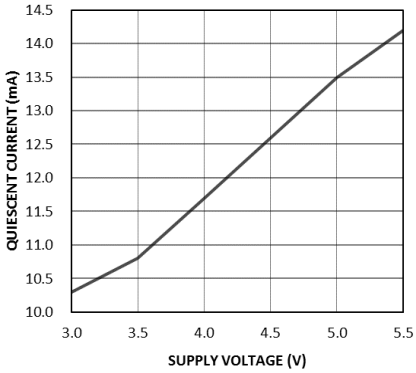
QUIESCENT CURRENT vs SUPPLY VOLTAGE



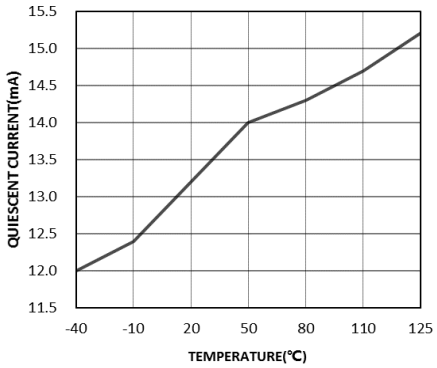
QUIESCENT CURRENT vs TEMPERATURE



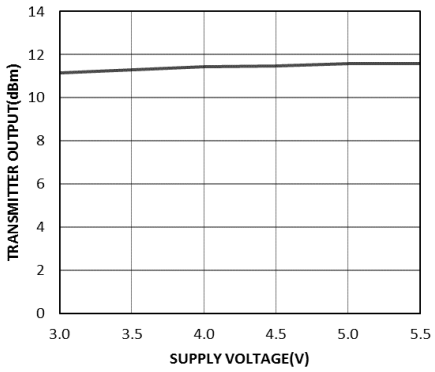
QUIESCENT CURRENT vs SUPPLY VOLTAGE in STANDBY MODE



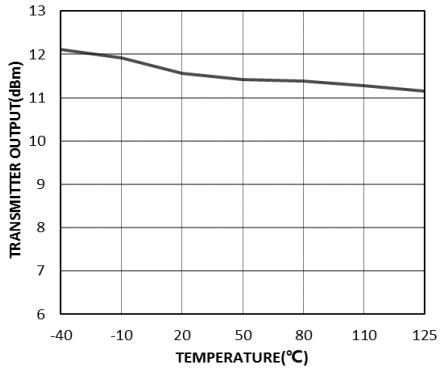
QUIESCENT CURRENT vs TEMPERATURE in STANDBY MODE



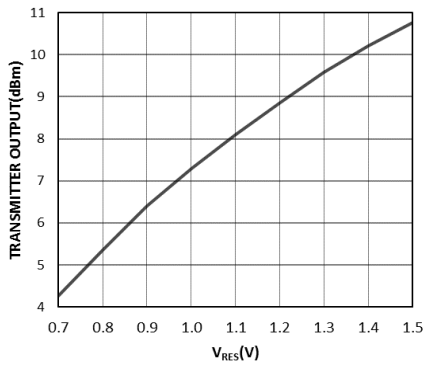
MAXIMUM TRANSMITTER OUTPUT vs SUPPLY VOLTAGE



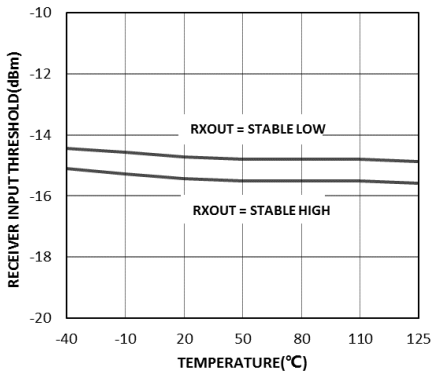
MAXIMUM TRANSMITTER OUTPUT vs TEMPERATURE



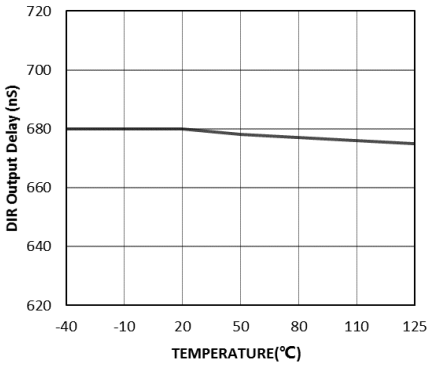
TRANSMITTER OUTPUT
vs V_{RES}



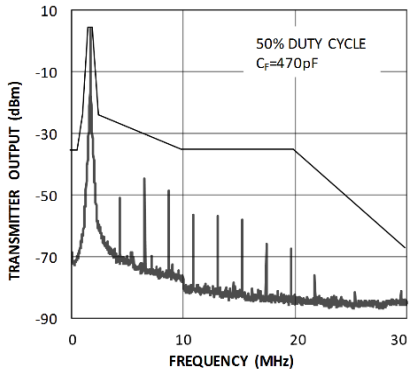
RECEIVER INPUT THRESHOLD
vs TEMPERATURE



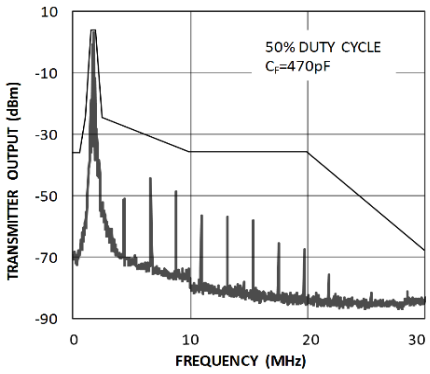
DIR TO RECEIVER OUTPUT DELAY
vs TEMPERATURE



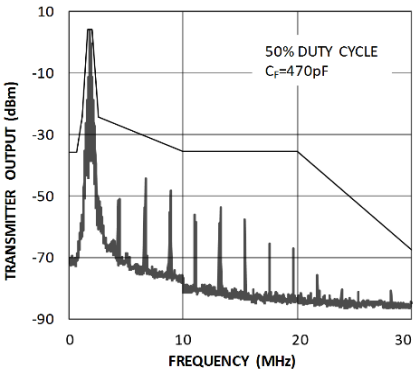
TRANSMITTER OUTPUT SPECTRUM
vs FREQUENCY (9.6kbps)



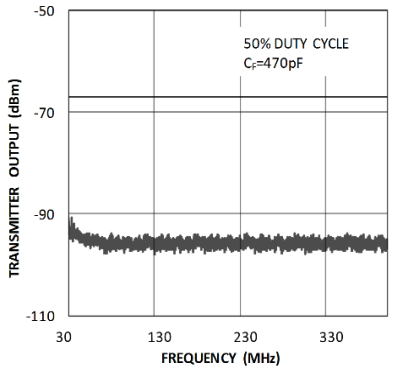
TRANSMITTER OUTPUT SPECTRUM
vs FREQUENCY (38.4kbps)



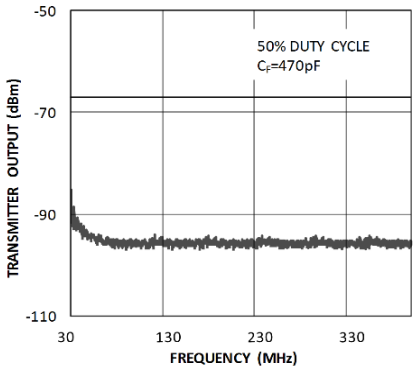
TRANSMITTER OUTPUT SPECTRUM
vs FREQUENCY (115.2kbps)



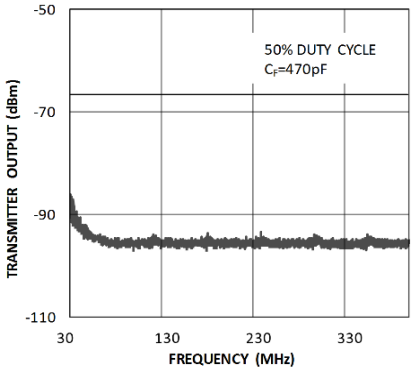
TRANSMITTER OUTPUT SPECTRUM
vs FREQUENCY (9.6kbps)



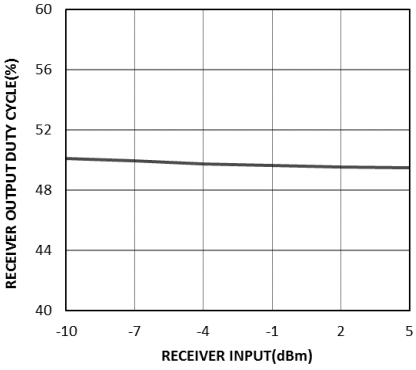
TRANSMITTER OUTPUT SPECTRUM
vs FREQUENCY (38.4kbps)



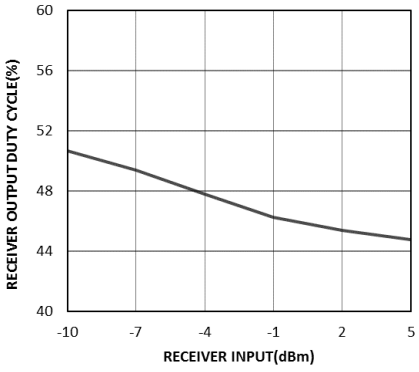
TRANSMITTER OUTPUT SPECTRUM
vs FREQUENCY (115.2kbps)



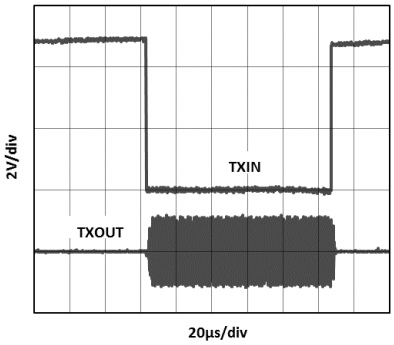
RECEIVER OUTPUT DUTY CYCLE
vs RECEIVER INPUT (9.6kbps)



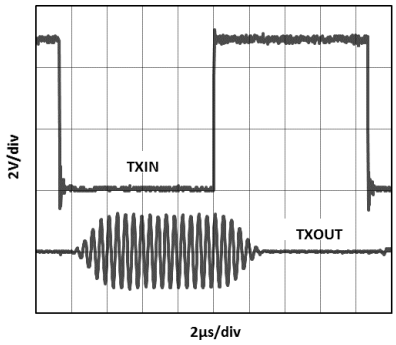
RECEIVER OUTPUT DUTY CYCLE
vs RECEIVER INPUT (115.2kbps)



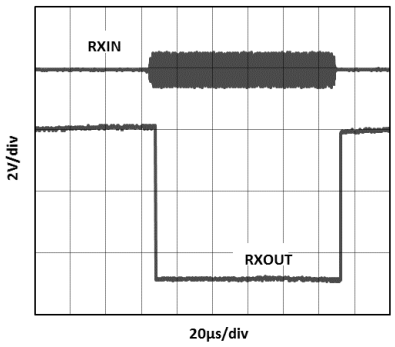
TRANSMITTER PROPAGATION DELAY
AT 9.6kbps



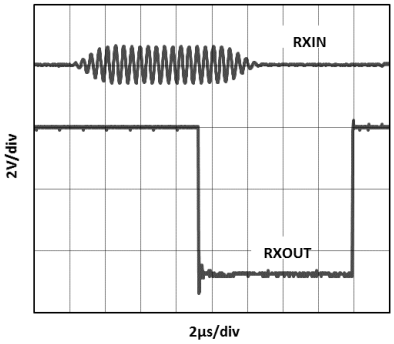
TRANSMITTER PROPAGATION DELAY
AT 115.2kbps



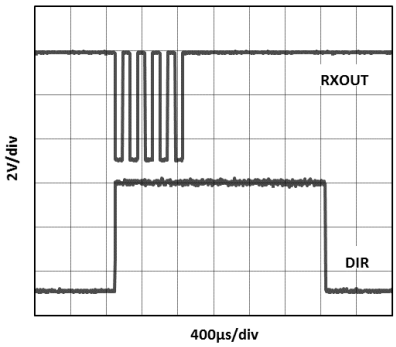
RECEIVER PROPAGATION DELAY
AT 9.6kbps



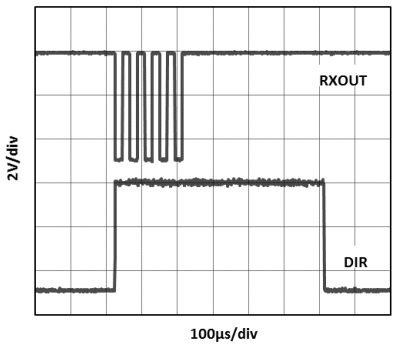
RECEIVER PROPAGATION DELAY
AT 115.2kbps



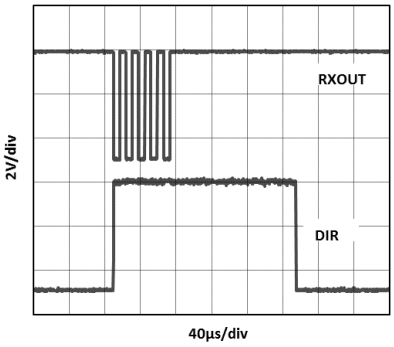
RECEIVER OUTPUT TO DIR
AT 9.6kbps



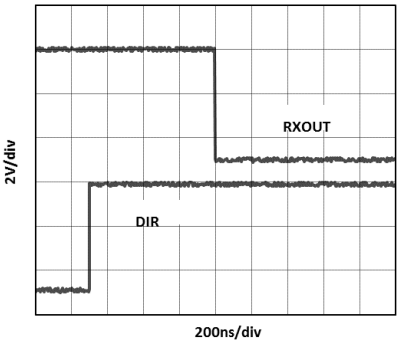
RECEIVER OUTPUT TO DIR
AT 38.4kbps



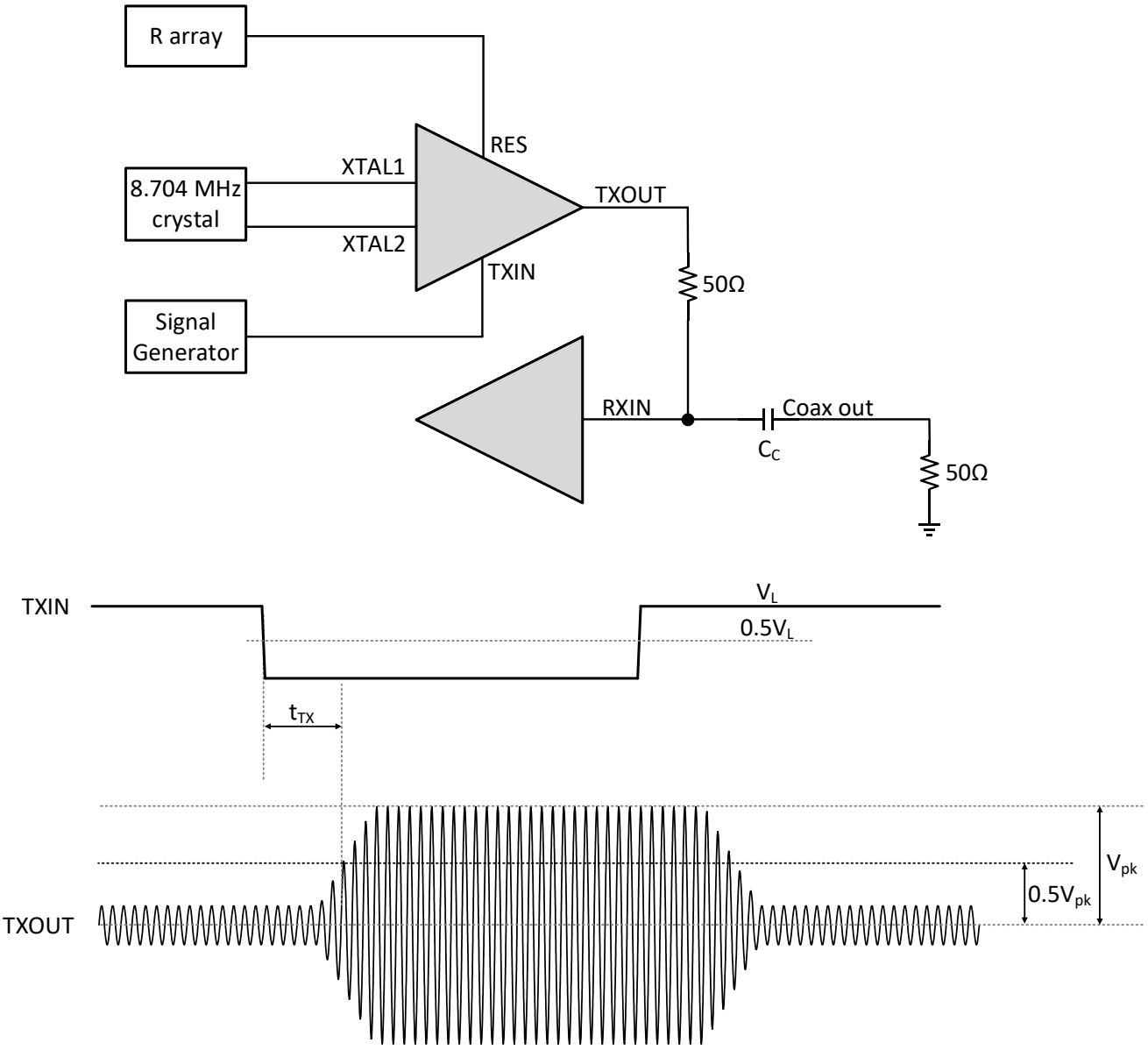
RECEIVER OUTPUT TO DIR
AT 115.2kbps



DIR TO RECEIVER OUTPUT



8. Parameter Measurement Information



Notes:

1. Signal generator rate is 115kbps, 50% duty cycle, rise and fall times less than 6 ns, nominal output levels 0V and 3.3V.
2. Coupling capacitor Cc is 100nF.

Figure 8-1. Measurement of Modem Driver Output Voltage With 50 Ω Loads

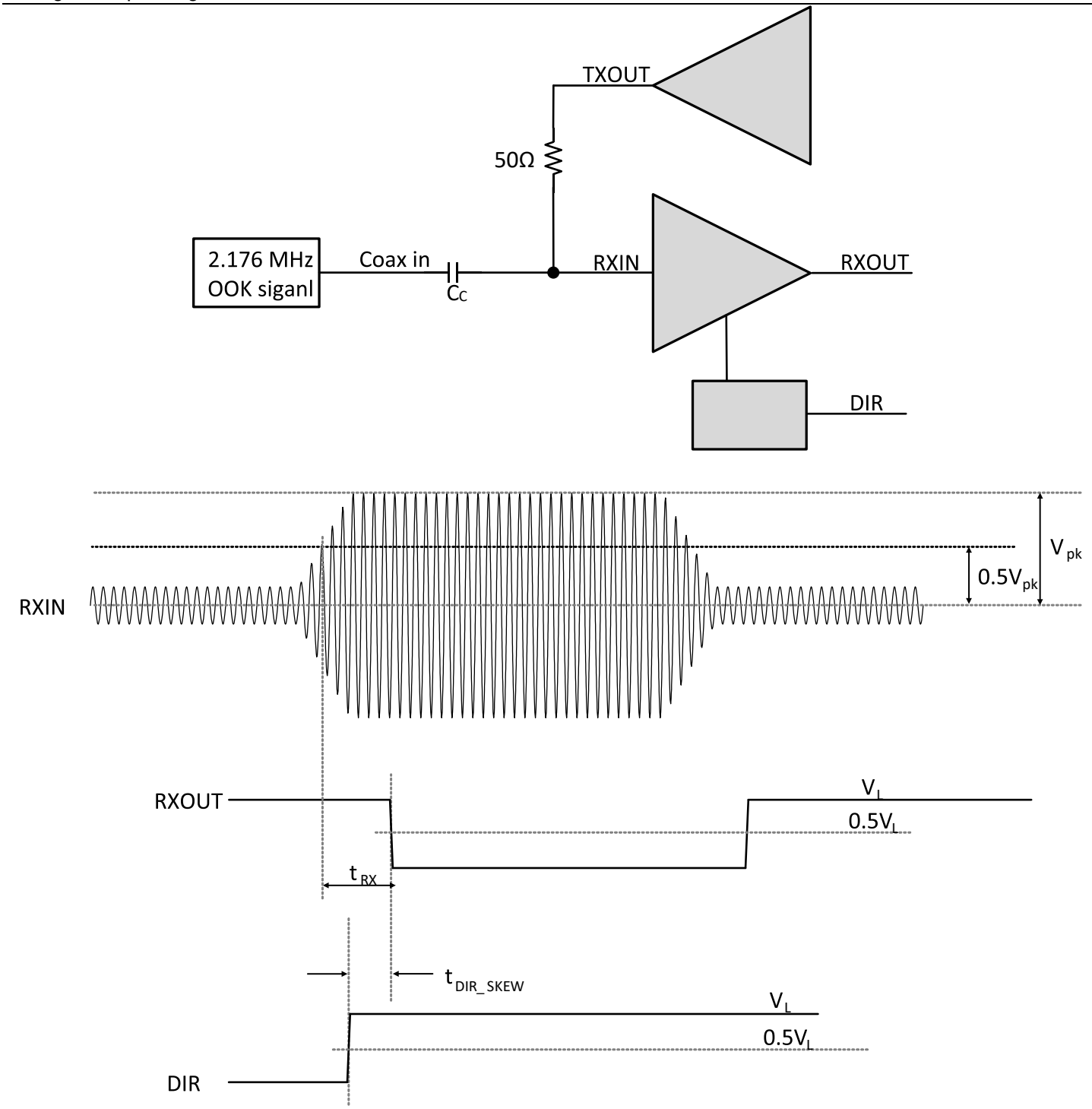


Figure 8-2. Measurement of Modem Receiver Propagation Delays

9. Detailed Description

9.1. Overview

AISG defines a protocol for communication between the base station and the tower equipment that uses a 2.176MHz sine-wave carrier with on-off-key (OOK) modulation. The communication is bidirectional, half-duplex, with a master (the base station) and a slave (the tower). The communication remotely changes the tilt of the antenna (RET) with commands from the base station. Also it monitors the status of the equipment in the tower, such as the RET and TMA (tower mounted amplifiers). The CA-IF4023 integrated AISG transceiver is designed to be compliant with Antenna Interface Standards Group v3.0 specification. These transceivers modulate and demodulate signals to support the data transmission between the base-station and the tower. This device supports up to 115.2kbps data rate.

The CA-IF4023 transmitter includes an OOK modulator; a bandpass filter that is compliant with the AISG spectrum-emission profile and operates around 2.176MHz; and an output amplifier with +5.4dBm to +12dBm (-0.6dBm to +6dBm at coax output) configurable output level to compensate for loss in the external circuitry and cabling. The OOK carrier is generated by applying an external crystal at 8.704MHz to the OOK internal modulator through the XTAL1 and XTAL2 pins. An external clock source at the same frequency can also be applied to XTAL1 by connecting XTAL2 to ground. The receiver includes an OOK demodulator and a comparator that reconstruct the digital signal, the input threshold of the receiver is -15dBm. It also includes a bandpass filter that operates around the 2.176MHz center frequency with narrow bandwidth to enable demodulation of signals even in the presence of spurious frequency components.

9.2. Device Functional Modes

The CA-IF4023 provides a direction output pin (DIR) that indicates the direction of the data flow to facilitate RS-485 bus arbitration in the tower equipment (slave) without involving the microcontroller. The base station (master) determines the direction of the data flow, while the tower equipment (slave) decodes the information and responds to commands from the master. See Figure 10-3 the Typical Application Circuit (Tower) that shows how the CA-IF4023 can be used in the tower in conjunction with the RS-485 transceiver such as the CA-IF4805. When the CA-IF4023 is located in the tower, the output DIR drives the driver output enable DE and receiver output enable REB of the RS-485 transceiver. Whenever the data are coming from the base station and are being demodulated at RXOUT, the direction output, DIR, on the transceiver chip is set to high to put the RS485 transceiver into driving mode to drive the RS-485 bus. DIR is released within 16 bit-times after the last stop bit. This interval is in compliance with the AISG protocol, which requests that the bus be released within 20 bit-times. On the other side, when the data flows in the opposite direction, from TXIN to TXOUT, or there is no valid signals at both TXIN and RXIN, the output DIR is asserted low. The CA-IF4023 internal state machine is sensing both the TXIN and RXIN lines, and can recognize the correct flow of data and avoid asserting the DIR high. The device stays in either RECEIVE or TRANSMIT mode until DIR Timeout (nominal 16 bit times) after the last activity on RXOUT or TXIN.

Figure 9-1 and Figure 9-2 show the timing diagrams of the DIR functionality. The direction control output DIR automatically toggles based on activity present on the coaxial input interface, and has an adjustable time constant in order to accommodate the signaling rates of 9.6kbps, 38.4kbps and 115.2kbps. When not in standby mode, the device operates as below status,

1) If there is no valid signals at RXIN and TXIN, the device state is in the default IDLE mode (power-on state). When in IDLE mode, RXOUT is High, and TXOUT is quiet, DIR is asserted low.

2) When the data flows from RXIN to RXOUT, the device transitions to RECEIVE mode, RXOUT responds to all valid modulated signals on RXIN, whether from the a remote transmitter, or long noise burst. The transmitter blocks all signals on Tx channel and TXOUT is quiet. DIR remains high for 16 bit-times after the last logic-level high bit within the 8-bit protocol data. Then DIR is asserted low and the devices transitions to IDLE mode. This is compliant with the AISG specification saying that the RS-485 transmitter stops driving the bus within 20 bit-times after the last stop bit is sent, see Figure 9-1.

3) When the data flows from TXIN to TXOUT, the device transitions to TRANSMIT mode. RXOUT stays high regardless of the input signal on RXIN; TXOUT responds to TXIN, generating 2.176 MHz signals on TXOUT when TXIN is Low, and TXOUT is quiet when TXIN is High. The device stays in TRANSMIT mode until 16 bit times after TXIN goes High, see Figure 9-2.

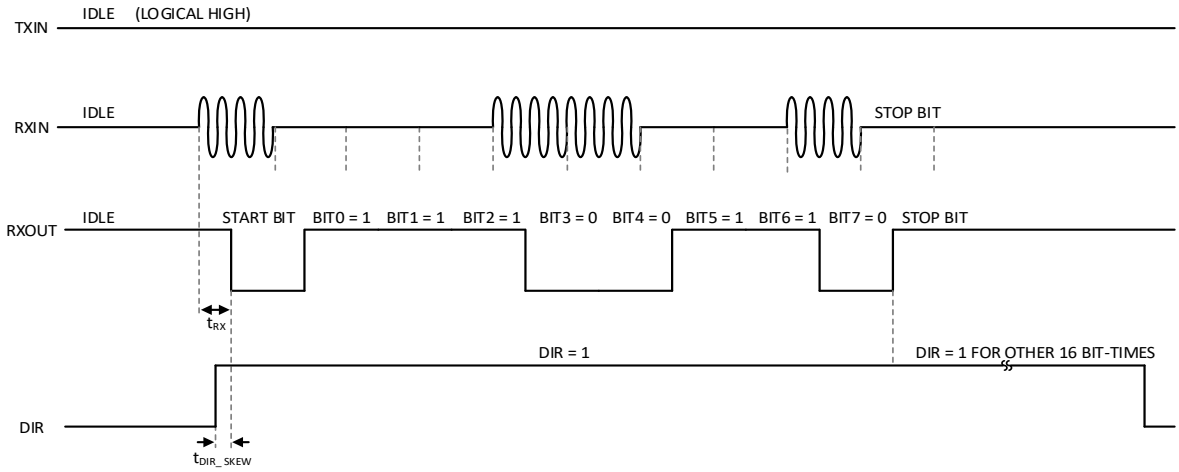


Figure 9-1. Communication Flow is from RXIN to RXOUT

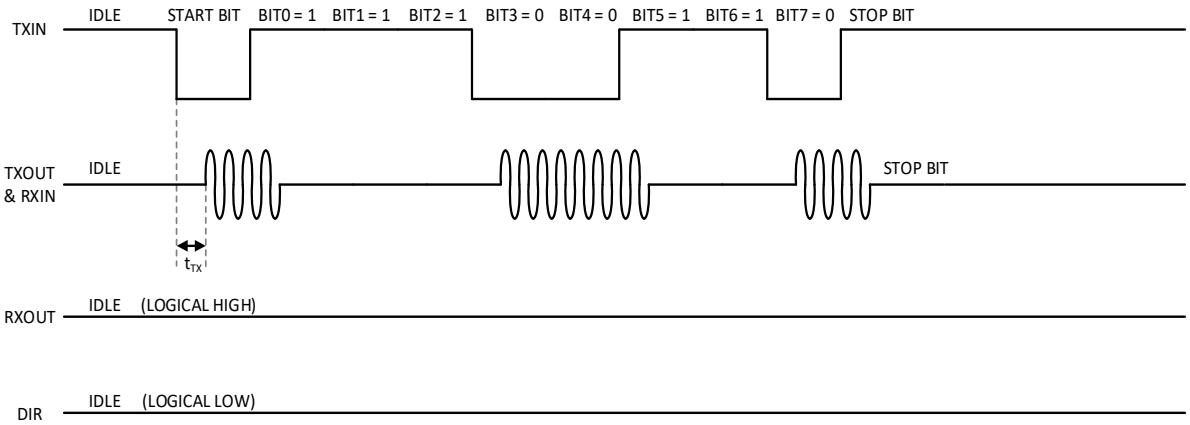


Figure 9-2. Communication Flow is from TXIN to TXOUT

The time constant for the direction control function can be set by the control mode pins, DIRMD2 and DIRMD1. These pins should be set to correspond to the desired data rate, as shown in Table 9-1. If DIRMD2 and DIRMD1 are in a logic High state, the device will be in standby mode. While in standby mode, both receiver and transmitter circuits are not active, the RXOUT pin is HIGH and the TXOUT pin is quit regardless of the logic state of RXIN and TXIN. The supply current in standby mode is significantly reduced.

Table 9-1. Bit-Time Duration Selector

DIRMD2[1]	DIRMD1[1]	AISG data rate (kbps)	Unity bit time (μs)
0	0	9.6	104.16
0	1	38.4	26.04
1	0	115.2	8.68
1	1	Standby[2]	Standby[2]

Notes:
1. DIRMD1 and DIRMD2 are internally pulled down.
2. While in standby mode, RXOUT is High, and TXOUT is quiet, do not respond any input signals.

10. Application Information

The AISG On-Off Keying (OOK) interface allows for command, control, and diagnostic information to be communicated between a base station and the corresponding tower-mounted antennae. Figure 10-2 and Figure 10-3 show the functionality of the CA-IF4023 as well as the system-level implementation of the AISG at the base station and the tower. On the base station side, the FPGA transmits and receives digital data to and from the CA-IF4023, which modulates and demodulates the OOK signal at the coaxial cable. On the tower side, the AISG transceiver interfaces between the OOK signal at the cable and the RS485 digital signal at the left side of the RS-485 transceiver. The CA-IF4023 's direction output (DIR) drives the direction of the data within the RS-485 transceiver.

10.1. Emission Output Profile

The AISG standard defines the maximum spectrum emission that all the OOK modulating devices must be compliant with, see Figure 10-1. The CA-IF4023 is compliant with the AISG standard. An external 470pF capacitor connected between RXIN and ground is recommended for compliance above 25MHz. The 50Ω termination is connected serially between TXOUT and the feeder cable. It acts as series termination for the transmitting path with data flowing from TXIN to TXOUT and acts as parallel termination when data is being received on RXIN, see Figure 10-2 and Figure 10-3. The output of the transmitter is biased at 1.5V to maximize the power-supply rejection ratio and minimize the emission. It is recommended that the device be AC-coupled to the feeder cable through either an external RF filter or a series 100nF capacitor.

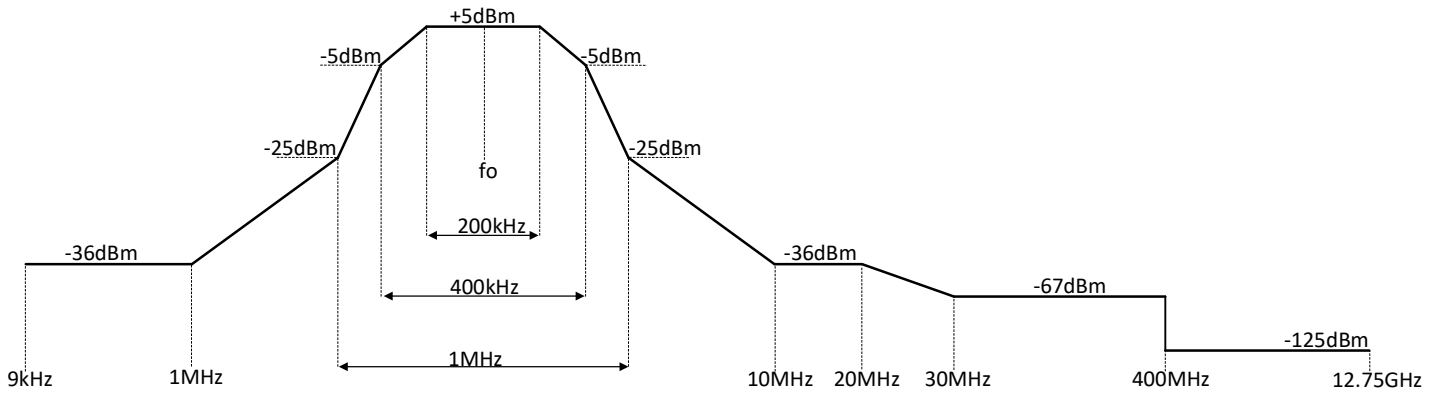


Figure 10-1. Emissions Spectrum with 50% Duty-Cycle OOK, Conforms to AISG TS 37.461

10.2. Receiver-Input Range and Threshold

The maximum OOK input level at RXIN into the 50Ω external termination is 1.12V_{P-P}, corresponds to 5dBm. The CA-IF4023 internal threshold is -15dBm (112.4mVP-P) with ±3dB accuracy in compliance with the AISG standard specifications. This threshold sets the minimum input signal level. To avoid the saturation of the receiver input stage, any other adjacent carrier with power-up to +5dBm must be either below 1.1MHz or above 4.17MHz.

10.3. Transmitter Output Level Adjust

The CA-IF4023 output power at TXOUT can be set by using external resistors R1 and R2 that connect at the RES and BIAS pins as shown in the Typical Application Circuit (see Figure 10-2, Figure 10-3). A 1μF capacitor should be connected between the BIAS pin and GND. The TXOUT voltage level can be varied according to the following equations:

$$V_{TXOUT}(V_{P-P}) = 2.52V_{P-P} \times R2 / (R1 + R2)$$

The voltage at the RES pin should be from 0.7 V to 1.5 V, the value of R2 / (R1 + R2) is between 0.467 and 1. Use R1 = 0Ω (connect RES directly to the BIAS) for maximum voltage level of 2.52V_{P-P}. Assuming that the feeder cable is terminated into a 50Ω impedance, the external filter is lossless at 2.176MHz, and a series 50Ω termination is being used as in the typical application circuit (see Figure 10-2, Figure 10-3), the output level of 2.52V_{P-P} corresponds to +6dBm at the feeder cable; To obtain a nominal power level of 3dBm at the feeder cable as the AISG standard requires, use R1 = 4.1 kΩ and R2 = 10 kΩ that provide 1.78 V_{PP} at TXOUT.

10.4. External Clock

The CA-IF4023 integrated AISG transceiver operates with an external crystal at 4x the 2.176MHz frequency, or 8.704MHz. The crystal is required to achieve the ±100ppm frequency stability specification of the AISG standard. A crystal with ±30ppm is recommended along with two 40pF (±10% tolerance) capacitors connected to ground, see Figure 10-2 and Figure 10-3 the typical application circuit . Multiple CA-IF4023 devices can share the same crystal by using the SYNCOUT pin. One device acts as a master and provides the 8.704MHz clock signal to the slave device(s) through SYNCOUT. To configure a device as a slave, XTAL2 should be connected to ground. The external clock coming from the master device feeds the XTAL1 pin of the slave device through a series 10kΩ resistor. Connect a 1kΩ pull-up resistor to V_{CC} from the SYNCOUT pin of the master device.

10.5. Power Supply

The CA-IF4023 has two power supply pins: the analog power supply pin V_{CC} and the logic power supply pin V_L. V_{CC} should be operated from 3 V to 5.5 V, while V_L can range from 1.6 V to 5.5 V to interface to different logic levels. Power supply decoupling capacitances of at least 0.1μF should be placed as close as possible to each power supply pin.

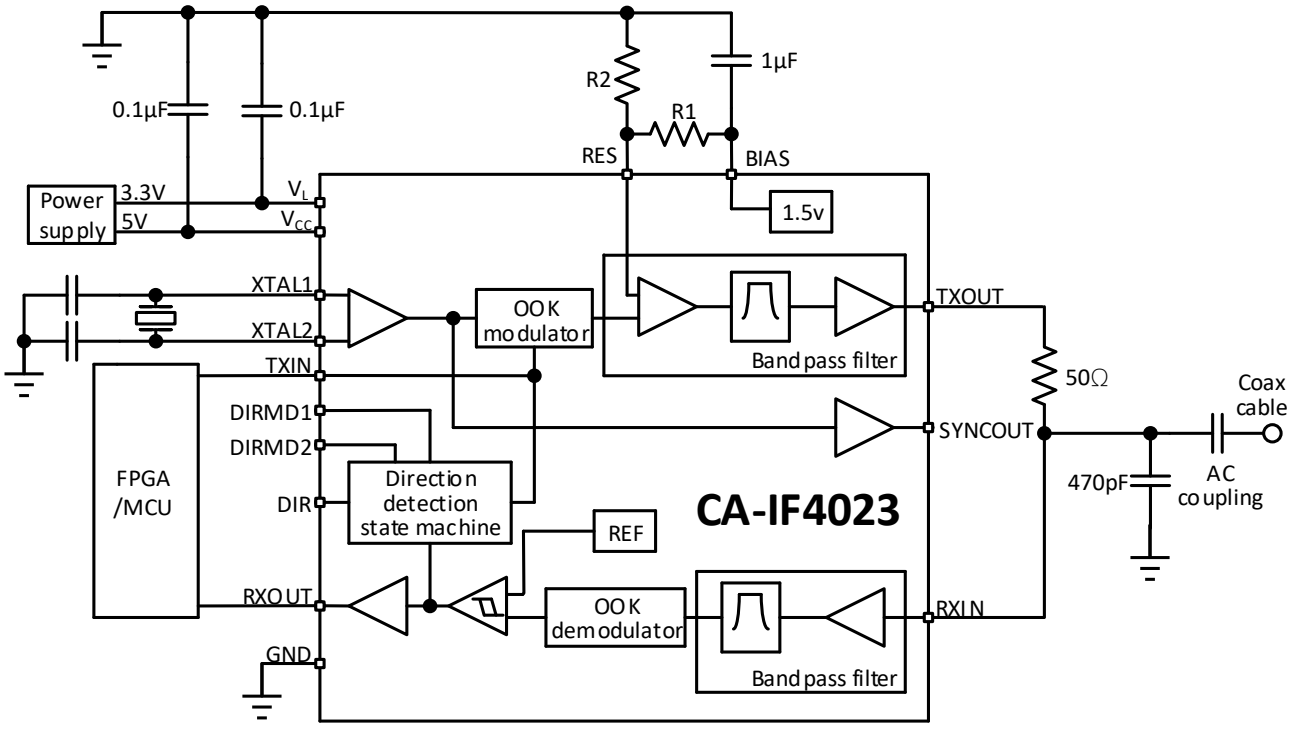


Figure 10-2. CA-IF4023 Typical Application Circuit (Base Station)

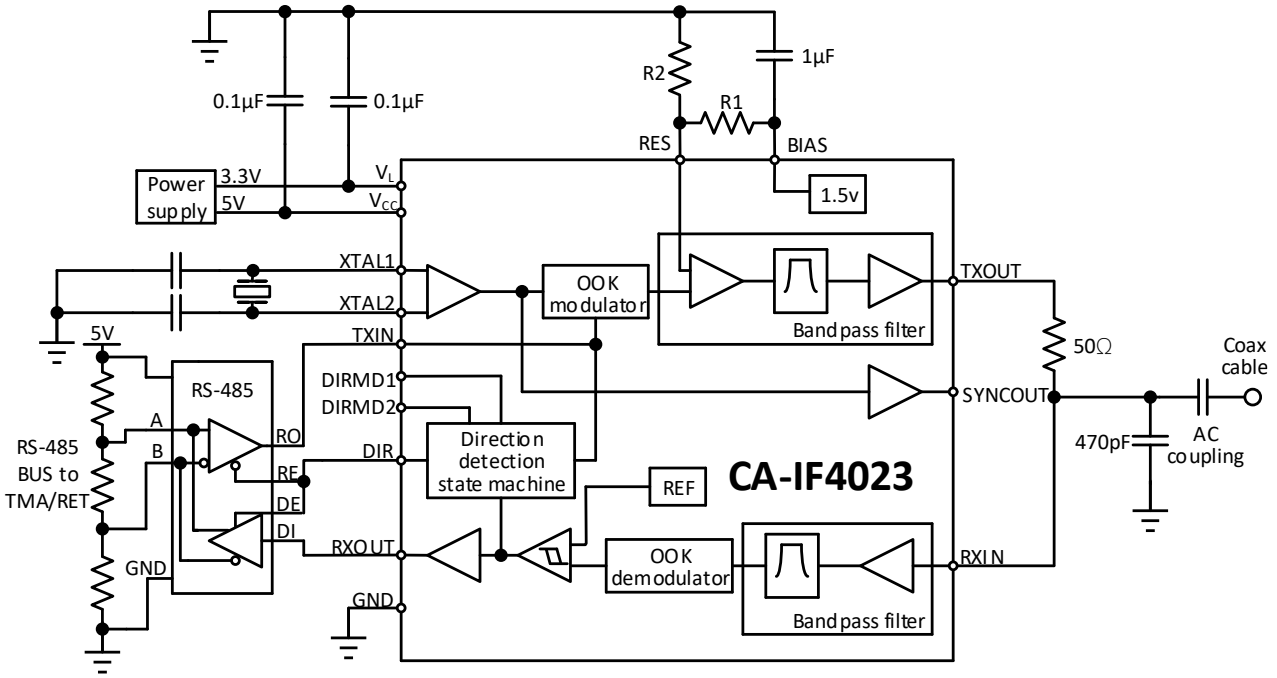


Figure 10-3. CA-IF4023 Typical Application Circuit (Tower)

11. Package Information

QFN16 Package Outline

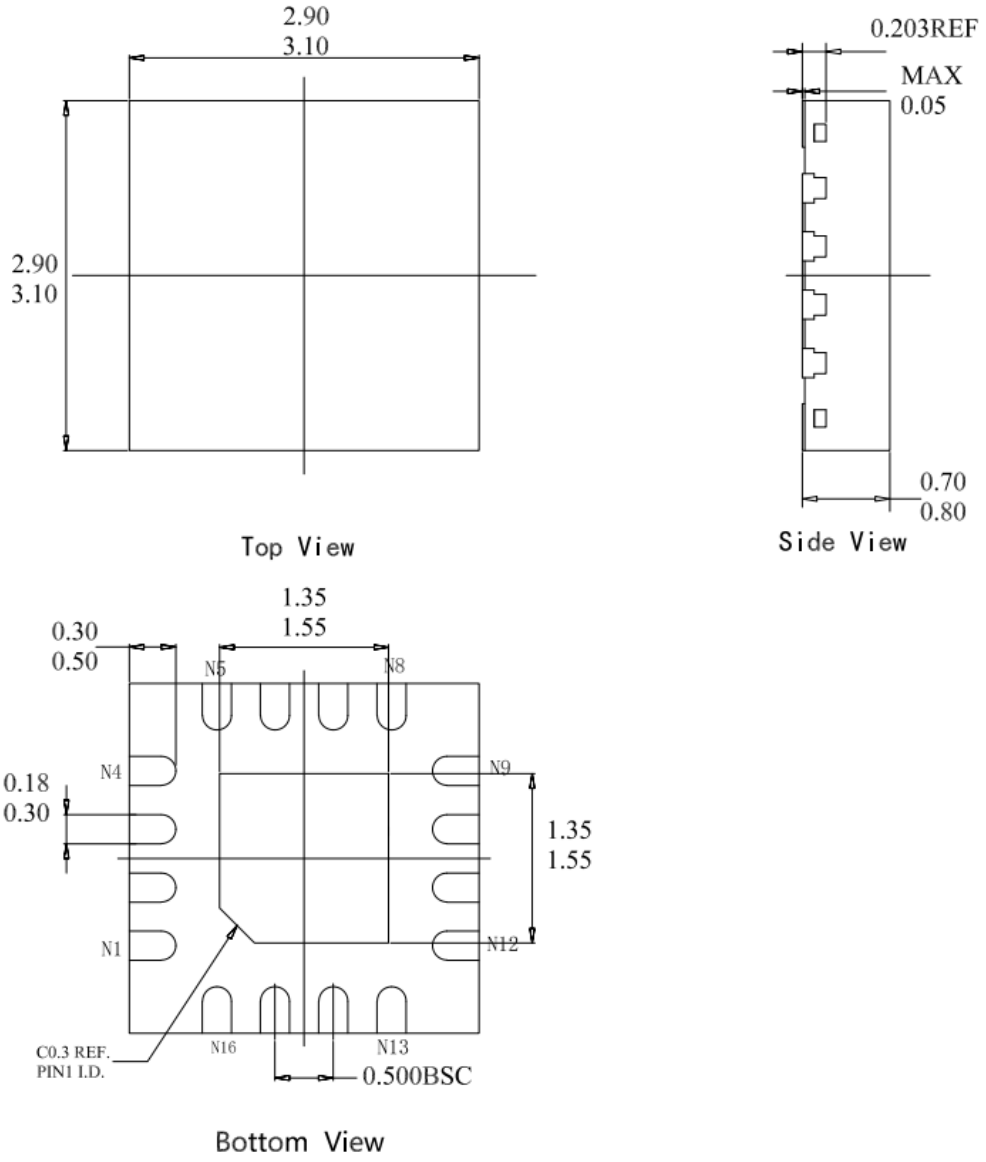


Figure 11-1 16-pin QFN Package Dimension Drawing

12. Soldering Temperature (reflow) Profile

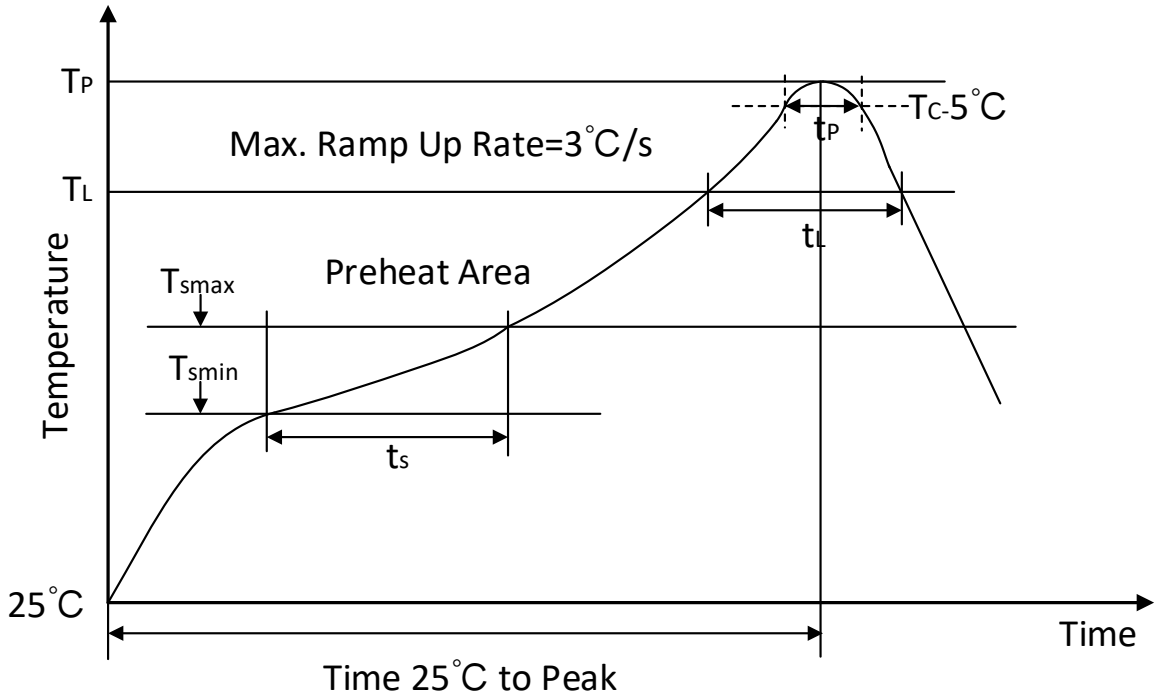


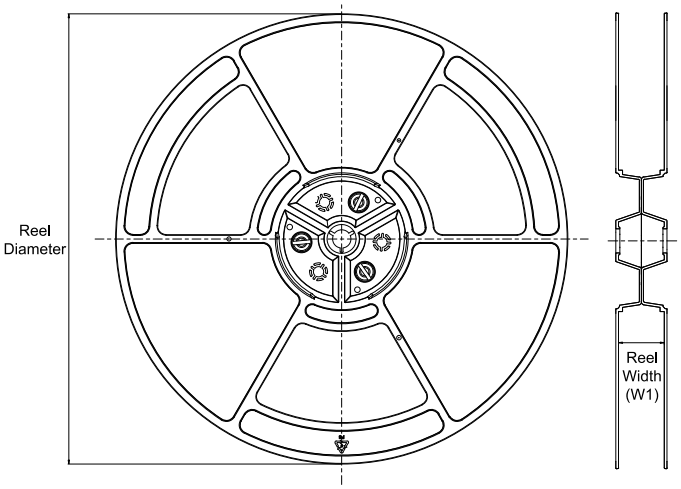
Figure 12-1. Soldering Temperature (reflow) Profile

Table 12-1. Soldering Temperature Parameter

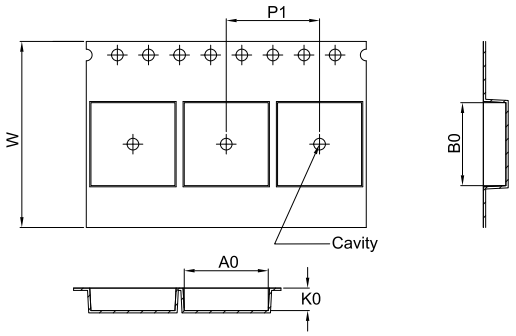
Profile Feature	Pb-Free Assembly
Average ramp-up rate(217 ℃ to Peak)	3℃/second max
Time of Preheat temp(from 150 ℃ to 200 ℃	60-120 second
Time to be maintained above 217 ℃	60-150 second
Peak temperature	260 +5/-0 ℃
Time within 5 ℃of actual peak temp	30 second
Ramp-down rate	6 ℃/second max.
Time from 25℃ to peak temp	8 minutes m

13. Tape and Reel Information

REEL DIMENSIONS

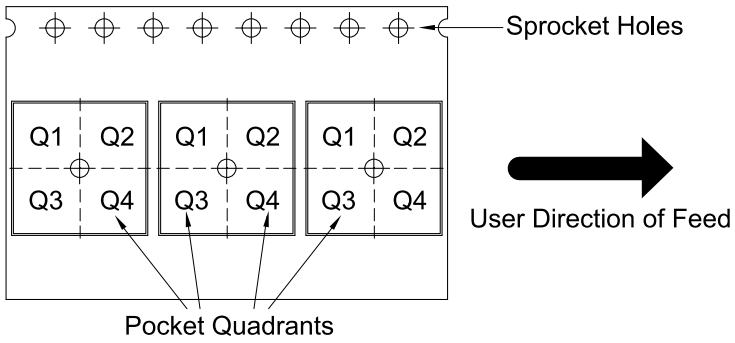


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CA-IF4023	QFN16	F	16	3000	330	12.4	3.35	3.35	1.13	8.0	12.0	Q1

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