EMI-Optimized Design for the CA-IS364x Quad-channel Digital Isolators

Contents

1. Introduction

This document is designed to complement the CA-IS364x data sheet to provide a low-EMI design solution for multi-channel digital isolators. This application note discusses EMI suppression methods, provides a reference design and the test result according to EN55032(CISPR32) Class-B standard with 30MHz to 1GHz frequency range for the CA-IS364x based on a 2-layer board design. Also refer AN001.pdf (chipanalog.com) for more details about EMI optimized design.

The CA-IS364x typical application circuit is shown in Figure 1-1.

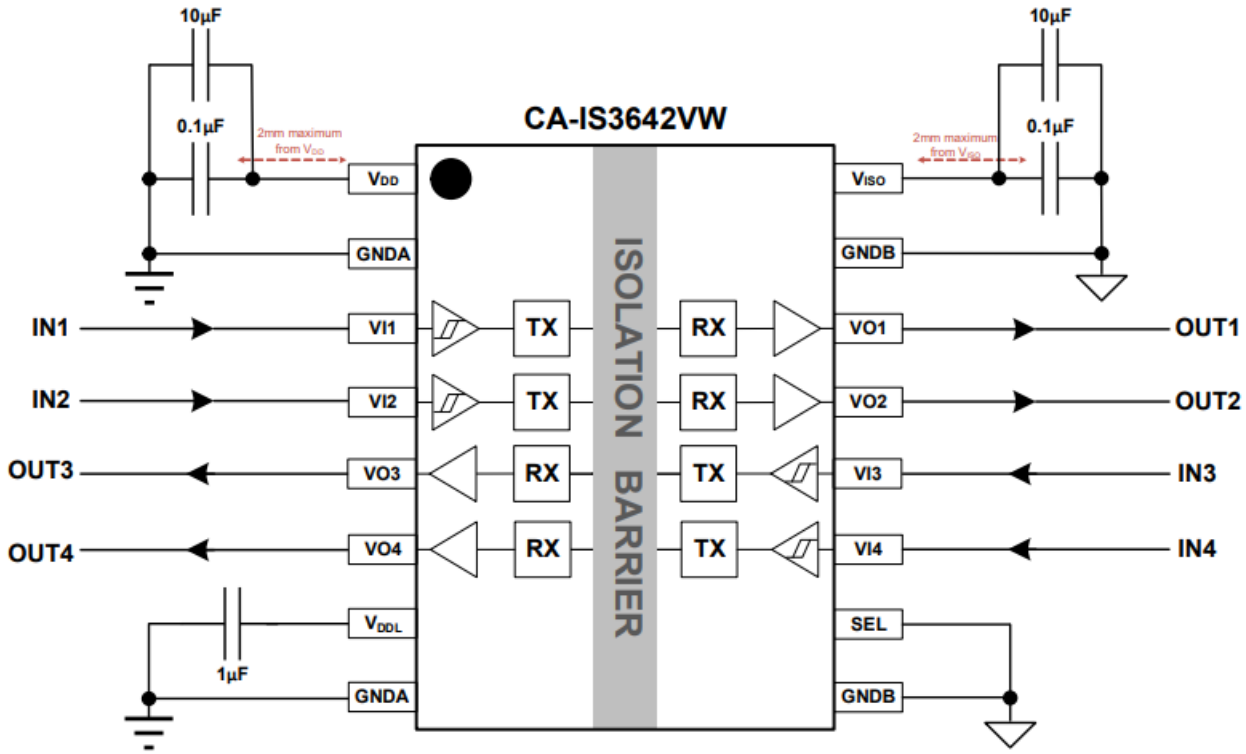

Figure 1-1. Typical application circuit

2. EMI-Optimized Design

2.1. CA-IS364x General Description

The CA-IS364x quad-channel digital isolators integrate most of the components needed for digital isolation application, a high-efficiency, low-emissions isolated DC-DC converter with internal transformer and high-speed isolated data channels, into a single, compact SOIC package. This results an efficient and compact fully integrated solution that makes system level design as easy as possible. The simplified functional block diagram of a typical signal isolation channel is shown in Figure 2-1.

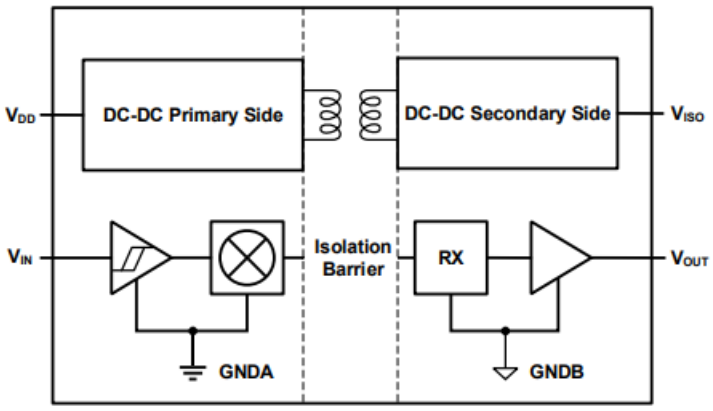

Figure 2-1. Functional block diagram of CA-IS364x

The high di/dt and dv/dt caused by on-chip transformer's high-frequency switching operation is the main radiation resource. Also, designers need to consider the common-mode noise generated by parasitic components on the primary-side and secondary-side transformer coils. The following sections provide detailed description about how to minimize EMI and reflections.

2.2. Optimized Design and Layout

2.2.1. Decoupling Capacitor Placement

Careful PCB layout is critical to achieve clean and stable communication operation. To make sure device operation is reliable at all data rates and supply voltages, we recommend to add a minimum 10nF high-frequency bypass capacitor and a bulk energy-storage capacitor(10μF) in paralleling between the supply input V_{DD} and GNDA, and between the isolated power supply output V_{ISO} and GNDB. Selecting a 10nF to 100nF low-ESL/low-ESR MLCC capacitor as the high frequency decoupling capacitor, also these capacitors must be placed closer to V_{DD} and V_{ISO} pins, the maximum distance is within 2mm, to reduce parasitic inductance and current loop. This is very essential for optimized radiated emissions performance, see Figure 2-2 recommended decoupling capacitors placement for the PCB layout.

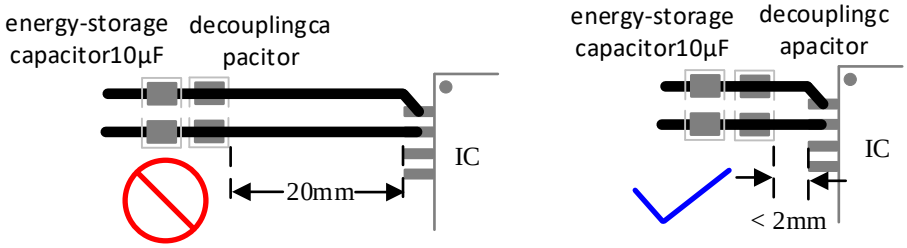

Figure 2-2. Decoupling capacitor placement

2.2.2. Y-capacitor

During high-frequency operation, the common-mode current generates a current loop between the parasitic capacitance of the primary and secondary coils, as well as the PCB parasitic capacitance. The larger the loop area, the stronger the radiation generated. It is recommended to place a Y capacitor across the isolation barrier, between the primary-side reference ground (GNDA) and secondary-side reference ground (GNDB). The Y-capacitor create a very short path with a small loop area for the parasitic current return to primary side, reducing the EMI generated on the board as shown in Figure 2-3. The larger capacitance value can better suppress EMI.

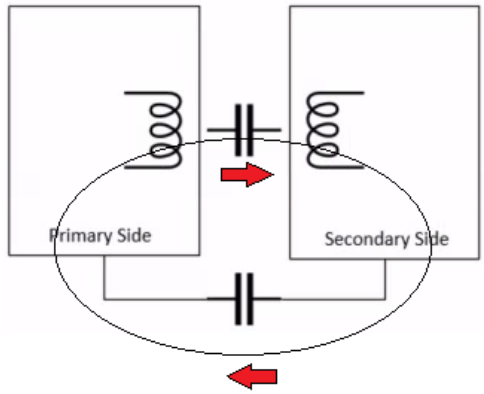

Figure 2-3. Y-capacitor across the isolation barrier

2.2.3. Ferrite Bead/Common-mode Inductor/Differential-mode Inductor

On the primary-side, a pair of ferrite beads with a high frequency impedance in the range of 1KΩ to 2KΩ @ 100MHz are inserted on the power line and ground line respectively, thereby breaking the path of larger common-mode current loops. This offers further high-frequency attenuation and blocks the switching noise. Place the bead close to decoupling capacitors as shown in Figure 2-4. Also, a common-mode inductor (1KΩ-2KΩ@100MHz CM choke) or/and a differential-mode inductor can be an option based on the EMI test result, see Figure 2-5. In the CA-IS364x reference design, to reduce low-frequency noise, two differential-mode inductors (L1, L2) are added between the input power supply and the primary-side supply inputs. Ground planes must be avoided under these magnetic components to avoid the parasitic capacitance affecting high-frequency attenuation.

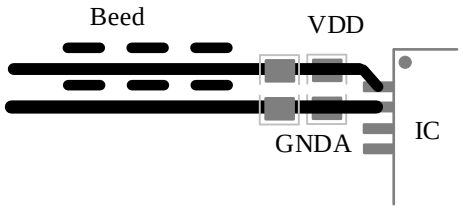

Figure 2-4. Ferrite beads placement

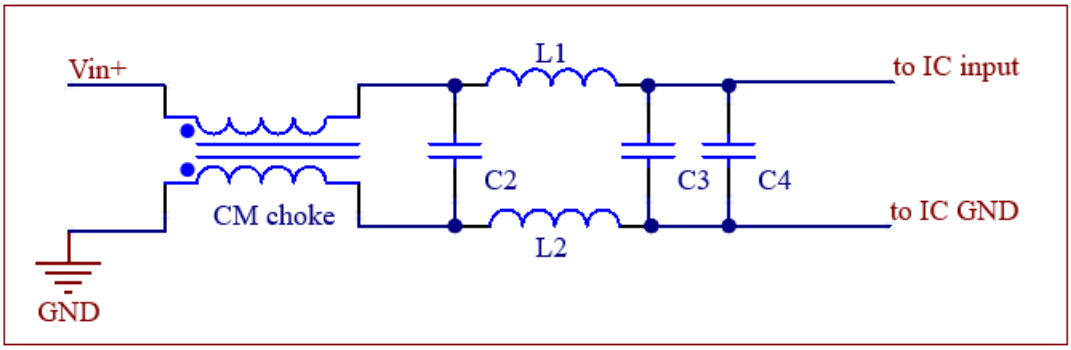

Figure 2-5. CM choke and differential-mode inductor

The CA-IS364xV has an individual logic supply input V_{DDL} allows fully compatible +3.3V and +5.0V logic on A-side digital lines. Pin V_{DDL} can be connected to an individual power supply or connected with pin V_{DD} for single supply design. In the single supply design, we recommend to add a bead between V_{DDL} and V_{DD} to reduce noise.

2.2.4. Building the edge guarding

A grounding vias can be added around the PCB to form a via guard ring and return the noise to the ground to reduce the radiation and interfere to the external system, as shown in Figure 2-6. If there are more than two rows of vias, the vias placed in the two rows shall be staggered from each other.

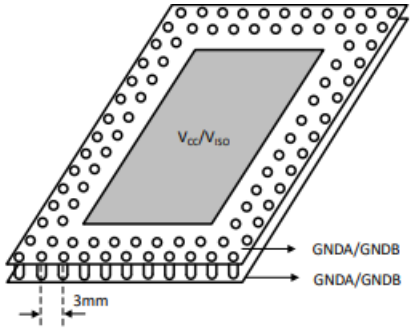

Figure 2-6. Vias guard ring around the edges of ground layers

3. CA-IS364x Low-EMI Reference Design

3.1. PCB Design Guide

1) On the reference design board, left of L1/L2, the LM1086ISX-ADJ 12V to 5V LDO is selected to provide a clean +5V supply for the CA-IS364x digital isolators on board.
2) Place decoupling capacitors as close as possible to the device pins, maximum distance is less than 2mm, see Figure 3-1, C3/C4 and C6/C7.

3) Place the beads BD1/BD2 close to C3/C4. Install the differential-mode inductors at L1/ L2 tag.
4) Across primary-side and secondary side grounds, place Y-capacitors and damping resistor between GNDA and GNDB of CA-IS364x.
5) Ro is the load of isolated power supply output (5V/100mA);
6) Components not installed on board include: BD3, BD4, C5, reserved for future applications.

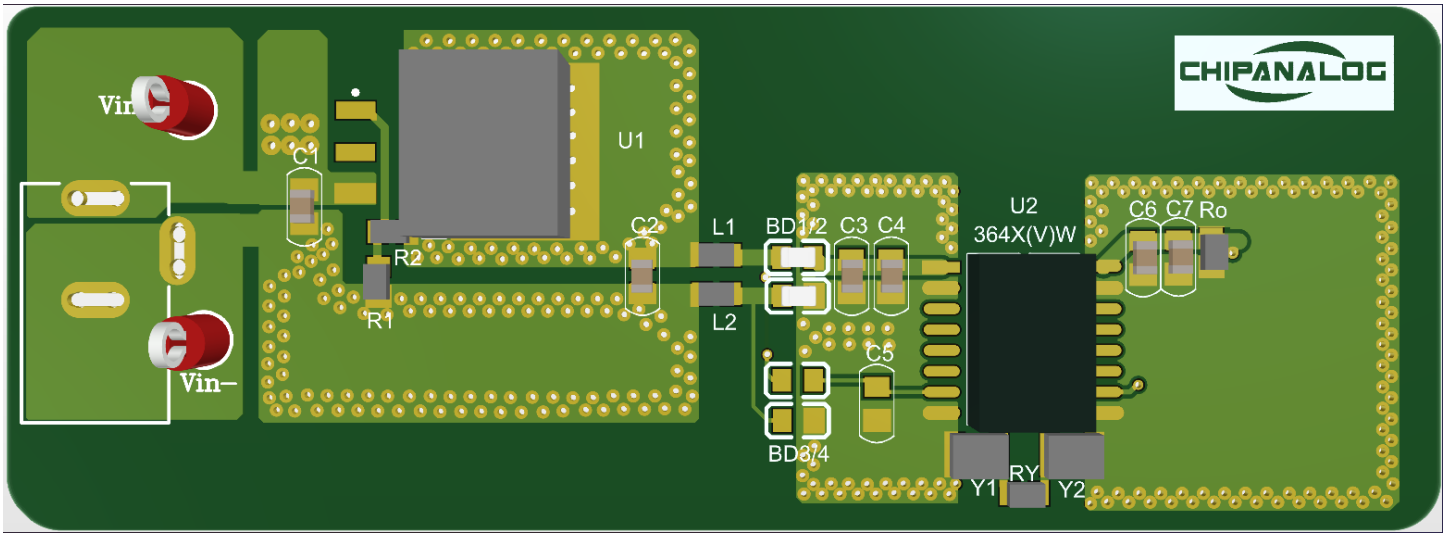

Figure 3-1. CA-IS364x reference design board(2-layer)

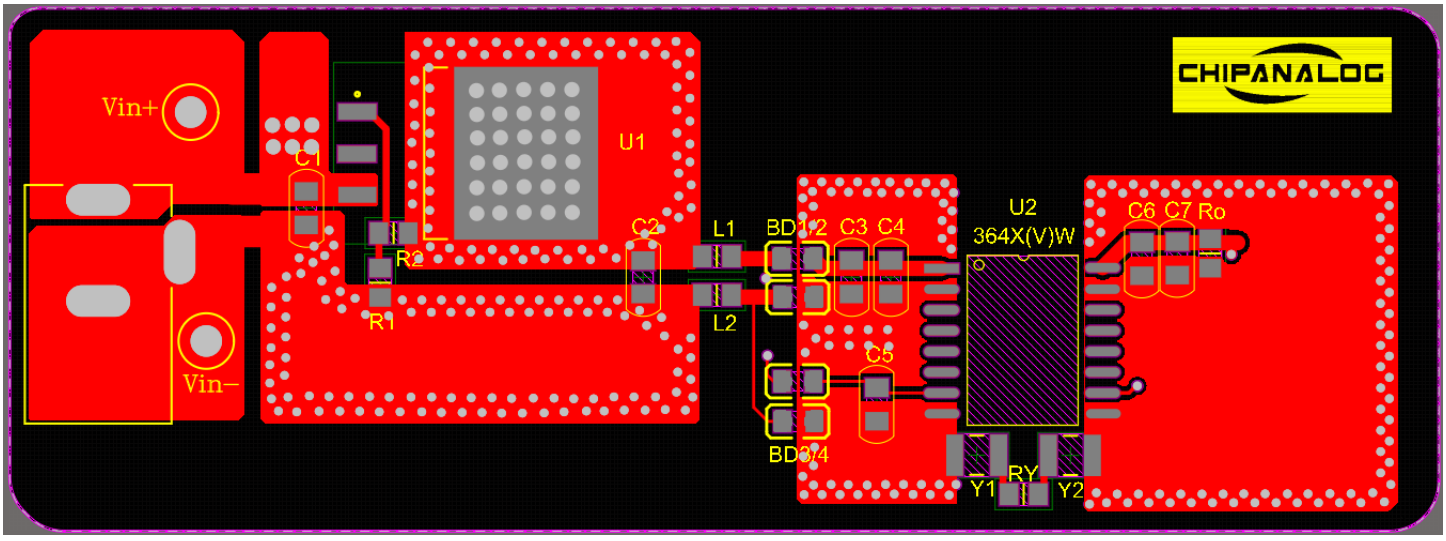

Figure 3-2. Reference design PCB top layer

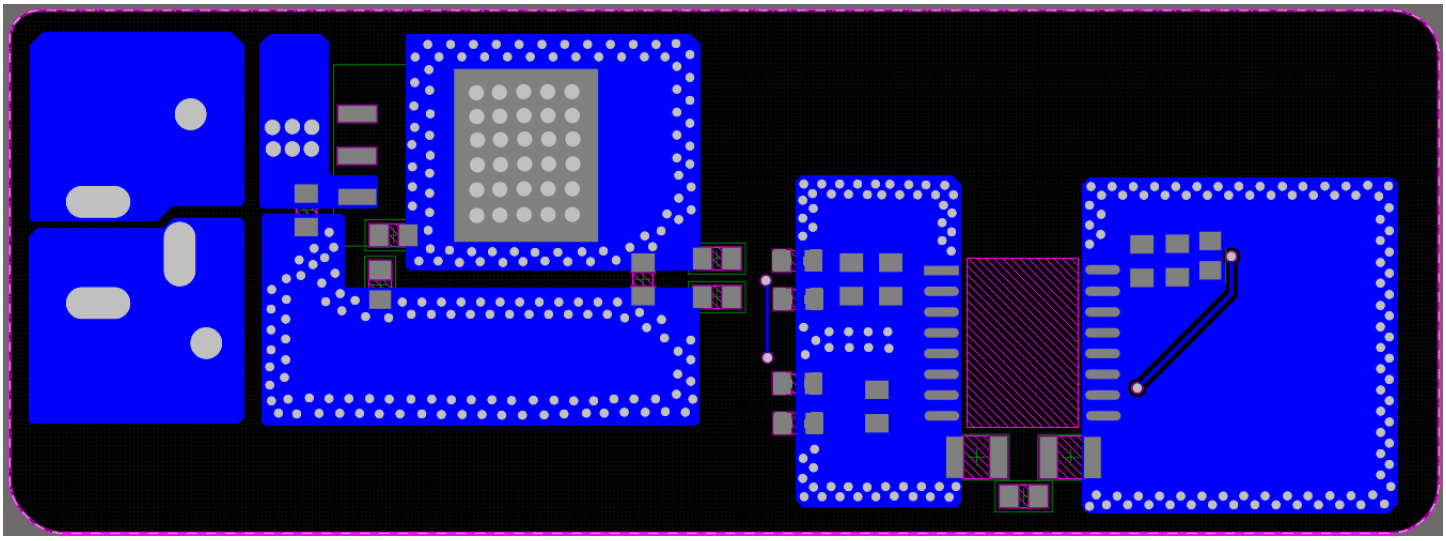

Figure 3-3. Reference design PCB bottom layer

3.2. CA-IS364x Reference Design Schematic

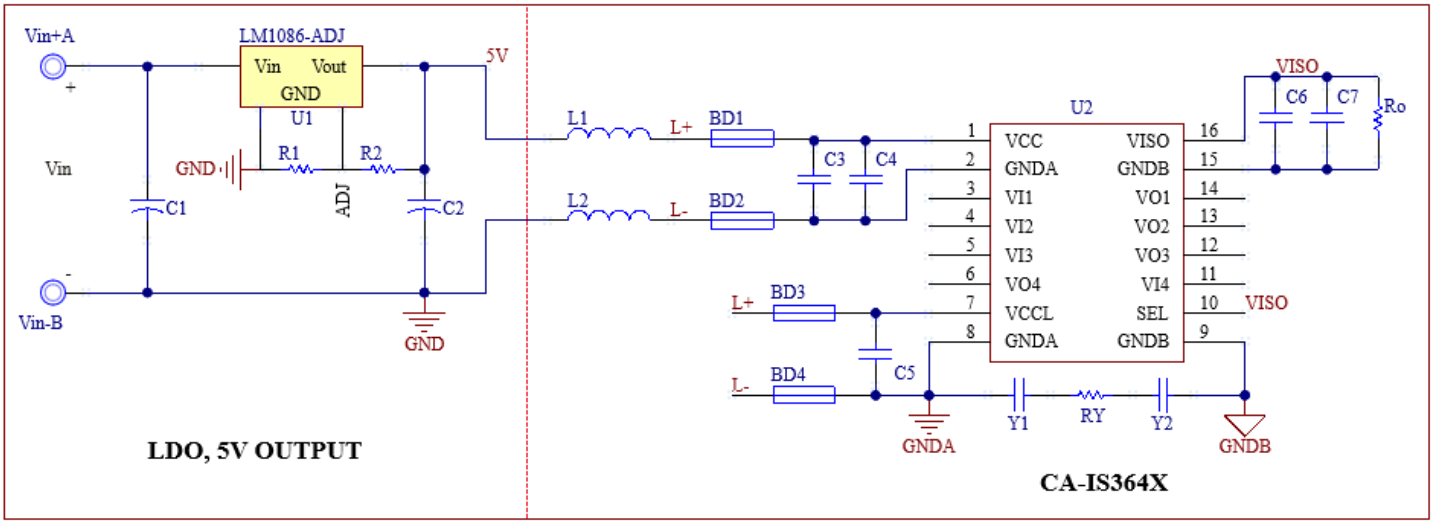

Figure 3-4. CA-IS364x test board schematic

Table 3-1. Component List

Device name	Designation	Spec	Part number	Note
Decoupling capacitors	C4, C6	10nF		
	C3, C7	10μF		
Ferrite bead	BD1, BD2	1kΩ (@100MHz)	BLM18HE102SN1	
Differential-mode inductors	L1, L2	1μH	MLZ2012M1R0HT000	
Y capacitor	Y1, Y2	39pF	GRM31A7U3D390JW31	
Damping resistor	RY	20Ω		Connected with Y-capacitor in series

Table 3-2. Reference design summary

Board	Design margin	Frequency	PCB-layers	Overlap capacitors	Y-capacitor	Common-mode inductor	Differential-mode inductor
Reference design	1.56dB	976MHz	2	N/A	19pF	N/A	1μH(2pcs)

3.3. Reference Design Test Result

The test result is shown in Figure 3-5 and Figure 3-6, this solution meets EN55032(CISPR32) radiated emissions Class B standard, and also leave 1.56dB (horizontal)/8.4dB(vertical) design margin.

Table 3-3. Reference design test result summary

Input voltage	Output voltage	Load current	Design margin	
			vertical	horizontal
5V	5V	100mA	8.4dB	1.56dB

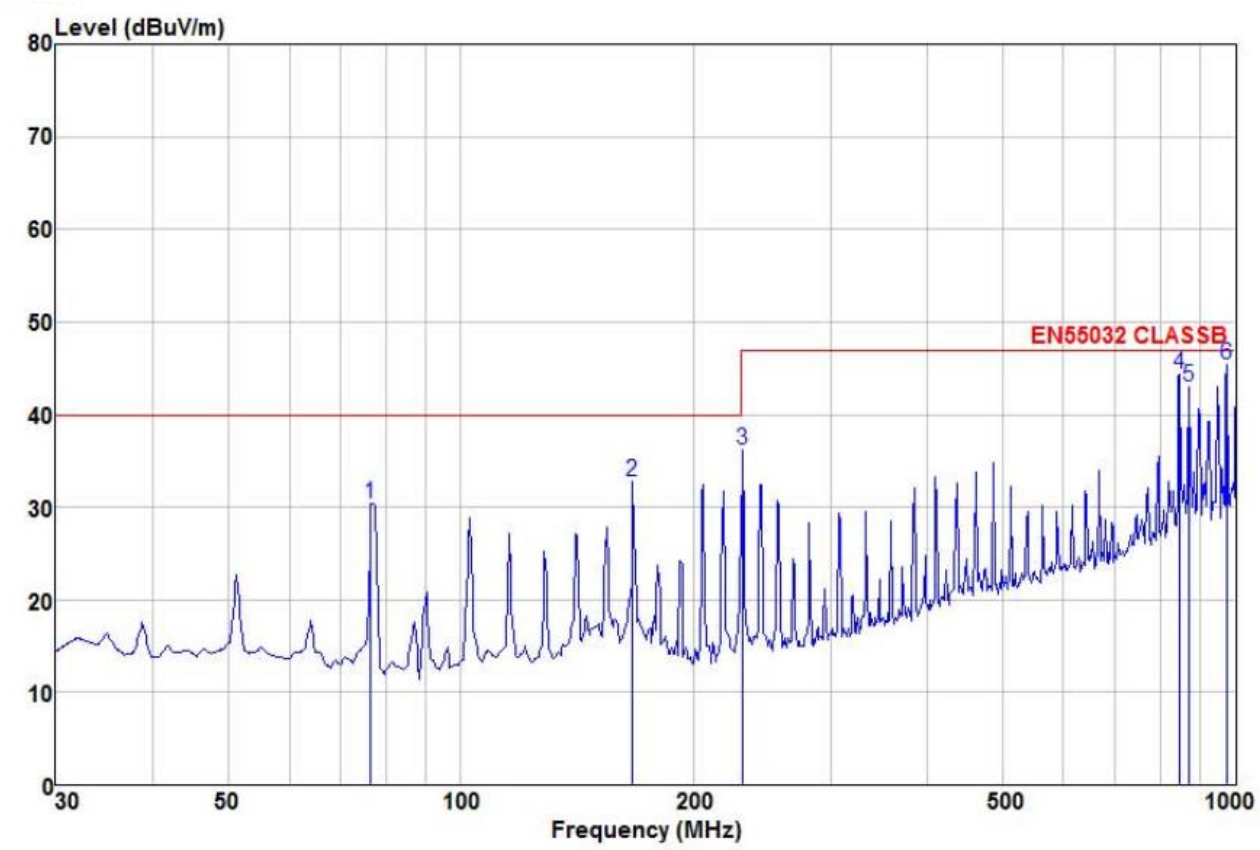

Figure 3-5. Horizontal radiation test result

Test result:

30MHz-1GHz, Margin = 1.56dB.

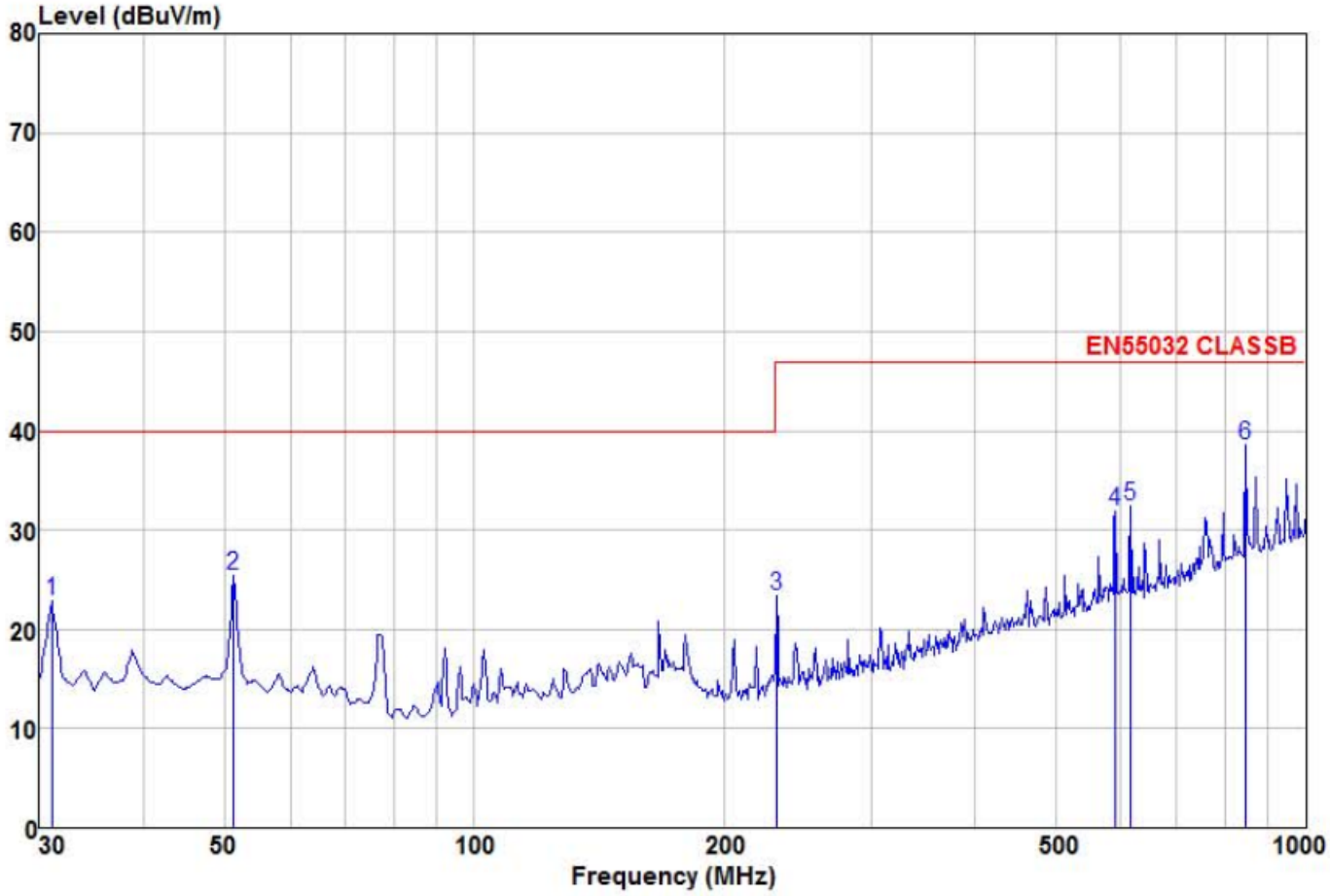

Figure 3-6. Vertical radiation test result

Test result:

30MHz-1GHz, Margin = 8.4dB

4. Revision History

Revision Number	Revision Date	Description
Ver 1.0	2024/2/5	Initial version

5. Important Statement

The above information is for reference only and used for helping Chipanalog customers with design, research and development. Chipanalog reserves the rights to change the above information due to technological innovation without advance notice.

All Chipanalog products pass ex-factory test. As for specific practical applications, customers need to be responsible for evaluating and determining whether the products are applicable or not by themselves. Chipanalog's authorization for customers to use the resources are only limited to development of the related applications of the Chipanalog products. In addition to this, the resources cannot be copied or shown, and Chipanalog is not responsible for any claims, compensations, costs, losses, liabilities and the like arising from the use of the resources.

Trademark information

Chipanalog Inc.® and Chipanalog® are registered trademarks of Chipanalog.

http://www.chipanalog.com