CA-IF1021Lx-Q1 Automotive LIN Transceiver with Inhibit and Wake-up

1. Features

- **Meets LIN2.0、LIN2.1、LIN2.2、LIN2.2A and ISO 17987-4:2016(12V) Physical-layer (EPL) Standards**
- **Compliant to SAE J2602-1 and SAE J2602-2 LIN Physical-layer Specification**
- **Designed to Support 12V Applications with Wide Operating Supply Range:**
  - 5.5V to 27V supply range (V_{BAT})
- **3.3V and 5.0V Input Logic Compatible**
- **System-level Power Control via INH pin**
- **Power-up/down Glitch-free Operation on LIN bus and RXD output**
- **Integrated 30kΩ LIN pull-up Resistor**
- **Support up to 20kbps LIN Transmission Data Rate**
- **Operating Mode:**
  - Normal operation
  - Low-power sleep
  - Low-power standby
  - Power-on
- **Wake-up from Low-power Mode:**
  - Remote wake-up via LIN bus
  - Local wake-up via WAKE_N or SLP_N pins
- **Integrated Protection Increases Robustness**
  - ±42V fault-tolerant LIN bus
  - 42V load dump protection
  - Enhanced ESD protection
  - Undervoltage protection on V_{BAT}
  - Transmitter dominant timeout prevents lockup
  - Thermal shutdown
  - System level fail-safe protection for the unpowered node or ground disconnection
- **–40°C to 150°C Junction Temperatures Range**
- **Available in SOIC8 and DFN8 (3.0mm x 3.0mm) Packages**
- **AEC-Q100 Qualified for Automotive Application**

2. Applications

- Body electronics
- Automotive gateway
- Infotainment and cluster
- Hybrid electric vehicles and powertrain systems

3. General Description

The CA-IF1021Lx-Q1 family of device is Local Interconnect Network (LIN) transceiver with integrated wake-up and protection features for automotive applications. LIN is low-speed universal asynchronous receiver transmitter (UART) communication protocol used to support in-vehicle networks. The CA-IF1021Lx-Q1 transceiver controls the LIN bus state via the TXD input and reports the bus state on its open-drain output RXD between the protocol controller and physical LIN networks. These device features slew-rate control and wave-shaping to reach a very low level of electromagnetic emission (EME) within a broad frequency range.

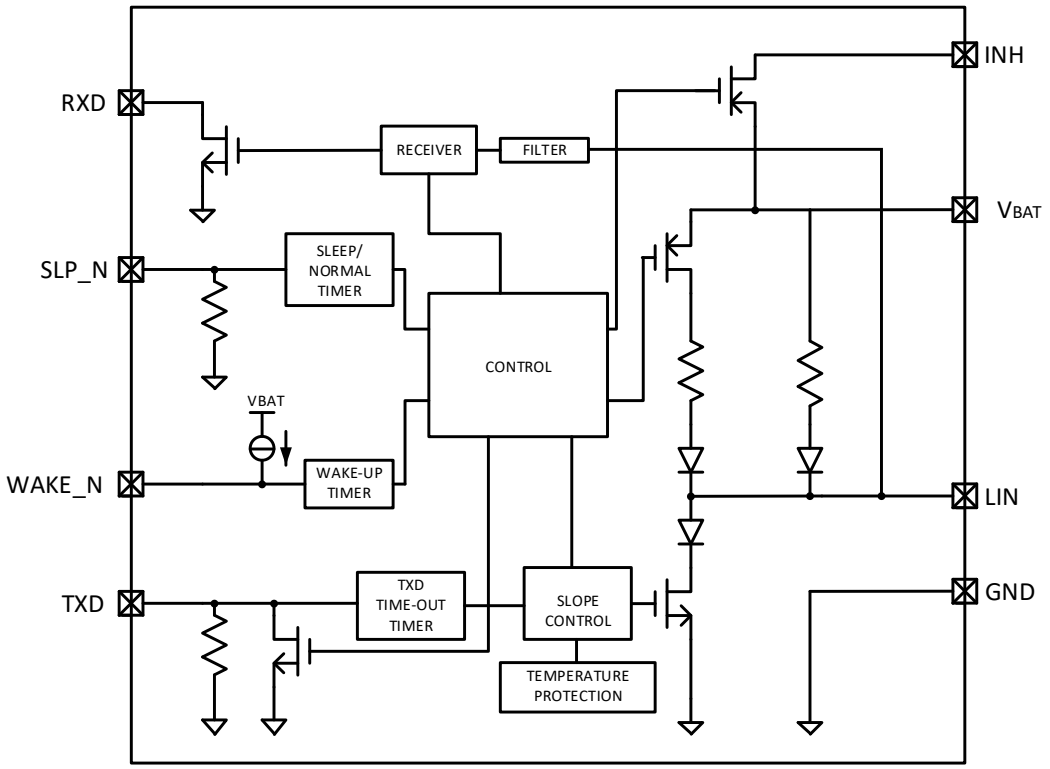
The CA-IS1021x-Q1 devices are designed to support 12V automotive applications with 5.5V to 27V wide V_{BAT} input voltage operating range and have up to ±42V fault protection on LIN bus, with integrated ESD protection, these devices help to reduce external components in the design. Also, these devices feature low-power sleep mode, as well as wake-up capability over LIN bus, or via the WAKE_N pin, SLP_N pin. Inhibit output (INH) can be used to control one or more external voltage regulators presented on a node to reduce the battery power consumption at system level. In the event of a ground shift or supply voltage disconnection, the devices can prevent back-feed current through LIN to the supply input.

The CA-IF1021Lx-Q1 transceiver is available in a standard 8-pin SOIC package and 8-pin DFN package, operates over the -40°C to +150°C junction temperature range.

Table 3-1. Device Information

Part number	Package	Package size(NOM)
CA-IF1021LS-Q1	SOIC8(S)	4.9mm x 3.9mm
CA-IF1021LD-Q1	DFN8(D)	3mm x 3mm

Figure 3-1. Simplified Block Diagram



4. Ordering Information

Table 4-1. Ordering Information

Part Number	Features	Package
CA-IF1021LS-Q1	Automotive qualified part	SOIC8(S)
CA-IF1021LD-Q1	Automotive qualified part	DFN8(D)

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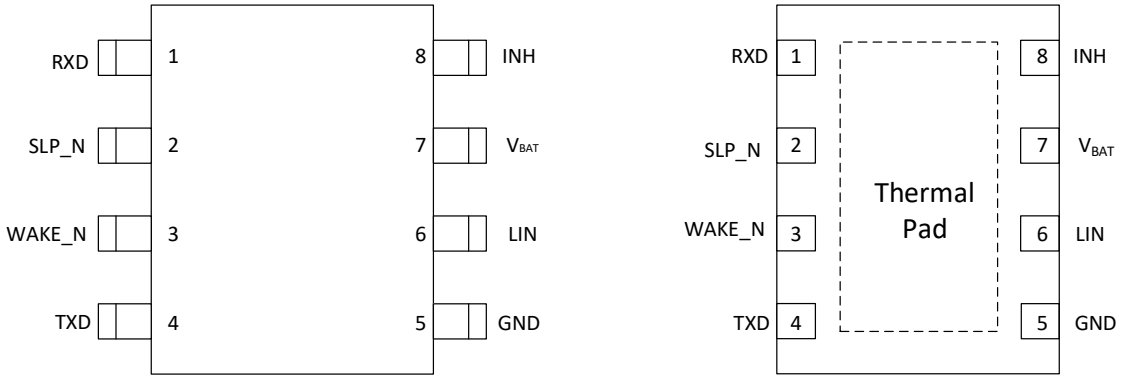
5. Revision History

Revision Number	Description	Page Changed
Version 1.00	N/A	N/A

6. Pin Configuration and Functions



CA-IF1021LS-Q1(SOIC8)　　CA-IF1021LD-Q1(DFN8)

Figure 6-1. CA-IF1021Lx-Q1 Pin Configuration

Table 6-1. CA-IF1021Lx-Q1 Pin Configuration and Description

Pin Name	Pin #	Type	Description
RXD	1	Digital I/O	Data receive output. Open-drain output, requires an external pull-up resistor. The RXD reads back information from the LIN bus in normal operation mode and indicates a wake-up event in standby mode, RXD is low if a wake event occurred.
SLP_N	2	Digital I/O	Enable input with integrated pull-down resistor to GND. A logic-high on SLP_N pin puts the transceiver in normal operating mode. A logic-low on SLP_N pin to select the sleep mode.
WAKE_N	3	High-voltage I/O	Active-low local wake-up input. Pull WAKE low to generate a local wake-up event.
TXD	4	Digital I/O	Transmit data input. TXD is a CMOS/TTL compatible input from microcontroller with an internal pulled down resistor to GND. Set this pin to “low” to drive a dominant stat on LIN bus. In standby mode, TXD indicates the wake-up source as an output. Active low after a wake-up event.
GND[1]	5	GND	Ground.
LIN	6	Bus I/O	LIN bus input/output.
V_{BAT}	7	Power	Battery voltage input. Bypass V_{BAT} to ground with at least 0.1μF ceramic capacitor as close as possible to the device.
INH	8	High-voltage I/O	Inhibit Output. INH can be used to control one or more external voltage regulators and microcontroller. Active high after a wake-up event.
Note：The Thermal Pad chip packaged in DFN8 is internally connected to GND to enhance heat dissipation.			

7. Specifications

7.1. Absolute Maximum Ratings

Symbol	PARAMETER	TEST CONDITIONS	Min.	Max.	Unit
V_{BAT}	Supply voltage range		-0.3	42	V
V_{TXD}	TXD voltage range	Without I_{TXD} current limit	-0.3	6	V
		I_{TXD} < 500μA	-0.3	7	V
V_{RXD}	RXD voltage range	Without I_{RXD} current limit	-0.3	6	V
		I_{RXD} < 500μA	-0.3	7	V
V_{SLP_N}	SLP_N voltage range	Without I_{SLP_N} current limit	-0.3	6	V
		I_{SLP_N} < 500μA	-0.3	7	V
V_{LIN}	LIN bus voltage range		-42	42	V
V_{WAKE_N}	WAKE_N voltage range		-0.3	42	V
I_{WAKE_N}	WAKE_N terminal current	V_{WAKE_N} < V_{GND}-0.3 only; from WAKE_N to ground.	-15		mA
V_{INH}	INH output voltage range		-0.3	V_{BAT}+0.3	V
$I_{O(INH)}$	INH output current		-50	15	mA
T_J	Virtual junction temperature range		-40	150	℃
T_{STG}	Storage temperature range		-55	150	℃

Note:

1. The stresses listed under "Absolute Maximum Ratings" are stress ratings only, not for functional operation condition. Exposure to absolute maximum rating conditions for extended periods may cause permanent damage to the device.

7.2. ESD Ratings

	TEST CONDITIONS		Value	Unit
HBM ESD	WAKE_N, LIN, V_{BAT}, INH pins to GND		±8000	V
	RXD, SLP_N, TXD pins to GND		±8000	
CDM ESD	Other pins to GND		±2000	V
System Level ESD[1]	WAKE_N, LIN and V_{BAT} pins to GND	IEC 61000-4-2: contact discharge, without power-up	±6000	V

Note：V_{BAT} GND:1nF, LIN GND:1nF, WAKE_ N pin series connection 30k Ω resistor.

7.3. Recommended Operating Conditions

PARAMETER		Min.	Max.	Unit
V_{BAT}	Battery voltage range	5.5	27	V
V_{LIN}	LIN bus voltage range	0	27	V
V_{LOGIC}	Logic voltage range	0	5.25	V
T_A	Operation temperature range	-40	125	℃

7.4. Thermal Information

Thermal Metric		DFN8	SOIC8	Unit
$R_{\theta JA}$	Junction-to-ambient thermal resistance	40	170	°C/W

7.5. Electrical Characteristics

Over recommended operating conditions, T_A = –40°C to 125°C (unless otherwise noted).

7.5.1. DC Characteristics (Power Supply)

PARAMETER		TEST CONDITIONS	Min.	Typ.	Max.	Unit
I_{BAT}	V_{BAT} Current	Sleep mode: V_{LIN}=V_{BAT} V_{WAKE_N}=V_{BAT} V_{TXD}=0V V_{SLP_N}=0V V_{BAT}=12V	3	15	25	μA
I_{BAT}	V_{BAT} Current	Standby mode(recessive): V_{INH}=V_{BAT} V_{LIN}=V_{BAT} V_{WAKE_N}=V_{BAT} V_{TXD}=0V V_{SLP_N}=0V	150	350	1000	μA
I_{BAT}	V_{BAT} Current	Standby mode(dominant): V_{BAT} =12V V_{INH}=12V V_{LIN}=0V V_{WAKE_N}=12V V_{TXD}=0V V_{SLP_N}=0V	200	670	1200	μA
I_{BAT}	V_{BAT} Current	Normal mode(recessive): V_{INH}=V_{BAT} V_{LIN}=V_{BAT} V_{WAKE_N}=V_{BAT} V_{TXD}=5V V_{SLP_N}=5V	200	320	1200	μA
I_{BAT}	V_{BAT} Current	Normal mode (dominant): V_{BAT} =12V V_{INH}=12V V_{WAKE_N}=12V V_{TXD}=0V V_{SLP_N}=5V	0.6	1.3	2	mA

7.5.2. Power on reset

PARAMETER		TEST CONDITIONS	Min.	Typ.	Max.	Unit
$V_{th(POR)L}$	Power-on reset threshold _low level		1.6	3.3	3.9	V
$V_{th(POR)H}$	Power-on reset threshold _high level		2.3	3.6	4.3	V
$V_{hys(POR)}$	Power-on reset hysteresis		0.05	0.3	1	V
$V_{th(VBATL)L}$	V_{BAT} low threshold _low level		3.9	4.3	4.7	V
$V_{th(VBATH)H}$	V_{BAT} low threshold _high level		4.2	4.5	4.9	V
$V_{hys(VBATL)}$	V_{BAT} low hysteresis		0.05	0.3	1	V

7.5.3. TXD

PARAMETER		TEST CONDITIONS	Min.	Typ.	Max.	Unit
V_{IH}	High-level input voltage		2		7	V
V_{IL}	Low-level input voltage		-0.3		0.8	V
V_{hys}	Hysteresis voltage		50	200	400	mV
$R_{PD(TXD)}$	TXD pull-down resistor	V_{TXD}=5V	140	500	1200	kΩ
I_{IL}	Low-level input current	V_{TXD}=0V	-5	0	5	μA
I_{OL}	Low-level output current	Local wake-up; Standby mode; V_{WAKE_N} = 0V; V_{LIN} = V_{BAT}; V_{TXD}=0.4V	1.5			mA

7.5.4. SLP_N

PARAMETER		TEST CONDITIONS	Min.	Typ.	Max.	Unit
V_{IH}	High-level input voltage		2		7	V
V_{IL}	Low-level input voltage		-0.3		0.8	V
V_{hys}	Hysteresis voltage		50	200	400	mV
$R_{PD(SLP\_N)}$	SLP_N pull-down resistor	V_{SLP_N}=5V	140	500	1200	kΩ
I_{IL}	Low-level input current	V_{SLP_N}=0V	-5	0	5	μA

7.5.5. RXD

PARAMETER		TEST CONDITIONS	Min.	Typ.	Max.	Unit
I_{OL}	Low-level output current	Normal mode： V_{RXD} = 0.4V; V_{LIN} = 0V	1.5			mA
I_{LH}	High-level leakage current	Normal mode: V_{RXD} = 5V; V_{LIN} = V_{BAT}	-5	0	5	μA

7.5.6. WAKE_N

PARAMETER		TEST CONDITIONS	Min.	Typ.	Max.	Unit
V_{IH}	High-level input voltage		V_{BAT}-1		V_{BAT}+0.3	V
V_{IL}	Low-level input voltage		-0.3		V_{BAT}-3.3	V
$I_{pu(L)}$	Low-level pull-down current	V_{WAKE_N} = 0V	-30	-12	-1	μA
I_{LH}	High-level input leakage current	V_{WAKE_N} = 27V; V_{BAT} = 27V;	-5	0	5	μA

7.5.7. INH

PARAMETER		TEST CONDITIONS	Min.	Typ.	Max.	Unit
R_{SW}	Switch-on resistance between V_{BAT} and INH	Standby, normal and power on : I_{INH} = -15mA; V_{BAT} = 12V		20	50	Ω
I_{LH}	High-level leakage current	Sleep mode: V_{INH} = 27V; V_{BAT} = 27V	-5	-	5	μA

7.5.8. LIN

PARAMETER		TEST CONDITIONS	Min.	Typ.	Max.	Unit
I_{BUS_LIM}	Driver output current limitation @dominant	V_{TXD}=0V;V_{LIN}=V_{BAT}=18V	40		150	mA
R_{pu}	Pull-up resistor	Sleep mode: V_{SLP_N}=0V	50	160	250	kΩ
$I_{BUS\_PAS\_rec}$	Receiver input leakage current@ recessive	V_{TXD}=5V;V_{LIN}= 27V;V_{BAT}=5.5V			20	μA
$I_{BUS\_PAS\_dom}$	Receiver input leakage current@ dominant	Normal mode; V_{TXD} = 5V; V_{LIN} = 0V; V_{BAT} = 12V	-600			μA
$V_{SerDiode}$[1]	Voltage drop on the serial diode	Pull-up path with R_{slave} $I_{SerDiode}$ = 10μA[1]	0.4	0.7	1	V
$I_{BUS\_NO\_GND}$	Bus current @ loss ground	V_{BAT}=27V; V_{LIN}= 0V	-750		10	μA
$I_{BUS\_NO\_BAT}$	Bus current @ loss battery	V_{BAT}=0V; V_{LIN}= 27V			10	μA
V_{BUSdom}	LIN receiver dominant state				0.4V_{BAT}	V
V_{BUSrec}	LIN receiver recessive state		0.6V_{BAT}			V
V_{BUS_CNT}	LIN receiver center threshold	V_{BUS_CNT} = (V_{BUSdom}+ V_{BUSrec})/2	0.44V_{BAT}	0. 5V_{BAT}	0.56V_{BAT}	V
V_{HYS}	LIN receiver hysteresis voltage	V_{HYS} = V_{BUSrec} -V_{BUSdom}			0.175V_{BAT}	V
R_{slave}	Slave resistance	Resistance between LIN and V_{BAT}; V_{LIN} = 0V; V_{BAT} = 12V	20	30	47	kΩ
C_{LIN}[1]	Capacitance on LIN pin	[1]			30	pF
$V_{O(DOM)}$	LIN dominant output	Normal mode; V_{TXD} = 0V; V_{BAT} = 7V			1.4	V
		Normal mode; V_{TXD} = 0V; V_{BAT} = 18V			2.0	V
Note：1.Guaranteed by design.						

7.5.9. Thermal Shutdown

PARAMETER		TEST CONDITIONS	Min.	Typ.	Max.	Unit
$T_{jsd(sd)}$[1]	Thermal shutdown temperature		160	175	200	℃
$T_{jsd(hys)}$[1]	Thermal shutdown temperature threshold hysteresis			20		℃
Note：1.Guaranteed by design.						

7.5.10. Duty cycle

PARAMETER		TEST CONDITIONS	Min.	Typ.	Max.	Unit
$\delta1$[1,2]	Duty cycle 1	$V_{th(rec)(max)}$=0.744xV_{BAT}; $V_{th(dom)(max)}$=0.581xV_{BAT}; t_{bit}=50μs; V_{BAT}=7V~18V	0.396			
		$V_{th(rec)(max)}$=0.76xV_{BAT}; $V_{th(dom)(max)}$=0.593xV_{BAT}; t_{bit}=50μs; V_{BAT}=5.5V~7V	0.396			
$\delta2$[2,3]	Duty cycle 2	$V_{th(rec)(min)}$=0.422xV_{BAT}; $V_{th(dom)(min)}$=0.284xV_{BAT}; t_{bit}=50μs; V_{BAT}=7.6V~18V			0.581	
		$V_{th(rec)(min)}$=0.41xV_{BAT}; $V_{th(dom)(min)}$=0.275xV_{BAT}; t_{bit}=50μs; V_{BAT}=6.1V~7.6V			0.581	
$\delta3$[1,2]	Duty cycle 3	$V_{th(rec)(max)}$=0.778xV_{BAT}; $V_{th(dom)(max)}$=0.616xV_{BAT}; t_{bit}=96μs; V_{BAT}=7V~18V	0.417			
		$V_{th(rec)(max)}$=0.797xV_{BAT}; $V_{th(dom)(max)}$=0.630xV_{BAT}; t_{bit}=96μs; V_{BAT}=5.5V~7V	0.417			
$\delta4$[2,3]	Duty cycle 4	$V_{th(rec)(min)}$=0.389xV_{BAT}; $V_{th(dom)(min)}$=0.251xV_{BAT}; t_{bit}=96μs; V_{BAT}=7.6V~18V			0.590	
		$V_{th(rec)(min)}$=0.378xV_{BAT}; $V_{th(dom)(min)}$=0.242xV_{BAT}; t_{bit}=96μs; V_{BAT}=6.1V~7.6V			0.590	

7.5.11. Switching Characteristics

Over recommended operating conditions, 5.5V≤ V_{BAT} ≤27V, T_J = –40°C to 150°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	Min.	Typ.	Max.	Unit
t_f[2]	Fall time				22.5	µs
t_r[2]	Rise time				22.5	µs
$\triangle t_{(r-f)}$[2]	Difference between rise and fall time	V_{BAT}=7.3V	-5		5	µs
$t_{P(TX)}$[2]	TXD propagation delay	Rise and fall			6	µs
$t_{P(TX)sym}$[2]	TXD propagation delay symmetry		-2.5		2.5	µs
$t_{P(RX)}$[4]	RXD propagation delay	Rise and fall			6	µs
$t_{P(RX)sym}$[4]	RXD propagation delay symmetry		-2		2	µs
$t_{wake(dom)LIN}$	LIN dominant wake-up time(remote wake-up)	Sleep mode	30	80	150	µs
$t_{wake(dom)WAKE\_N}$	Dominant wake-up time @ WAKE_N(local wake-up)	Sleep mode	7	30	50	µs
$t_{gotonorm}$	Mode change time, from sleep, power-on or standby mode to normal mode		2	5.5	10	µs
$t_{gotosleep}$	Mode change time: from normal mode to sleep mode		2	6.5	10	µs
$t_{to(dom)TXD}$	TXD-dominant timeout	V_{TXD} = 0V	27	55	90	ms

Notes:

1. δ1, δ3 = $\frac{t_{bus(rec)(\min)}}{2\times t_{bit}}$

2.LIN bus load condition: (1) C_{BUS} = 1nF, R_{BUS} = 1kΩ； (2) C_{BUS} = 6.8nF, R_{BUS} = 660Ω； (3) C_{BUS} = 10nF, R_{BUS} = 500Ω.

3. δ2, δ4 = $\frac{t_{bus(rec)(\max)}}{2\times t_{bit}}$

4.Receiver output (RXD) load condition: C_{RXD} = 20pF, R_{RXD} = 2.4kΩ.

8. Parameter Measurement Information

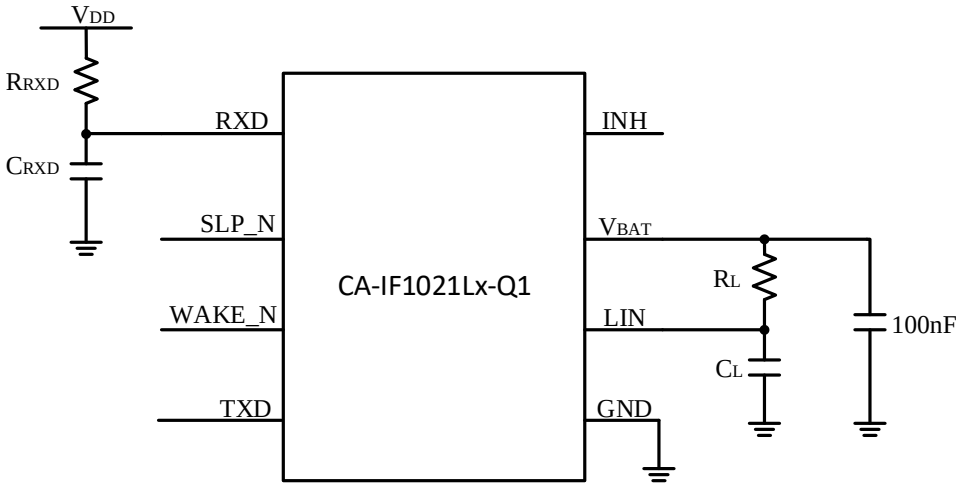


Figure 8-1. LIN Transceiver Timing Test Circuit

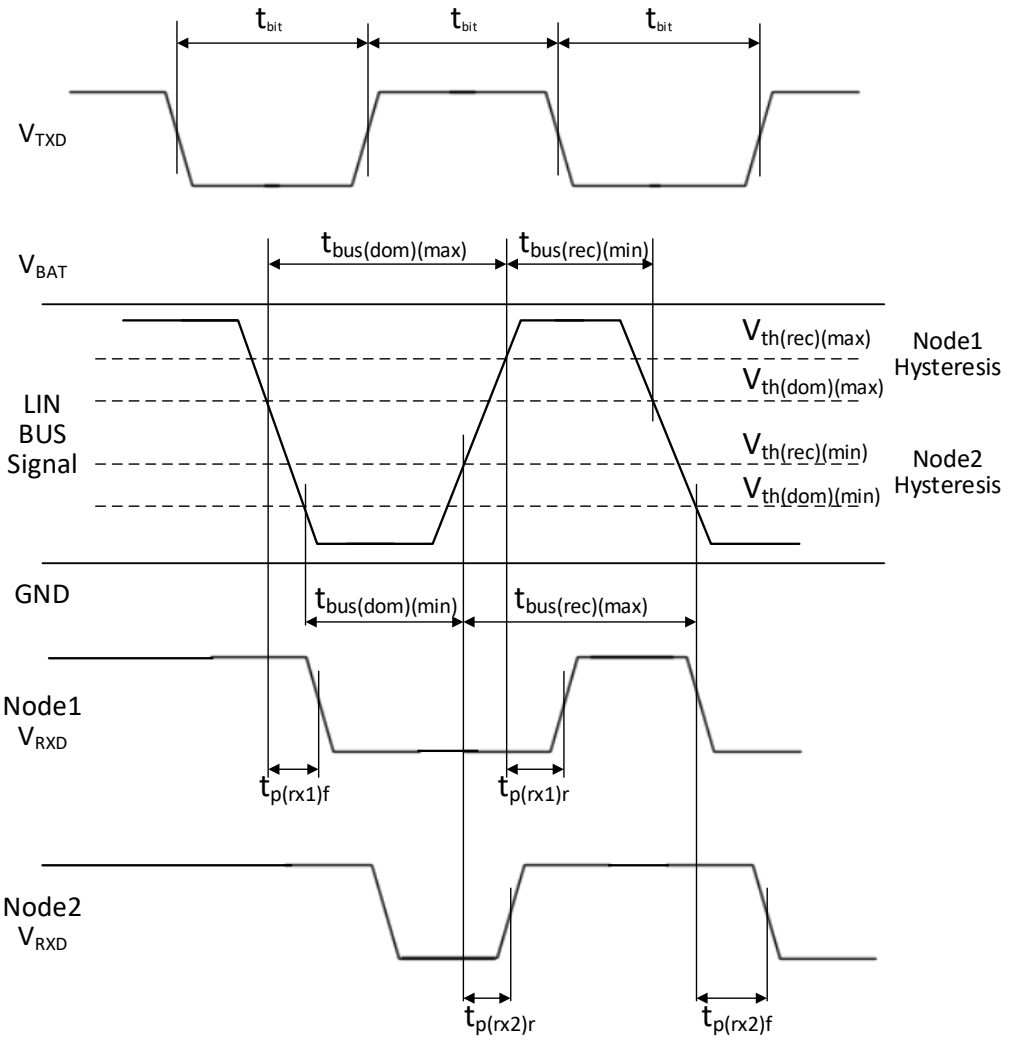


Figure 8-2. LIN Bus Transmission Timing Diagram

9. Detailed Description

9.1. Overview

The CA-IF1021Lx-Q1 family of devices is fault-protected Local Interconnect Network (LIN) transceiver, meets the LIN 2.x/ISO 17987-4:2016/SAE J2602 physical layer standard. These devices are designed for harsh automotive applications with a number of integrated robust protection features that improve the reliability of end equipment. The extended fault-protected voltage range of ±58V on LIN bus line and 5.5V to 27V wide input voltage operating range allow for use in +12V automotive and truck applications. Dominant timeout prevents the bus from being blocked by a hung-up microcontroller. The LIN driver output is short-circuit current-limited and protected against excessive power dissipation by thermal shutdown circuitry that disable the transmitter to protect the device.

The LIN bus has two valid states: dominant and recessive. In the dominant state, LIN bus voltage level close to GND level; In the recessive state, LIN bus voltage level pulled up to the supply voltage V_{BAT} by bus termination, see Figure 8-2 for more detail about the LIN bus specification definition. The CA-IF1021Lx-Q1 transceiver can operate up to 20kbps data rate and the LIN driver converts the transmit data streams on the TXD input to LIN bus signals with optimized slew rates in order to minimize the level of electromagnetic emission on the LIN networks. The LIN receiver output reads back the information from the LIN bus to the microcontroller.

9.2. Protection Functions

9.2.1. Overvoltage Protection

The CA-IF1021Lx-Q1 devices have an internal ±42V overvoltage protection circuit on the driver output and receiver input to protect the devices from accidental shorts between a local power supply and the data line of the transceiver. This level of protection is present whether the transceiver is powered or un-powered.

9.2.2. Short-circuit Protection

The CA-IF1021Lx-Q1 protects the transmitter output stage against a short-circuit to pin V_{BAT} or GND by limiting the driver current. However, this will cause large supply current and dissipation. Thermal shutdown further protects the devices from excessive temperatures that may result from a short circuit. The transmitter returns to normal operation once the short is removed.

9.2.3. Thermal Shutdown

If the junction temperature of the CA-IF1021Lx-Q1 devices exceed the thermal shutdown threshold $T_{jsd(sd)}$, the device turns off the LIN driver circuits thus blocking the TXD-to-bus transmission path, and put the LIN bus terminal to recessive state. The shutdown condition is cleared and LIN driver enabled when the junction temperature drops at least the thermal shutdown hysteresis temperature below the thermal shutdown threshold.

9.2.4. Undervoltage Lockout

The CA-IF1021Lx-Q1 has undervoltage detection on V_{BAT} supply terminal, if the supply voltage V_{BAT} is less than $V_{th(VBATL)L}$, and greater than $V_{th(POR)L}$, will disable LIN driver. Once the undervoltage condition is cleared, the battery supply voltage has returned to a valid level: $V_{BAT} > V_{th(VBATL)H}$, the driver enabled again. During normal operation, if supply voltage drops to $V_{BAT} < V_{th(POR)L}$, the transceiver enters sleep mode. Once V_{BAT} increased to greater than $V_{th(POR)H}$ from power down, the device enters power-on mode.

9.2.5. Fail-safe

The CA-IF1021Lx-Q1 LIN transceivers feature fail-safe design. Both TXD and SLP_N pins have internal pull-down resistors to GND that place the input to low-level when floating. RXD pin is floating when V_{BAT} off. When the device is unpowered, the bus terminal and logic I/O pins have extremely low leakage currents, and there is no impact on both LIN bus and microcontroller. Also, there is no reverse current from the LIN bus in the even of supply voltage or ground disconnection. The LIN transceiver can be disconnected from the power supply without influencing the LIN bus.

9.2.6. Dominant Timeout

The CA-IF1021Lx-Q1 family of devices features a transmitter-dominant timeout($t_{to(dom)TXD}$) that prevents erroneous LIN controllers from clamping the bus to a dominant level by maintaining a continuous low TXD signal. When TXD remains in the dominant state (low) for greater than $t_{to(dom)TXD}$, the transmitter is disabled, releasing the bus to a recessive state. After a dominant timeout fault, the transmitter is re-enabled when receiving a rising edge at TXD. The transmitter-dominant timeout limits the minimum possible data rate.

9.3. Operating Mode

All devices have four operating modes: power-on mode, normal operation mode, low-power standby mode and very low-power sleep mode. The operating mode is determined by an internal state machine controlled by SLP_N and WAKE_N, as well as several internal flags, see Table 9-1 and Figure 9-1 for more details about the CA-IF1021Lx-Q1 operating modes.

Table 9-1. Operating Mode

MODE	SLP_N	TXD	RXD	INH	LIN Driver	Note
Sleep mode	Low	Weak pull-down	Floating	Floating	Off	No wake-up event detected.
Standby mode	Low	Weak pull-down if LIN bus wake-up; Strong pull-down if local wake-up.	Low	High	Off	Detected wake-up request; TXD is wake-up source output; Waiting microcontroller to enable the transceiver via SLP_N pin.
Normal mode	High	High: recessive state	Recessive state: High	High	Normal operation	Transmission data rate is up to 20kbps.
		Low: dominant state	Dominant state: Low			
Power-on	Low	Weak pull-down	Floating	High	Off	Power-on mode after V_{BAT} power up.

9.3.1. Normal Mode

Select the normal mode of devices operation by setting SLP_N terminal to logic-high. The LIN driver and receiver are fully operational and LIN communication is bi-directional. Drive TXD to transmit data on the LIN bus line, the LIN bus state is presented on RXD. INH is logic-high during normal operation, can be used to enable external voltage regulators and microcontroller.

The driver translates a logic input on TXD to LIN bus output. The receiver translates the LIN bus signal to a single-ended logic output on RXD. By setting the TXD input of the CA-IF1021Lx-Q1 to logic low, the transceiver generates a dominant level on the LIN bus (LIN pin); the RXD output reads the signal on the corresponding LIN bus and indicates the dominant LIN bus signal with a logic-low signal to the microcontroller. Setting the TXD pin to logic-high, the CA-IF1021Lx-Q1 driver sets the LIN interface pin LIN to the recessive level; at the same time a logic-high signal on the RXD output indicates the recessive level on the LIN bus.

During normal operation, the CA-IF1021Lx-Q1 switches to sleep mode in case of a low-level on pin SLP_N and maintained at least $t_{gotosleep}$. The normal operation mode can be entered from all modes of operation by setting the SLP_N input to high-level and maintained at least $t_{gotonorm}$.

9.3.2. Sleep mode

Sleep mode is the lowest-power operating mode. In sleep mode, the LIN transmitter and receiver are disabled, while the transceiver is still able to wake-up by a message on the LIN bus or local wake-up events through WAKE_N pin or SLP_N pin. The LIN Bus, WAKE_N pin and SLP_N pin are continuously monitored for a valid bus wake-up signal in sleep mode. To improve the system operation reliability and prevent false wake-up, the CA-IF1021Lx-Q1 features filtered LIN bus status wake-up detection and WAKE_N, SLP_N wake-up signal detections. This means, for a valid wake-up events to be considered, the LIN bus or WAKE_N, or pin SLP_N inputs must be kept in that state for more than the respective blocking time.

If the SLP_N input pin remains low, whenever a local or remote wake-up occurs, the transceiver will enter the standby mode automatically; Drive SLP_N input pin to high-level and maintained at least $t_{gotonorm}$, the transceiver will enter to normal operation directly. The CA-IF1021Lx-Q1 enters sleep mode if SLP_N is pulled to low-level and maintained at least $t_{gotosleep}$ when the transceiver is in normal operation mode. Also, when V_{BAT} drops below the power-on-reset threshold $V_{th(POR)L}$, the CA-IF1021Lx-Q1 enters sleep mode. In sleep mode, INH becomes floating; The internal slave termination between pins LIN and V_{BAT} is disabled to minimize the power dissipation, only a weak pull-up between pins LIN and V_{BAT} is present.

9.3.3. Standby mode

Standby mode is low-power operating mode. The LIN transmitter and receiver are disabled and no communication with the LIN bus is possible in standby mode. TXD input is inactive and this pin indicates wake-up source as an output: weak pull-down for a remote wake-up request and strong pull-down for a local wake-up request; RXD is placed at low-level that can be used as an interrupt for the microcontroller. INH output is switched on and remains logic-high to enable external voltage regulators and microcontroller.

Standby mode is entered automatically whenever a local or remote wake-up occurs while the CA-IF1021Lx-Q1 transceiver is in sleep mode and the SLP_N input pin remains low. This also enable the slave termination resistor at the pin LIN. In standby mode, pulling pin SLP_N to logic high results in the following events immediately:

· Reset TXD wake-up source flag and release the strong pull-down at pin TXD before the mode changed;
· Reset the wake-up request signal on pin RXD;
· Enter to normal operation mode if the high-level on SLP_N pin has been maintained for at least $t_{gotonorm}$.

9.3.4. Power-on mode

When V_{BAT} exceeds the power-on-reset threshold voltage $V_{th(POR)H}$ from power-down, the CA-IF1021Lx-Q1 transceiver enters power-on mode. Though the CA-IF1021Lx-Q1 is powered-up and INH is high, both LIN transmitter and receiver are still inactive. The RXD output is floating, TXD is at weak pull-down. INH is logic-high, can be used to enable external voltage regulators. The normal operation mode can be entered by setting the SLP_N input pin to high-level for $t_{gotonorm}$.

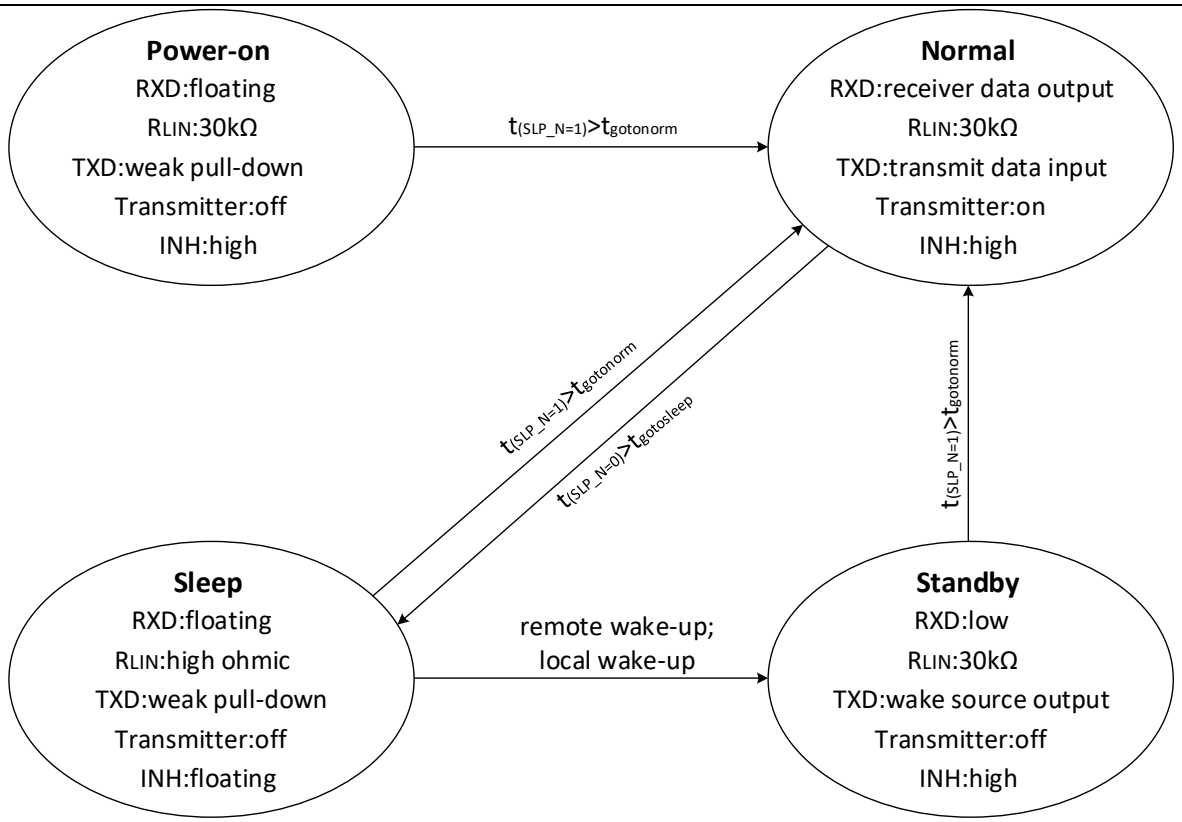


Figure 9-1. State Diagram

9.4. Wake-up Events

Advanced power management and wake-up capability make the CA-IF1021Lx-Q1 ideal for automotive electronic control unit (ECU) modules or other battery power applications that are permanently supplied by battery. For CA-IF1021Lx-Q1 devices, there are two different ways to exit sleep mode:

- **Remote wake-up:**
  The transceiver wake-up via a valid dominant signal on the LIN bus for at least the time $t_{wake(dom)LIN}$.
- **Local wake-up:**
  The operation mode changed by setting the SLP_N input high at least the time $t_{gotonorm}$, or
  The transceiver waked-up by setting the WAKE_N low for at least $t_{wake(dom)WAKE\_N}$.

The TXD output is used to indicate wake-up source while the device is in standby mode: weak pull-down for a remote wake-up request and strong pull-down for a local wake-up request; RXD is placed at low-level that can be used as an interrupt for the microcontroller. These wake-up source flags are cleared once the CA-IF1021Lx-Q1 leaves standby mode

9.4.1. Remote Wake-up

The bus wake-up, also called remote wake-up, changes the transceiver's operation mode from sleep mode to standby mode. A falling edge on the LIN Bus, followed by a valid dominant bus signal for $t > t_{wake(dom)LIN}$, bus results in a bus wake-up event. The mode change to standby mode is performed with the subsequent rising edge on the LIN bus(the change from dominant to recessive), see Figure 9-2. Remote Wake-up.

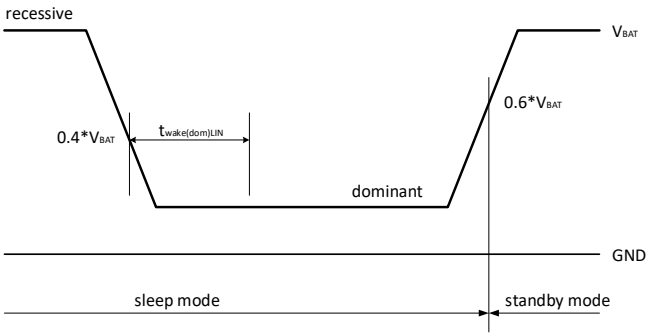


Figure 9-2. Remote Wake-up

Remote wake-up capability allows the CA-IF1021Lx-Q1 to restore power to the node upon detection of LIN bus activity. Once a successful wake-up event is detected. The external microcontroller can drive the SLP_N high based on the wake-up signal from RXD for normal operation. RXD is floating until a valid wake-up is received during sleep mode, see Figure 9-1 for more details.

9.4.2. Local Wake-Up

A valid local wake-up request is generated when the logic level on WAKE_N changes to low and remains low-level stable for $t_{wake(dom)WAKE\_N}$. The WAKE_N pin has internal pull-up towards pin V_{BAT}. However, for the unused pin WAKE_N, it is recommended to connect pin WAKE_N to pin V_{BAT} to prevent EMI issues. The wake-up request is indicated by an active low signal on pin RXD, that can be used to interrupt the external microcontroller.

Also, it is possible to change a transceiver's mode from sleep mode to normal operation mode directly by setting the corresponding SLP_N input to high at least the time $t_{gotonorm}$. This feature is useful with an external microcontroller that is continuously powered, instead of being controlled by the INH output. The SLP_N pin has integrated pull-down resistor to ensure the transceiver remains in sleep mode or in standby mode even in case the pin SLP_N is unsupplied.

10. Application Information

The LIN interface is a single wire bidirectional bus used for in-vehicle networks. The CA-IF1021Lx-Q1 LIN transceiver is the interface between the microcontroller and physical LIN bus (see Figure 10-1). Every LIN network consists of a master node and one or more slave nodes. To configure the CA-IF1021Lx-Q1 transceiver for master node applications, a 1kΩ termination resistor and a diode must be connected between LIN bus and battery power supply V_{BAT} , connect 1nF bypass capacitor between LIN and GND, see Figure 10-1. As there is an internal pull-up resistor with a serial diode structure to V_{BAT} for the CA-IF1021Lx-Q1 LIN transmitter, so no external pull-up components are required for LIN slave node applications, a 220pF bypass capacitor is needed between LIN and GND.

The CA-IF1021Lx-Q1 devices support 3.3V and 5.0V logic input, allowing operation with a variety of microcontrollers with common I/O voltage levels. The receive data outputs RXD features open drain behavior for allowing the output level to the microcontroller supply voltage. In case the microcontroller port pin does not provide integrated pull-up, an external pull-up resistor connected to the microcontroller logic supply voltage is required as shown in below typical application circuit.

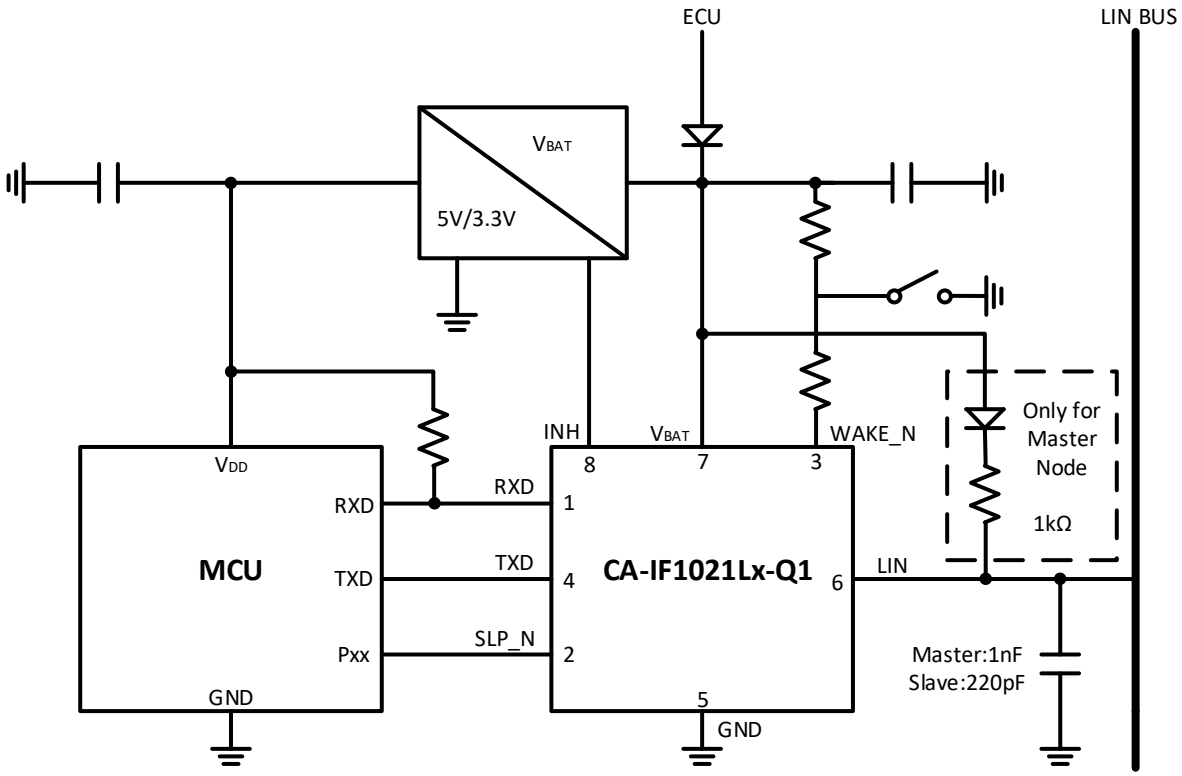
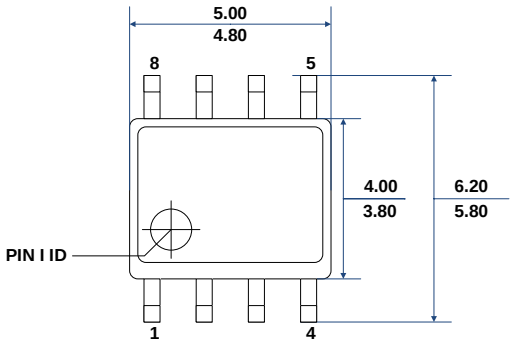


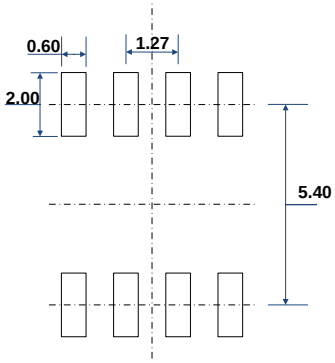
Figure 10-1. CA-IF1021 Typical Application Circuit in LIN Bus

11. Package Information

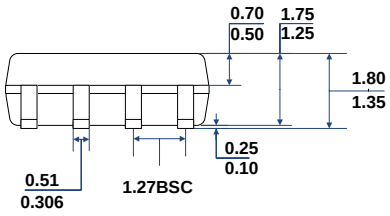
SOIC8 Package Outline



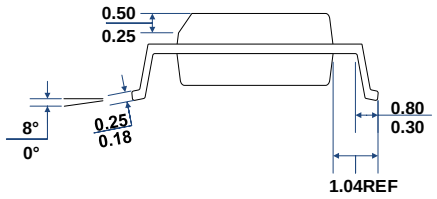
TOP VIEW



RECOMMENDED LAND PATTERN



FRONT VIEW



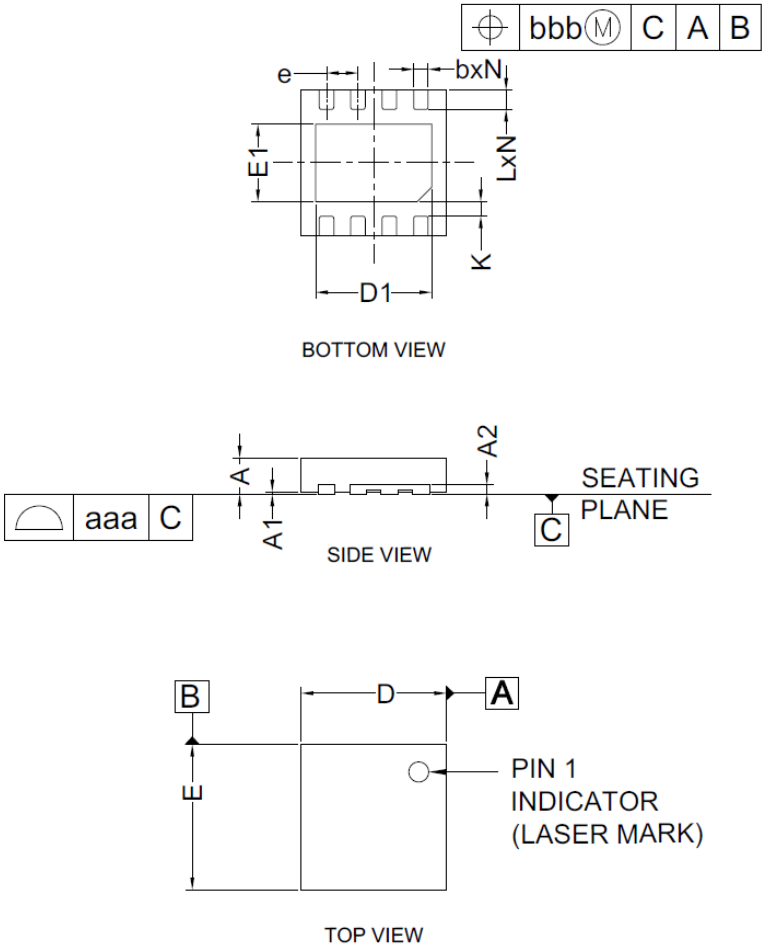
LEFT-SIDE VIEW

Note:

1. Controlling dimensions are in millimeters.

Figure 11-1. SOIC8 Package Outline

DFN8 Package Outline



COMMON DIMENSIONS

(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	TYP	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A2		0.203	
b	0.25	0.30	0.35
D	2.90	3.00	3.10
D1	2.35	2.40	2.45
E	2.90	3.00	3.10
E1	1.55	1.60	1.65
e		0.65BSC	
L	0.35	0.40	0.45
K	0.20	-	-
N		8	
aaa		0.08	
bbb		0.10	

Note:

1. Controlling dimensions are in millimeters.

Figure 11-2. DFN8 Package Outline

12. Soldering Temperature (reflow) Profile

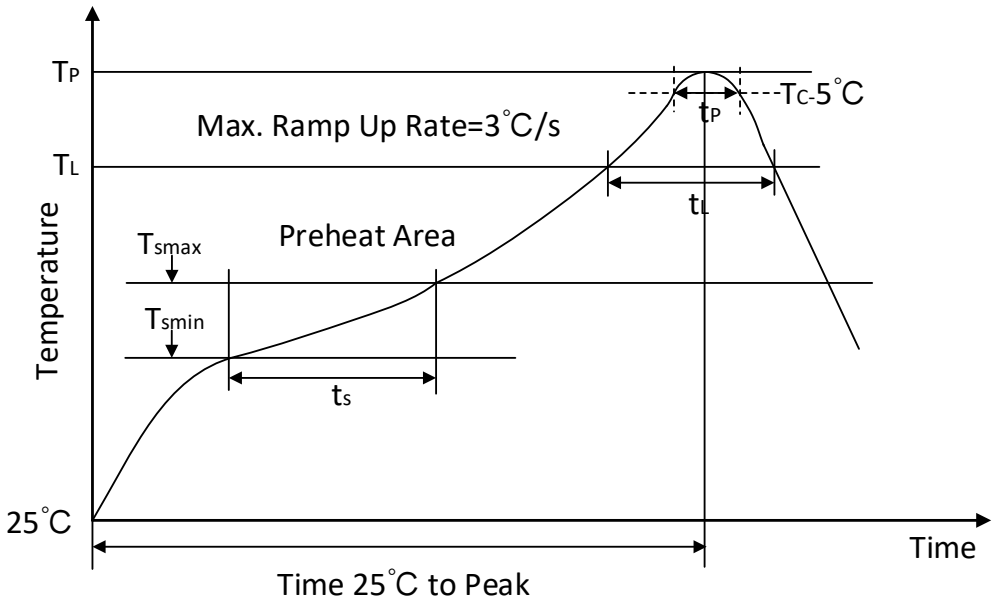


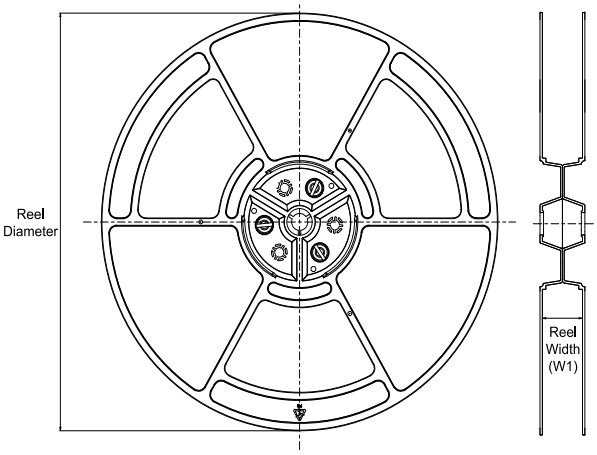
Figure 12-1. Soldering Temperature (reflow) Profile

Table 12-1. Soldering Temperature Parameter

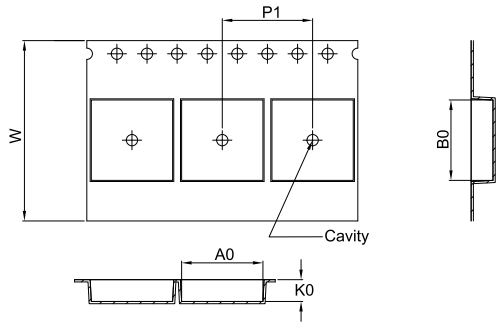
Profile Feature	**Pb-Free Assembly**
Average ramp-up rate(217 ℃ to Peak)	3℃/second max
Time of Preheat temp(from 150 ℃ to 200 ℃	60-120 second
Time to be maintained above 217 ℃	60-150 second
Peak temperature	260 +5/-0 ℃
Time within 5 ℃of actual peak temp	30 second
Ramp-down rate	6 ℃/second max.
Time from 25℃ to peak temp	8 minutes max

13. Tape and Reel Information

REEL DIMENSIONS

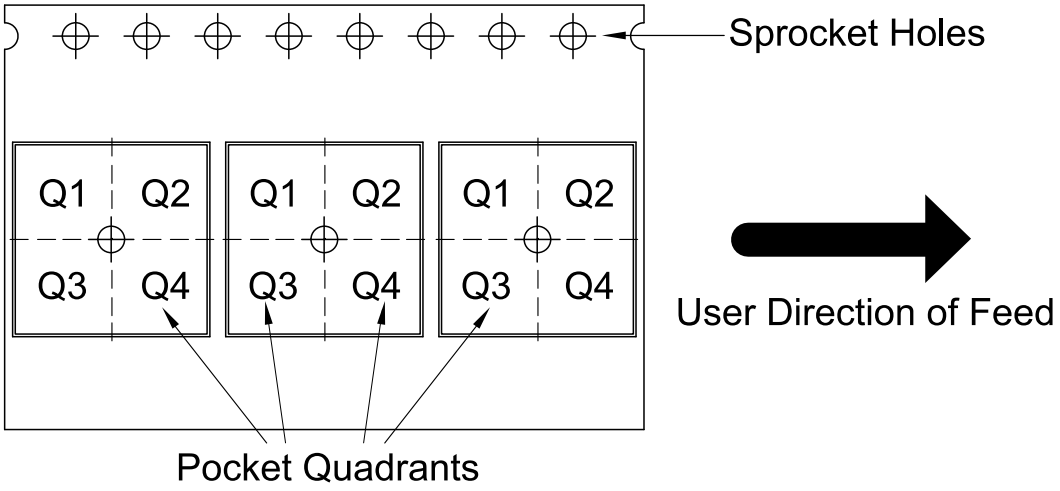


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CA-IF1021LS-Q1	SOIC	S	8	2500	330	12.4	6.5	5.4	2.1	8	12	Q1
CA-IF1021LD-Q1	DFN	D	8	3000	330	12.4	3.3	3.3	1.1	8	12	Q1

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