# EMI-Optimized Design for the CA-IS3115AW Isolated DC-DC Converter

## Contents

# 1. Introduction

This document is designed to complement the CA-IS3115AW data sheet to provide a low-EMI design solution for isolated power supply. This application note discusses EMI suppression, provides a reference design and the test result according to EN55032(CISPR32) Class-B standard for the CA-IS3115AW based on both 2-layer and 4-layer board designs. Also refer AN001.pdf (chipanalog.com) for more details about EMI optimized design.

The CA-IS3115X typical application circuit is shown in Figure.

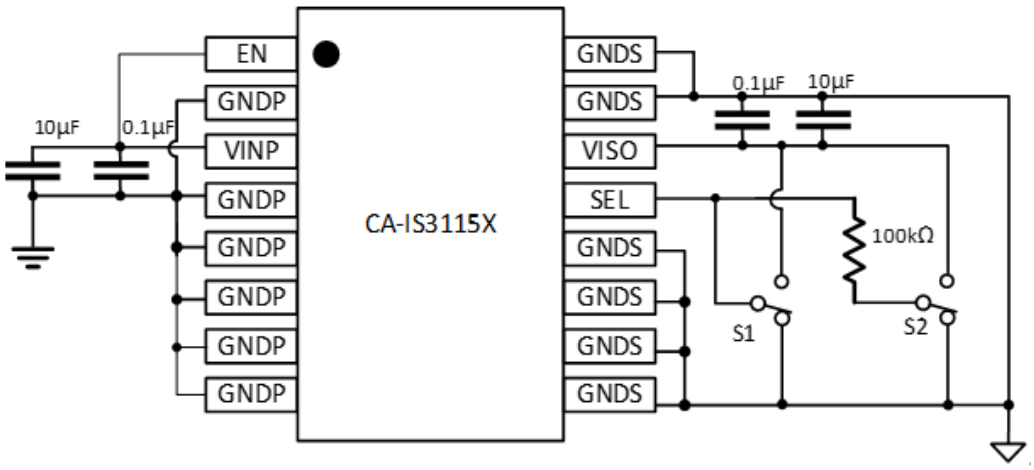


**Figure 1-1. Typical application circuit**

# 2. EMI-Optimized Design

## 2.1. CA-IS3115AW General Description

he CA-IS3115AW is a complete isolated DC/DC converter with up to 5kV$_{RMS}$ isolation. This device integrates most of the components required for an isolated power supply - switching regulator, power switches, transformer, soft start, protection circuitry, etc. - in a single, compact SOIC package. The CA-IS3115AW operates from an input voltage range of 4.5V to 5.5V and provides a fixed output voltage of 3.3V, 3.7V, 5V or 5.4V set by pin SEL. The 3.7V and 5.4V output options provide headroom to drive an LDO. Only output and input bypass capacitors and a pull-up resistor for 3.7V or 5.4V outputs are required to complete the design. Figure 2 1 shows the block diagram of the CA-IS3115AW.

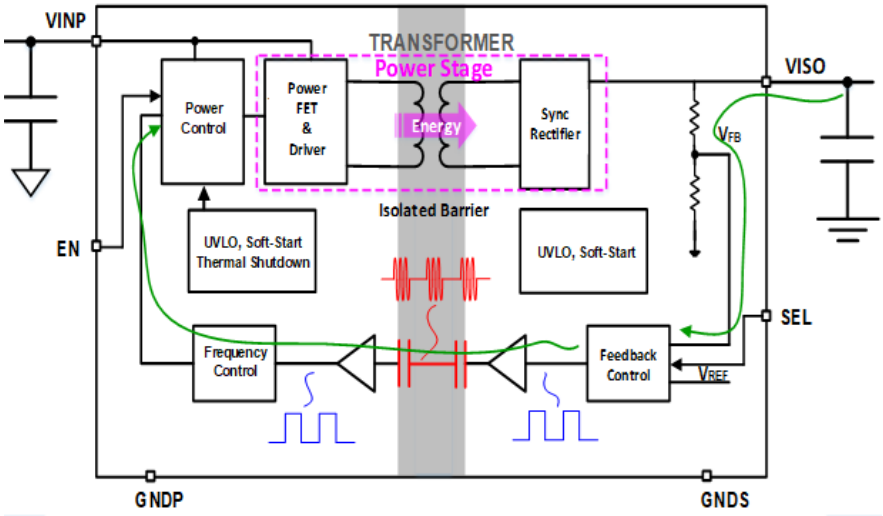


**Figure 2-1. Functional Block Diagrams**

Connecting the EN pin to VINP or force this pin high to turn on the DC-DC converter. The secondary-side (VISO) controller sends control signal to the primary-side through a individual digital isolation channel, and the primary-side control circuit adjusts the energy transmission based-on the feedback signal from the secondary-side to provide a regulated output at VISO. The CA-IS3115AW features a unique control scheme, which can quickly respond to load transient and accurately regulate the output voltage. The device is capable of delivering a load up to 1.5W output power and offering soft-start, UVLO, short-circuit protection and thermal shutdown protection features to better enhance the reliability of the system. The high di/dt and dv/dt caused by on-chip transformer's high-frequency switching operation is the main radiation resource. Also, designers need to consider the common-mode noise generated by parasitic components on the primary-side and secondary-side transformer coils. The following sections provide detailed description about how to minimize EMI and reflections.

## 2.2. EMI Filter and Component Placement

### 2.2.1. Decoupling Capacitor Placement

Careful PCB layout is essential to achieve clean and stable operation. To ensure reliable operation of the device in noisy environments, we recommend the addition of a minimum 10nF high frequency bypass capacitor and a bulk energy storage capacitor (10μF) in parallel between the power supply input VINP and GNDP, and between the isolated power supply output VISO and GNDS. By selecting a 10nF to 100nF low ESL/low ESR MLCC capacitor as the high frequency decoupling capacitor, these capacitors must also be placed closer to the VINP and VISO pins, the maximum distance being within 2mm, to reduce parasitic inductance and current loop. This is very important for optimised EMI performance, see Figure 2 2 recommended decoupling capacitor placement for PCB layout.

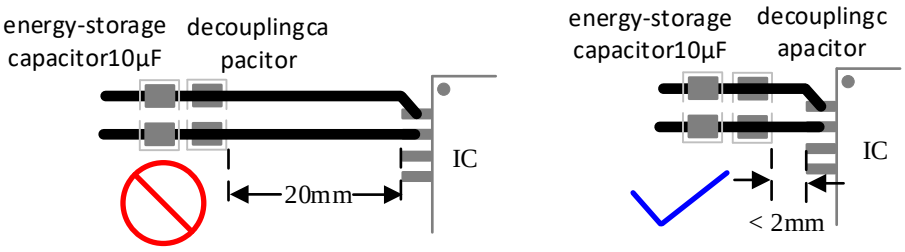


**Figure 2-2. Decoupling capacitor placement**

### 2.2.2. Y-capacitor

During high frequency operation, the common mode current creates a current loop between the parasitic capacitance of the primary and secondary coils and the parasitic capacitance of the PCB. The larger the loop area, the greater the radiation generated. It is recommended that a Y capacitor is placed across the isolation barrier, between the primary reference ground (GNDP) and the secondary reference ground (GNDS). The Y-capacitor creates a very short path with a small loop area for the parasitic current to return to the primary side, reducing the EMI generated on the board as shown in Figure 2 3. The larger capacitance value can better suppress EMI. For the multi-layer PCB design, the overlap stitch capacitance is usually chosen. In the 4-layer board reference design of the CA-IS3115AW, a stitch capacitance is placed in the middle two layers as shown in Figure 2-3(right), which provides better EMI performance. The stitch capacitance is proportional to the overlapping area(s) of two PCB layers and inversely proportional to the relative distance (d) between the two layers.

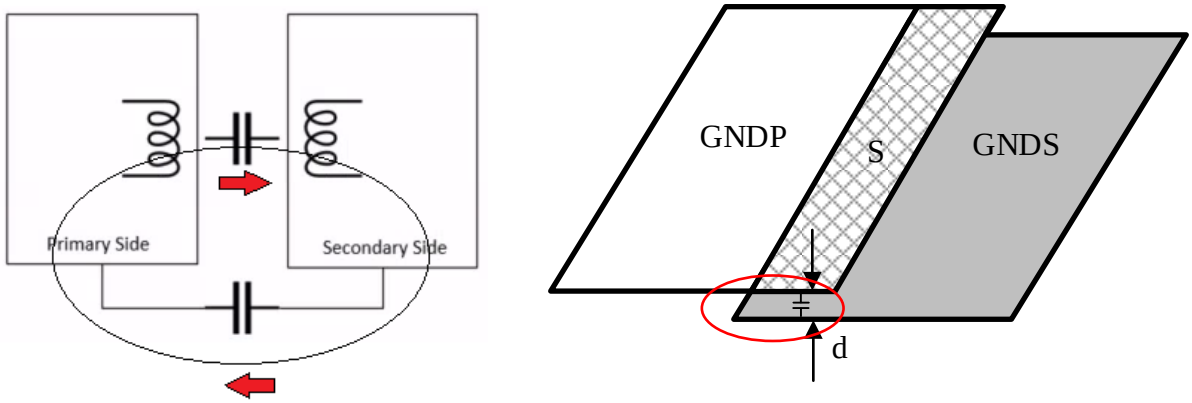


**Figure 2-3. Y-capacitor placement**

### 2.2.3. Ferrite Bead/Common-mode Inductor/Differential-mode Inductor

On the primary side, a pair of ferrite beads with high frequency impedance in the range of 600Ω to 2KΩ @ 100MHz are placed in series with the power line and ground, breaking the path of larger common mode current loops. This provides further high frequency attenuation and blocks switching noise. Place the bead close to the decoupling capacitors as shown in Figure 2-4.

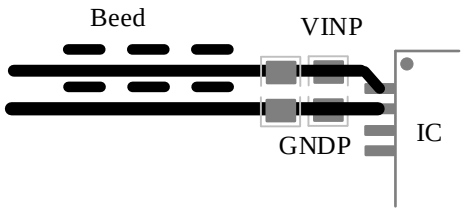


**Figure 2-4. Ferrite beads placement**

Also, a common mode inductor (CM choke, 1KΩ-5KΩ@100MHz) or/and a differential mode inductor may be an option based on the EMI test result, see Figure 2-5. In the CA-IS3115AW reference design, to reduce low-frequency noise, a CM choke or/and two differential mode inductors (L1, L2) are added between the input power supply and the primary-side power supply input in the different solutions, see CA-IS3115AW Low-EMI Reference Design section for more details. Ground planes under these magnetic components must be avoided to prevent the parasitic capacitance from affecting the high-frequency attenuation.

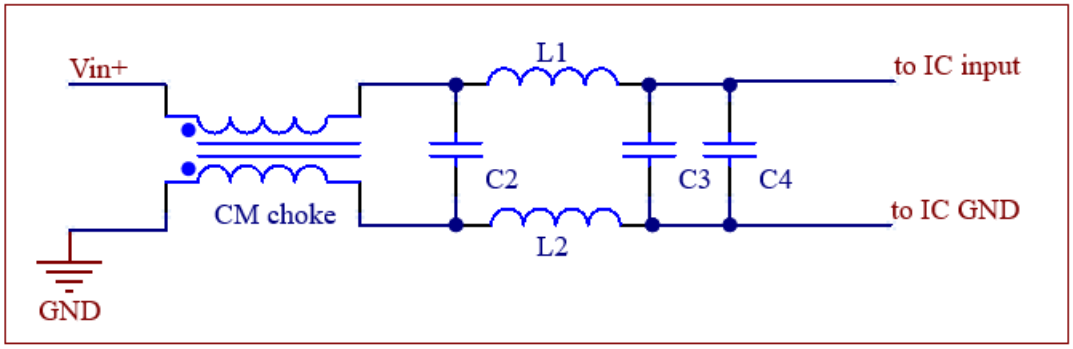


**Figure 2-5. CM choke and differential-mode inductor**

### 2.2.4. Building the edge guarding

A grounding via can be added around the board to form a via guard ring and return the noise to ground to reduce radiation and interference to the external system, as shown in Figure 2-6. If there are more than two rows of vias, the vias placed in the two rows should be staggered.

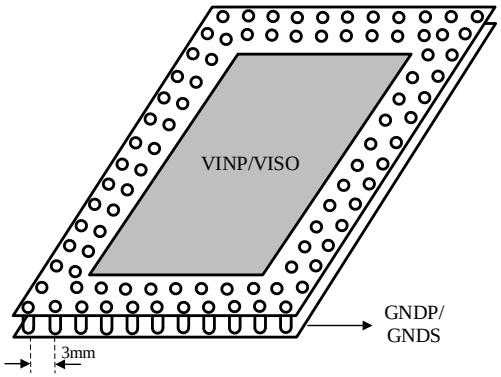


**Figure 2-6. Vias guard ring around the edges of ground layers**

# 3. CA-IS3115AW Reference Designs

## 3.1. Reference Design Overview

Chipanalog offers three reference designs for the CA-IS3115AW,

a) 2-layer PCB with CM-choke and without overlap stitching capacitance, differential-mode inductor on board;

b) 4-layer PCB with CM-choke, overlap stitching capacitance and differential-mode inductor on board;

c) 4-layer PCB with overlap stitching capacitance and differential-mode inductor, without CM-choke on board

**Table 3-1. Reference design summary**

| Board | Design margin | Frequency | PCB-layers | Overlap capacitors | Y-capacitor | Common-mode inductor | Differential-mode inductor |
|---|---|---|---|---|---|---|---|
| Reference design I | 1.07dB | 287MHz | 2 | N/A | 19pF | 500Ω(@100MHz) | N/A |
| Reference design II | 4.31dB | 277MHz | 4 | S = 120mm² d = 1mm | 19pF | 1000Ω(@100MHz) | 2μH(2pcs) |
| Reference design III | 1.29dB | 462MHz | 4 | S = 120mm² d = 1mm | 19pF | N/A | 2μH(2pcs) |

**Note:**
S is the overlapping area of two PCB layers, d is the relative distance between the two layers.

## 3.2. 2-layer PCB with CM-choke on Board

### 3.2.1. PCB Layout Procedure

1) On the reference design board, the LM1086ISX-ADJ(U1) 12V to 5V LDO is selected to provide a clean +5V supply for all components on board.
2) Place decoupling capacitors as close as possible to the device pins, maximum distance is less than 2mm, see Figure 3-1, C3/C4 and C5/C6.
3) Install the CM-chock (CM2) and ferrite beads on the primary-side supply input. Place BD1/BD2/BD3/BD4 close to C3/C4.
4) Across primary-side and secondary side grounds, place Y-capacitors and damping resistor between GNDP and GNDS of the CA-IS3115AW.
5) R3 and R4 are the load of isolated power supply output ( 5V/200mA).
6) A grounding vias are added around the PCB to form a via guard ring for both primary-side and secondary-side.

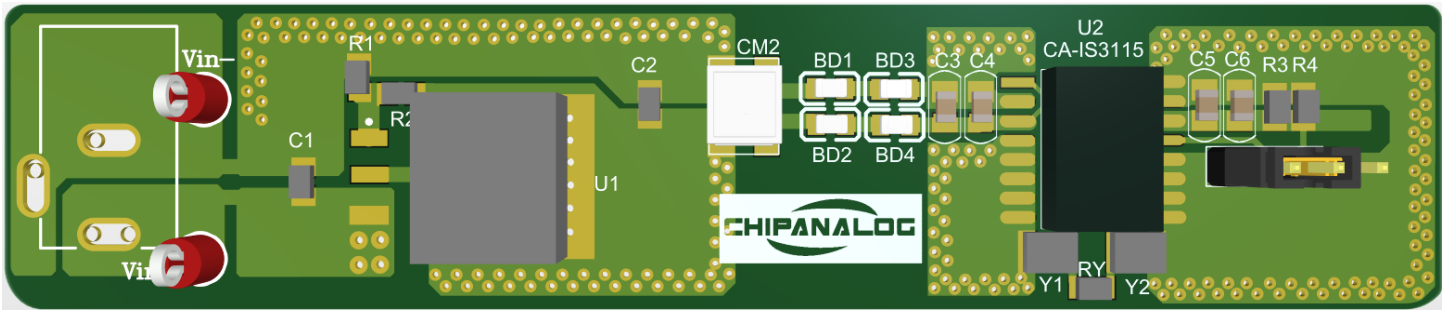


**Figure 3-1. CA-IS3115AW reference design board (2-layer PCB)**

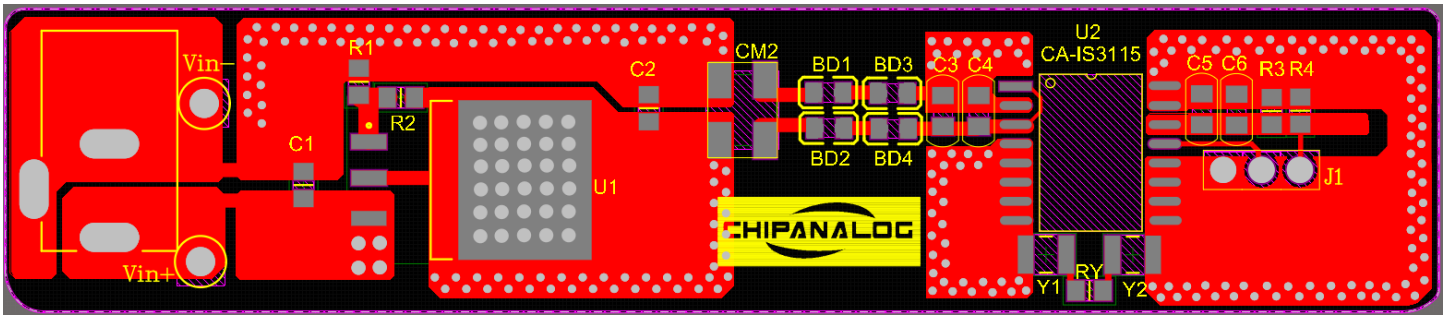


**Figure 3-2. Reference design PCB_ top layer**

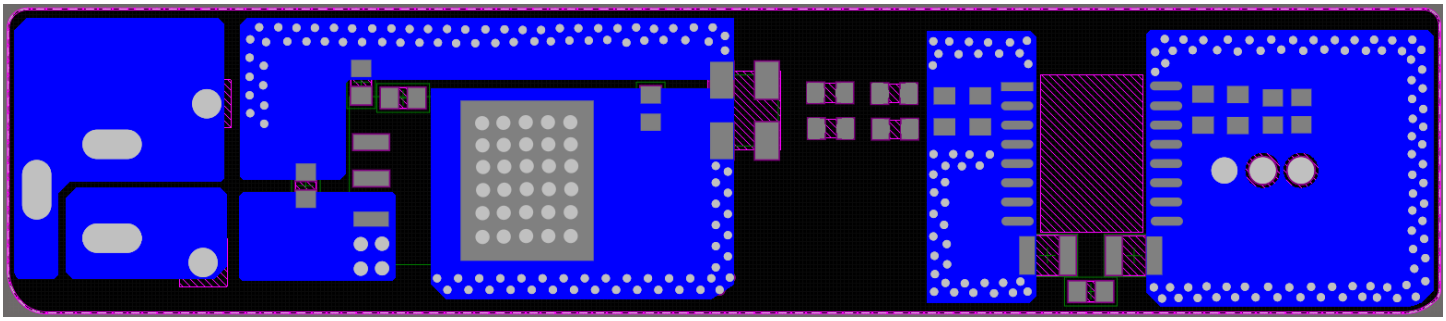

**Figure 3-3. Reference design PCB_ bottom layer**

### 3.2.2. CA-IS3115AW Reference Design Schematic (2-layer PCB)

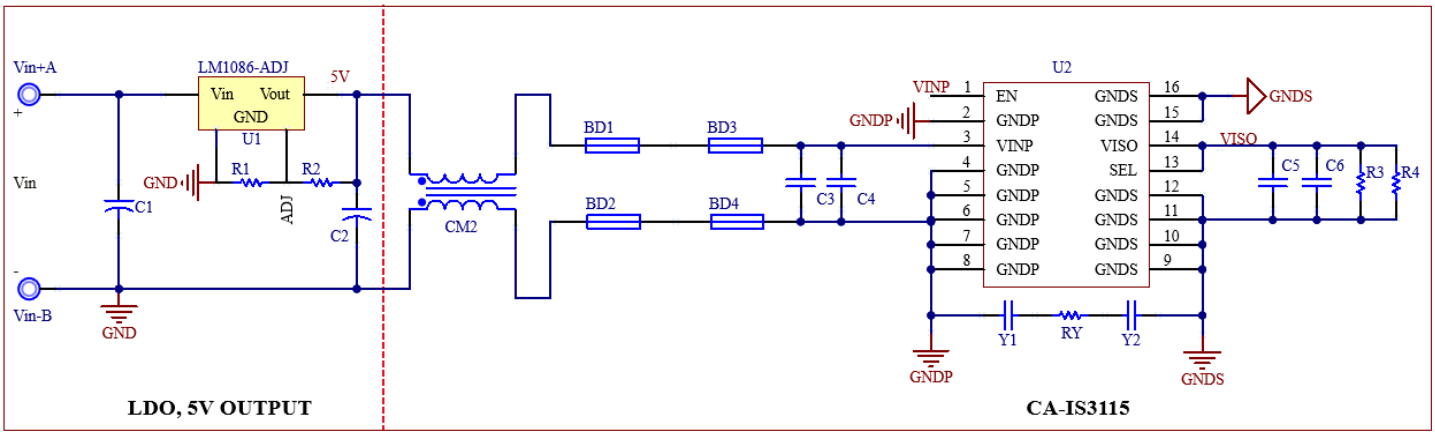


**Figure 3-4. CA-IS3115AW test board schematic (2-layer PCB)**

**Table 3-2. Component List**

| Device name | Designation | Spec | Part number | Note |
|---|---|---|---|---|
| Decoupling capacitors | C4, C5 | 10nF | | |
| | C3, C6 | 10μF | | |
| Common-mode inductor | CM2 | 500Ω (@100MHz) | DLW5ATH501TQ2 | |
| Ferrite bead | BD1, BD2 | 600Ω (@100MHz) | BLM18DN601SN1 | |
| | BD3, BD4 | 1KΩ (@100MHz) | BLM18HE102SN1 | |
| Y capacitor | Y1, Y2 | 39pF | GRM31A7U3D390JW31 | |
| Damping resistor | RY | 10Ω | | Connected with Y-capacitor in series |

### 3.2.3. Reference Design Test Result for the 2-layer PCB

The test result for the 2-layer PCB design is shown in Figure 3-5 and Figure, this solution meets EN55032(CISPR32) radiated emissions Class B standard, and also leave 1.07dB (horizontal)/4.31dB(vertical) design margin.

**Table 3-3. Reference design EMI test result summary**

| Input voltage | Output voltage | Load current | Design margin | |
|---|---|---|---|---|
| | | | vertical | horizontal |
| 5V | 5V | 200mA | 4.31dB | 1.07dB |

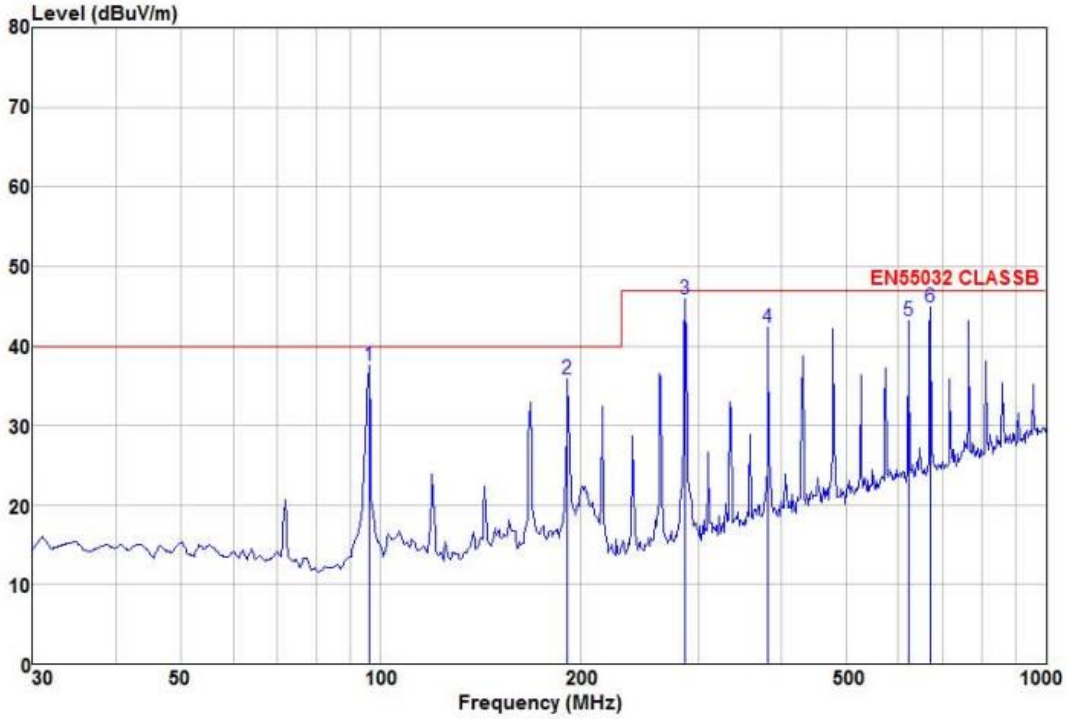


**Figure 3-5. Horizontal radiation test result**

**Test result:** 30MHz to 1GHz frequency range, Margin = 1.07dB.

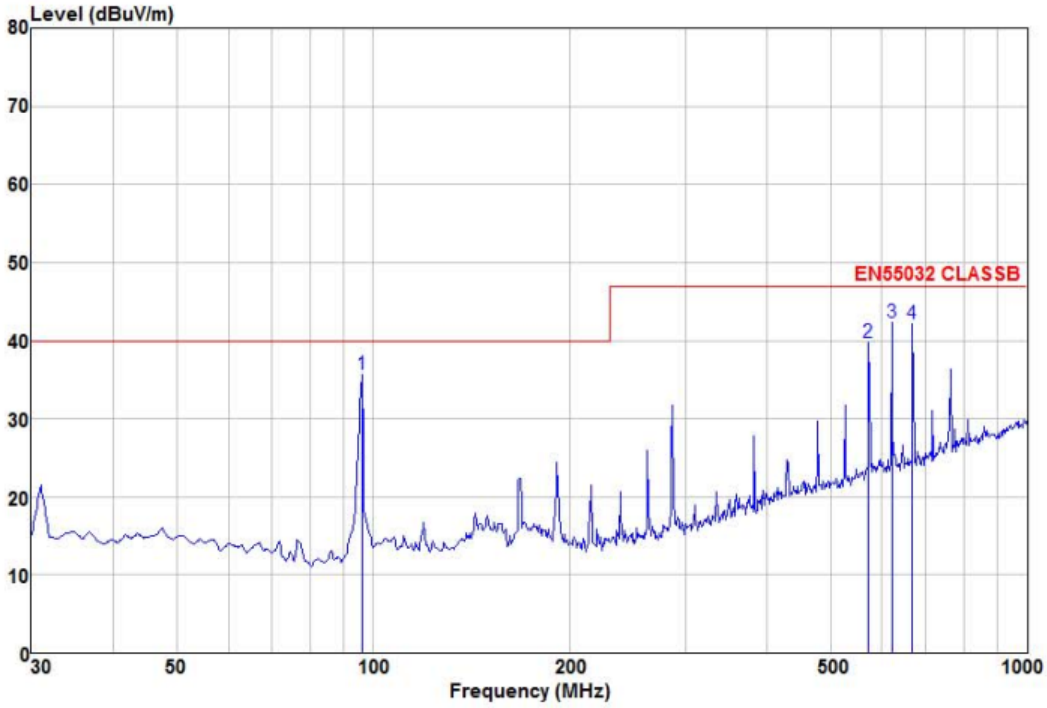


**Figure 3-6. Vertical radiation test result**

**Test result:** 30MHz to 1GHz frequency range, Margin = 4.31dB

### 3.3. 4-Layer PCB with CM-choke on Board

#### 3.3.1. PCB Layout Procedure

1) On the reference design board, the LM1086ISX-ADJ(U1) 12V to 5V LDO is selected to provide a clean +5V supply for all components on board.
2) Place decoupling capacitors as close as possible to the device pins, maximum distance is less than 2mm, see Figure 3-7, C3/C4 and C5/C6.
3) Install the CM-chock (CM2), differential-mode inductors(L1/L2) and ferrite beads on the primary-side supply input. Place BD1/BD2 close to C3/C4.
4) Across primary-side and secondary side grounds, place Y-capacitors and damping resistor between GNDP and GNDS of the CA-IS3115AW.
5) R3 and R4 are the load of isolated power supply output (5V/200mA);
6) Place stitching capacitance in the middle two layers (layer 2/3).
7) A grounding vias are added around the PCB to form a via guard ring for both primary-side and secondary-side.

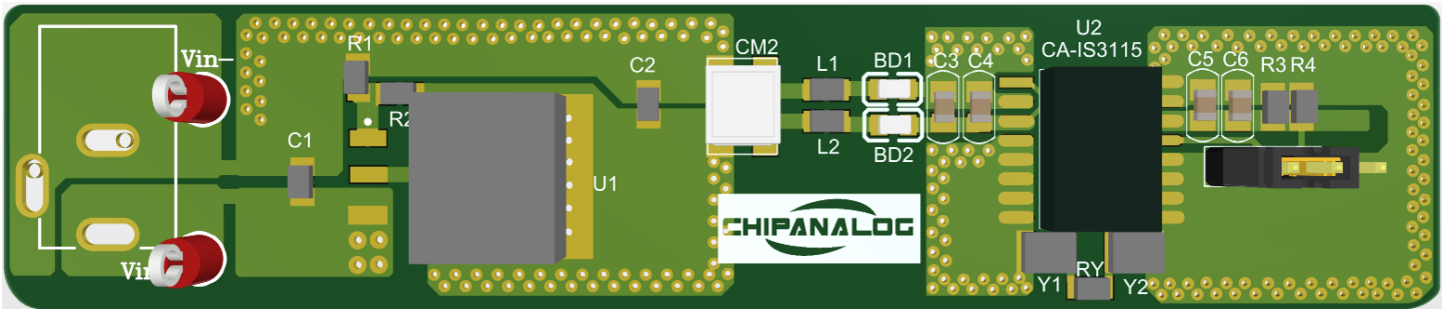


**Figure 3-7. CA-IS3115AW reference design board (4-layer PCB)**

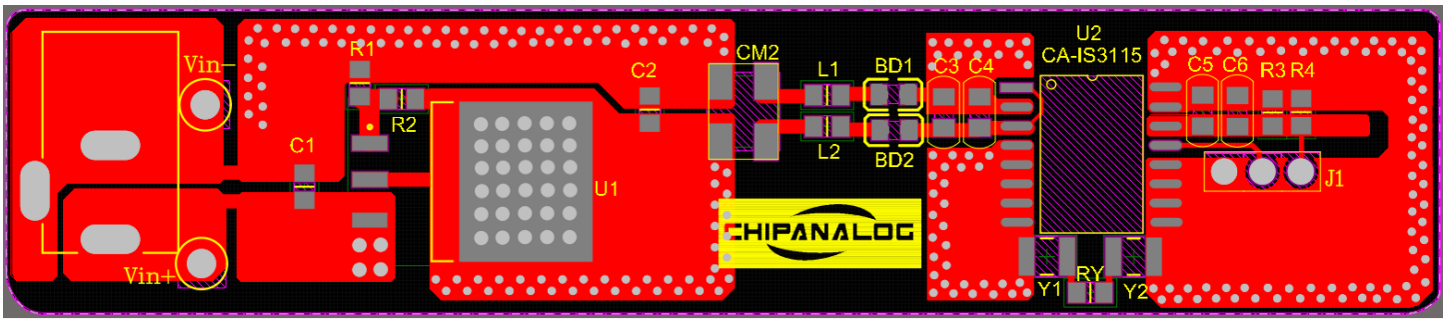


**Figure 3-8. Reference design PCB_ top layer**

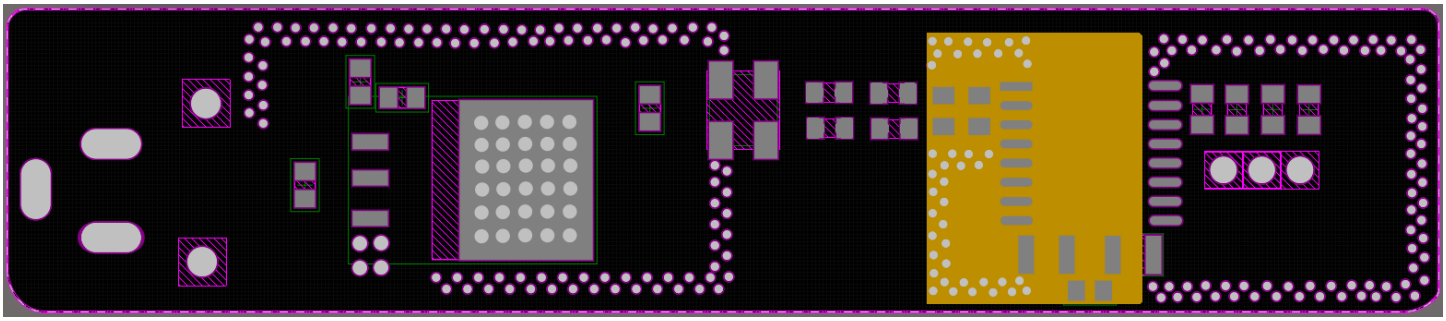

Figure 3-9. Reference design PCB_ layer 2

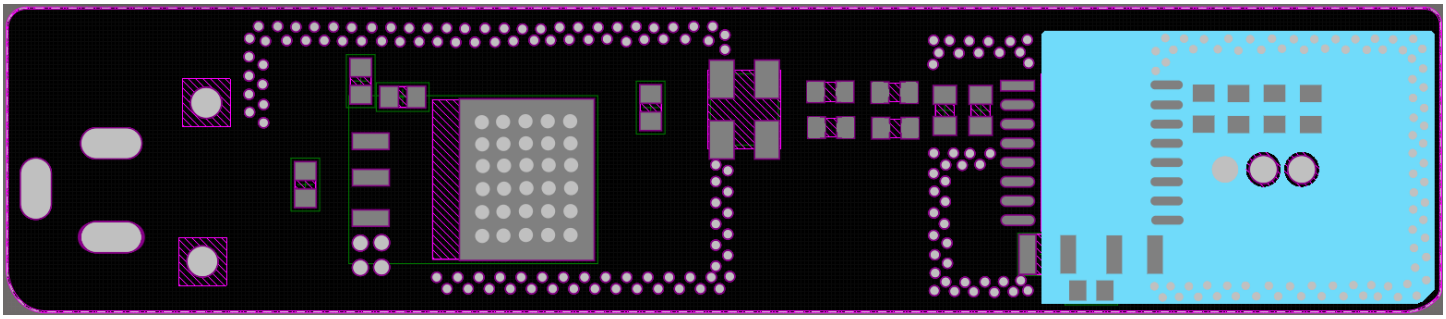

Figure 3-10. Reference design PCB_ layer 3

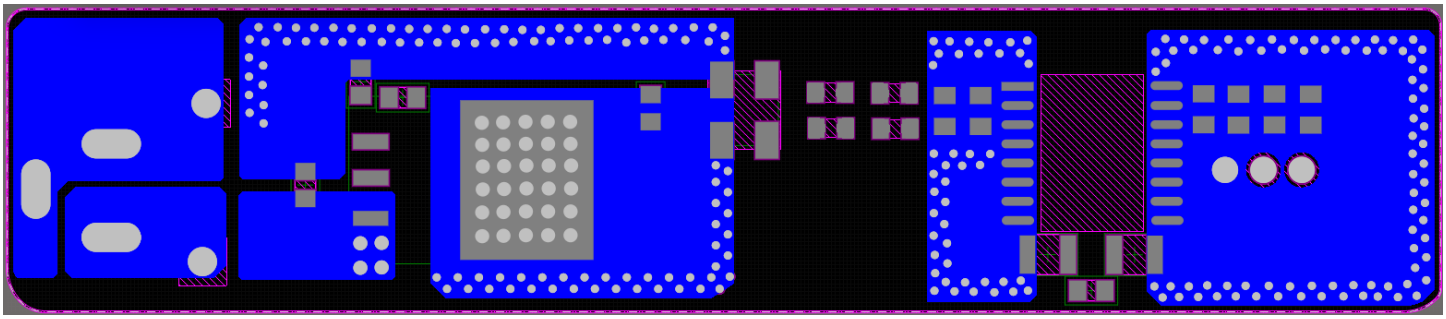

Figure 3-11. Reference design PCB_ bottom layer

### 3.3.2. CA-IS3115AW Reference Design Schematic(4-layer PCB)

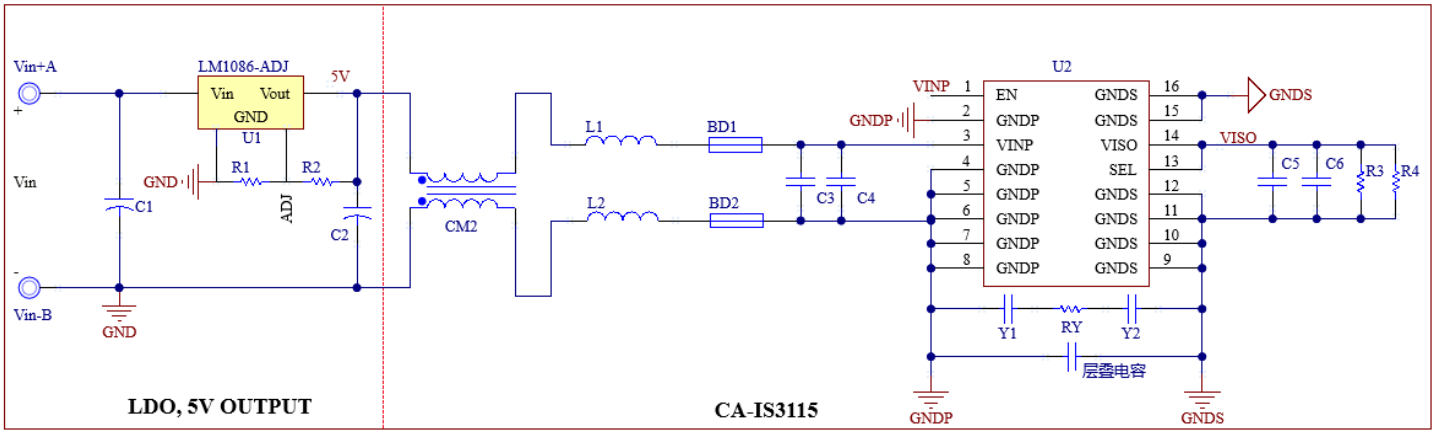


**Figure 3-12. CA-IS3115AW test board schematic (4-layer PCB)**

**Table 3-4. Component List**

| Device name | Designation | Spec | Part number | Note |
|---|---|---|---|---|
| Decoupling capacitors | C4, C5 | 10nF | | |
| | C3, C6 | 10μF | | |
| Common-mode inductor | CM2 | 1kΩ (@100MHz) | DLW5BTH102TQ2 | |
| Ferrite bead | BD3, BD4 | 1KΩ (@100MHz) | BLM18HE102SN1 | |
| Differential-mode inductors | L1, L2 | 2.2μH | MLZ2012M2R2HT000 | |
| Y capacitor | Y1, Y2 | 39pF | GRM31A7U3D390JW31 | |
| Overlap Y capacitance | Between layer 2 and layer 3 | S = 120mm²<br>d = 1mm | | |
| Damping resistor | RY | 10Ω | | Connected with Y-capacitor in series |
| **Note:**<br>S is the overlapping area of two PCB layers, d is the relative distance between the two layers. | | | | |

### 3.3.3. Reference Design Test Result for the 4-layer PCB

The test result for a 4-layer PCB design is shown in Figure 3-13 and Figure 3-14, this solution meets EN55032(CISPR32) radiated emissions Class B standard, and also leave 4.31dB (horizontal)/9dB(vertical) design margin.

**Table 3-5. Reference design EMI test result summary**

| Input voltage | Output voltage | Load current | Design margin | |
|---|---|---|---|---|
| | | | vertical | horizontal |
| 5V | 5V | 200mA | 9dB | 4.31dB |

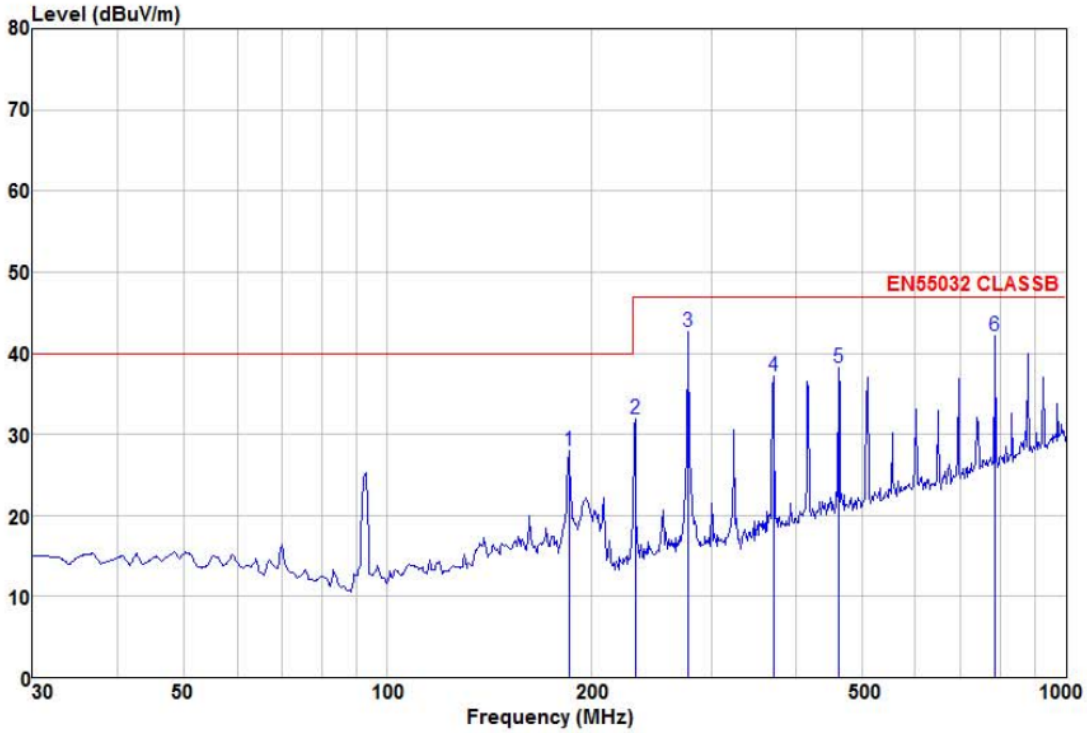


**Figure 3-13. Horizontal radiation test result**

**Test result:** 30MHz to 1GHz frequency range, Margin = 4.31dB.

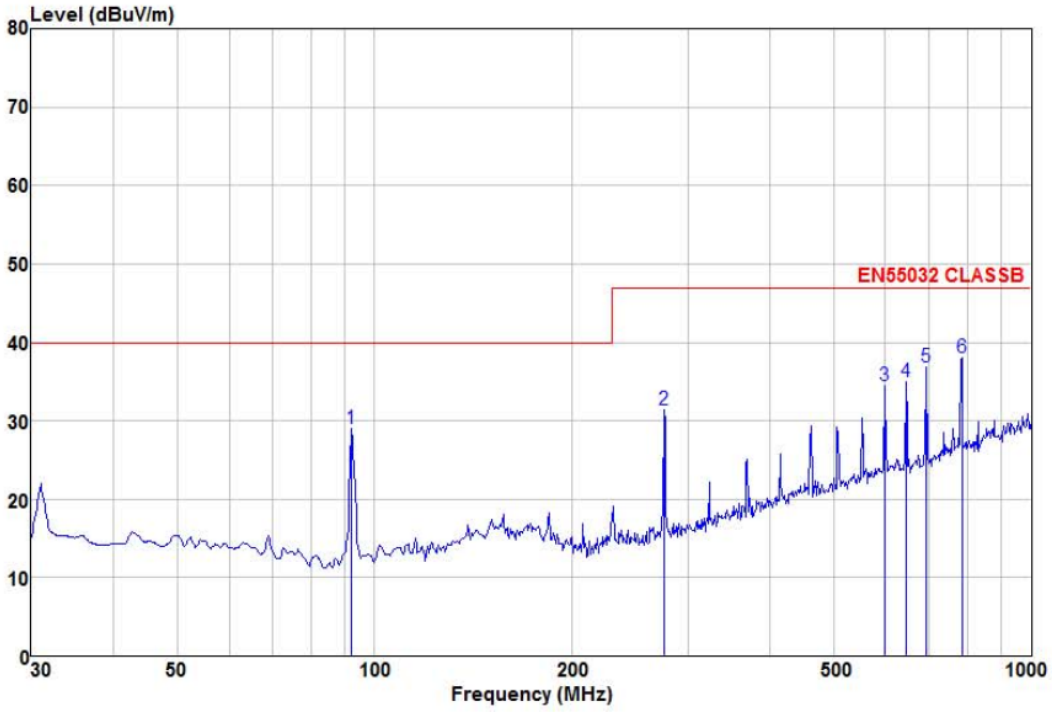


**Figure 3-14. Vertical radiation test result**

**Test result:** 30MHz to 1GHz frequency range, Margin = 9dB.

### 3.4. 4-Layer PCB without CM-choke on Board

#### 3.4.1. PCB Layout Procedure

1) On the reference design board, the LM1086ISX-ADJ(U1) 12V to 5V LDO is selected to provide a clean +5V supply for all components on board.
2) Place decoupling capacitors as close as possible to the device pins, maximum distance is less than 2mm, see Figure 3-7, C3/C4 and C5/C6.
3) Install the differential-mode inductors(L1/L2) and ferrite beads on the primary-side supply input. Place BD1/BD2 close to C3/C4.
4) Across primary-side and secondary side grounds, place Y-capacitors and damping resistor between GNDP and GNDS of the CA-IS3115AW.
5) R3 and R4 are the load of isolated power supply output ( 5V/200mA);
6) Place stitching capacitance in the middle two layers (layer 2/3).
7) A grounding vias are added around the PCB to form a via guard ring for both primary-side and secondary-side.

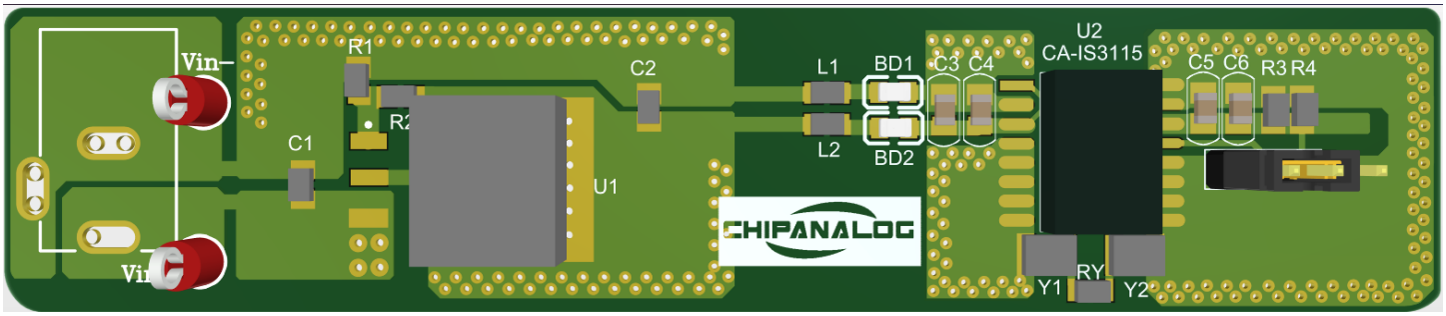


**Figure 3-15. CA-IS3115AW reference design board (4-layer PCB)**

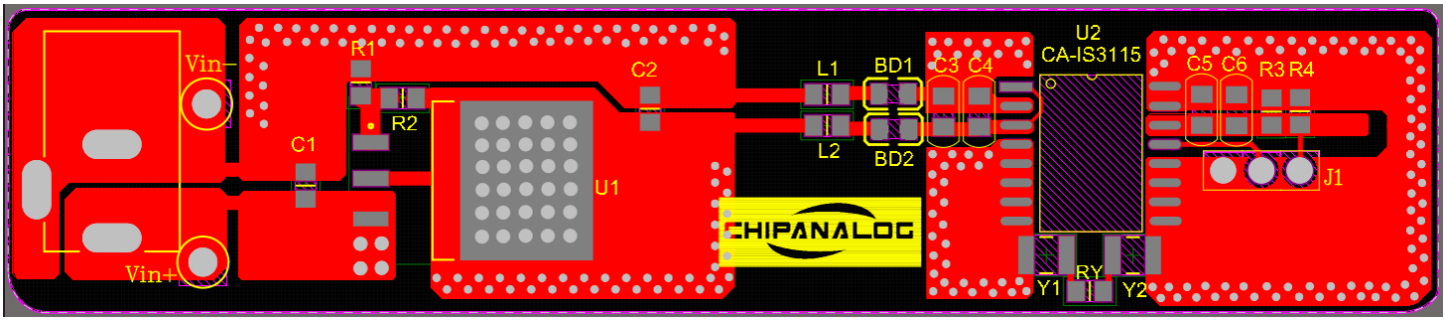


**Figure 3-16. Reference design PCB_ top layer**

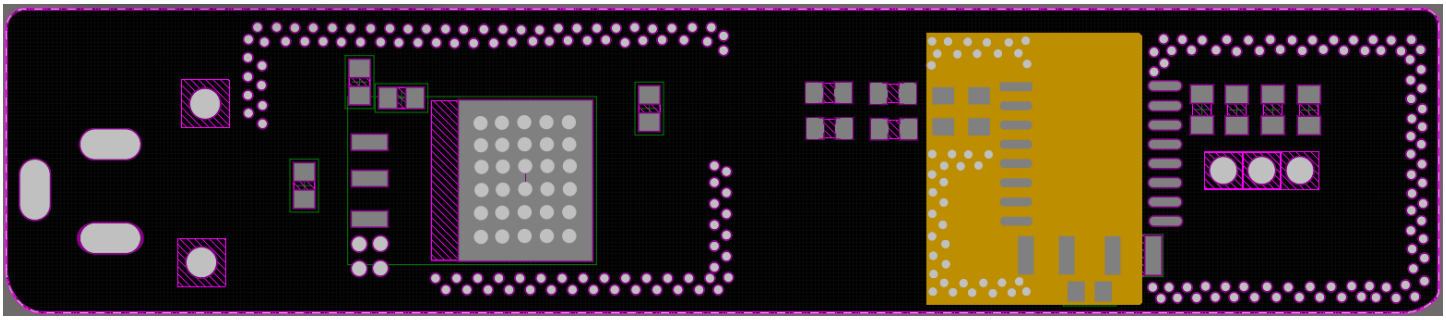

Figure 3-17. Reference design PCB_ layer 2

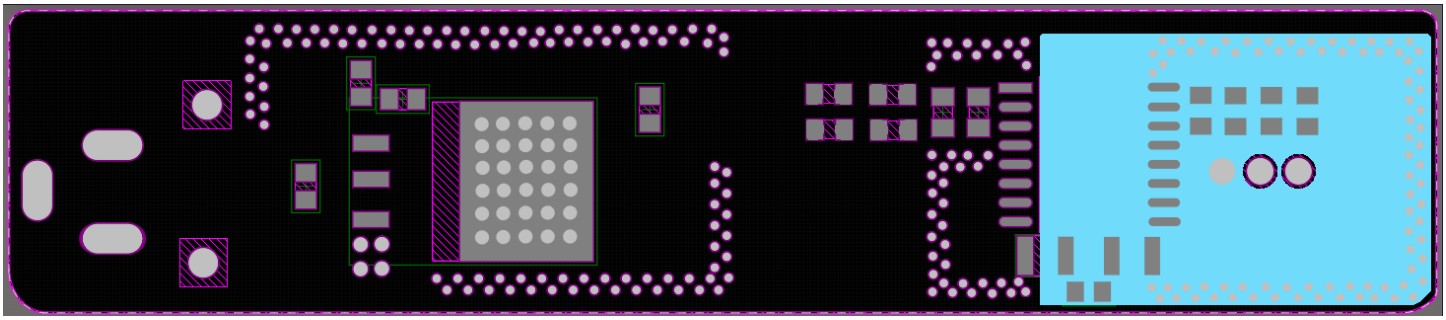

Figure 3-18. Reference design PCB_ layer 3

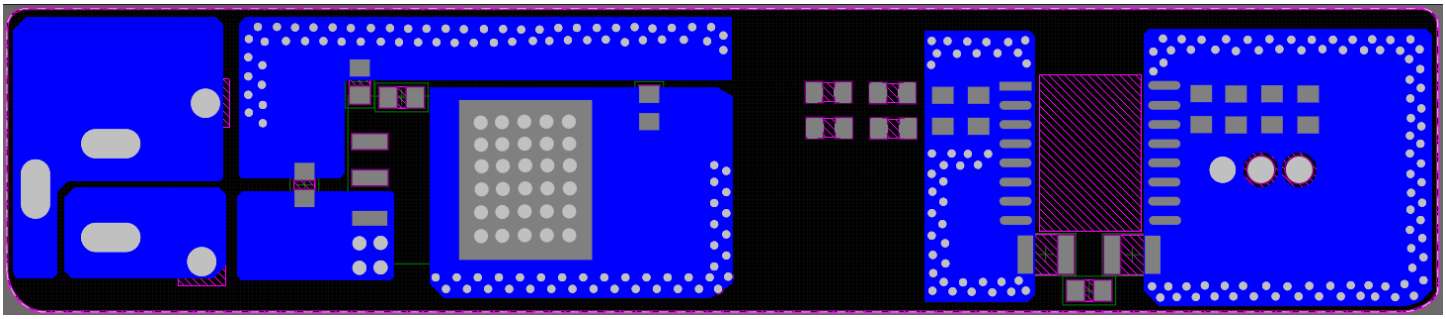

Figure 3-19. Reference design PCB_ bottom layer

### 3.4.2. CA-IS3115AW Reference Design Schematic (4-layer PCB)

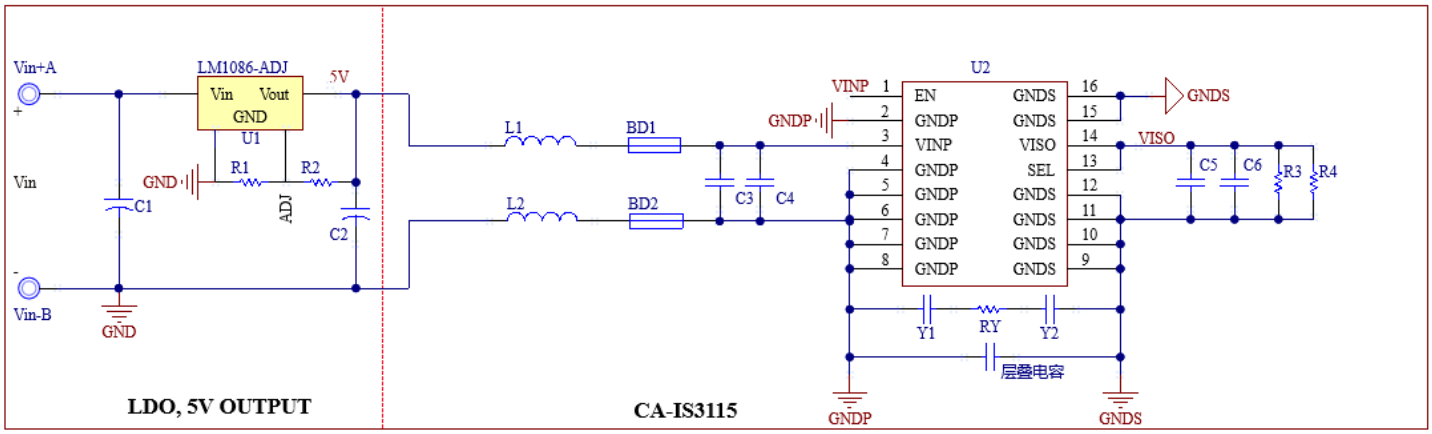


**Figure 3-20. CA-IS3115AW test board schematic (4-layer PCB)**

**Table 3-6. Component List**

| Device name | Designation | Spec | Part number | Note |
|---|---|---|---|---|
| Decoupling capacitors | C4, C5 | 10nF | | |
| | C3, C6 | 10μF | | |
| Ferrite bead | BD3, BD4 | 1KΩ (@100MHz) | BLM18HE102SN1 | |
| Differential-mode inductors | L1, L2 | 2.2μH | MLZ2012M2R2HT000 | |
| Y capacitor | Y1, Y2 | 39pF | GRM31A7U3D390JW31 | |
| Overlap Y capacitance | Between layer 2 and layer 3 | S = 120mm²<br>d = 1mm | | |
| Damping resistor | RY | 10Ω | | Connected with Y-capacitor in series |
| **Note:**<br>S is the overlapping area of two PCB layers, d is the relative distance between the two layers. | | | | |

### 3.4.3. Reference Design Test Result for the 4-layer PCB

The test result for a 4-layer PCB design is shown in Figure 3-21 and Figure 3-22, this solution meets EN55032(CISPR32) radiated emissions Class B standard, and also leave 1.29dB (horizontal)/2.77dB(vertical) design margin.

**Table 3-7. Reference design EMI test result summary**

| Input voltage | Output voltage | Load current | Design margin | |
|---|---|---|---|---|
| | | | vertical | horizontal |
| 5V | 5V | 200mA | 2.77dB | 1.29dB |

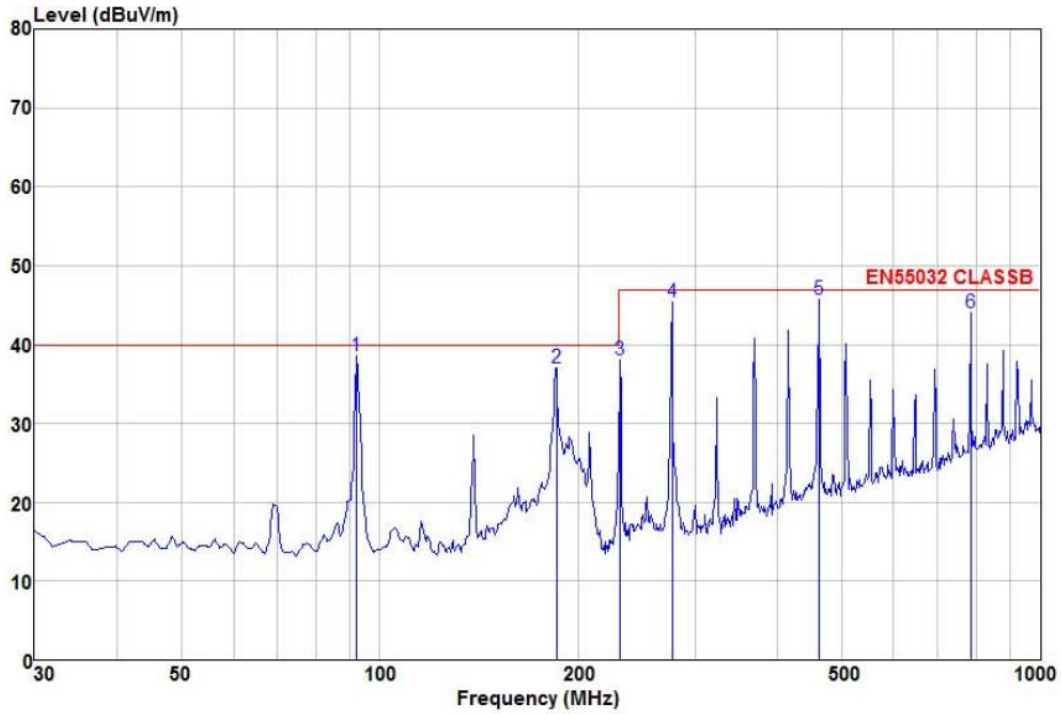


**Figure 3-21. Horizontal radiation test result**

**Test result:** 30MHz to 1GHz frequency range, Margin = 1.29dB.

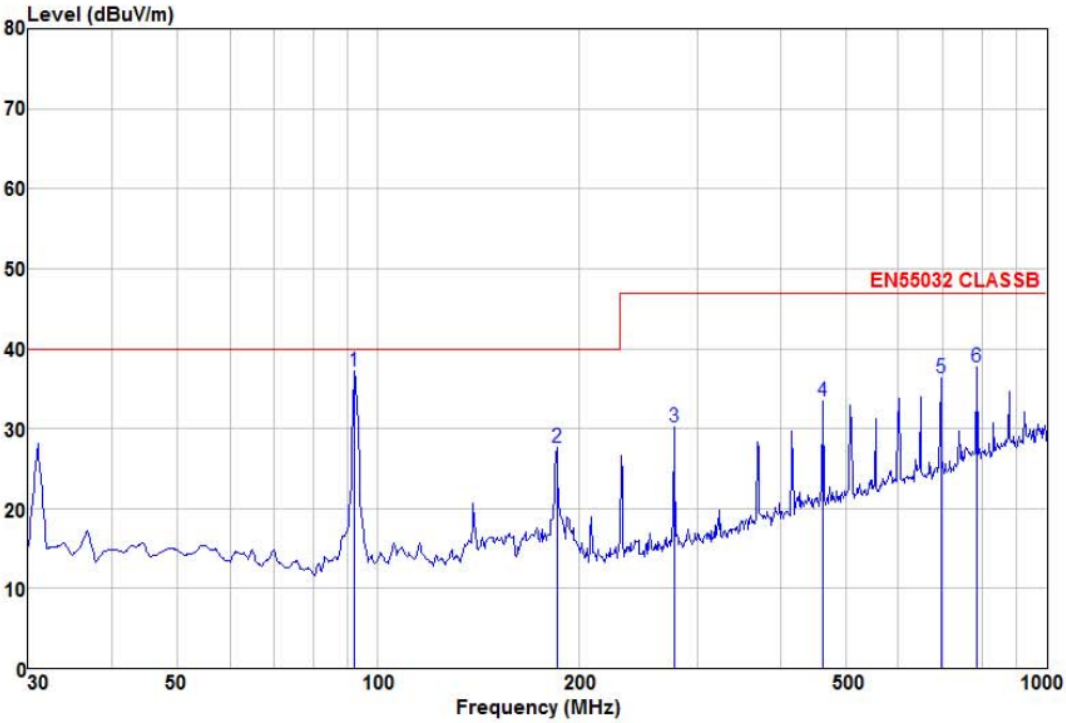


**Figure 3-22. Vertical radiation test result**

**Test result:** 30MHz to 1GHz frequency range, Margin = 2.77dB

## 4. Revision History

| Revision Number | Revision Date | Description |
|---|---|---|
| Ver 1.0 | 2024/7/29 | Initial version |
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