EMI-Optimized Design for the CA-IS2092A Ultra-small, Isolated RS-485 Transceiver

Contents

1. Introduction

This document is designed to complement the CA-IS2092A data sheet to provide a low-EMI design solution for the isolated RS-485 communication. This application note discusses EMI suppression methods, provides a reference design and the test result according to EN55032(CISPR32) Class-B standard for the CA-IS2092A based on a 2-layer board design. Also refer AN001.pdf (chipanalog.com) for more details about EMI optimized design.

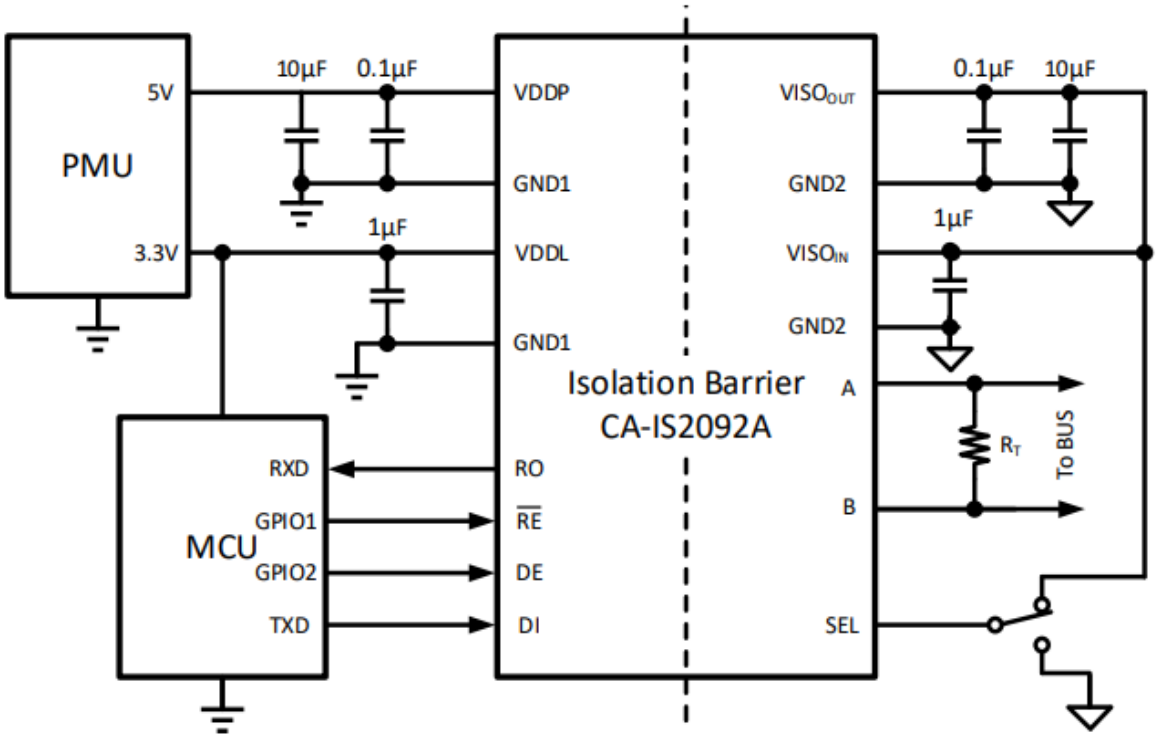

Figure 1-1. Typical application circuit

2. EMI-Optimized Design

2.1. CA-IS2092A General Description

Figure 2-1 shows the CA-IS2092A pin configuration.

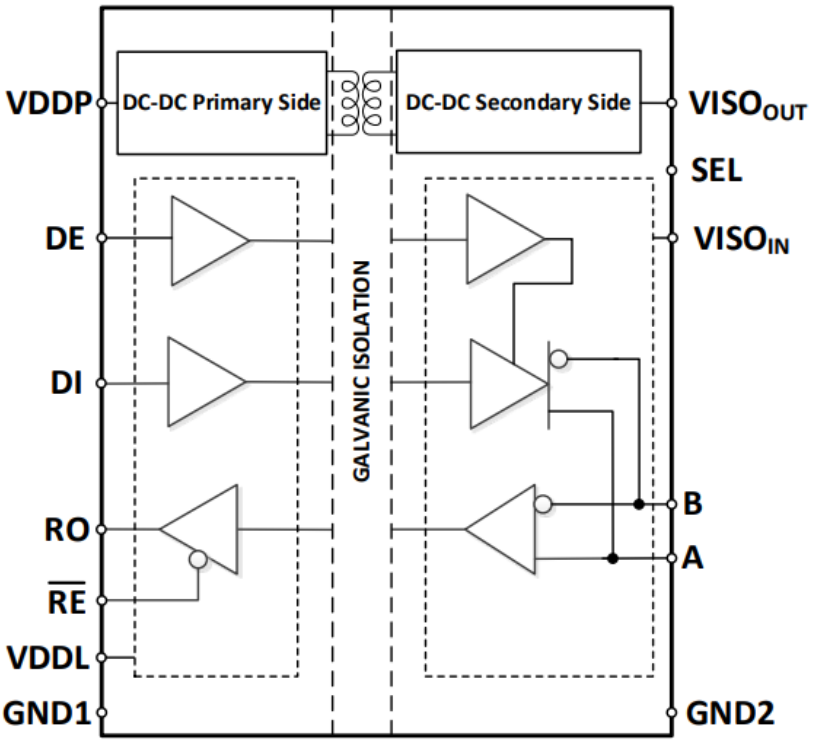

Figure 2-1. CA-IS2092A pin configuration

The CA-IS2092A is an ultra-small (LGA16 package), galvanically isolated RS-485 transceiver with an integrated isolated DC/DC converter and transformer, eliminating the need for a separate isolated power supply in space-constrained designs. The high di/dt and dv/dt caused by the high-frequency switching operation of the on-chip transformer are the main sources of are the main radiated resource. Designers must also consider the common mode noise generated by parasitic components on the primary and secondary sides. The following sections describe in detail how to minimize EMI and reflections.

The CA-IS2092A has an individual logic supply input VDDL, allowing fully compatible 2.5V to 5.5V logic on the logic input/output lines. Pin VDDL can be connected to an individual power supply or to pin VDDP for a single supply design. In the single supply design, the internal DC-DC converter generates a 3.3V or 5V supply for the cable side.

2.2. Optimized Design and Layout

2.2.1. Decoupling Capacitor Placement

Careful PCB layout is essential to achieve clean and stable communications operation. To ensure reliable device operation at all data rates and supply voltages, we recommend the addition of a minimum 10nF high frequency bypass capacitor and a bulk energy storage capacitor in parallel between VDDP and GND1, VISOOUT and GND2. When selecting a 10nF to 100nF low ESL/low ESR MLCC capacitor as the RF decoupling capacitor, this capacitor must also be placed closer to the VDDP and VISOOUT pins, the maximum distance being within 2mm, to reduce parasitic inductance and current loop. This is very important for optimised EMI performance, see Figure 2-2 recommended decoupling capacitor placement for PCB layout.

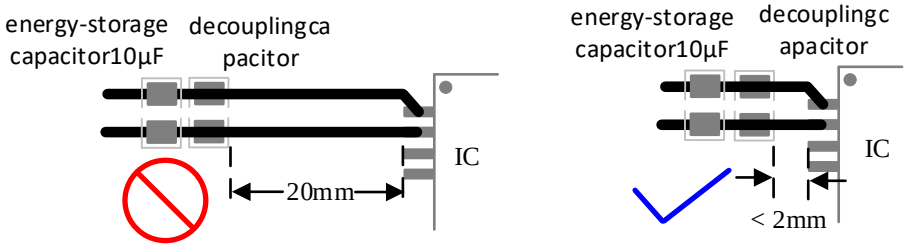

Figure 2-2. Decoupling capacitor placement

2.2.2. Y-capacitor Placement Between Primary and Secondary Side

During high frequency operation, the common mode current creates a current loop between the parasitic capacitance of the primary and secondary coils and the parasitic capacitance of the PCB. The larger the loop area, the greater the radiation generated. It is recommended that a Y capacitor is placed across the isolation barrier, between the primary reference ground (GND1) and the secondary reference ground (GND2). The Y-capacitor creates a very short path for the parasitic current to return to the primary side to reduce the loop area and to reduce the high frequency radiation from the board, see Figure 2-3.

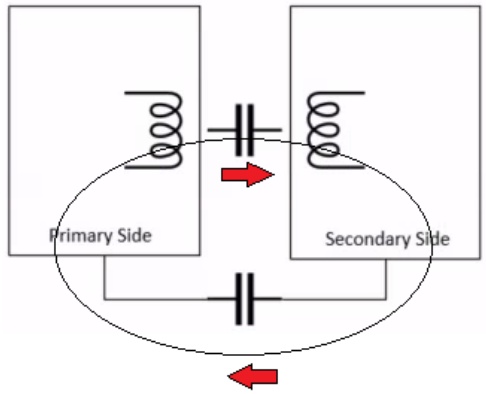

Figure 2-3. Y-capacitor across the isolation barrier

2.2.3. Ferrite Bead/Common-mode Inductor/Differential-mode Inductor

On the primary side, a pair of ferrite beads with a high frequency impedance of 1KΩ @ 100MHz are inserted on the power and ground lines for VDDP and VDDL respectively, breaking the path of larger common mode current loops. This provides further high frequency attenuation and blocks switching noise. Place the bead close to the decoupling capacitors as shown in Figure 2-4. A common-mode and/or differential-mode inductor may also be an option, depending on the EMI test result. In the CA-IS2092A reference design, two differential-mode inductors are added between the input power supply and the primary-side supply inputs to reduce low-frequency noise. Ground planes under these magnetic components must be avoided to prevent parasitic capacitance from affecting high-frequency attenuation.

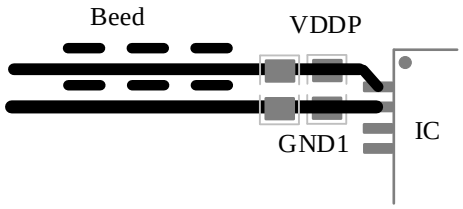

Figure 2-4. Ferrite beads placement

2.2.4. Building the edge guarding

A grounding via can be added around the board to form a via guard ring and return the noise to ground to reduce radiation and interference to the external system, as shown in Figure 2-5. If there are more than two rows of vias, the vias placed in the two rows should be staggered.

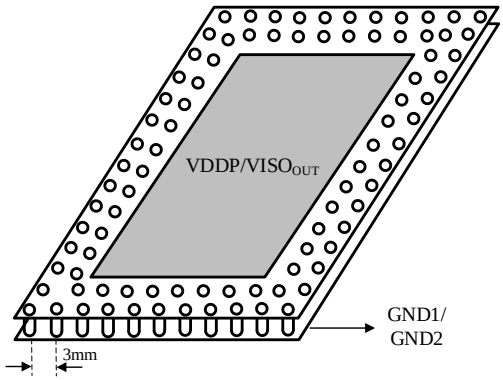

Figure 2-5. Vias guard ring around the edges of ground layers

3. CA-IS2092A Low-EMI Reference Design

3.1. PCB Design Guide

1) Place decoupling capacitors as close as possible to the device pins, maximum distance is less than 2mm, see Figure 3-1, C3/C4 and C6/C7. For the individual logic supply input VDDL and power supply input for cable-side $VISO_{IN}$, we recommend to place a 0.1μF ceramic capacitors (C5, C8 in Figure 3-1) between VDDL and GND1, $VISO_{IN}$ and GND2 respectively.
2) Place the beads BD1/BD2 and BD3/BD4 close to C3/C4 and C5. Install the differential-mode inductors at L1/ L2 tag;
3) On PCB bottom layer, place Y-capacitors between GND1 and GND2;
4) There are 2 pcs of CA-IS2092A installed on the reference board. On the left of L1/L2, the LM1086ISX-ADJ 12V to 5V LDO is selected to provide a clean +5V supply for both CA-IS2092A RS-485 transceivers on the board.
5) 3-pin header J1 is reserved for signal inputs. Jumper J2 is used for the isolated output voltage setup: 3.3V or 5V; Rab is the terminating resistor.

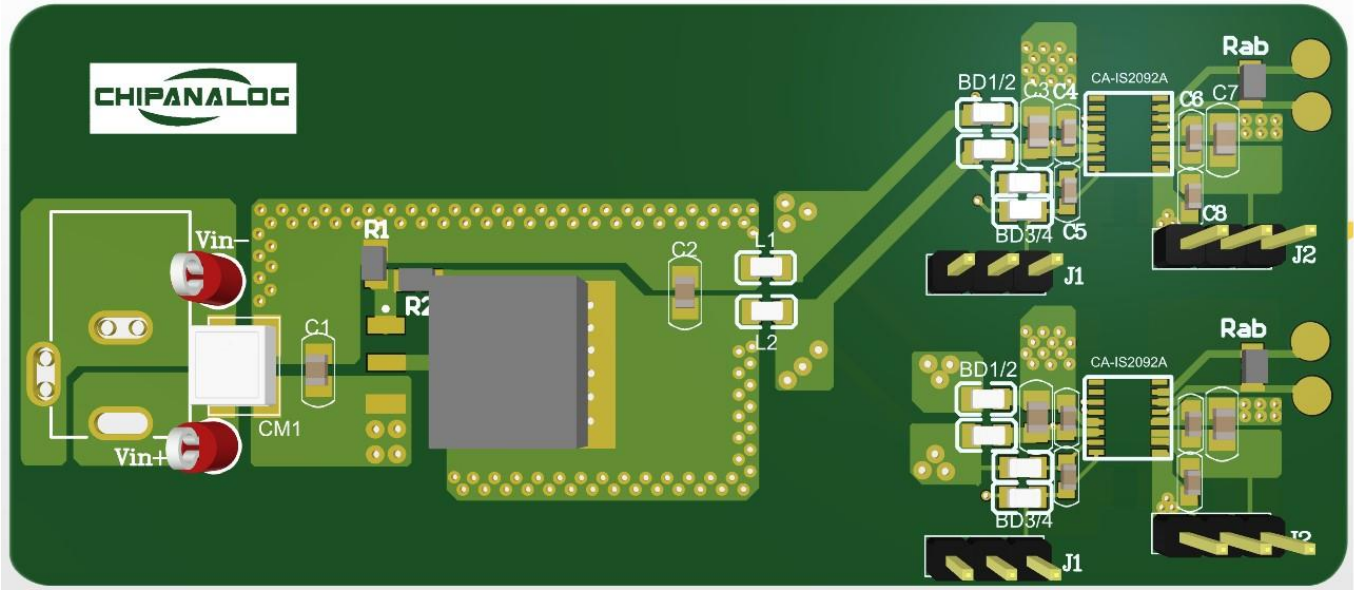

Figure 3-1. CA-IS2092A reference design board

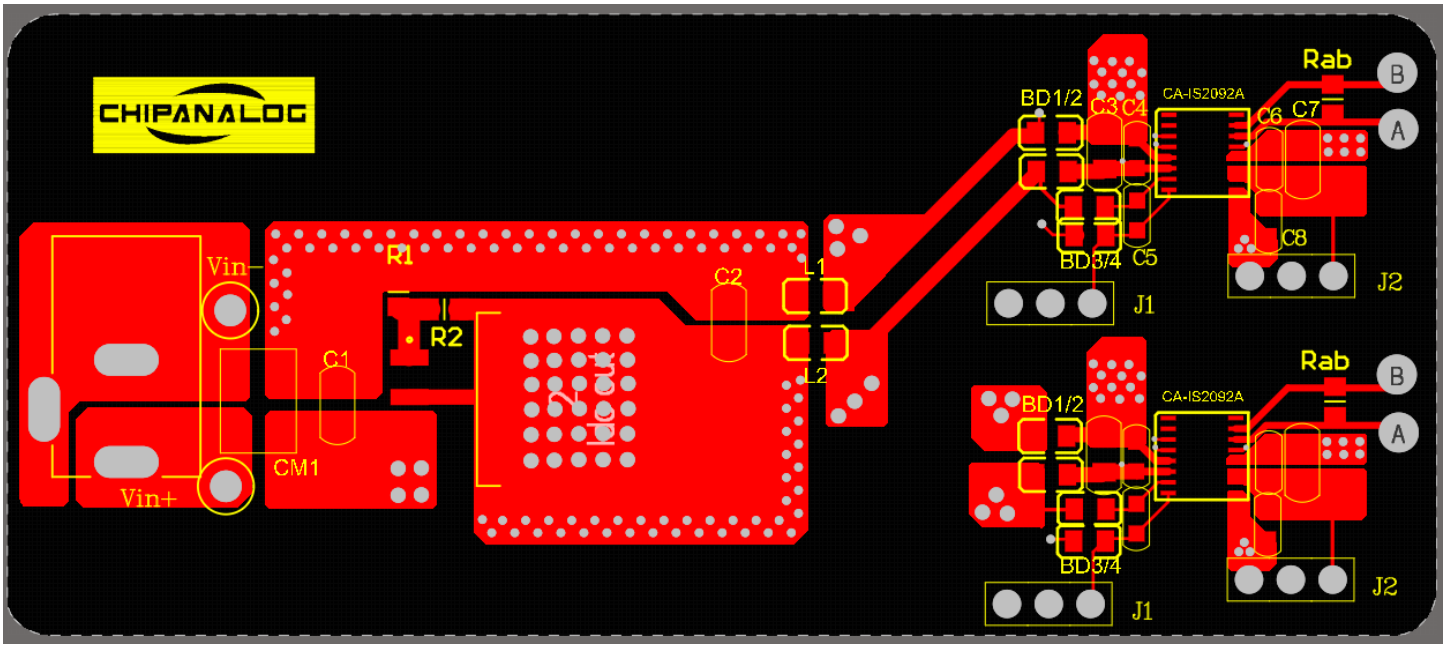

Figure 3-2. Reference design PCB top layer

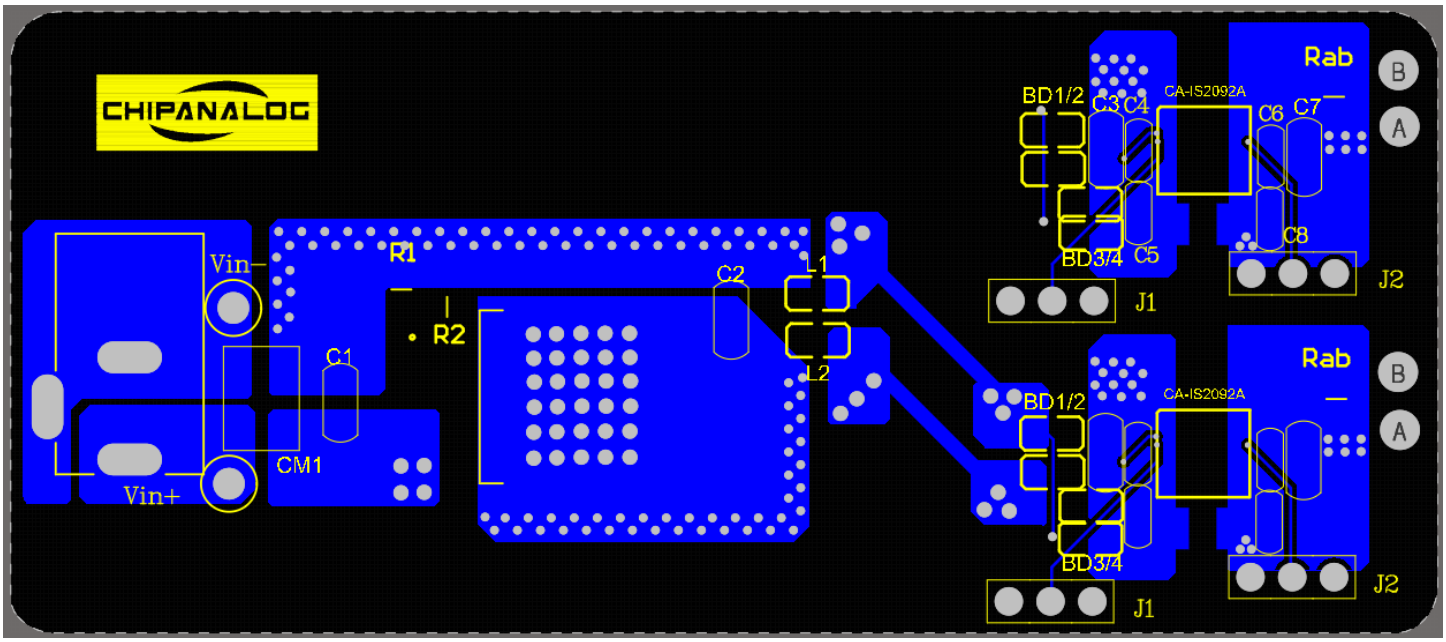

Figure 3-3. Reference design PCB bottom layer

3.2. CA-IS2092A Reference Design Schematic

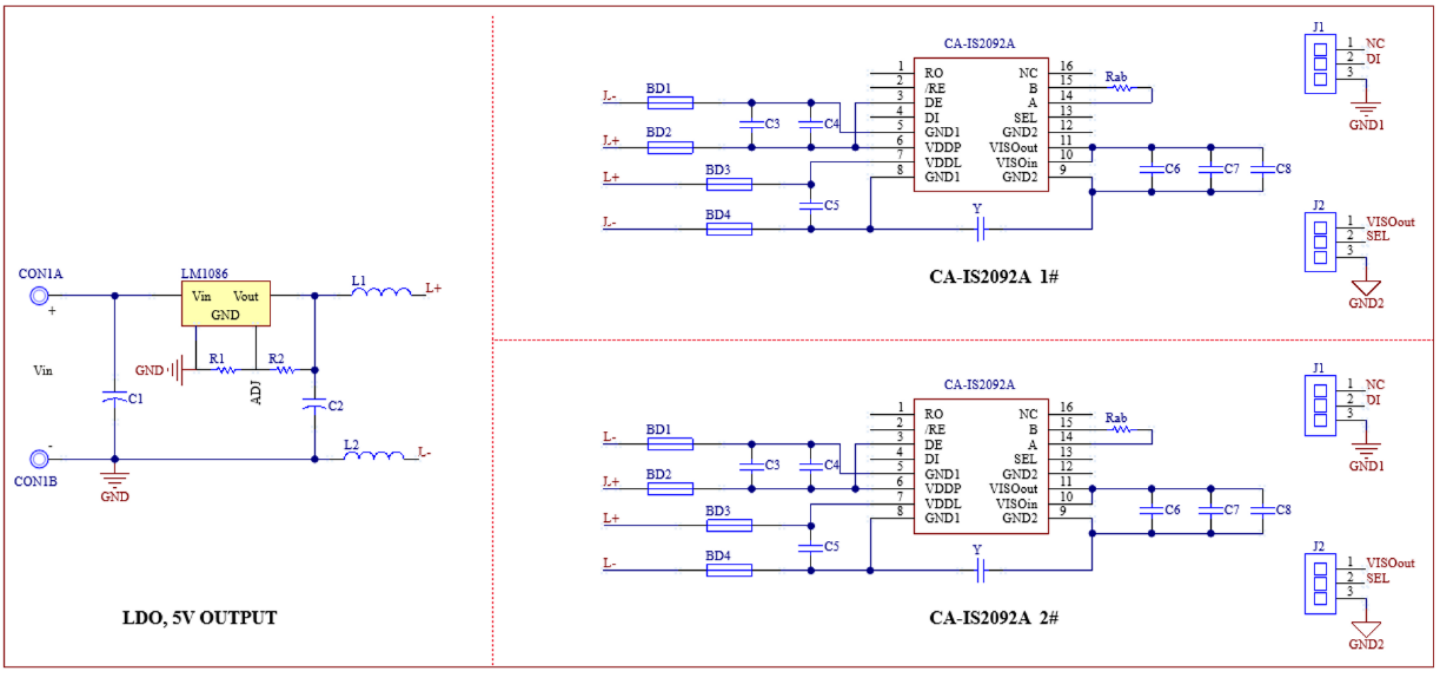

Figure 3-4. CA-IS2092A test board schematic

Table 3-1. Component List

Device name	Designation	Spec	Part number	Note
Ferrite bead	BD1~4	1kΩ at 100MHz	BLM18HE102SN1	
Y capacitor	Y	39pF	GRM31A7U3D390JW31	
Differential-mode inductors	L1, L2	2.2μH	MLZ2012M2R2HT000	
Termination resistor	Rab	54Ω	N/A	
Decoupling capacitors	C4, C6	10nF	N/A	
	C3, C7	10μF	N/A	
	C5, C8	1μF	N/A	

Table 3-2. Reference design summary

Board	Design margin	Frequency	PCB-layers	Overlap capacitors	Y-capacitor	Common-mode inductor	Differential-mode inductor
Reference design	3.4dB	593MHz	2	N/A	39pF	N/A	2.2μH(2pcs)

3.3. Reference Design Test Result

The test result is shown in Figure 3-5 and Figure 3-6, this solution meets the EN55032(CISPR32) Class B emission standard and also leaves a design margin of 4.7dB (horizontal)/3.4dB(vertical).

Table 3-3. Reference design test result summary

Input voltage	Differential output voltage	Load current	Design margin	
			vertical	horizontal
5V	3.6V	67mA	3.4dB	4.7dB

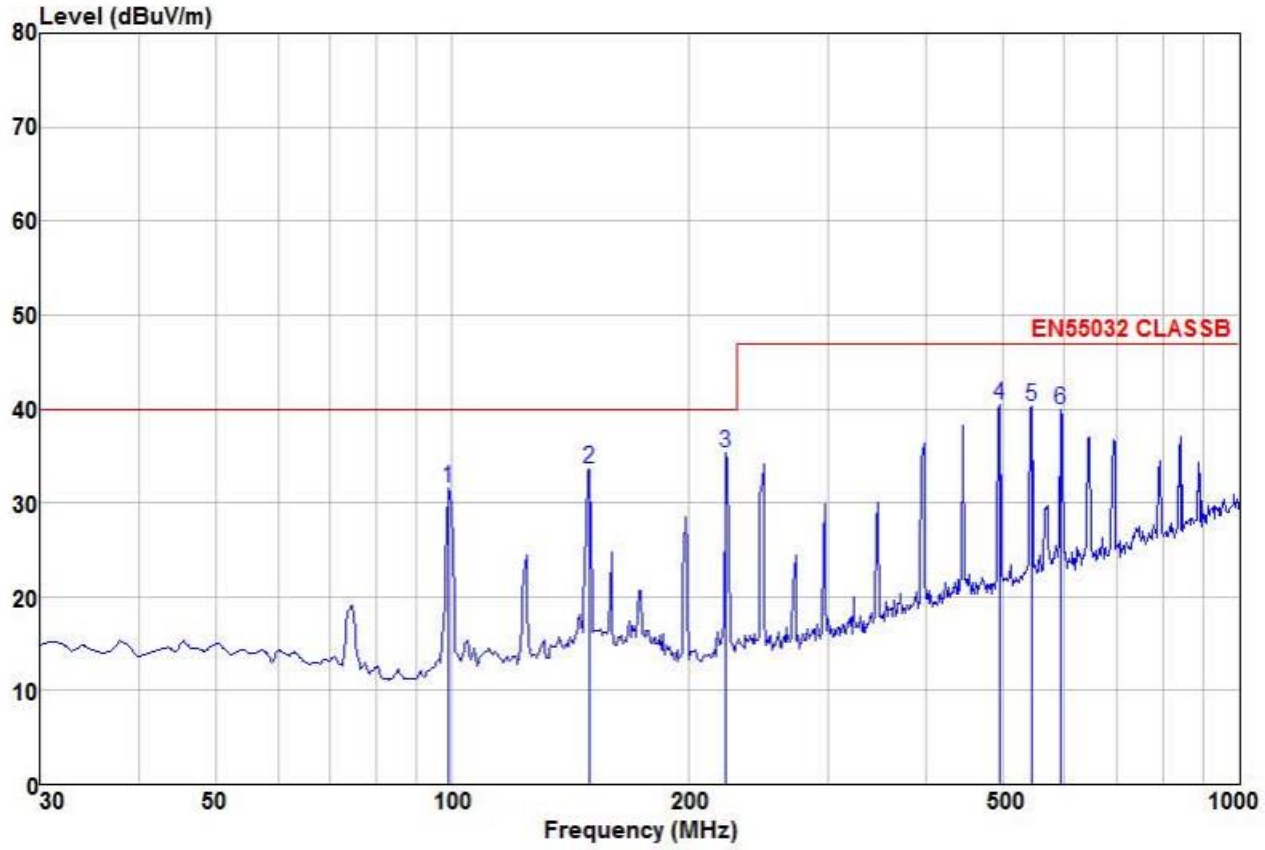

Figure 3-5. Horizontal radiation test result

Test conditions:

1) RS-485 bus load: 3.6V differential output voltage @ 67mA load current;
2) $VISO_{OUT}$: without additional load.

Test result:

30MHz-1GHz, Margin = 4.7dB.

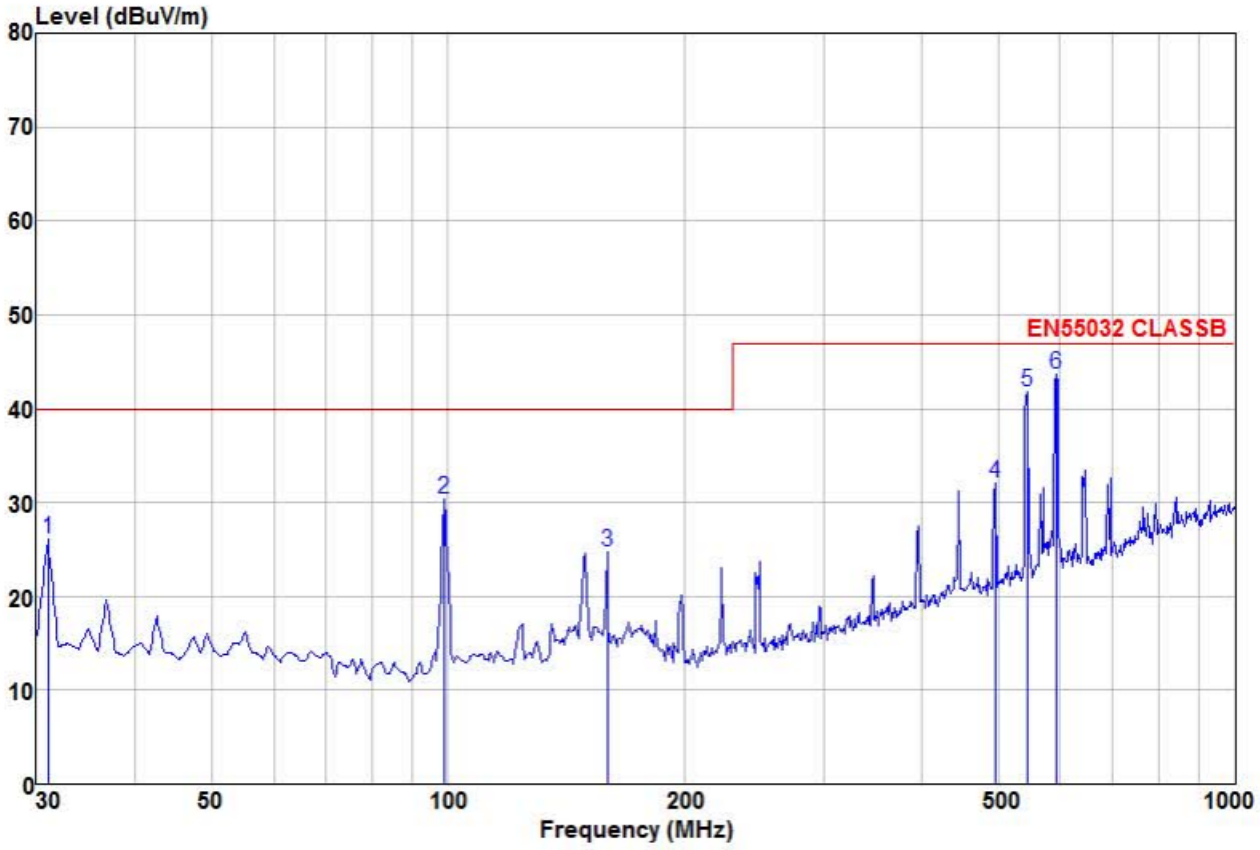

Figure 3-6. Vertical radiation test result, 30MHz-1GHz, Margin = 3.4dB

Test conditions:

3) RS-485 bus load: 3.6V differential output voltage @ 67mA load current;

4) $VISO_{OUT}$: without additional load.

Test result:

30MHz-1GHz, Margin = 3.4dB

4. Revision History

Revision Number	Revision Date	Description
Ver 1.0	2024/7/29	Initial version

5. Important Statement

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