EMI-Optimized Design for CA-IS3417WT/CA-IS3417WT-Q1 1700V High-Voltage Isolated Switches

Contents

1. Introduction

This document is designed to complement the CA-IS3417x application to provide a low-EMI design solution for multi-channel isolated switches. This application note discusses EMI suppression methods, provides a reference design and the test result according to EN55032(CISPR32) Class-B standard for the CA-IS3417WT and EN55025(CISPR25) Class-5 standard for CA-IS3417WT-Q1 based on a 2-layer board design.

The CA-IS3417x typical application circuit is shown in Figure 1-1.

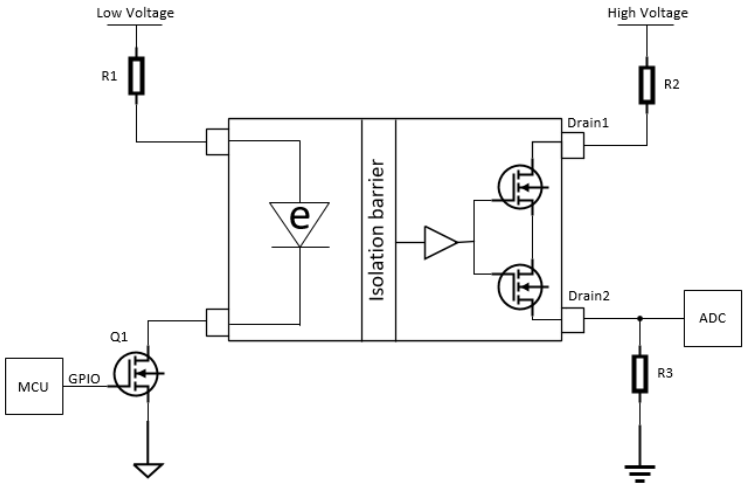

Figure 1-1. Typical application circuit

2. EMI-Optimized Design

2.1. CA-IS3417x General Description

The CA-IS3417WT and CA-IS3417WT-Q1 are opto-compatible isolated switches. These devices' input stage (primary side) is an emulated diode (e-diode) and the output stage (secondary side) are two SiC MOSFETs with back-to-back structure. The CA-IS3417x integrates galvanic isolation between the primary side and secondary side that features isolation for a withstand voltage rating of up to $5kV_{RMS}$ for 60 seconds. This isolated high-voltage switch can be used as replacement for the industry standard optocoupler-based devices while providing low propagation delay and long term reliability. The CA-IS3417WT and the CA-IS3417WT-Q1 have the same pin-configurations but different target markets, the CA-IS3417WT is designed for industrial application and the CA-IS3417WT-Q1 is automotive grade solution.

The simplified functional block diagram and pin configuration of CA-IS3417x is shown in Figure -21.

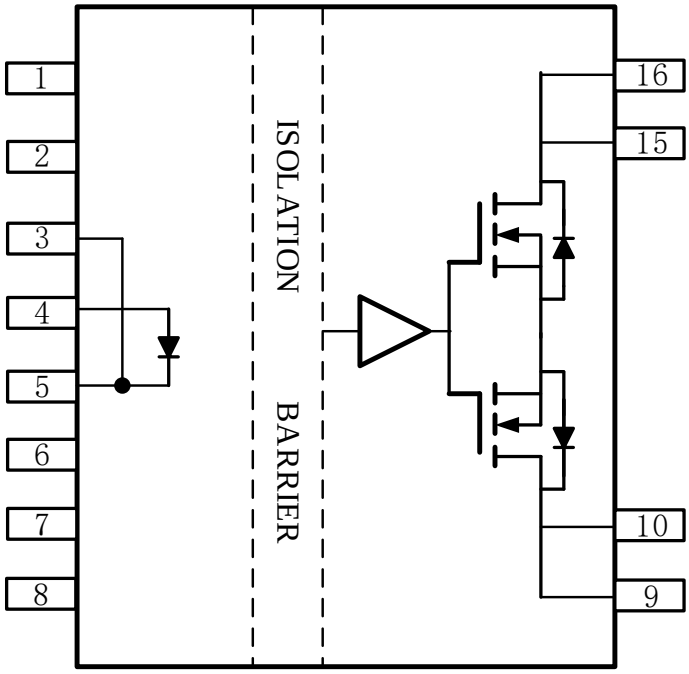

Figure 2-1. Functional block diagram and pin configuration of CA-IS3417x

Table 2-1. CA-IS3417x pin description

Pin Name	Pin Number	Type	Description
NC	1, 2, 6, 7, 8	---	No internal connection.
ANODE	4	Input	Switch input, the anode of input diode.
CATHODE	3, 5	Input	Switch input, the cathode of input diode.
Drain2	9, 10	Output	Switch output, MOSFET second drain.
Drain1	15, 16	Output	Switch output, MOSFET first drain.

During the CA-IS3417x operation, the primary side simulates the optocoupler characteristic, when there is 10mA current flow, through the primary and secondary side integrated on-chip transformer and the back-end rectifier, charge pump circuit boosting output of an isolated DC voltage to drive the internal integrated SiC MOSFETs. high frequency switching of the on-chip transformer caused by a high di/dt, dv/dt is the main source of radiation, in addition to the primary and secondary side of the parasitic parameter resulting in a common mode noise. common mode noise due to parasitic parameters on the primary and secondary sides. In order to meet the EMI limits of automotive and industrial standards, external measures for EMI suppression need to be considered.

2.2. Optimized Design and Layout

2.2.1. Decoupling Capacitor Placement

To ensure device reliable operation, we recommend to add a minimum 10nF high-frequency bypass capacitor between the anode and cathode on the primary-side. Selecting a 10nF to 100nF low-ESL/low-ESR MLCC capacitor as the high frequency decoupling capacitor, also this capacitor must be placed closer to the device, the maximum distance is within 2mm, to reduce parasitic inductance and current loop. It is not necessary to place any energy-storage capacitors because the input-stage is just an analog-diode. See Figure 2-2 recommended decoupling capacitors placement for the PCB layout.

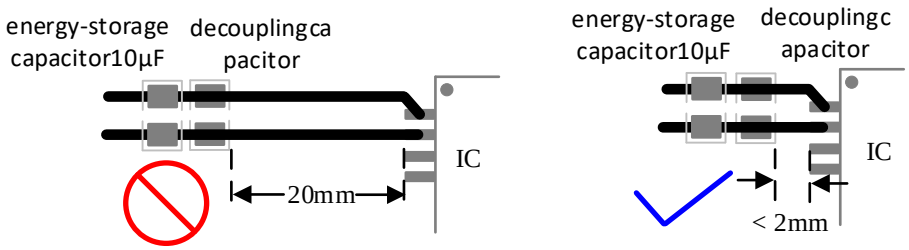

Figure 2-2. Decoupling capacitor placement

2.2.2. Y-capacitor

During high-frequency operation, the common-mode current generates a current loop between the parasitic capacitance of the primary and secondary coils, as well as the PCB parasitic capacitance. The larger the loop area, the stronger the radiation generated. It is recommended to place a Y capacitor across the isolation barrier, between the primary-side ground and secondary-side ground as shown in Figure 2-3 (left). The Y-capacitor create a very short path with a small loop area for the parasitic current return to primary side, reducing the EMI generated on the board. For the multi-layer PC board design, stitching capacitance is generally placed in the middle two layers (right of Figure 2-3). The stitch capacitance is proportional to the overlapping area of two PCB layers, and inversely proportional to the relative distance between the two layers. The larger capacitance value can better suppress EMI.

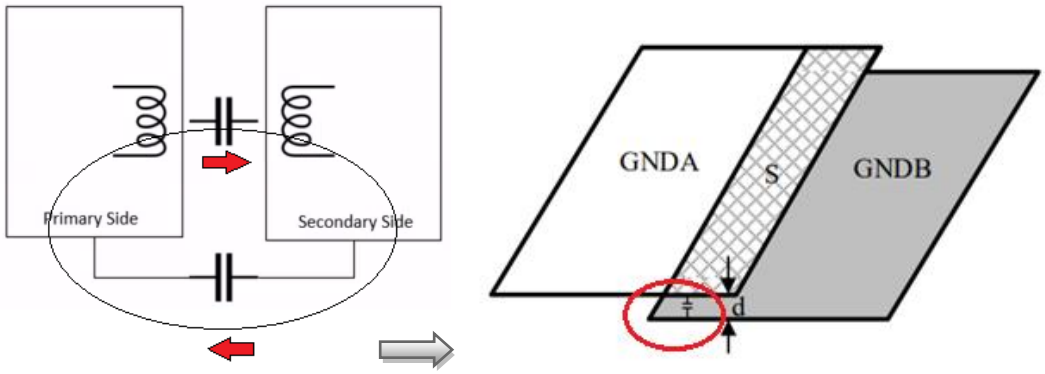

Figure 2-3. Y-capacitor

2.2.3. Ferrite Bead

On the primary-side, a pair of ferrite beads with a high frequency impedance in the range of 600Ω to 1KΩ @ 100MHz can be placed in series with the anode and cathode respectively, thereby breaking the path of larger common-mode current loops. This offers further high-frequency attenuation and blocks the switching noise. Place the beads close to decoupling capacitor as shown in Figure 2-4. Ground planes must be avoided under these magnetic components to avoid the parasitic capacitance affecting high-frequency attenuation.

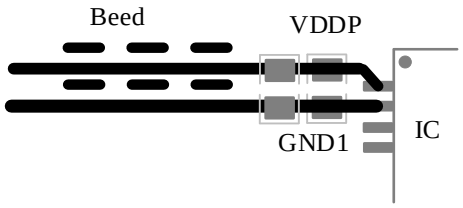

Figure 2-4. Ferrite beads placement

2.2.4. Building the edge guarding

A grounding vias can be added around the PCB to form a via guard ring and return the noise to the ground to reduce the radiation and interfere to the external system, as shown in Figure 2-5. If there are more than two rows of vias, the vias placed in the two rows shall be staggered from each other.

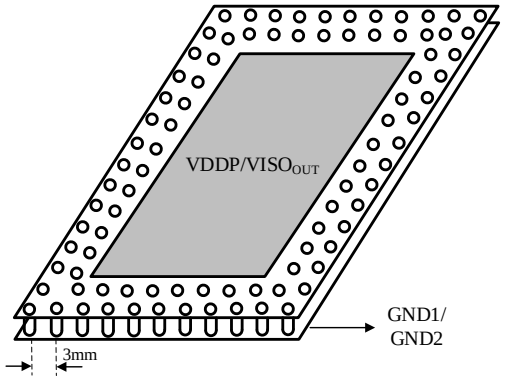

Figure 2-5. Vias guard ring around the edges of ground layers

3. CA-IS3417x Low-EMI Reference Design

3.1. CA-IS3417WT Reference Design (CISPR32 Class B)

3.1.1. CA-IS3417WT EMI Reference Result Summary

Table 3-1.CA-IS3417WT reference design summary

Board	Design margin	Frequency	PCB-layers	Overlap capacitors	Y-capacitor	Common-mode inductor	Differential-mode inductor
Reference design	>17 dB	1GHz	2	N/A	N/A	N/A	N/A

3.1.2. CA-IS3417WT PCB Design

1) On the reference design board, +3.3V input provides supply for the 6 pcs of CA-IS3417WT on board. R1 current limit resistance is 150Ω.
2) Components not installed on board include: BD1 --- BD4, C1 and Y-capacitor, the board can meet the EMI test requirement without these parts. These can be reserved for future applications.
3) The secondary-side is open, R2 is not installed.

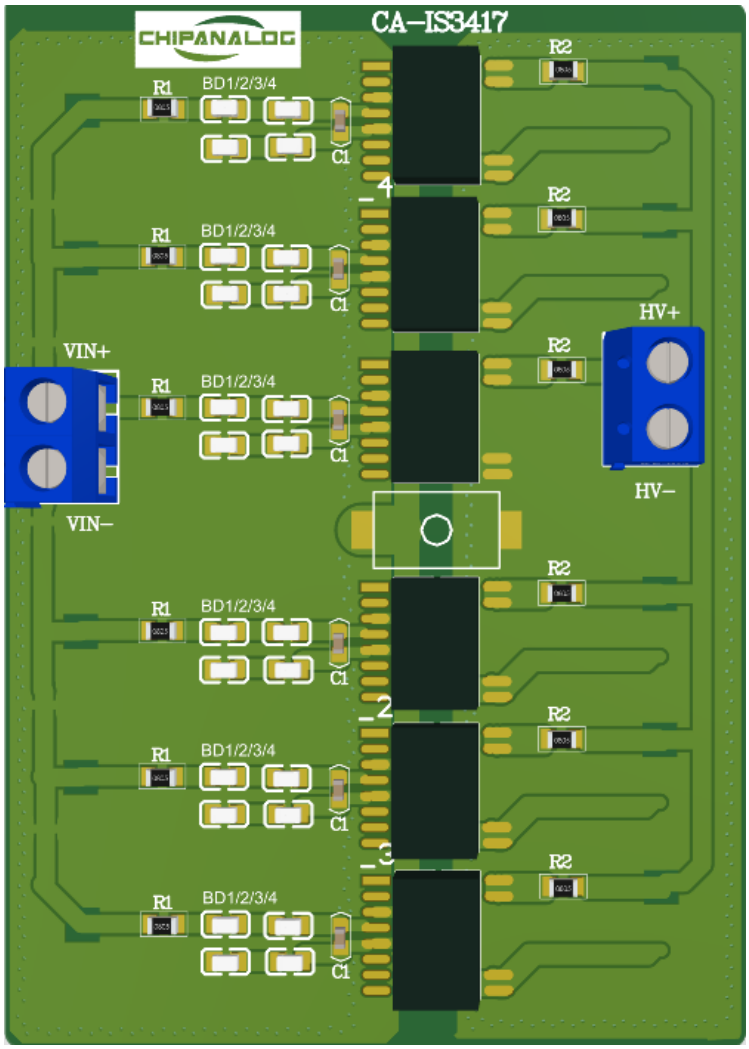

Figure 3-1. CA-IS3417WT reference design board(2-layer)

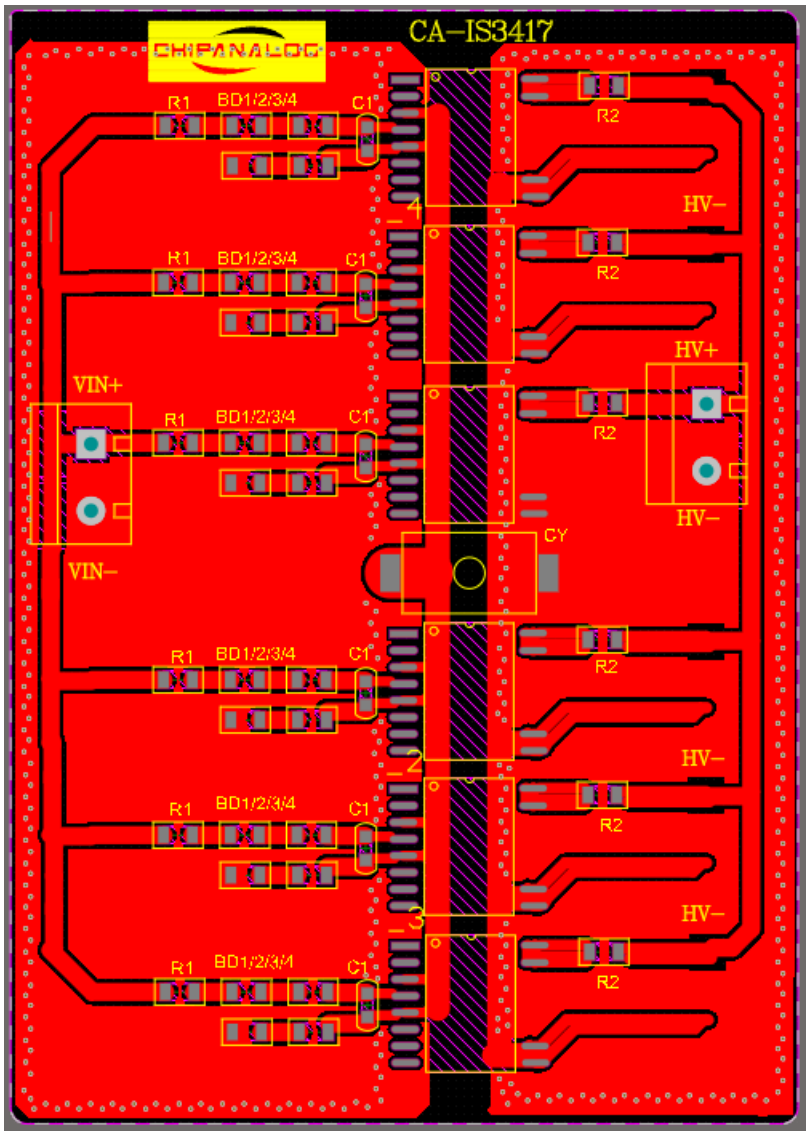

Figure 3-2. CA-IS3417WT Reference design PCB top layer

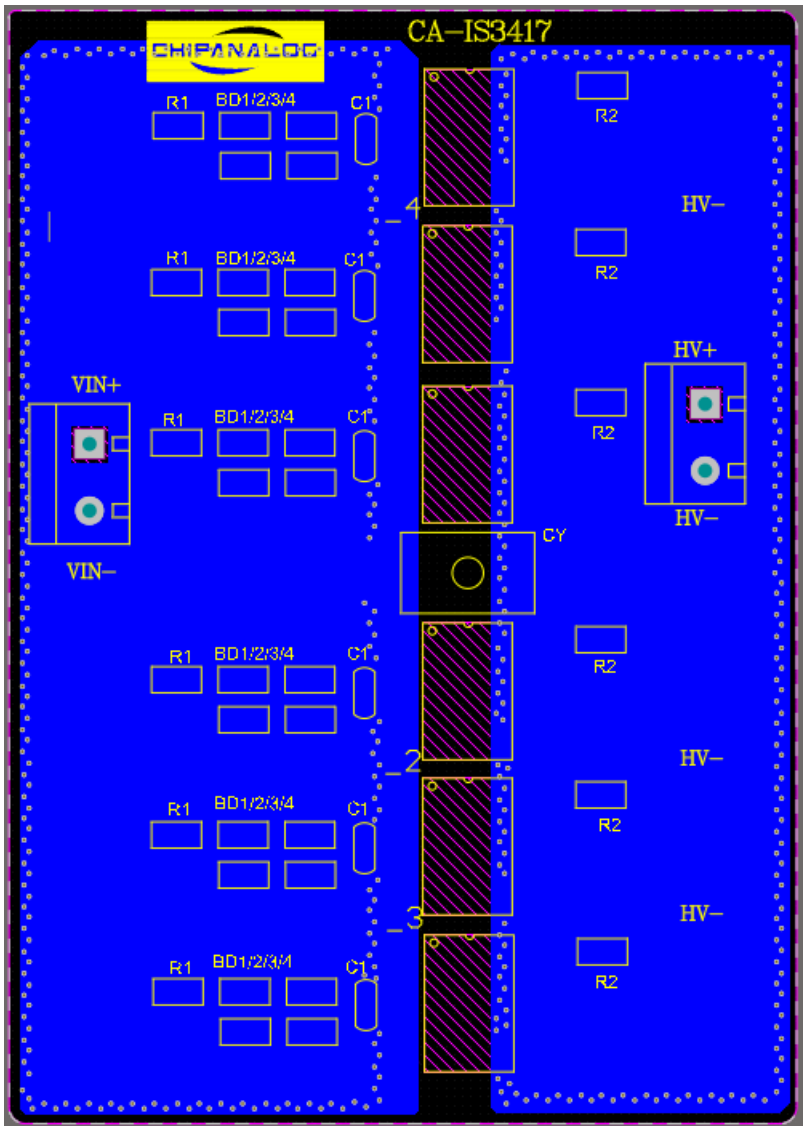

Figure 3-3. CA-IS3417WT Reference design PCB bottom layer

3.1.3. CA-IS3417WT Reference Design Schematic

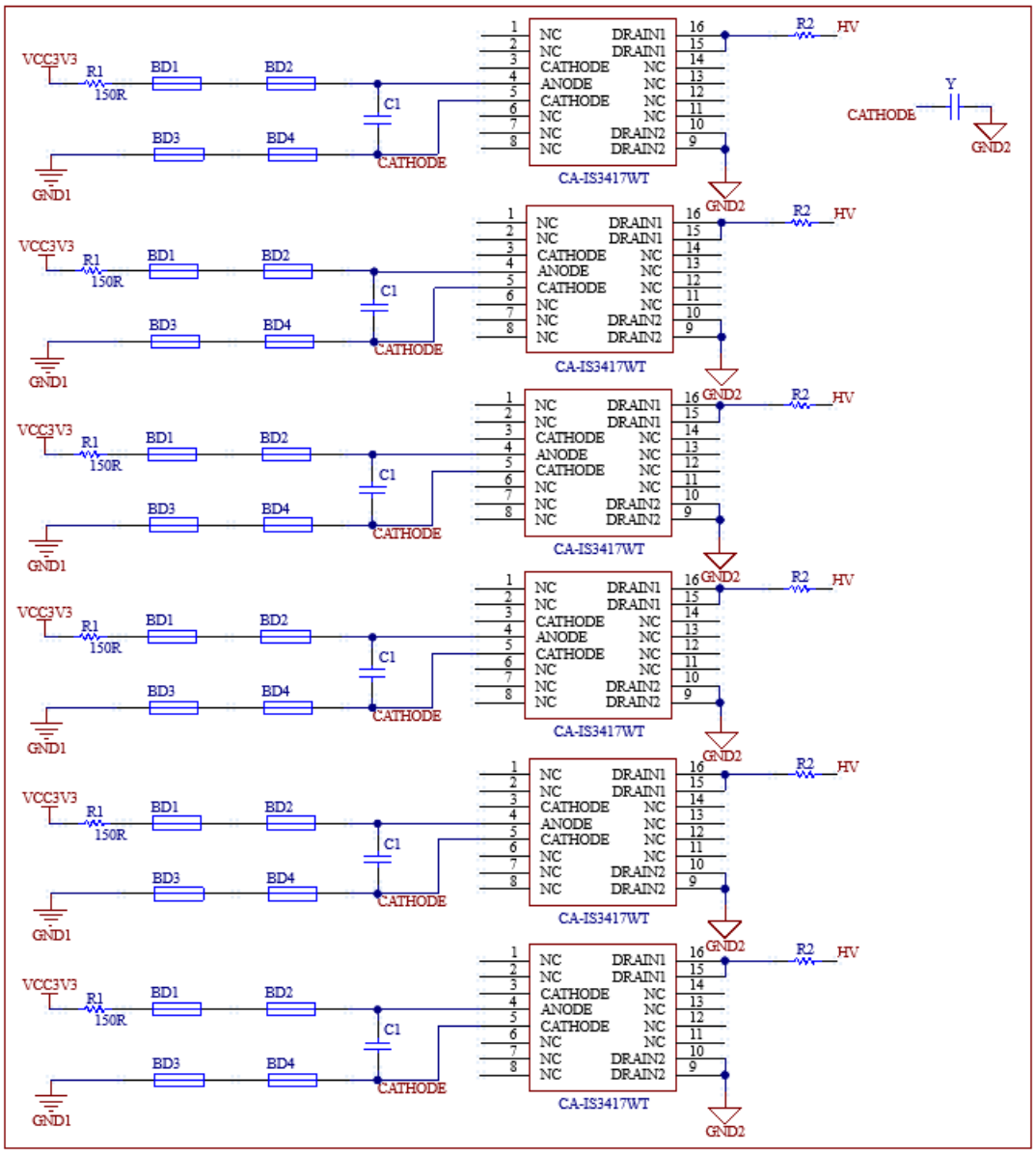

Figure 3-4. CA-IS3417WT test board schematic

Table 3-2. BOM List

Device name	Designation	Spec	Part number	Note
Decoupling capacitors	C1	10nF		not installed
Ferrite bead	BD1~4	1kΩ (@100MHz)		not installed
Y capacitor	Y	1nF		not installed

3.1.4. CA-IS3417WT Reference Design Test Result

The test result is shown in Figure 3-5 and Figure 3-6, there are 6 pcs of CA-IS3417WT on the 2-layer board operating simultaneously. This solution meets EN55032(CISPR32) radiated emissions Class B standard, and also leave 19.9dB (horizontal)/17.4dB(vertical) design margin.

Table 3-3. Reference design test result summary(CISPR32 Class B)

Load current	Design margin	
	vertical	horizontal
Primary-side emulated diode power consumption: 1.8V/10mA	17.4dB	19.9dB

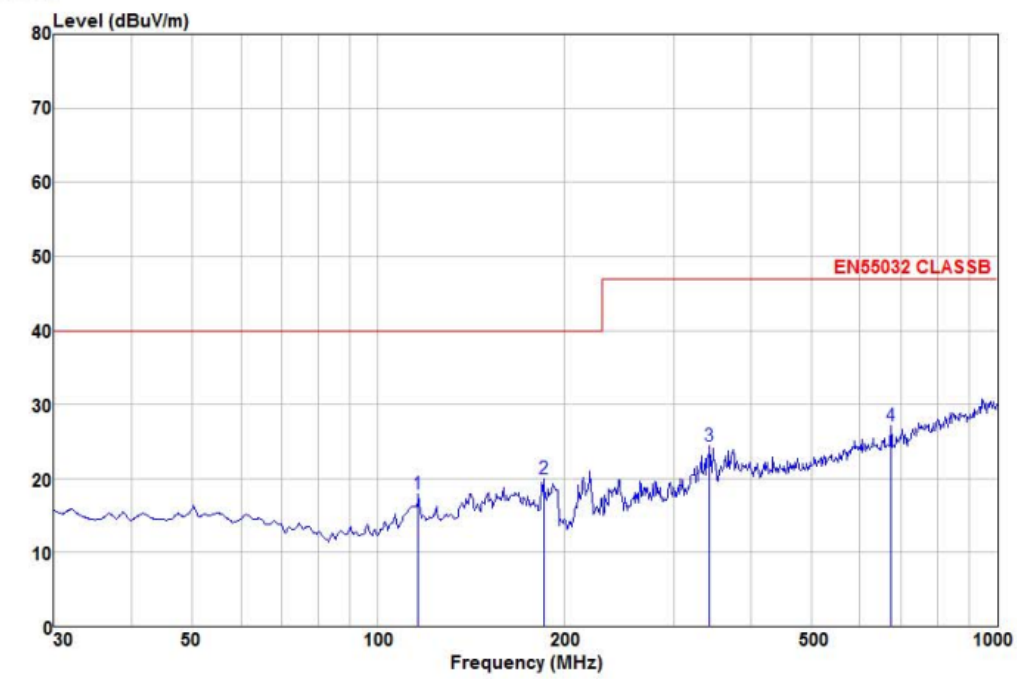

Figure 3-5. Horizontal radiation test result

Test result:

30MHz-1GHz, Margin = 19.9dB.

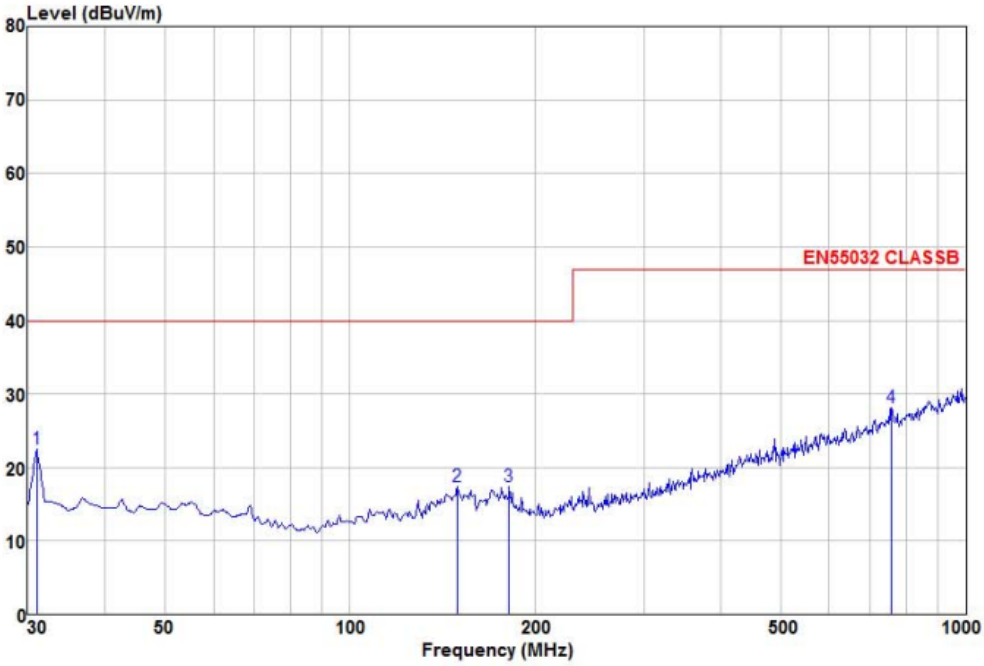

Figure 3-6. Vertical radiation test result

Test result:

30MHz-1GHz, Margin = 17.4dB

3.2. CA-IS3417WT-Q1 Reference Design (CISPR25 Class 5)

3.2.1. CA-IS3417WT-Q1 EMI Reference Result Summary

Table 3-4. CA-IS3417WT-Q1 Reference design summary

Board	Design margin	Frequency	PCB-layers	Overlap capacitors	Y-capacitor	Common-mode inductor	Differential-mode inductor
Reference design	2.09 dB	240MHz	2	N/A	N/A	N/A	N/A

3.2.2. CA-IS3417WT-Q1 PCB Design

1) On the reference design board, +3.3V input provides supply for the 3 pcs of CA-IS3417WT-Q1 on board. Also, there is a post LDO(U1) on board, can be used to provide clean +3.3V power supply. R1 current limit resistance is 150Ω.
2) Components not installed on board include: BD1/BD2, C1 and Y1/Y2-capacitors, because the board can meet the EMI test requirement. These can be reserved for future applications.
3) The secondary-side is open, R2 is not installed.

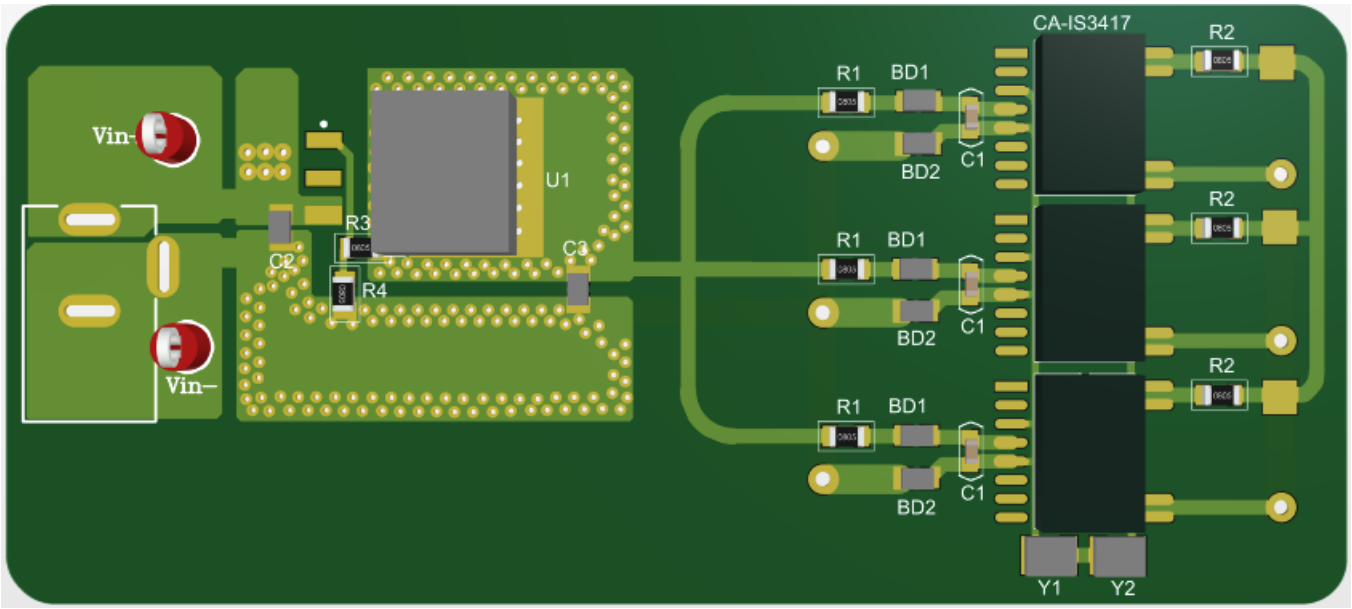

Figure 3-7. CA-IS3417WT-Q1 reference design board(2-layer)

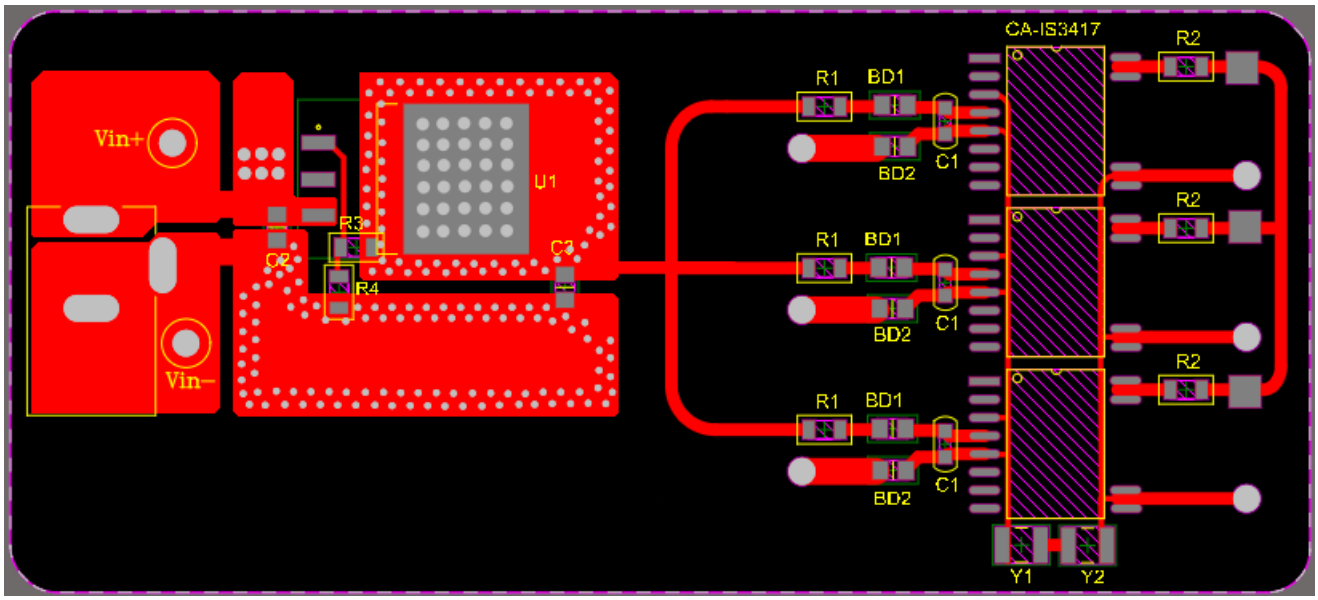

Figure 3-8. CA-IS3417WT-Q1 Reference design PCB top layer

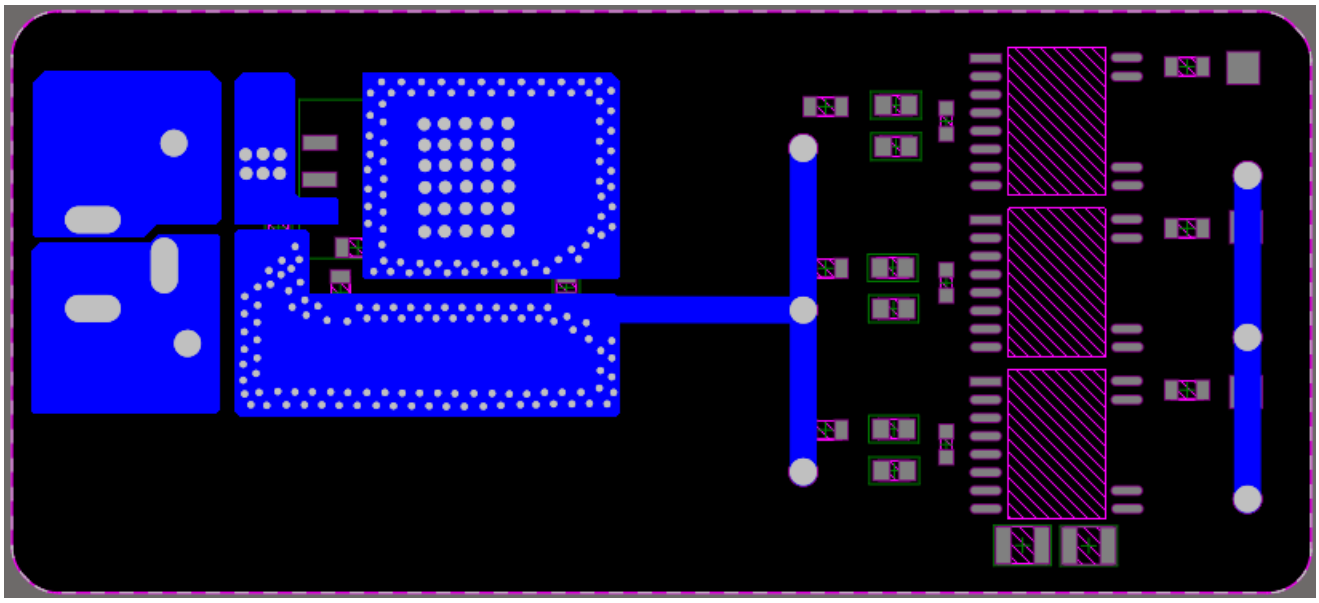

Figure 3-9. CA-IS3417WT-Q1 Reference design PCB bottom layer

3.2.3. CA-IS3417WT-Q1 Reference Design Schematic

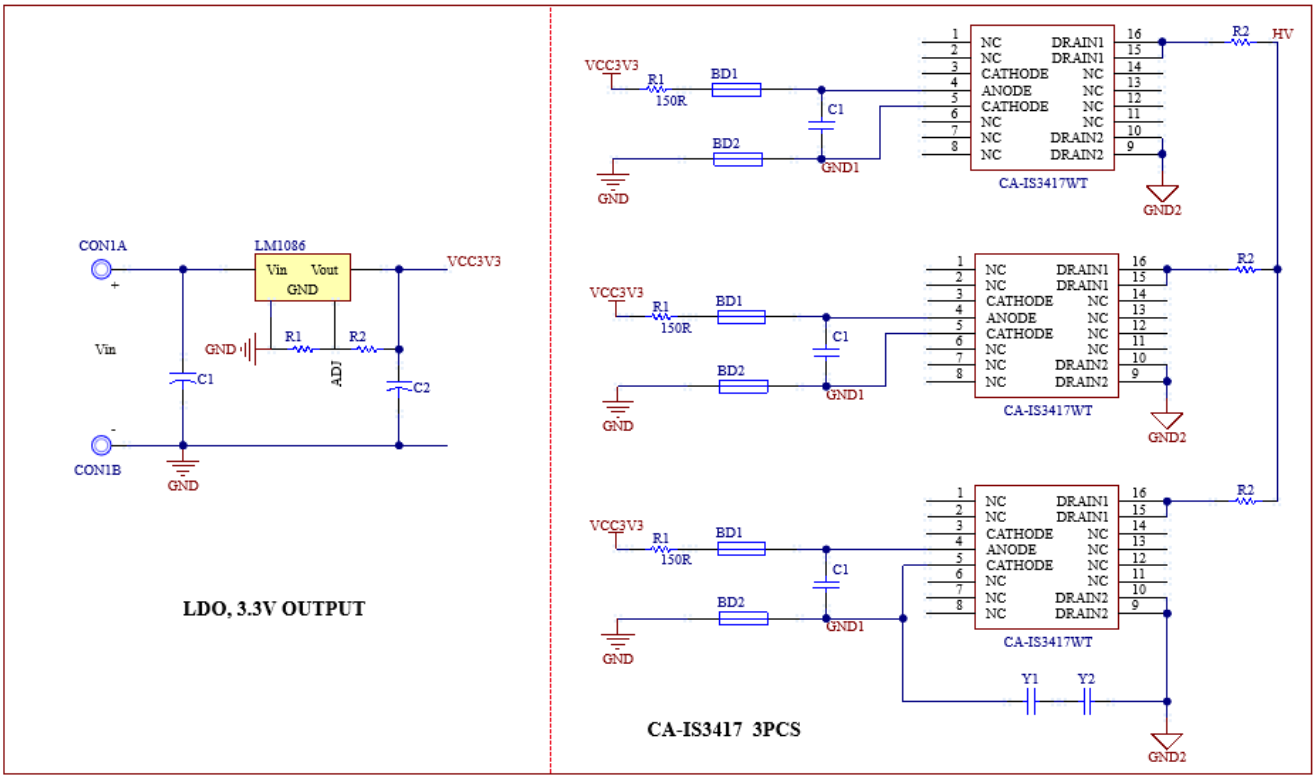

Figure 3-10. CA-IS3417WT-Q1 test board schematic (3 pcs on board)

Table 3-5.BOM List

Device name	Designation	Spec	Part number	Note
Decoupling capacitors	C1	10nF		not installed
Ferrite bead	BD1，BD2	1kΩ (@100MHz)		not installed
Y capacitor	Y1，Y2	1nF		not installed

3.2.4. CA-IS3417WT-Q1 Reference Design Test Result

The test result is shown in Figure 3-11 to Figure 3-14, there are 3 pcs of CA-IS3417WT-Q1 on the 2-layer board operating simultaneously. This solution meets EN55025(CISPR25) radiated emissions Class 5 standard without any external EMI filters, and leave design margin.

Table 3-6. Reference design test result summary(CISPR25 Class 5)

Load current	Design margin	
	vertical	horizontal
Primary-side emulated diode power consumption: 1.8V/10mA	2.09dB	2.71dB

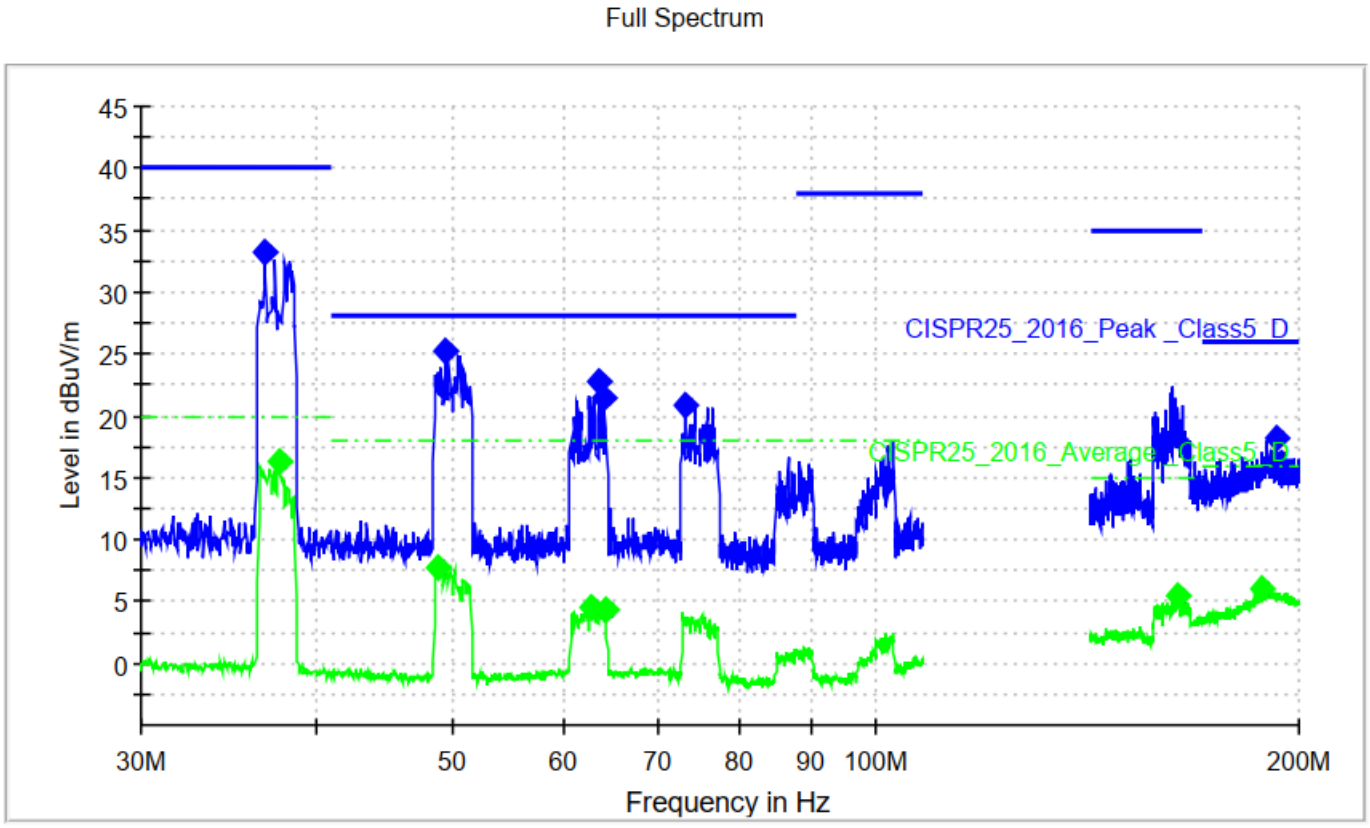

Figure 3-11. Horizontal radiation test result

Test result:

30MHz-200MHz, Margin = 2.71dB.

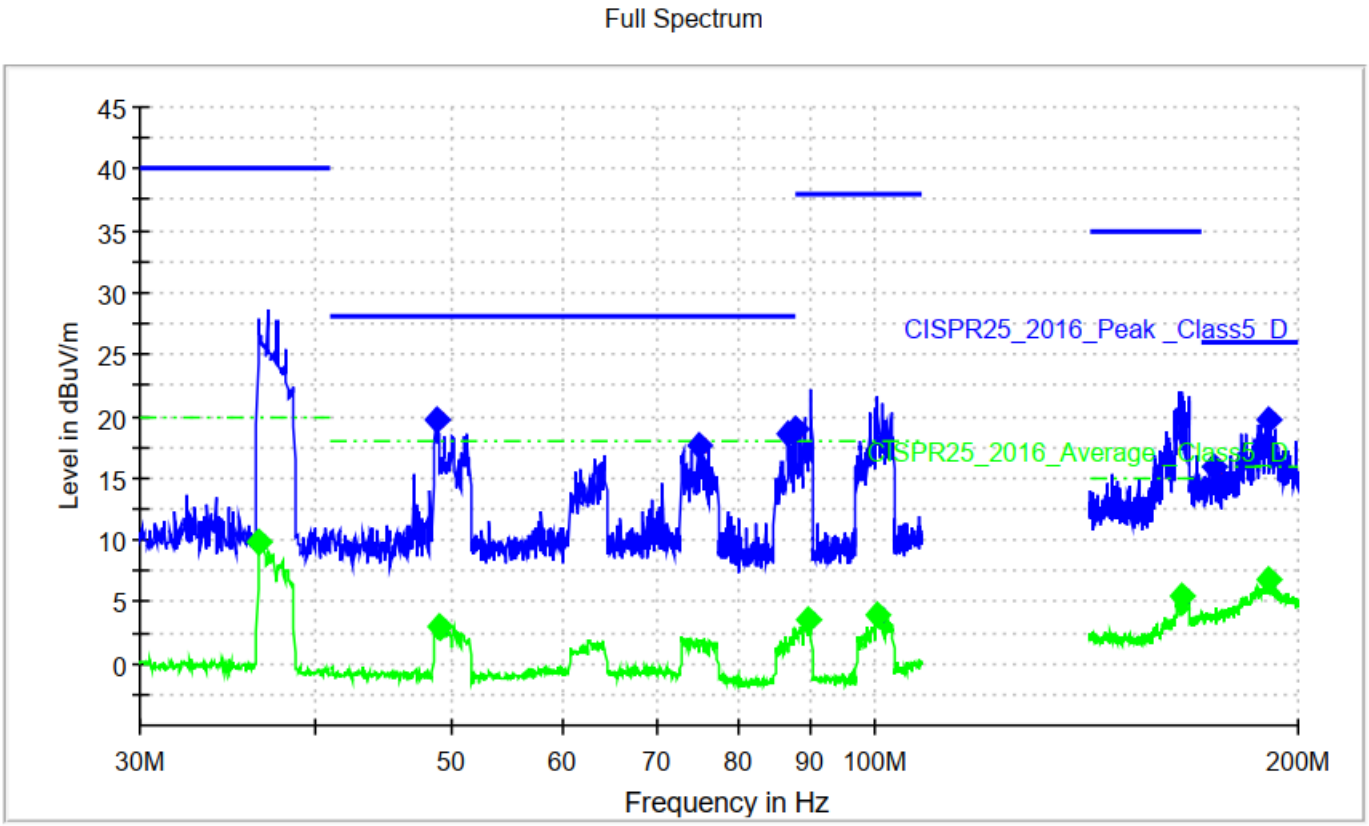

Figure 3-12. Vertical radiation test result

Test result:

30MHz-200MHz, Margin = 6.35dB

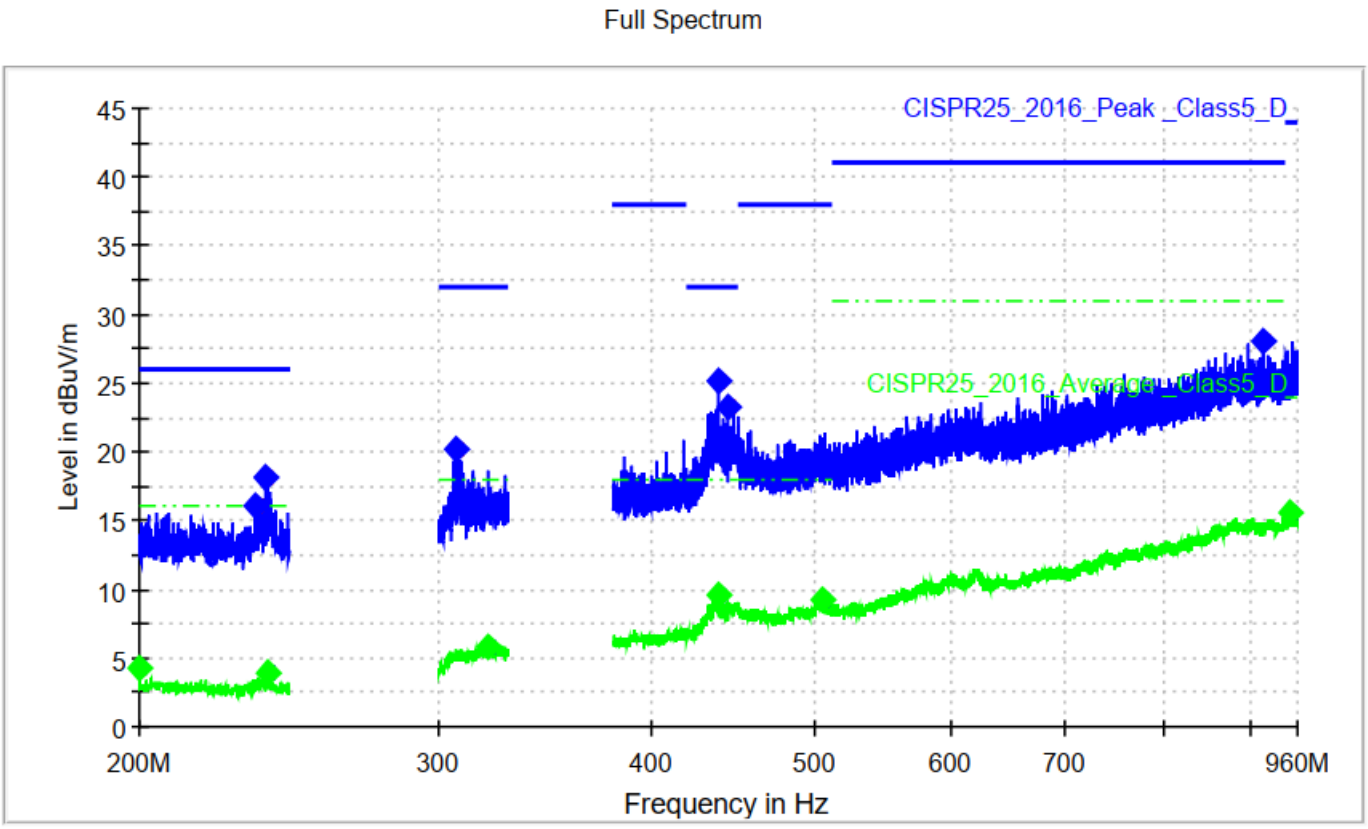

Figure 3-13. Horizontal radiation test result

Test result:

200MHz-960MHz, Margin = 6.89dB.

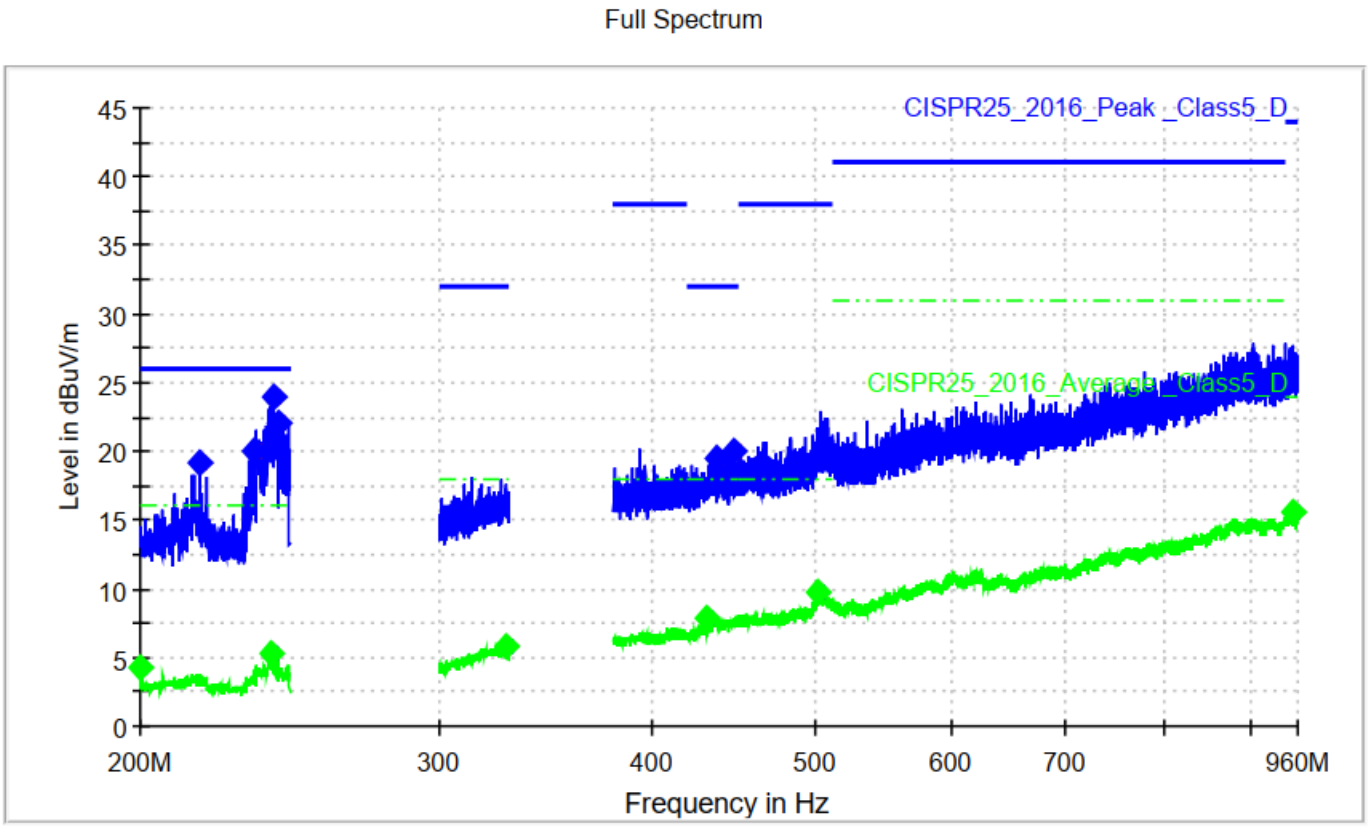

Figure 3-14. Vertical radiation test result

Test result:

200MHz-960MHz, Margin = 2.09dB

4. Revision History

Revision Number	Revision Date	Description
Rev 1.0	2023/12/25	Initial version
Rev 1.1	2024/7/30	Added EMI solution (Cispr25 Class 5)

5. Important Statement

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