CA-IF10285/3x-Q1 LIN Transceiver Evaluation Module

General Description

The CA-IF10285/3x-Q1 evaluation module (EVM) provides a proven reference design to evaluate the CA-IF10285-Q1 and CA-IF10283-Q1 LIN transceivers with internal voltage regulator. This documentation introduces the CA-IF10285/3x-Q1 evaluating and testing procedure step by step and details about PCB layout guidelines. The CA-IF10285/3x-Q1 EVM BOM, schematics and layout files are available.

CA-IF10285/3x-Q1 Introduction

The CA-IF10285/3x-Q1 device is Local Interconnect Network (LIN) transceiver optimized for automotive applications. LIN is low-speed universal asynchronous receiver transmitter (UART) communication protocol used to support in-vehicle networks. The CA-IF10285/3x-Q1 transceiver controls the LIN bus state via the TXD input and reports the bus state on its push-pull output RXD between the protocol controller and physical LIN networks. These device features slew-rate control and wave-shaping to reach a very low level of electromagnetic emission (EME) within a broad frequency range.

The CA-IF10285/3x-Q1 devices are designed to support 12V automotive applications with integrated ESD protection. It blocks current flowing into the power supply from LIN bus during powered off or the case of large ground offset. Also, it features low-power sleep mode, as well as wake-up capability over LIN bus or EN pin.

The CA-IF10285/3x-Q1 LIN transceiver integrates a low dropout regulator (LDO) to provide 5V or 3.3V output voltage with up to 100mA (SOIC8) or 125mA (DFN8) load current.

Note: this EVM is designed for CA-IF10285D-Q1 and CA-IF10283D-Q1 (DFN-8) evaluation.

Part number	Fault protection(V)	Data rate (kbps)	VCC (V)	Bus wake-up	AEC-Q100	Package
CA-IF10285S-Q1	±40	20	5	Yes	Yes	SOIC8
CA-IF10283S-Q1	±40	20	3.3	Yes	Yes	SOIC8

CA-IF10285/3x-Q1 EVM Board

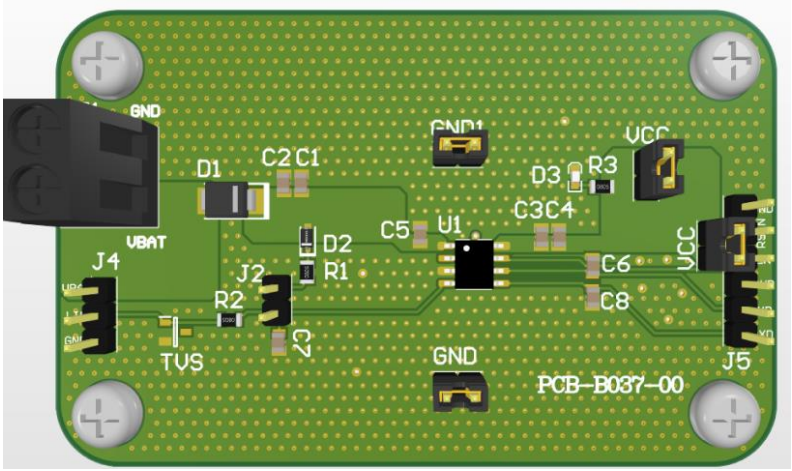

Figure 1. CA-IF10285/3x-Q1 EVM board

CA-IF10285/3x-Q1 EVM Schematic

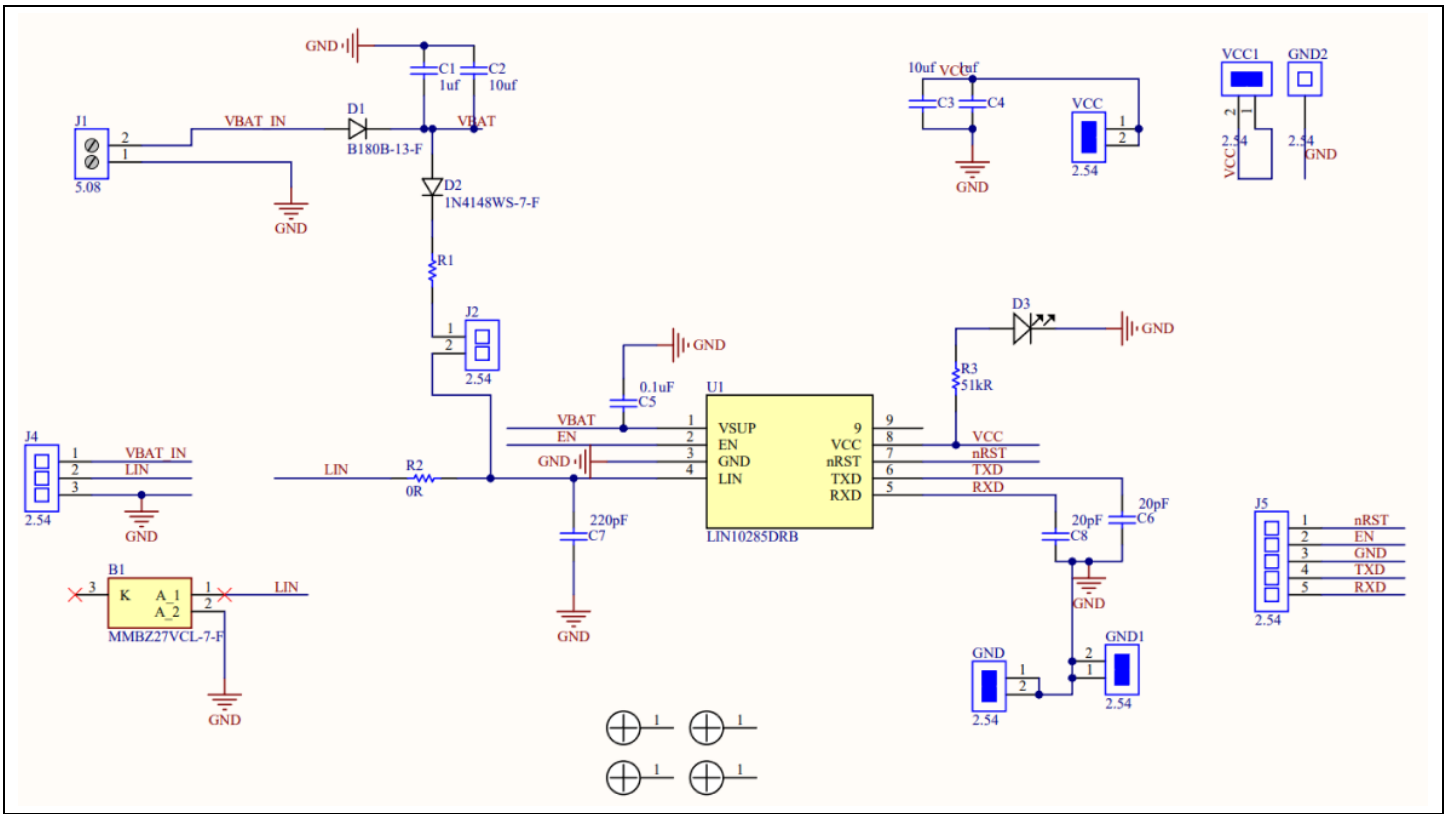

Figure 2. CA-IF10285/3x-Q1 EVM schematic

CA-IF10285/3x-Q1 EVM PCB Layouts

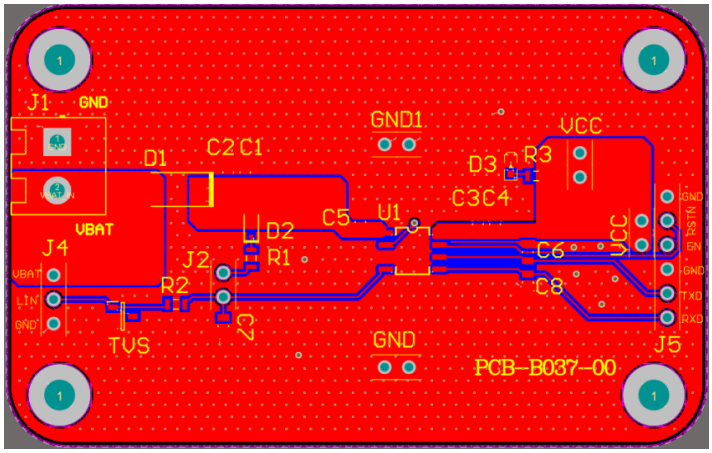

Figure 3. CA-IF10285/3x-Q1 EVM PCB layout _ top layer

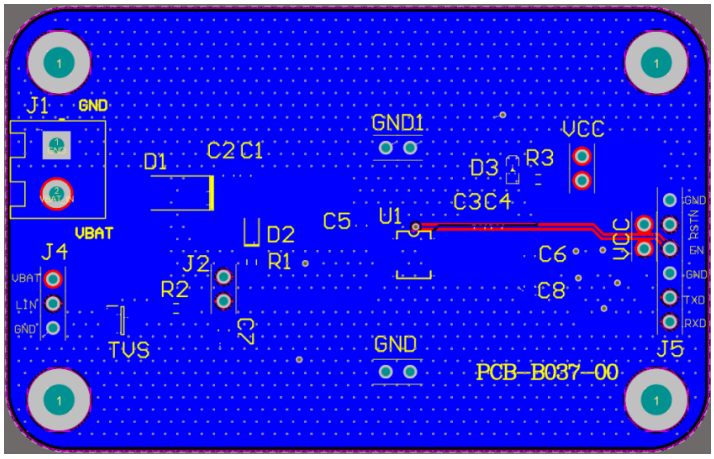

Figure 4. CA-IF10285/3x-Q1 EVM PCB layout _ bottom layer

EVM Bill of Materials

Item	Ref Des	Qty	Description	Package	MFR	PN.
1	B1	1	ESD Suppressors / TVS Diodes 225MW 22V 3PIN 1 TVS	MMBZ27VCL-7-F	WURTH Elektronik	824094024
2	C1, C4	2	Capacitor, Ceramic,	C0805		1uF
3	C2, C3	2	Capacitor, Ceramic,	C0805		10uF
4	C5	1	Capacitor, Ceramic,	C0805	-	100nF
5	C6, C8	2	Capacitor, Ceramic,	C0805	-	20pF
6	C7	1	Capacitor, Ceramic,	C0805	-	220pF
7	D1	1	Diode, General	Diode, General	-	1N4148WS-7-F
8	D2	1	Diode, General	Diode, General	-	1N4148WS-7-F
9	D3	1	Diode, Led, red	Diode, Led	XINGLIGHT	XL-1608SURC-06
10	GND2	1	Header, Unshrouded , 2.54, Male, 1p	CON, Header, 2.54, Male, 1P, TH	-	2.54, Male, 3P
11	GND, GND1, VCC, VCC1	4	Connector, Jumper, 2.54, 2p	CON, Jumper, 2.54, 2p	-	2.54, Male, 2P
12	H1, H2, H3, H4	4	MACHINE SCREW PAN PHILLIPS 4-40	ACC,NY PMS 440 0025 PH	-	-
13	J1	1	Connector, Screw Terminal, 5.08, 2P	CON, Screw Terminal, 5.08, 2P	WURTH Elektronik	691236510002
14	J2	1	Header, Unshrouded , 2.54, Male, 2P	CON, Header, 2.54, Male, 2P, TH	--	2.54, Male, 2P
15	J4	1	Header, Unshrouded , 2.54, Male, 3P	CON, Header, 2.54, Male, 3P, TH	-	2.54, Male, 3P
16	J5	1	Header, Unshrouded , 2.54, Male, 5P	CON, Header, 2.54, Male, 5P, TH	-	2.54, Male, 5P
17	R1	1	Resistor,	R0805		2.4kΩ
18	R2	1	Resistor,	R0805		0Ω
19	R3	1	Resistor,	R0805		51kΩ
20	U1	1		Chipanalog		CA-IS10285DRB

Test Equipment

- DC Power Supplies (GPD-3303S)
- 500MHz Wideband Oscilloscope (Agilent DSOX3104G)
- High-frequency Signal Generator

Hardware Setup

Figure 5 provides the hardware connections for the CA-IF10285DRB.

1. Connect the DC power supply to J1. Set the power-supply voltage to 12V, and the internal LDO generates 5V regulated output；
2. Connect EN to VCC to enable the transceiver operation;
3. Setup the frequency, duty cycle and output amplitude of signal generator at suitable level, connect the signal generator output to LIN transmitter input TXD;
4. Connect the oscilloscope probes to LIN transmit output, LIN receiver output RXD and regulator output VCC.
5. Turn on the power supply and apply the signal to the transmitter input to measure outputs: LIN, RXD and VCC.

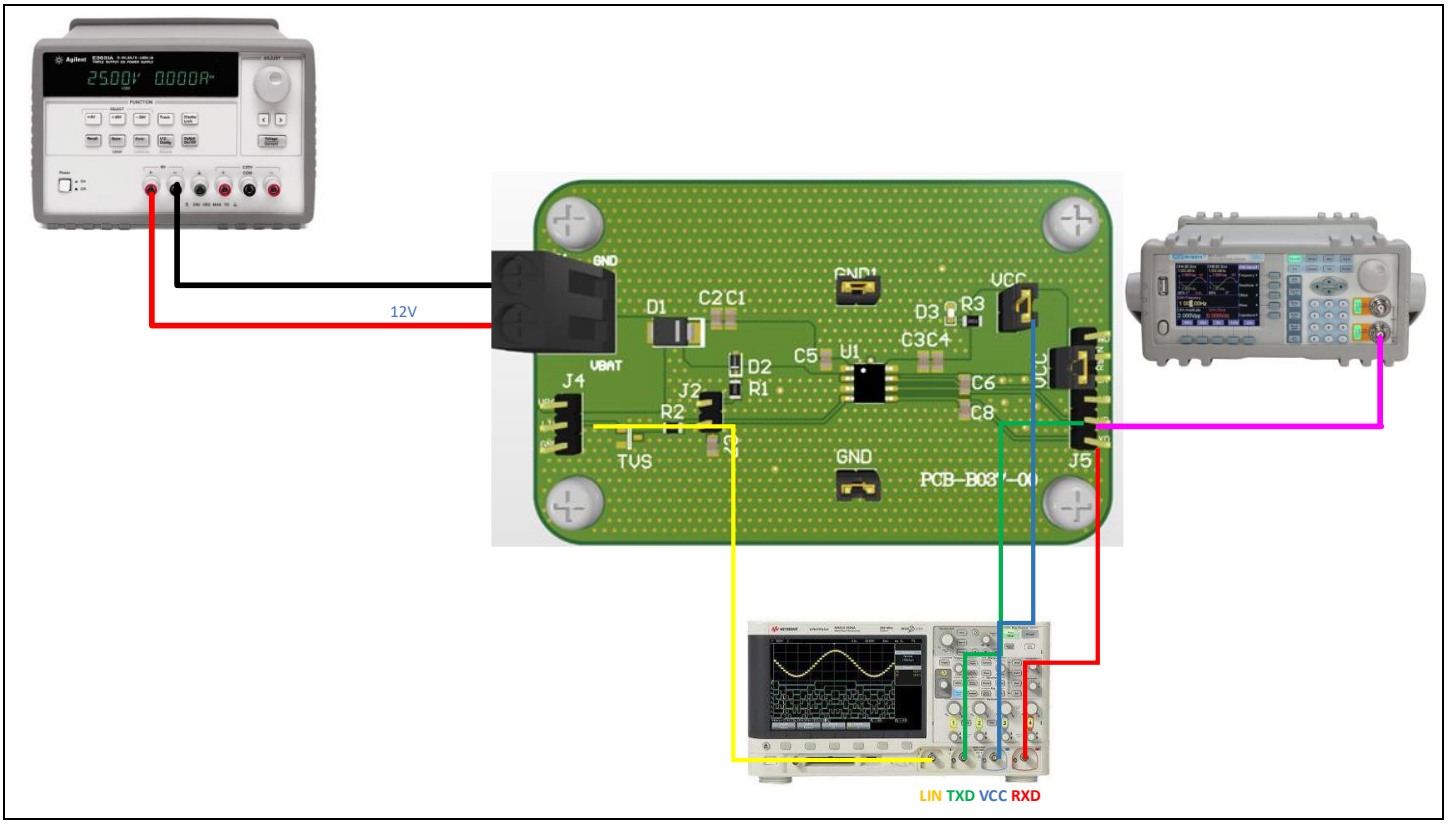

Figure 5. Hardware setup diagram

Test Result

Figure 6 shows the typical operating waveforms for the CA-IF10285DRB, including TXD input, LIN and RXD outputs and supply output VCC.

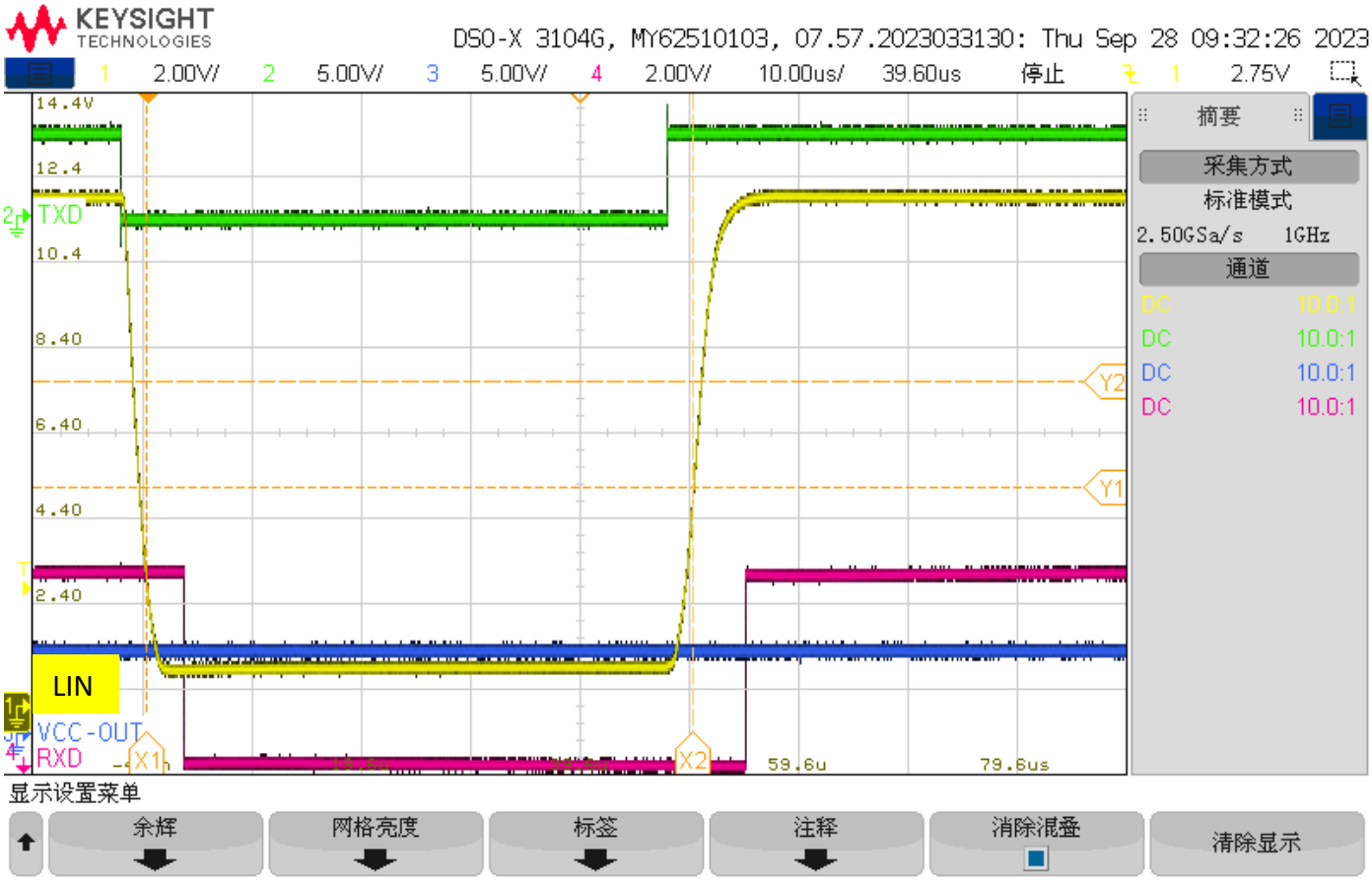

Figure 6. CA-IF10285/3x-Q1 input: TXD; output: LIN, RXD; supply output: VCC

PCB Layout Guidelines

Pin 1(Vbat): power supply input. A 100nF ceramic input filter capacitor should be placed close to the Vbat pin of the IC. This eliminates as much trace inductance effects as possible and give the transceiver a cleaner voltage supply.

Pin 2(EN): enable control input. RSTN, TXD input and EN pins are combined to switch the device operating modes between normal operation, standby or sleep. Connect a resistor in series to limit digital input current. If not use enable control, connect a 1kΩ - 10kΩ pull-up resistor to the controller's power supply.

Pin 3(GND): device ground. Keep the ground traces as short as possible to reduce the total loop inductance. Also, add thermal vias around GND pin to improve heat dissipation.

Pin 4(LIN): LIN bus input/output, connect the CA-IF10285/3X-Q1 to LIN bus. In a multipoint master/slave configuration, a 220pF capacitor are recommend connecting between LIN pin and GND at the slave node; also, an additional resistor and a block diode between LIN and Vbat at the master node are necessary.

Pin 5(RXD): RXD is data receive output, push-pull output. Insert a resistor and bypass RXD to GND with a 20pF capacitor to reduce overshoot.

Pin 6(TXD): TXD is transmit data input. Insert a resistor and bypass TXD to GND with a 20pF capacitor to reduce overshoot.

Pin 7(RSTN): RSTN is VCC supply reset output, push-pull output.

Pin 8(VCC): the CA-IF10285/3x-Q1 internal low-dropout regulator output. Bypass VCC with at least 10μF capacitor to GND to reduce output ripple. Place the decoupling capacitor as close to the VCC pin as possible on the same PCB layer to ensure the best performance.

THERMAL-GND: THERMAL-GND is the thermal pad on the bottom of DFN8 package. Connect THERMAL-GND to a large copper plane below the IC to improve heat dissipation capability. A few thermal vias that connect to a large ground plane should be provided under the thermal pad of the part for efficient heat dissipation. Refer to the CA-IF10285/3x-Q1 EVM board for a layout example.

Note that, keep all the power traces and ground connections as short as possible to reduce the total loop inductance.

Revision History

Revision Number	Revision Date	Description
Ver1.0	Oct. 2023	Preliminary-Datasheet

Important statement

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