CA-IF4888HS Bus-Polarity Correcting RS-485 Transceiver

1 Key Features

- Meets Requirements of TIA/EIA-485A Standard
- Bus-Polarity Correction Within 114ms (t_{FS-max})
- Data Rate: 300bps to 500kbps
- Supply Voltage: 3V to 5.5V
- Current-limiting Driver and Thermal Shutdown Function
- Bus I/O ESD Protection:
  - ±30kV HBM
  - ±8kV IEC 61000-4-2 Contact Discharge
- 1/8 Unit Load (Up to 256 Nodes on a Bus)
- Operating Temperature Range: –40°C to 125°C
- Common Mode Voltage Range: ±15V
- Fault Protection Range: ±30V
- Low Power Current: 960μA (max.) @ Receive Mode
- Standby Current: < 5μA
- Narrow-Body SOIC8 Package

2 Applications

- Industrial Automation
- HVAC Systems
- DMX512-Networks
- Process Control
- Battery-Powered Applications
- Motion Control
- Telecom Equipment

3 Description

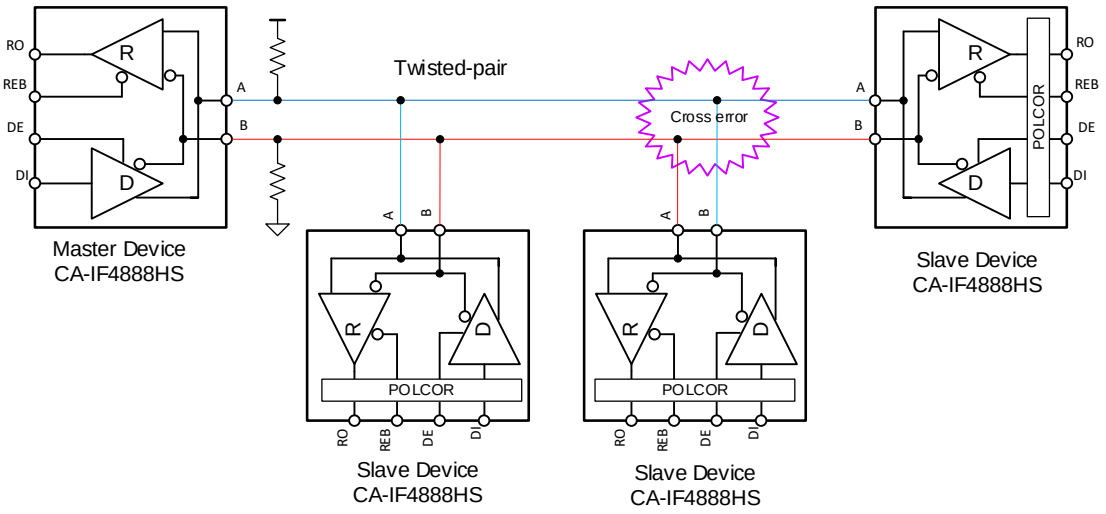
The CA-IF4888HS is a low-power RS-485 transceiver with automatic bus-polarity correction. Upon hot plug-in, the device detects and corrects the bus polarity within the first 114ms (t_{FS-max}) of bus idling. This device can extend the common mode voltage range to ±15V, and the fault protection range to ±30V. Therefore, this device is suitable for long cable applications. The bus pins are robust to electrostatic discharge (ESD) events, with high levels of protection to human-body model (HBM), and contact discharge specifications.

The CA-IF4888HS is available in a narrow-body SOIC8 package, which is suitable for space-constrained applications. This device is specified over ambient free-air temperature range of –40°C to 125°C.

Device Information

PART NUMBER	PACKAGE	BODY SIZE (NOM)
CA-IF4888HS	SOIC8 (S)	3.9mm × 4.9mm

Typical Network Application With Polarity Correction



4 Ordering Guide

Table 4-1 Ordering Guide for Valid Ordering Part Number

Part Number	Full/Half-Duplex	Function	Date Rate (kbps)	Package
CA-IF4888HS	Half-Duplex	Automatic bus-polarity correction	500	SOIC8 (S)

Table of Contents

5 Revision History

Revision	Description	Date	Page
Version 1.00	NA	2022.02.08	NA

6 Pin Descriptions and Functions

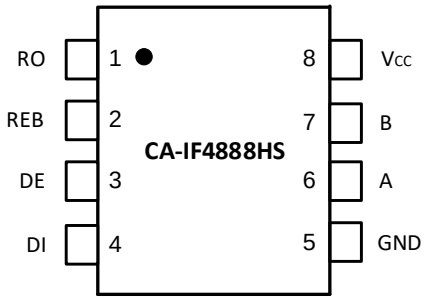


Figure 6-1 CA-IF4888HS Pin Configuration

Table 6-1 CA-IF4888HS Pin Description and Functions

NAME	PIN NUMBER	TYPE	DESCRIPTION
RO	1	Digital Output	Receiver data output.
REB	2	Digital Input	Receiver enabled control, pulled up internally: 1. When REB is low, receiver is enabled; 2. When REB is high or open, receiver is disabled.
DE	3	Digital Input	Driver enabled control, pulled down internally: 1. When DE is high, driver is enabled; 2. When DE is low or open, driver is disabled.
DI	4	Digital Input	Driver data input, pulled up internally.
GND	5	Ground	Ground.
A	6	Bus Input/Output	Noninverting driver output/receiver input.
B	7	Bus Input/Output	Inverting driver output/receiver input.
V_{CC}	8	Power	Power supply input, bypass V_{CC} to GND with at least 0.1μF capacitors as close as possible to the device.

7 Specifications

7.1 Absolute Maximum Ratings[1]

PARAMETER		MIN	MAX	UNIT
V_{CC}	Supply voltage[2]	–0.5	7	V
V_{IO}	Bus voltage of A and B[2]	–30	30	V
V_{IO}	Input logical voltage of DI, DE and REB	–0.3	7	V
V_{IO}	Output logical voltage of RO	–0.3	V_{CC} + 0.3[3]	V
T_J	Junction Temperature		150	°C
T_{STG}	Storage Temperature	–65	150	°C

NOTE:

1. Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. All voltage values are with respect to the ground terminal and are peak voltage values.
3. Maximum voltage must not exceed 7V.

7.2 ESD Ratings

			VALUE	UNIT
V_{ESD} Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001	Bus pins (A, B) to GND	±30	kV
		All other pins	±6	
	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins		±2	
	Contact discharge, per IEC 61000-4-2		±8	kV

7.3 Recommended Operating Conditions

PARAMETER		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage, with respect to GND	3.0	5.0	5.5	V
V_{IN}	Bus input voltage	–15		15	V
V_{IH}	High-level input voltage of DI, DE and REB	2.0		V_{CC}	V
V_{IL}	Low-level input voltage of DI, DE and REB	0		0.8	V
R_L	Differential load resistance	54			Ω
$1/t_{UI}$	Data Rate	0.3		500	kbps
T_A	Ambient Temperature	–40		125	°C
T_J	Junction Temperature	–40		150	°C

7.4 Thermal Information

THERMAL METRIC		SOIC8 (S)	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	115	°C/W
$R_{\theta JC}$	Junction-to-case (top) thermal resistance	60	°C/W

7.5 Electrical Characteristics

Over recommended operating temperature range (unless otherwise noted). All typical specifications are at T_A = 25°C and V_{CC} = 5V.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Driver							
$\|V_{OD}\|$	Differential output voltage	R_L = 60Ω, –15V ≤ V_{test} ≤ 15V, see Figure 8-1[1]		1.5	3.5		V
		R_L = 60Ω, –15V ≤ V_{test} ≤ 15V, 4.5V ≤ Vcc ≤ 5.5V, see Figure 8-1		2.1			V
		R_L = 100Ω, C_L = 50pF, see Figure 8-2		2	4		V
		R_L = 54Ω, C_L = 50pF, see Figure 8-2		1.5	3.7		V
$\Delta\|V_{OD}\|$	Change in magnitude of differential-output voltage	R_L = 100Ω or 54Ω, C_L = 50pF, see Figure 8-2		–200		200	mV
V_{OC}	Common-mode output voltage			1	V_{CC}/2	3	V
$\Delta V_{OC(SS)}$	Change in magnitude of common-mode output voltage			–200		200	mV
I_{OS}	Driver short-circuit output current	DE = V_{CC}, –7V ≤ V_O ≤ 12V, or A shorted to B		–250		250	mA
Receiver							
I_I	Bus input current	DE = 0V, V_{CC} = 0V or 5V	V_I = 12V		72	125	μA
			V_I = –7V	–100	–43		
			V_I = 15V		91	125	
			V_I = –15V	–200	–97		
V_{TH+}	Positive-going receiver input voltage threshold	Over common-mode range			–100	–20	mV
V_{TH-}	Negative-going receiver input voltage threshold			–200	–130		mV
V_{HYS}[2]	Receiver differential-input voltage threshold hysteresis, $V_{TH+} - V_{TH-}$				30		mV
V_{OH}	High-level output voltage	I_{OH} = –4mA		V_{CC} – 0.4	V_{CC} – 0.2		V
V_{OL}	Low-level output voltage	I_{OL} = 4mA			0.2	0.4	V
I_{OZR}	High-impedance output current	REB = V_{CC}, V_O = 0V or V_{CC}		–1		1	μA
Input Logic (DI, DE, REB)							
I_{IN}	Input Current	0V ≤ V_{IN} ≤ V_{CC}		–6.2		6.2	μA
Supply							
I_{CC}	Quiescent supply current	Both driver and receiver enabled, REB = 0V, DE = V_{CC}, empty load, no switching			2.4	3	mA
		Driver enabled and receiver disabled, REB = V_{CC}, DE = V_{CC}, empty load, no switching			0.8	1.2	
		Driver disabled and receiver enabled, REB = 0V, DE = 0V, empty load, no switching			0.7	0.96	
		Both driver and receiver disabled, REB = DI = V_{CC}, DE = 0V, empty load, no switching			2.4	5	μA
TSD	Thermal shutdown threshold				180		°C

NOTE:

1. $|V_{OD}|$ ≥ 1.4V when T_A > 85°C, V_{test} < –7V and V_{CC} < 3.135V.
2. Under any specific conditions, V_{TH+} is specified to be at least V_{HYS} higher than V_{TH-}.

7.6 Timing Characteristics

Over recommended operating temperature range (unless otherwise noted). All typical specifications are at T_A = 25°C and V_{CC} = 5V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Driver						
t_r, t_f	Differential output rise and fall time	R_L = 54Ω, C_L = 50pF, see Figure 8-3	250	360	680	ns
t_{PHL}, t_{PLH}	Driver propagation delay			280	500	ns
$t_{SK(P)}$	Driver pulse skew, $\lvert t_{PHL} - t_{PLH} \rvert$				10	ns
t_{PHZ}, t_{PLZ}	Driver disable time	see Figure 8-4 and Figure 8-5		10	200	ns
t_{PZH}, t_{PZL}	Driver enable time[1]	REB = 0V, see Figure 8-4 and Figure 8-5		100	600	ns
		REB = V_{CC}, see Figure 8-4 and Figure 8-5		7.2	11	µs
Receiver						
t_r, t_f	Receiver output rise and fall time	C_L = 15pF[2], see Figure 8-6		3.8	10	ns
t_{PHL}, t_{PLH}	Receiver propagation delay time			23	110	ns
$t_{SK(P)}$	Receiver pulse skew, $\lvert t_{PHL} - t_{PLH} \rvert$				7	ns
t_{PHZ}, t_{PLZ}	Receiver disable time	See Figure 8-7		7	20	ns
$t_{PZH(1)}$, $t_{PZL(1)}$, $t_{PZH(2)}$, $t_{PZL(2)}$	Receiver enable time[3]	DE = V_{CC}, see Figure 8-7		8	20	ns
		DE = 0V, see Figure 8-8		7	14	µs
t_{FS}	Bus failsafe time	Driver disabled	38	76	114	ms

NOTE:

1. When DE and REB are shorted together, driver enable time refers to the case when REB = 0V.
2. C_L includes probe and fixture capacitance.
3. When DE and REB are shorted together, receiver enable time refers to the case when DE = V_{CC}.

7.7 Typical Characteristics

All typical specifications are at T_A = 25°C and V_{CC} = 5V (unless otherwise noted).

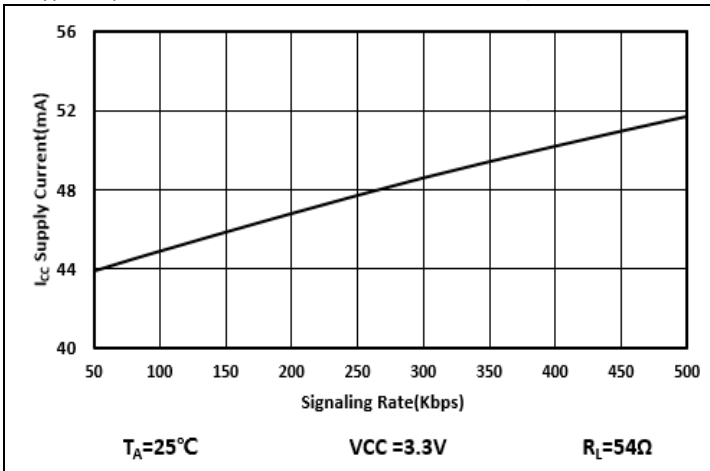


Figure 7-1 Supply Current vs. Signaling Rate @ V_{CC} = 3.3V

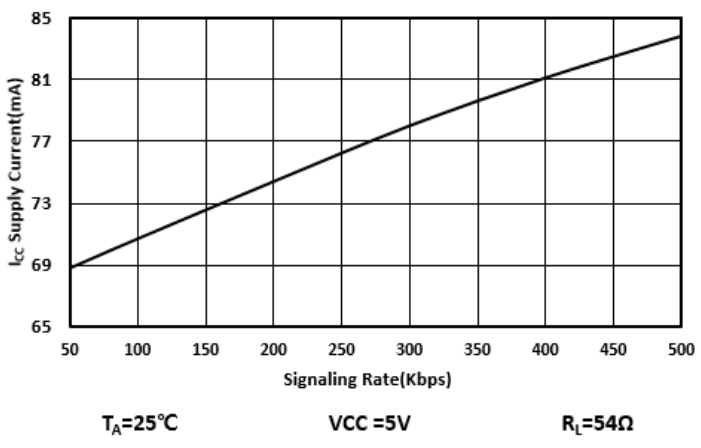


Figure 7-2 Supply Current vs. Signaling Rate @ V_{CC} = 5V

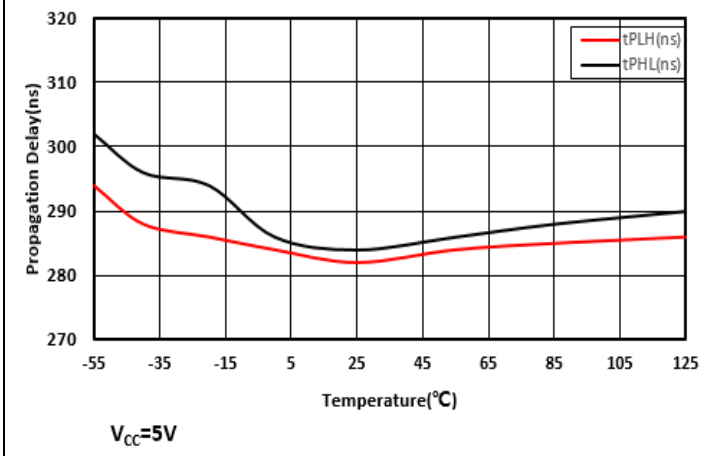


Figure 7-3 Driver Propagation Delay vs. Temperature

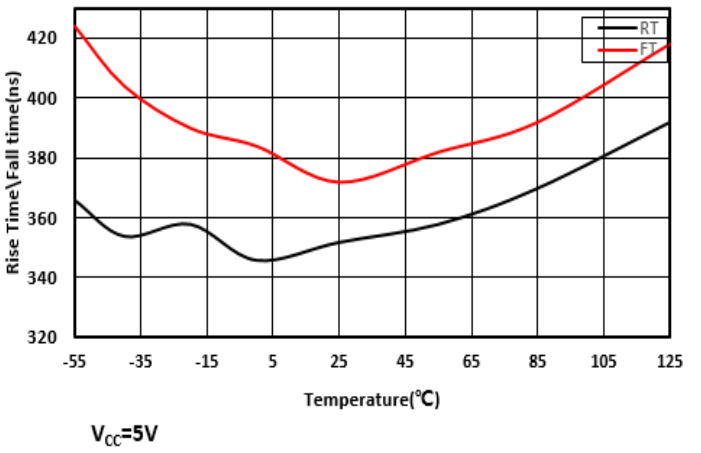


Figure 7-4 Driver Output Rise and Fall Time vs. Temperature

8 Parameter Measurement Information

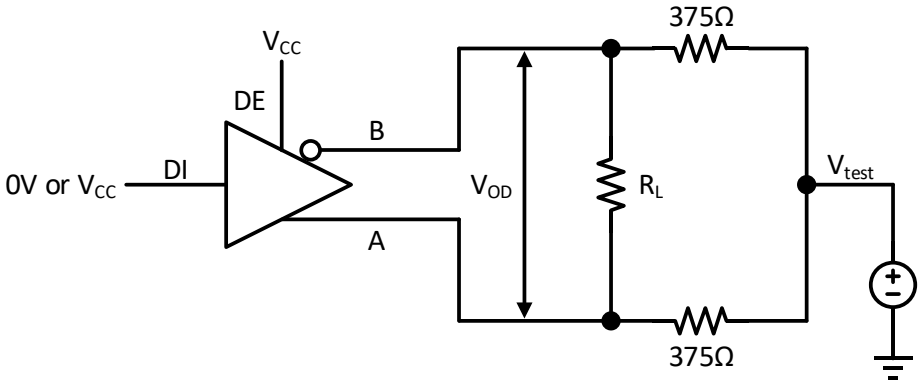


Figure 8-1 Measurement of Driver Differential Output Voltage With Common-Mode Load

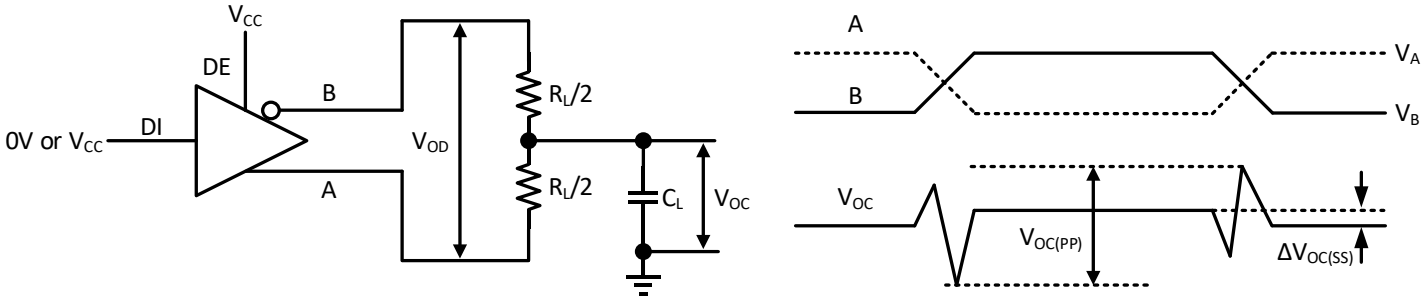


Figure 8-2 Measurement of Driver Differential and Common-Mode Output Voltage With RS-485 Load

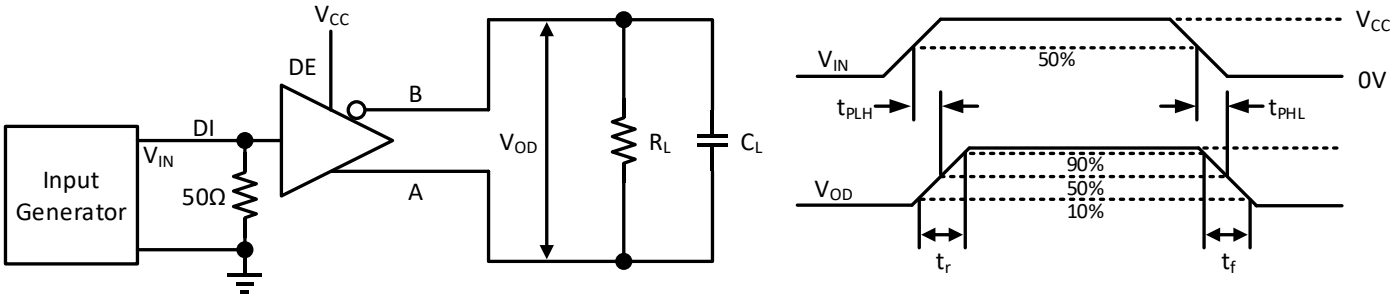


Figure 8-3 Measurement of Driver Output Rise and Fall Time and Propagation Delay

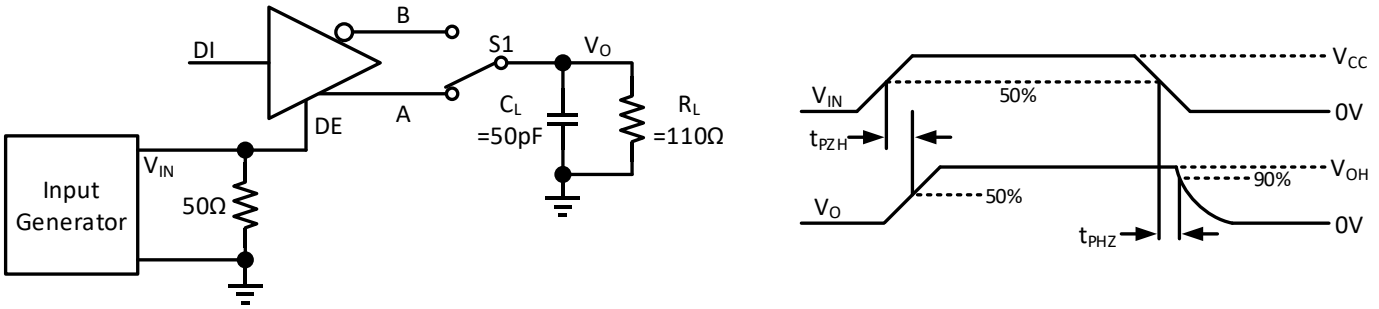


Figure 8-4 Measurement of Driver Enable and Disable Time With Active High Output and Pull-Down Load

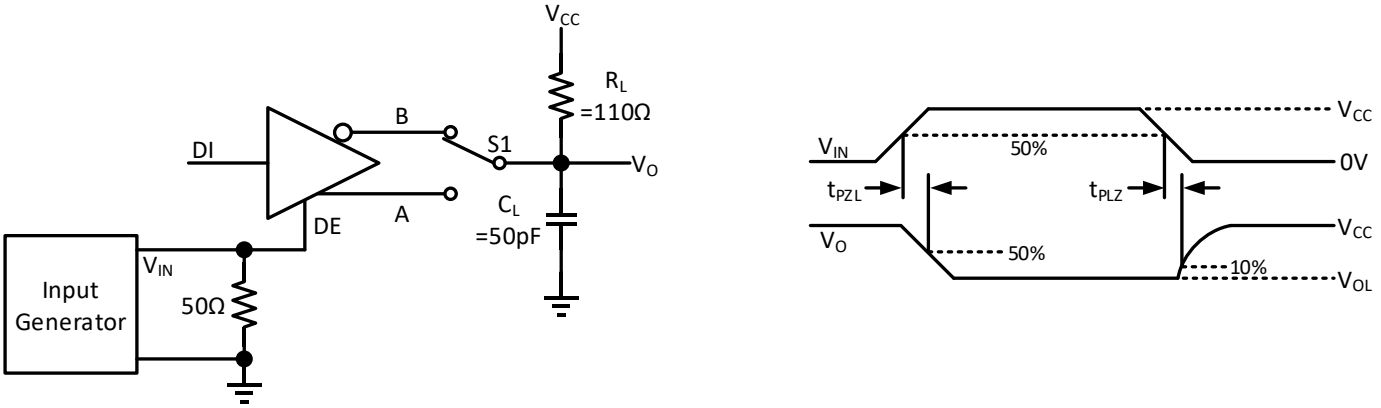


Figure 8-5 Measurement of Driver Enable and Disable Time With Active Low Output and Pull-Up Load

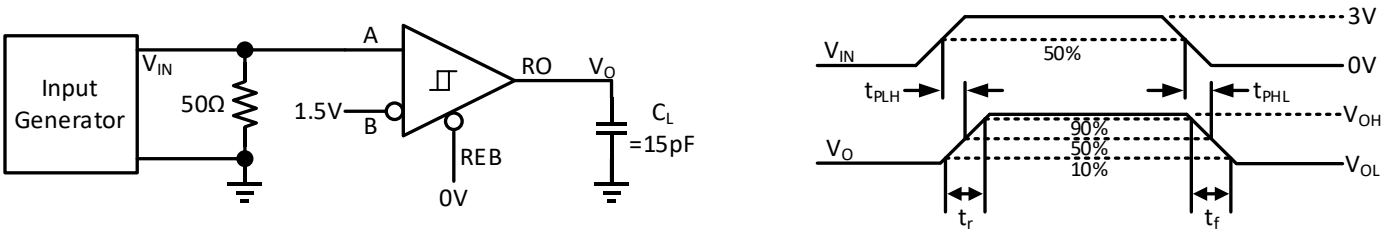


Figure 8-6 Measurement of Receiver Output Rise and Fall Time and Propagation Delay

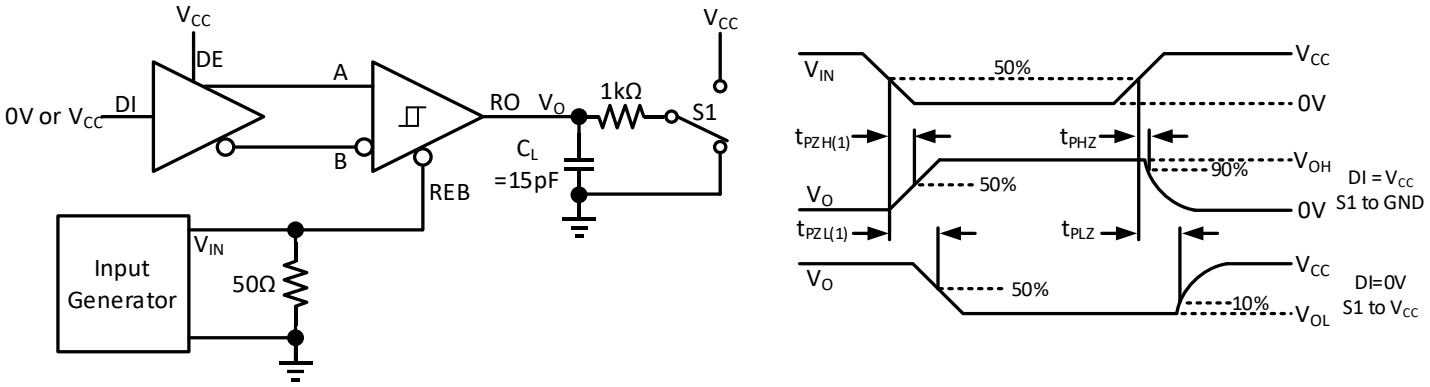


Figure 8-7 Measurement of Receiver Enable/Disable Time With Driver Enabled

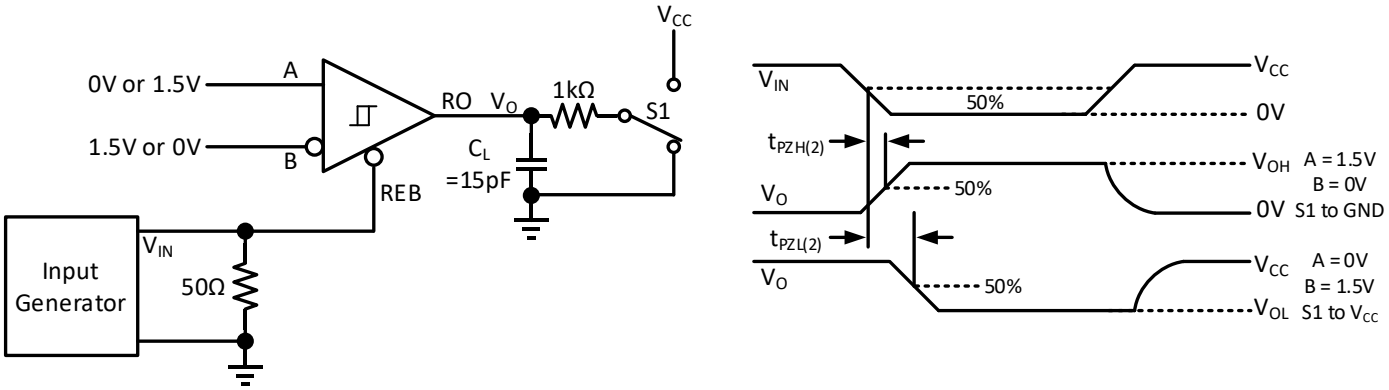


Figure 8-8 Measurement of Receiver Enable Time With Driver Disabled

9 Detailed Description

9.1 Overview

The CA-IF4888HS device integrates hysteresis input thresholds to provide an internal bias for the receiver input threshold. When the bus is idle or short-circuited, the receiver output remains logic-high level without the need of an external fail-safe bias resistor. Device operation is specified over a wide ambient temperature range from –40°C to 125°C. The device integrates automatic bus polarity correction to detect crossover errors at initial power-up to exchange polarity definitions for buses A and B internally.

9.2 Device Function Mode

9.2.1 Driver

When the driver enabled pin DE is at logic high level, differential output A and B follow with the data input DI. Under normal mode, the logic high level of DI causes A to high level and B to low level. In this case, the differential output voltage of $V_{OD} = V_A – V_B$ is defined to be positive. When DI is at low level, the output state is reversed: A becomes low level, B becomes high level, and V_{OD} is negative.

When DE is at low level, both outputs of driver become high-impedance. In this case, the logic state at DI is irrelevant. The pin DE has an internal pull-down resistance to ground, so the driver is disabled when DE is open. The pin DI has an internal pull-up resistance to V_{CC}, so the output A becomes high level and B becomes low level when DI is open as well as the driver is enabled under normal mode.

The truth table of driver is shown in Table 9-1. The detailed mechanism of polarity-correcting mode is shown in 9.3.

Table 9-1 Truth Table of Driver[1]

INPUT	ENABLE	OUTPUT		FUNCTION
DI[2]	DE[3]	A	B	
Normal Mode				
H	H	H	L	Actively drive bus high
L	H	L	H	Actively drive bus low
X	L	High-Z	High-Z	Driver disabled
X	Open	High-Z	High-Z	Driver disabled by default
Open	H	H	L	Actively drive bus high
POLARITY-CORRECTING MODE[4]				
H	H	L	H	Actively drive bus low
L	H	H	L	Actively drive bus high
X	L	High-Z	High-Z	Driver disabled
X	Open	High-Z	High-Z	Driver disabled by default
Open	H	L	H	Actively drive bus low

NOTE:
1. H = high level, L = low level, X = irrelevant, High-Z = high impedance.
2. DI is weakly pulled up to V_{CC} internally.
3. DE is weakly pulled down to GND internally.
4. The polarity-correcting mode is entered when $V_{ID} < V_{TH–}$ and $t > t_{FS\text{-}max}$ and DE = low. This state is latched when REB turns from low to high.

9.2.2 Receiver

When the enable pin REB of receiver is logical low, receiver is enabled. The truth table of receiver is shown in Table 9-2. The detailed mechanism of polarity-correcting mode is shown in 9.3.

When CA-IF4888HS is under normal mode and the bus differential input voltage V_{ID} is greater than or equal to –20mV, receiver output RO is logical high. When V_{ID} is less than or equal to –200mV, receiver output RO is logical low. When V_{ID} is between –20mV and –200mV, receiver output RO is indeterminate.

When REB is logical high or open, the receiver output RO is high-impedance and is irrelevant to the magnitude and polarity of V_{ID}.

When the bus inputs are open, short or on idle state, a failsafe logic high output at RO pin is achieved, avoiding indeterminate state which may result in system communication errors.

Table 9-2 Truth Table of Receiver[1]

DIFFERENTIAL INPUT	ENABLE	OUTPUT	FUNCTION
$V_{ID} = V_A - V_B$	REB[2]	RO	
Normal Mode			
$V_{ID} \geq -20mV$	L	H	Output valid high
$-200mV < V_{ID} < -20mV$	L	?	Indeterminate bus state
$V_{ID} \leq -200mV$	L	L	Output valid low
X	H	High-Z	Receiver disabled
X	Open	High-Z	Receiver disabled by default
Open-circuit bus	L	H after t_{FS}	Failsafe output high
Short-circuit bus	L	H after t_{FS}	Failsafe output high
Idle (terminated) bus	L	H after t_{FS}	Failsafe output high
POLARITY-CORRECTING MODE[3]			
$V_{ID} \geq -20mV$	L	L	Output valid low (polarity corrected)
$-200mV < V_{ID} < -20mV$	L	?	Indeterminate bus state
$V_{ID} \leq -200mV$	L	H	Output valid high (polarity corrected)
X	H	High-Z	Receiver disabled
X	Open	High-Z	Receiver disabled by default
Open-circuit bus	L	H after t_{FS}	Failsafe output high
Short-circuit bus	L	H after t_{FS}	Failsafe output high
Idle (terminated) bus	L	H after t_{FS}	Failsafe output high

NOTE:
1. H = high level, L = low level, X = irrelevant, High-Z = high impedance, Open = no connection, ? = indeterminate.
2. REB is weakly pulled up to V_{CC} internally.
3. The polarity-correcting mode is entered when $V_{ID} < V_{TH-}$ and $t > t_{FS\text{-}max}$ and DE = low. This state is latched when REB turns from low to high.

9.3 Bus Polarity Correction

The CA-IF4888HS automatically corrects a wrong bus-signal polarity caused by cross-wire fault. The typical application is shown in Figure 9-1. In order to detect the bus polarity, all three of the following conditions must be met:

1. A failsafe-biasing network (commonly at the master node) must define the signal polarity of the bus;
2. A slave node must enable the receiver and disable the driver (REB = DE = 0V);
3. The bus must be idle for the failsafe time, $t_{FS\text{-}max}$.

After the failsafe time has passed, the polarity correction completes and is applied to both the receiving and transmitting channels. The status of the bus polarity is latched within the transceiver and is maintained for subsequent data transmissions.

Prior to initiating data transmission, the master transceiver must be idle for a time span that exceeds the maximum failsafe time, $t > t_{FS\text{-}max}$, of a slave transceiver. This idle time is accomplished by driving the direction control line (DIR) low. After the time $t > t_{FS\text{-}max}$, the master could begin transmitting data.

Because of the indicated cross-wire fault between master and slave, the slave node receives bus signals with reversed polarity. Assuming the slave node has just been connected to the bus, the direction-control pin is pulled-down during power-up and then

is actively driven low by the slave MCU. The polarity correction begins as soon as the slave supply is established and ends after the time span which ranges from 38ms to 114ms.

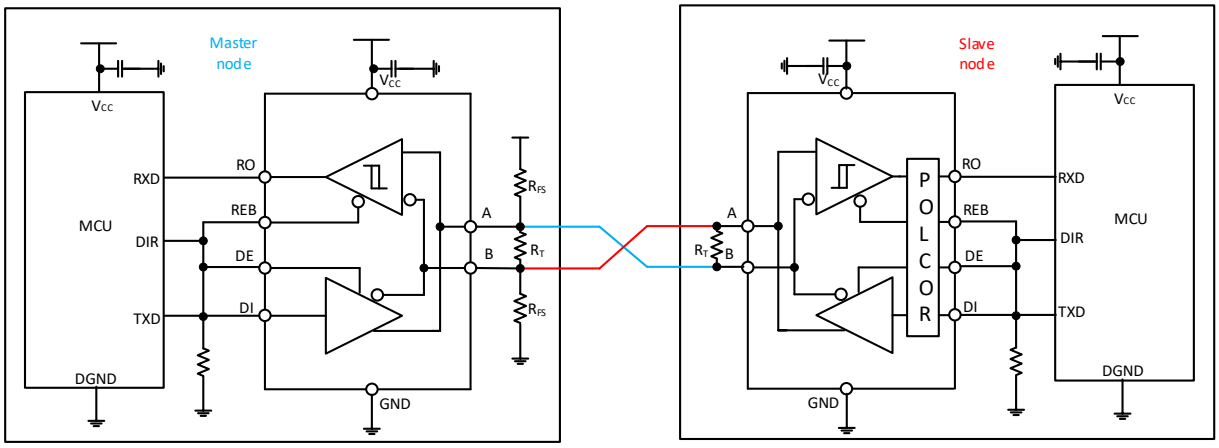


Figure 9-1 Bus Polarity Correction in Point-to-Point Application

Initially the slave receiver assumes that the correct bus polarity is applied to the inputs and performs no polarity reversal. Because of the reversed polarity of the bus-failsafe voltage, the output of the slave receiver turns low. After t_{FS} has passed and the receiver has detected the wrong bus polarity, the internal POLCOR logic reverses the input signal and output of receiver turns high. At this point all incoming bus data with reversed polarity are polarity corrected within the transceiver. Because polarity correction is also applied to the transmitting path, the data sent by the slave MCU are reversed by the POLCOR logic and then fed into the driver.

The reversed data from the slave MCU are reversed again by the cross-wire fault in the bus, and the correct bus polarity is reestablished at the master end. This process repeats each time when the device powers up and detects an incorrect bus polarity.

The bus polarity correction timing diagram is shown in Figure 9-2.

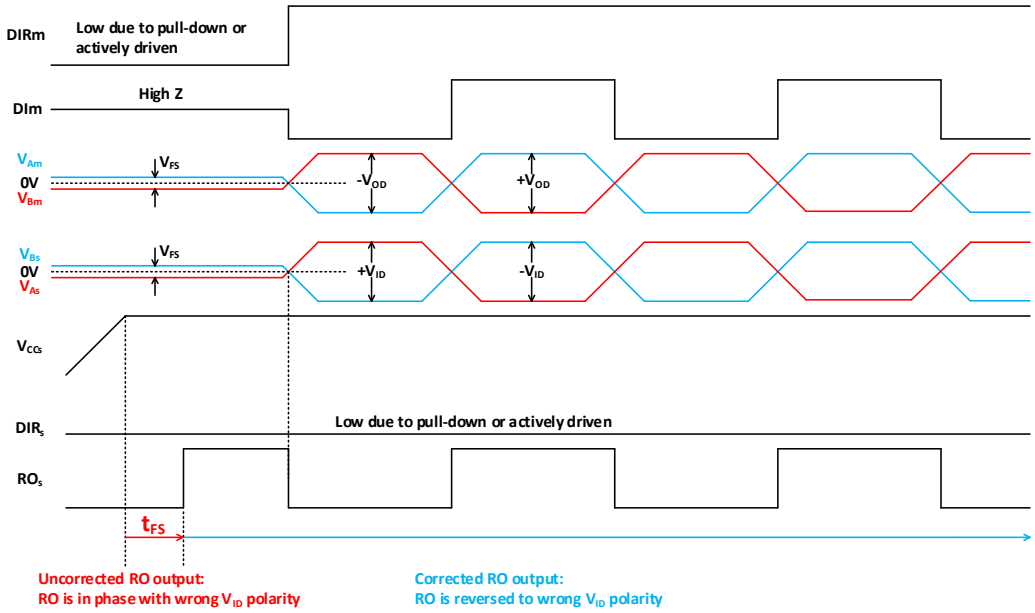


Figure 9-2 Bus Polarity Correction Timing Diagram

10 Application and Implementation

10.1 Power Supply Recommendation

To ensure reliable operation at all data rates and supply voltages, each supply should be decoupled with at least 0.1μF ceramic capacitors located as close as possible to the supply pins. This helps to reduce supply voltage ripple present on the outputs of switched-mode power supplies and also helps to compensate for the resistance and inductance of the PCB power planes. At the same time, please keep the voltage in V_{CC} pin with respect to GND pin is below 5.5V.

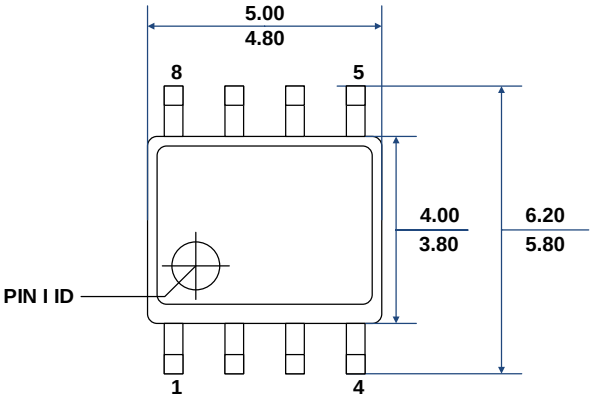
10.2 Cautions

Because of the bus correction feature in CA-IF4888HS, the data string durations of consecutive 0s or 1s exceeding $t_{FS\text{-}min}$ (38ms) can accidently trigger a wrong polarity correction and must be avoided. The minimum recommended data rate of CA-IF4888HS is 300bps.

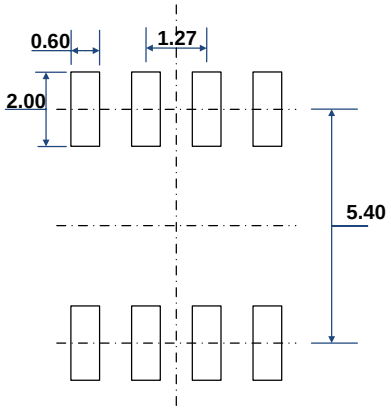
11 Package Information

11.1 SOIC8 (S) Package

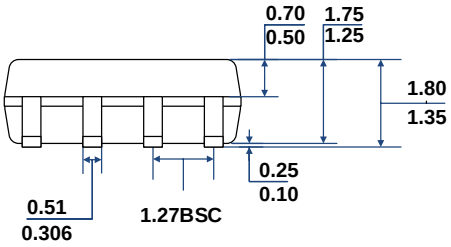
The values for the dimensions are shown in millimeters.



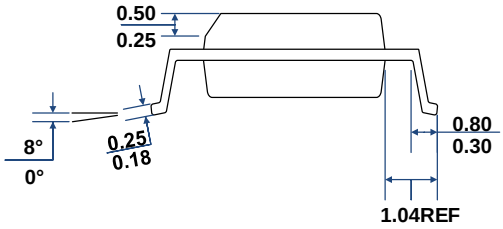
TOP VIEW



RECOMMENDED LAND PATTERN



FRONT VIEW



LEFT-SIDE VIEW

12 Soldering Information

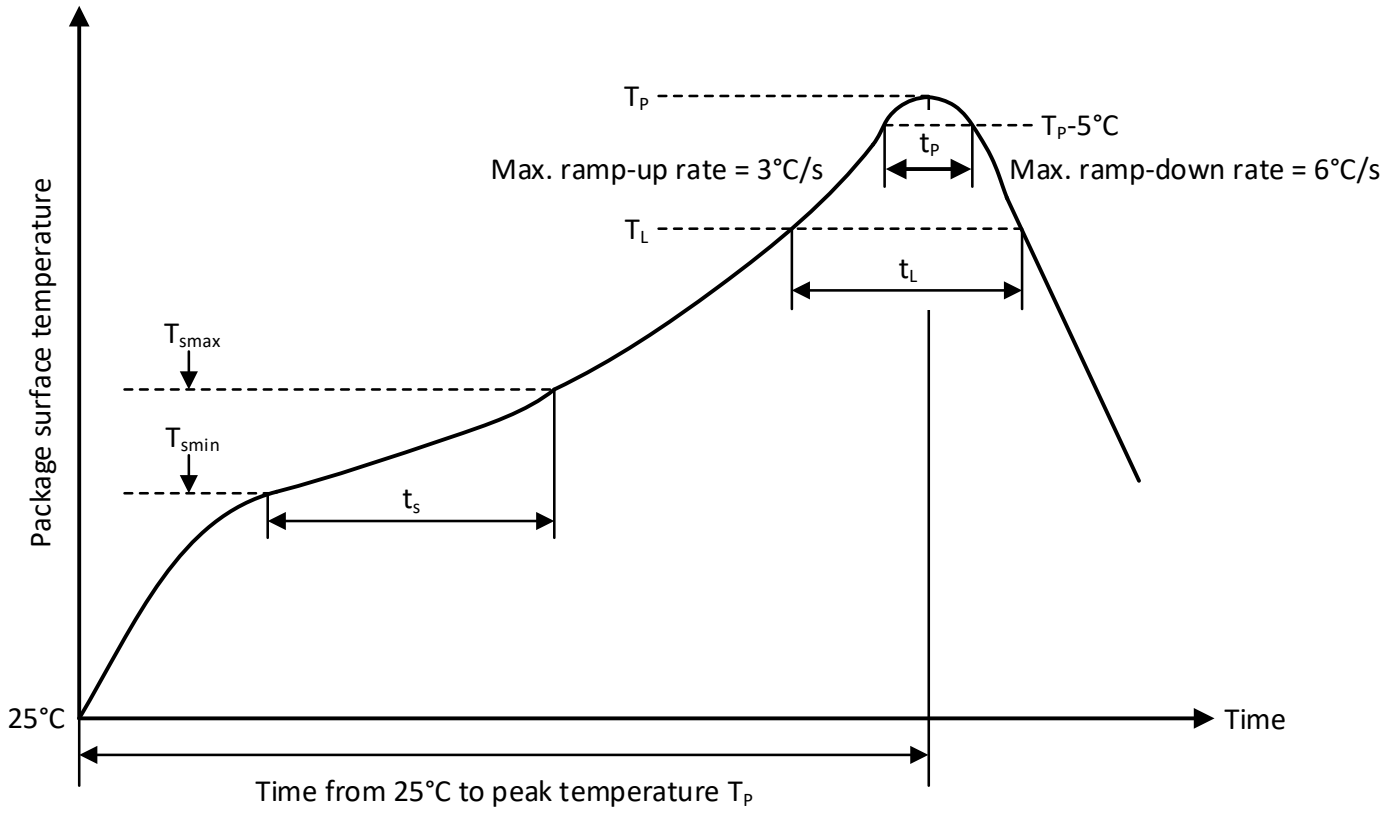


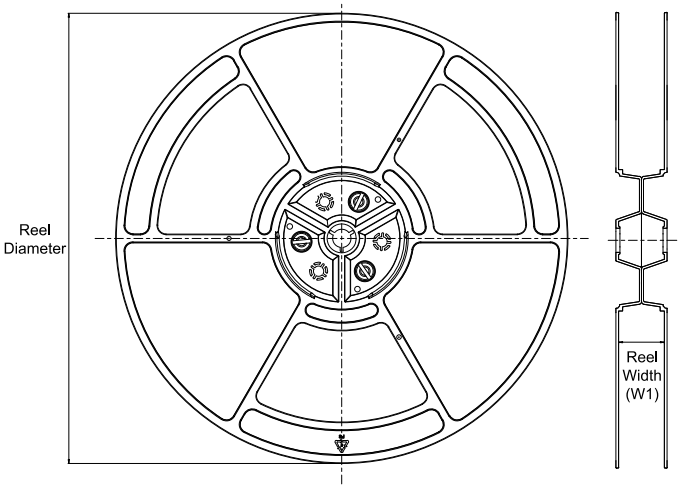
Figure 12-1 Soldering Temperature Curve

Table 12-1 Soldering Temperature Parameters

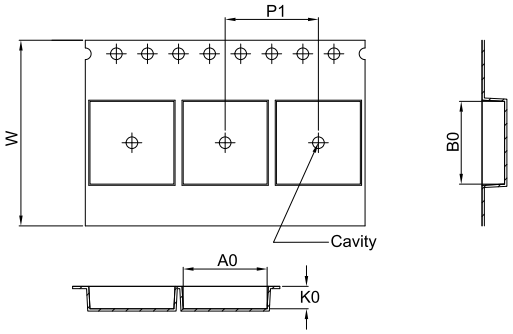
Profile Feature	Pb-Free Soldering
Ramp-up rate (T_L = 217°C to peak T_P)	3°C/s max
Time t_s of preheat temp (T_{smin} = 150°C to T_{smax} = 200°C)	60~120 seconds
Time t_L to be maintained above 217°C	60~150 seconds
Peak temperature T_P	260°C
Time t_P within 5°C of actual peak temp	30 seconds max
Ramp-down rate (peak T_P to T_L = 217°C)	6°C/s max
Time from 25°C to peak temperature T_P	8 minutes max

13 Tape and Reel Information

REEL DIMENSIONS

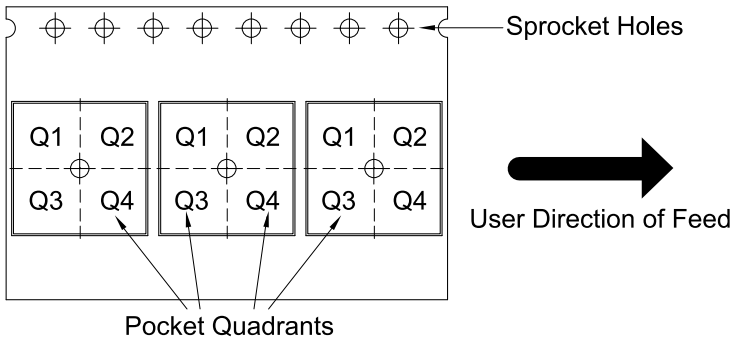


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CA-IF4888HS	SOIC	S	8	2500	330	12.4	6.5	5.4	2.1	8.0	12.0	Q1

14 Important Notice

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