CA-IF103x 3.3V Powered CAN Bus Transceiver

1. Features

- 3.3V single power supply
- Meets the ISO 11898-2:2016 and ISO 11898-5:2007 physical layer standards
- Ideal passive behavior when unpowered
  - Bus and logic terminals are high impedance (no load)
  - Power up/down with glitch free operation on bus and RXD output
- Integrated protection increases robustness
  - ±18V fault-tolerant CANH and CANL
  - ±12V extended common-mode input range (CMR)
  - Undervoltage protection on V_{CC}
  - Transmitter dominant timeout prevents lockup, data rates down to 6.25kbps
  - Thermal shutdown
- Maximum standby current I_{CC}: 15μA
- Maximum shutdown current I_{CC}: 1μA
- –55°C to 150°C Junction Temperatures Range
- –40°C to 125°C Operation Temperatures Range
- Available in SOIC8 and SOT23-8(CA-IF1033ZS) Packages
- Bus pin ESD Protection Exceeds 25kV HBM
- Bus pin ESD Protection Exceeds 8kV IEC61000-4-2

2. Applications

- Industrial control
- HVAC
- Building/Temperature Control Automation

3. General Description

This CAN transceiver series complies with the ISO 11898-2 (2016) CAN (Controller Area Network) physical layer standard and can be directly connected to 3.3V other controllers with CAN control protocol for use.

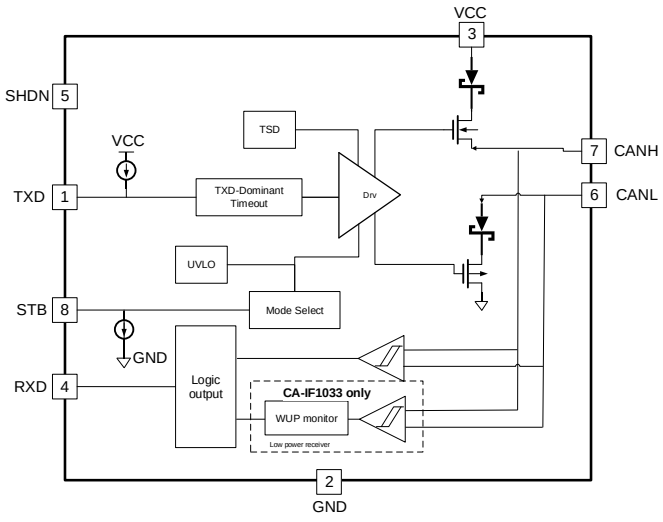
The CA-IF1030S and CA-IF1034S devices have a silent mode, in which the transmitter is turned off and the receiver continues to operate; The CA-IF1033S/ZS device has low power standby mode and remote wake-up request characteristics. The CA-IF1033S/ZS and CA-IF1034S devices have a shutdown mode, where the device Icc current is below 1μA.

The series of devices include multiple protection functions, including driver explicit timeout function and bus fault protection, to improve the stability of the device and CAN network. The series of devices has 25 kV HBM ESD protection, 8kV IEC61000-4-2 ESD contact discharge, etc.

In addition, CA-IF1033ZS is packaged in a miniaturized SOT23-8 package (2.9mm x 1.6mm) to save PCB space for application circuits.

Device Information

Part number	Package	Package size(NOM)
CA-IF1030S	SOIC8(S)	4.9mm x 3.9mm
CA-IF1033S	SOIC8(S)	4.9mm x 3.9mm
CA-IF1033ZS	SOT23-8(ZS)	2.9mm x 1.6mm
CA-IF1034S	SOIC8(S)	4.9mm x 3.9mm



Simplified Block Diagra(CA-IF1033S/ZS)

4. Ordering Information

Table 4-1 Ordering Information

Part Number	Features		Package
CA-IF1030S	Pin5 = NC, Pin8 =S	Silent Mode	SOIC8(S)
CA-IF1033S	Pin5 = SHDN, Pin8 =STB	Standby Mode/Shutdown Mode	SOIC8(S)
CA-IF1033ZS	Pin5 = SHDN, Pin8 =STB	Standby Mode/Shutdown Mode	SOT23-8(ZS)
CA-IF1034S	Pin5 = EN, Pin8 =S	Silent Mode/ Shutdown Mode	SOIC8(S)

Contents

Revision History

Revision Number	Description	Page Changed
V1.0	Initial Version	NA

5. Pin Configuration and Functions

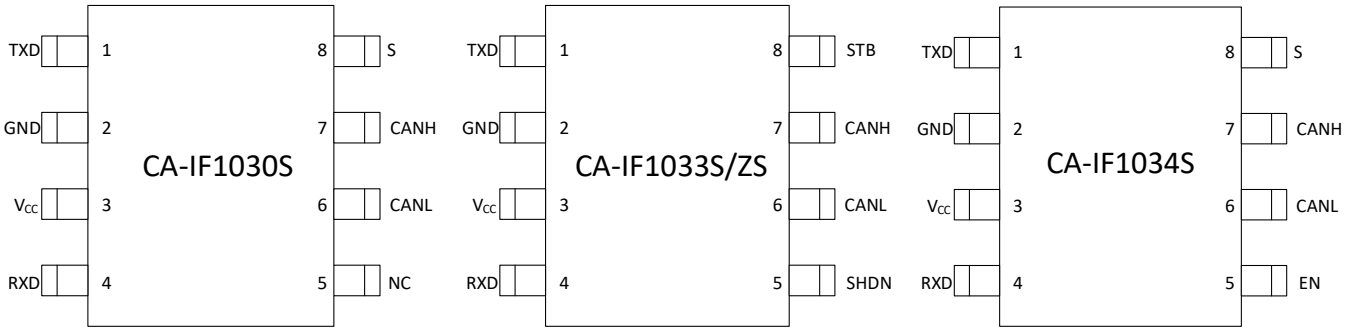


Figure 5-1 CA-IF103x Pin Configuration

Table 5-1 CA-IF103x Pin Configuration and Description

Pin #			Pin Name	Type	Description
CA-IF1030S	CA-F1033S/ CA-F1033ZS	CA-IF1034S			
1	1	1	TXD	Digital I/O	Transmit Data Input, Drive TXD high to set the driver in the recessive state. Drive TXD low to set the driver in the dominant state.
2	2	2	GND	GND	Ground.
3	3	3	V_{CC}	Power	+5V Supply Voltage. Bypass V_{CC} to GND with an at least 0.1μF capacitor.
4	4	4	RXD	Digital I/O	Receive Data Output, RXD is LOW for dominant bus state and HIGH for recessive bus state.
5	-	-	NC	NC	No connect.
-	-	5	EN	Power	Enable input pin, Logic high for enabling, integrated pull up.
	5		SHDN	Digital I/O	Drive high for shutdown mode, integrated pull down.
6			CANL	Bus I/O	CAN bus line low.
7			CANH	Bus I/O	CAN bus line high.
8	-	8	S	Digital I/O	Silent Mode Selcetion. Drive high for silent mode, integrated pull down.
-	8	-	STB	Digital I/O	Standby Mode Selcetion. Drive high for low power standby mode, integrated pull down.

6. Specifications

6.1. Absolute Maximum Ratings

PARAMETER		MIN	MAX	UNIT
V_{CC}	5V Bus Supply Voltage Range	-0.3	7	V
V_{BUS}	CAN Bus I/O voltage range (CANH,CANL)	-18	18	V
$V_{(DIFF)}$	Max differential voltage between CANH and CANL	-18	18	V
$V_{(Logic\_Input)}$	Logic input terminal voltage range (TXD, S, STB, EN)	-0.3	V_{CC}+0.3 and <+7	V
$V_{(Logic\_Output)}$	Logic output terminal voltage range (RXD)	-0.3	V_{CC}+0.3 and <+7	V
$I_{O(RXD)}$	RXD (receiver) terminal output current	-8	8	mA
T_J	VirtµAl junction temperature range	-55	150	℃
T_{STG}	Storage temperature range	-65	150	℃

Note:

1. The stresses listed under “Absolute Maximum Ratings” are stress ratings only, not for functional operation condition. Exposure to absolute maximum rating conditions for extended periods may cause permanent damage to the device.

6.2. ESD Ratings

Parameters	TEST CONDITIONS		VALUE	UNIT
HBM[1] ESD	CAN bus terminals (CANH, CANL) to GND		±25000	V
	Other pins		±4000	
CDM ESD	All pins		±2000	V
System Level ESD	CAN bus terminals (CANH, CANL) to GND	IEC 61000-4-2: unpowered contact discharge.	±8000	V

Note:

1. Per JEDEC document JEP155, 500V HBM allows safe manufacturing of standard ESD control process.

6.3. Recommended Operating Conditions

PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage Range	3.0		3.6	V
$I_{OH(RXD)}$	RXD terminal high level output current	-2			mA
$I_{OL(RXD)}$	RXD terminal low level output current			2	mA
T_A	Operation Temperature Range	-40		125	°C

6.4. Thermal Information

Thermal Metric		SOIC8	SOIC23-8	UNIT
$R_{\theta JA}$	Junction to Ambient	170	180	°C/W

6.5. Electrical Characteristics

Over recommended operating conditions, T_A = –40°C to 125°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER						
I_{CC}	Supply Current: Normal Mode	STB, SHDN=0V/ S=0V, EN= V_{CC}, TXD=0V, R_L=60 Ohm, C_L=open, R_{CM}=open, Typical Bus Load,see Figure7- 1		40	55	mA
		STB, SHDN=0V/ S=0V, EN= V_{CC}, TXD=0V, R_L=50 Ohm, C_L=open, R_{CM}=open, High Bus Load, see Figure7- 1		44	60	mA
		STB, SHDN=0V/ S=0V, EN= V_{CC}, TXD=0V, CANH=-12V, R_L=open, C_L=open, R_{CM}=open, EN= V_{CC}, see Figure7- 1		110	180	mA
		STB, SHDN=0V/ S=0V, EN= V_{CC}, TXD=V_{CC}, R_L=50 Ohm, R_{CM} =open, C_L=open, R_{CM}=open, see Figure7- 1		0.9	2	mA
	Supply Current: Silent Mode (CA-IF1030S / CA-IF1034S)	EN= V_{CC}, S = V_{CC}, TXD=V_{CC}, R_L=50 Ohm, R_{CM} =open, C_L=open, C_L=open, R_{CM}=open, see Figure7- 1		0.9	2	mA
	Supply Current: Standby Mode (CA-IF1033S/ZS)	SHDN=0V, STB = V_{CC}, TXD=V_{CC}, R_L=50 Ohm, R_{CM} =open, C_L=open, C_L=open, R_{CM}=open, see Figure7- 1		9	15	µA
	Supply Current: Shutdown (CA-IF1034S/CA-F1033S/ZS)	SHDN = V_{CC} /EN=0V, TXD=V_{CC}, R_L=50 Ohm, R_{CM} =open, C_L=open, C_L=open, R_{CM}=open, see Figure7- 1			1	µA
UV_{VCC+}	V_{CC} UVLO Voltage	Rising		2.2	2.6	V
UV_{VCC-}	V_{CC} UVLO Voltage	Fallng	1.65	2	2.5	V
$V_{HYS(UVVCC)}$		Hysteresis Voltage		200		mV
LOGIC INTERFACE (S/STB/SHDN/EN Input)						
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_{IH}	High-level input leakage current		-3		10	µA
I_{IL}	Low-level input leakage current		-4		1	µA
$I_{lek(off)}$	Unpowered leakage curren		-3		5	µA
LOGIC INTERFACE (TXD Input)						
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_{IH}	High-level input leakage current	TXD=V_{CC}= 3.6V	-2.5	0	3	µA
I_{IL}	Low-level input leakage current	TXD=0V, V_{CC}= 3.6V	-4		0	µA

$I_{lek(off)}$	Unpowered leakage curren	TXD=3.6V, V_{CC}= 0V	-2	0	2.5	μA
C_i[1]	Input Capacitance			1		pF
Note: 1. The test data is based on bench test and design simulation.						
LOGIC INTERFACE (RXD Output)						
V_{OH}	High-level output voltage	Io=-2mA	0.8*V_{CC}			V
V_{OL}	Low-level output voltage	Io=2mA		0.2	0.4	V
$I_{lek(off)}$	Unpowered leakage curren	RXD=3.6V, V_{CC}=0V	-1	0	1	μA
CAN BUS DRIVER						
$V_{O(DOM)}$	Bus output voltage (dominant)	Normal Mode[1] TXD=0V, RL=60Ohm, CL=open, RCM=open, CANH, see Figure7- 1	2.45		V_{CC}	V
		Normal Mode[1] TXD=0V, RL=50-65Ohm, CL=open, RCM=open, CANL, see Figure7- 1	0.5		1.25	V
$V_{O(REC)}$	Bus output voltage (recessive)	Normal Mode[1] TXD=VCC, RL=open, RCM=open, CANH/CANL, see Figure7- 1		1.85		V
$V_{O(STB)}$	Bus output at standby mode	Standby Mode[3] RL open, RCM open, CANH	-0.1		0.1	V
		Standby Mode[3] RL open, RCM open, CANL	-0.1		0.1	V
		Standby Mode[3] RL open, RCM open, CANH-CANL	-0.2		0.2	V
$V_{OD(DOM)}$	Bus output differential voltage (dominant	Normal Mode[1] TXD=0V, R_L=45-50 Ohm , R_{CM} open, see Figure7- 1	1.5	2	3	V
		Normal Mode[1] TXD=0V, R_L=50-65 Ohm , R_{CM} open, see Figure7- 1	1.6		3.0	V
$V_{OD(REC)}$	Bus output differential voltage (recessive)	Normal Mode1 TXD=V_{CC}, R_L =60 Ohm, C_L=open, R_{CM}=open, CANH-CANL, see Figure7- 1	-120		12	mV
		Normal Mode[1] TXD=V_{CC}, R_L =open, C_L=open, R_{CM}=open, CANH-CANL, see Figure7- 1	-50		50	mV
V_{sym_DC}	DC Output symmetry (dominant or recessive)	Normal Mode[1] R_L=60 Ohm, R_{CM} open, see Figure7- 1	-0.4		0.4	V

$I_{OS(SS\_DOM)}$	Short-circuit current (dominant)	Normal Mode[1] TXD=0V, CANL Open, CANH=-12V, see Figure7- 6	-200		mA
		Normal Mode[1] TXD=0V, CANH Open, CANL=12V, see Figure7- 6		200	mA
$I_{OS(SS\_rec)}$	Short-circuit current (recessive)	Normal Mode[1] TXD=V_{CC}, V_{BSU}=CANH=CANL=-12V to 12V, see Figure7- 6	-5	5	mA
V_{CM}	Common-mode input range	Normal Mode[1] /Silent Mode[2]/Standby Mode[3], RXD output valid, see Figure7- 2	-12	12	V
V_{IT}	Input differential threshold voltage at normal /Silent mode	Normal Mode[1] /Silent Mode[2] TXD=0V, Vcm = -12V to 12V, see Figure7- 2	500	900	mV
V_{HYS}	Input differential threshold hysteresis at normal /Silent mode	Normal Mode[1] /Silent Mode[2] Vcm -12V to 12V, see Figure7- 2	120		mV
$V_{IT(STB)}$	Input differential threshold voltage at standby mode	Standby Mode[3], Vcm= -12V to 12V, see Figure7- 2	400	1150	mV
R_{IN}	CANH/CANL input resistance	Normal Mode[1] TXD=V_{CC}	10	40	kΩ
R_{DIFF}	Differential input resistance	Normal Mode[1] TXD=V_{CC}	20	80	kΩ
$R_{DIFF\ (M)}$	Input resistance matching	CANH=CANL	-3	3	%
I_{LKG}	Input Leakage Current	V_{CC} = 0V, V_{CANH}= V_{CANL}=3.3V		5	μA
C_{IN} [4]	Input capacitance	Normal Mode[1] TXD=V_{CC}, CANH to GND/CANL to GND	24		pF
C_{IN_DIFF} [4]	Differential Input Capacitance	TXD= V_{CC}, CANH to CANL	12		pF

Note:
1. Normal Mode：CA-IF1030S ： S=0V, CA-IF1034S ： S=0V,EN= VCC； CA-IF1033S/ZS ： STB =0V, SHDN =0V.
2. Silent mode：CA-IF1030S ： S= VCC； CA-IF1034S ： S=VCC/ EN= VCC.
3. Standby：CA-IF1033S/ZS ： SHDN =0V/ STB= VCC.
4. The test data is based on bench test and design simulation.

OTP

T_{TSD}[1]	Thermal shutdown temperature		170	°C
T_{TSD_HYS}[1]	Thermal shutdown temperature threshold hysteresis		10	°C

Note: 1. The test data is based on bench test and design simulation.

6.6. Switching Characteristics

Over recommended operating conditions, T_A = –40°C to 125°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DRIVER						
t_{ONTXD}	TXD propagation delay (recessive to dominant)	Normal Mode[1] R_L=60Ω, C_L=100pF, see Figure7- 1		40		ns
t_{OFFTXD}	TXD propagation delay (dominant to recessive)	Normal Mode[1] R_L=60Ω, C_L=100pF, see Figure7- 1		45		ns
t_{DTO}	TXD-dominant Timeout	Normal Mode[1] R_L=60Ω, C_L open, see Figure7- 5	1.6	3	5	ms
RECEIVER						
t_{ONRXD}	RXD propagation delay (recessive to dominant)	Normal Mode[1] C_{RXD}=15pF, see Figure7- 2		75		ns
t_{OFFRXD}	RXD Propagation delay (dominant to recessive)	Normal Mode[1] C_{RXD}=15pF, see Figure7- 2		80		ns
DEVICE						
t_{loop1}	Total loop delay, driver input (TXD) to receiver->output (RXD), recessive to dominant	R_L=60Ω, C_{RXD}=15pF, C_{LD}=100pF, see Figure7- 3		125	255	ns
t_{loop2}	Total loop delay, driver input (TXD) to receiver-> output (RXD), dominant to recessive	R_L=60Ω, C_{RXD}=15pF, C_{LD}=100pF, see Figure7- 3		155	255	ns
t_{MODE}	Mode change time, from normal to silent or from silent to normal	see Figure7- 4		12	45	µs
T_{wk_FILTER}	Filter time for a valid wake-up pattern	see Figure9- 4	0.5		1.8	µs
$T_{WK\_TIMEOUT}$	Bus wake-up timeout	see Figure9- 4	0.8		10	ms

Note:

1. Normal Mode： CA-IF1030S ： S=0V, CA-IF1034S ： S=0V,EN= VCC； CA-IF1033S/ZS ： STB =0V, SHDN =0V.

7. Parameter Measurement Information

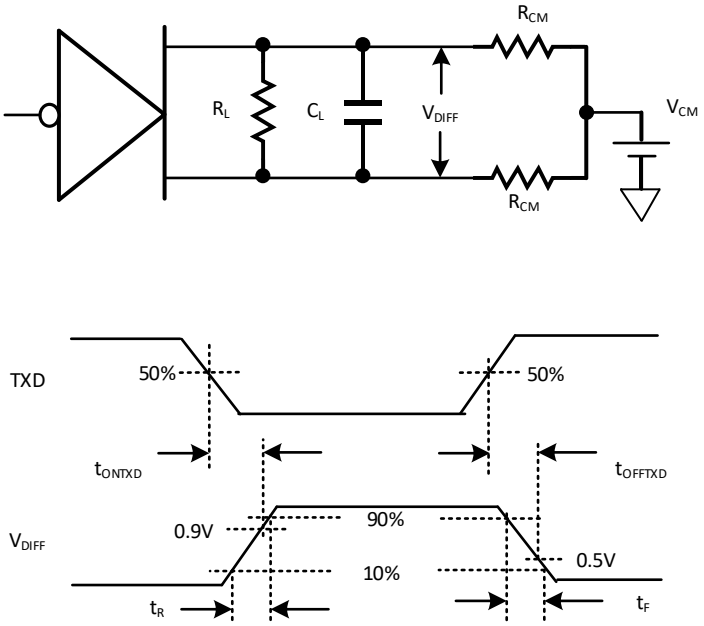


Figure7- 1 Transmitter Test Circuit and Timing Diagram

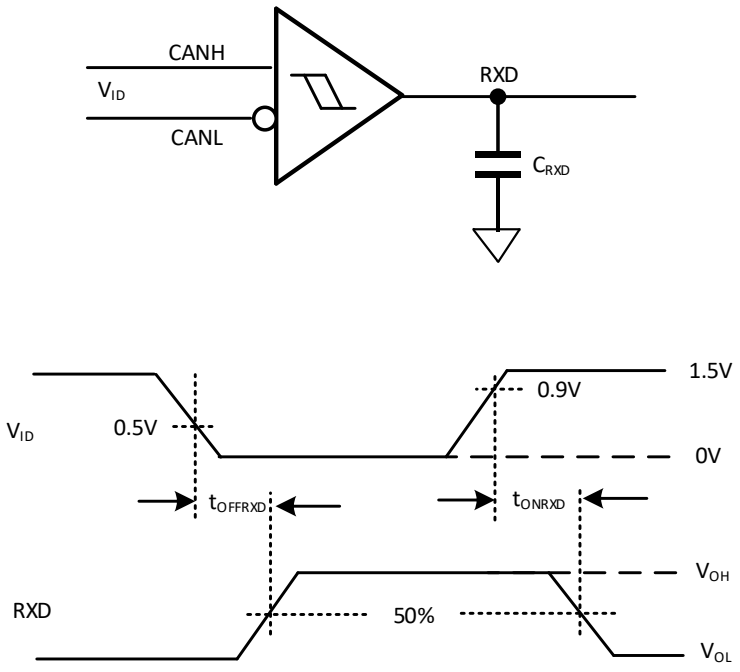


Figure7- 2 Receiver Test Circuit and Measurement

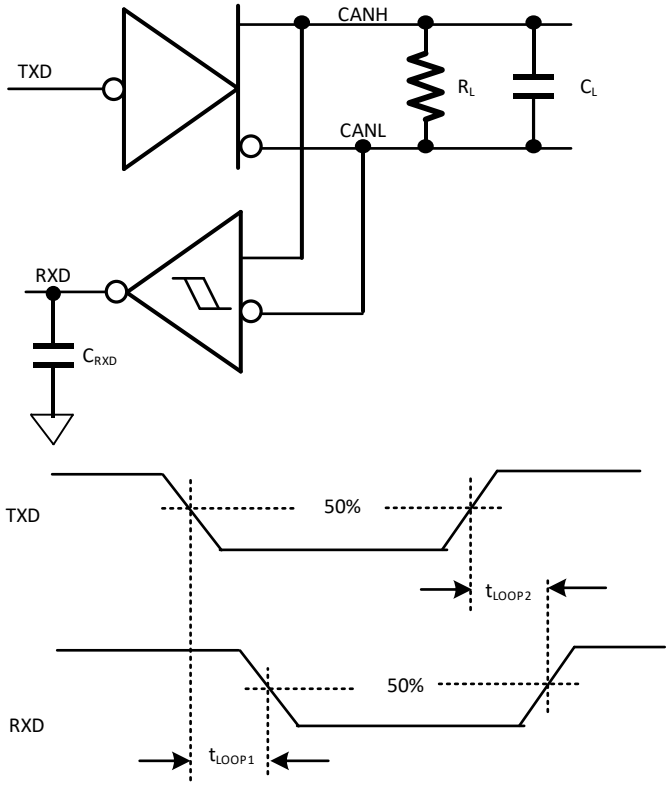


Figure7- 3 TXD to RXD Loop Delay

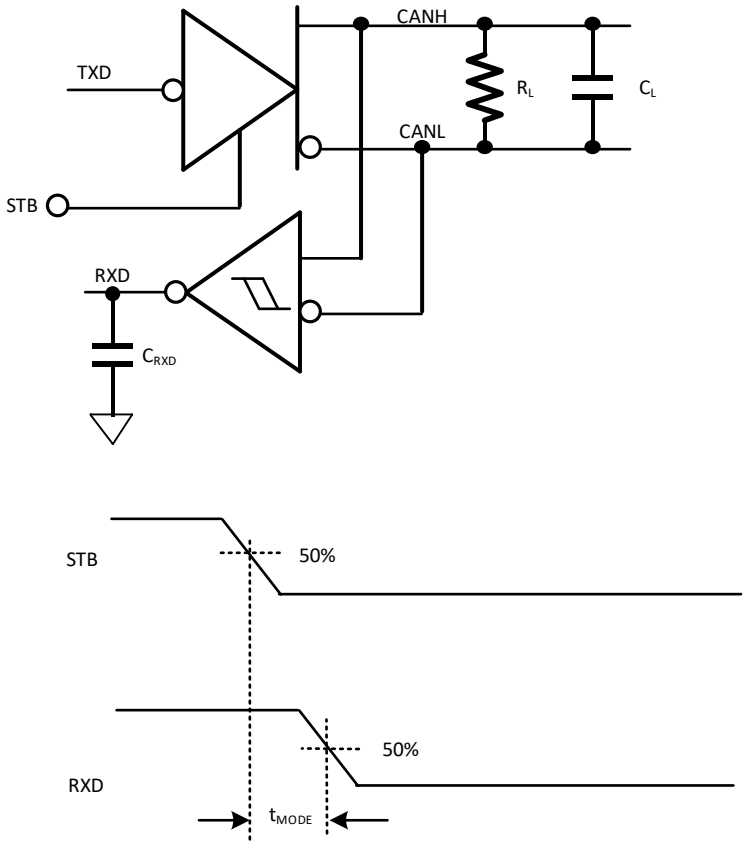


Figure7- 4 Mode Change Test Circuit and Measurement

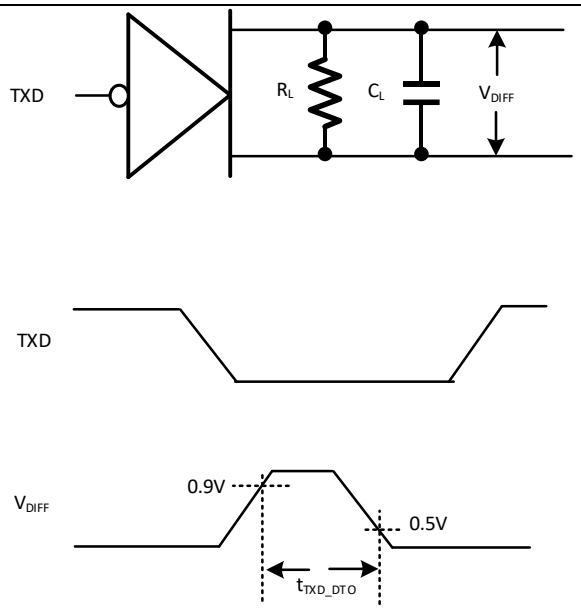


Figure7- 5 Transmitting Dominant Timeout Timing Diagram

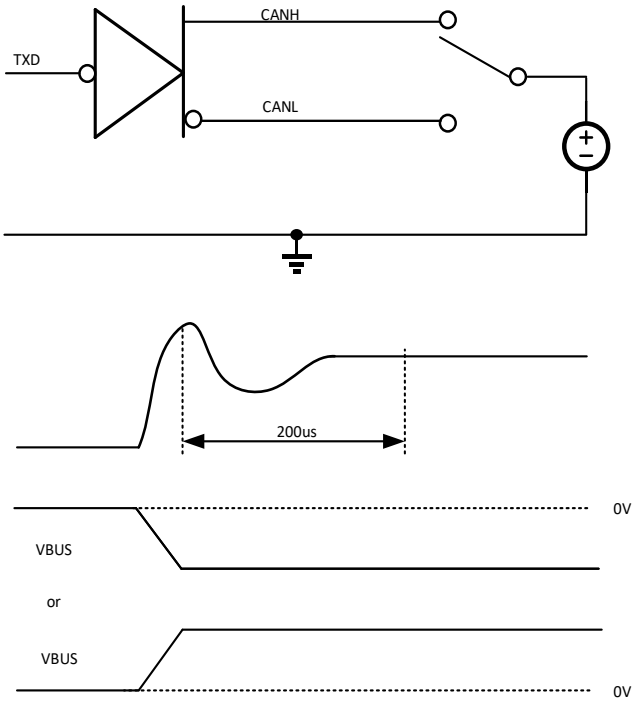


Figure7- 6 Driver Short Circuit Current Test Circuit and Measurement

8. Typical Operating Characteristics

Over recommended operating conditions, T_A = –40°C to 125°C (unless otherwise noted).

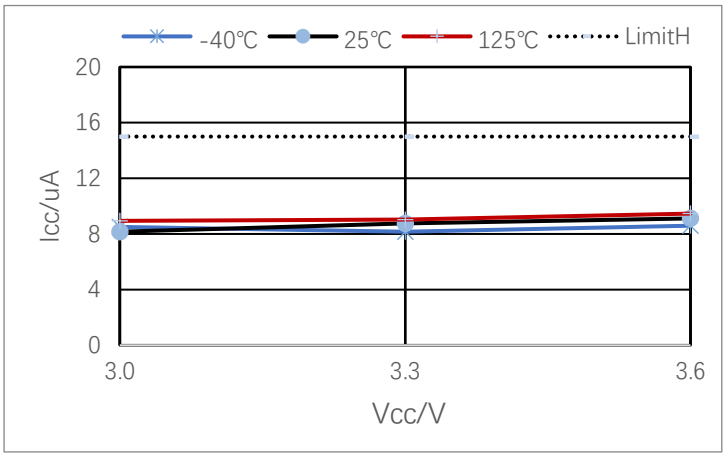


Figure 8-1 CA-IF1033S/ZS V_{CC} Supply Current @ Standby

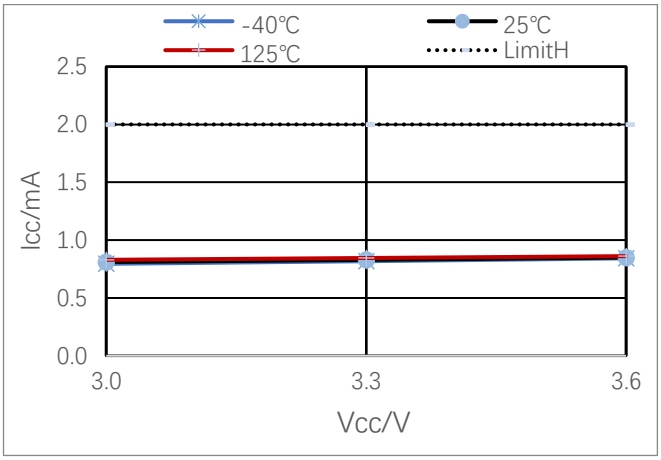


Figure 8-2 V_{CC} Supply Current @ Recessive

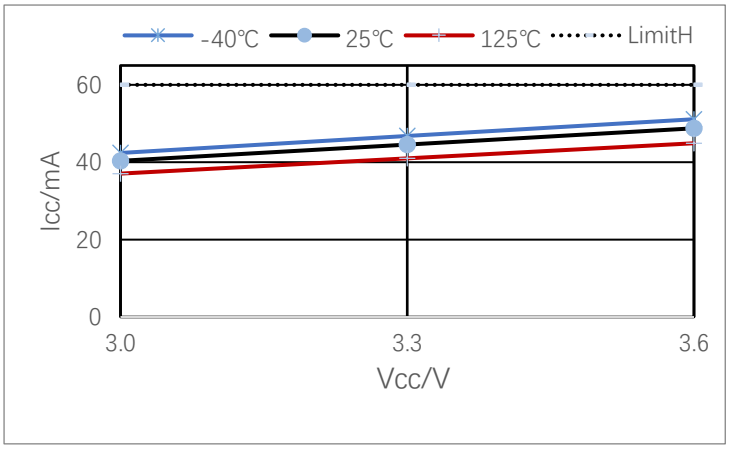


Figure 8-3 V_{CC} Supply Current @ Dominant (R_L = 50Ω)

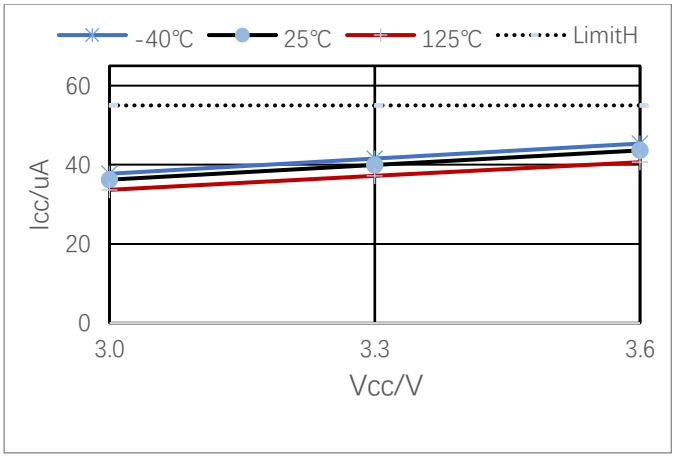


Figure 8-4 V_{CC} Supply Current @ Dominant (R_L = 60Ω)

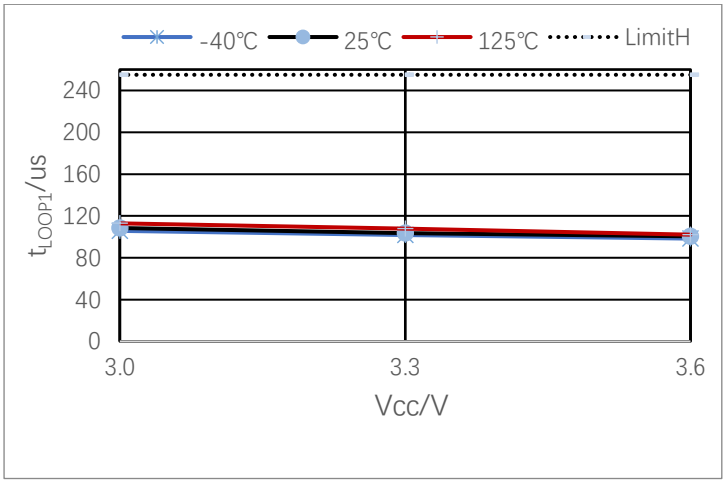


Figure 8-5 Total Loop Delay t_{LOOP1}

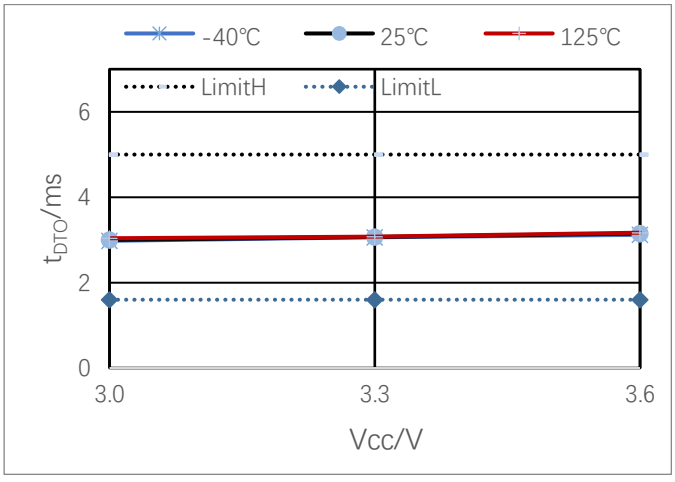


Figure 8-6 TXD-Dominant Timeout t_{DTO}

9. Detailed Description

The A-IF103x series complies with the ISO 11898-2 (2016) CAN (Controller Area Network) physical layer standard and can be directly connected to 3.3V controllers with CAN control protocols, supporting a CAN data rate of 1Mbps.

9.1. Operating Mode

The operating modes of CA-IF1030S and CA-IF1034S devices include conventional mode and Silent mode, among which CA-IF1034S also has relevant shutsdown mode; The operating modes of CA-IF1033S/ZS devices include normal mode, low-power standby mode, and shutdown mode.

9.1.1. CA-IF1030S/34S operating mode

The CA-IF1030S chip has two working modes: normal mode and silent mode, and the mode selection is controlled by the S pin.

The CA-IF1034S chip has three operating modes: normal mode, silent mode, and shutdown mode, with mode selection controlled by the EN and S pins.

Table 9- 1 CA-IF1030S Operating Mode Selction

S	Operating Mode	DRIVER	RECEIVER
L[1] or Floating	Normal	Enalble	Enabled
H[1]	Silent	OFF	Enalbled

Table 9- 2 CA-IF1034S Operating Mode Selction

EN[1]	S	Operating Mode	DRIVER	RECEIVER
H[1]	L[1] or Floating	Normal	Enalble	Enabled
H[1]	H[1]	Silent	OFF	Enalbled
L[1]	X[1]	Shutdown	OFF	OFF

Note： 1. X =Don't Care, H =High-Level, L = Low-Level;

Normal Mode

When the EN pin is high level, pull down or float the S pin, and the device is in normal operating mode. In this mode, the CAN driver and receiver are fully operational and CAN communication is bi-directional. The driver translates a digital input on TXD to a differential output on CANH and CANL. The receiver translates the differential signal from CANH and CANL to a single-ended output on RXD.

Silent Mode

The EN pin is high level, the S pin is set to high level, and the device is in silent mode. In this mode, this disables the transmitter regardless of the voltage level at TXD. However, The RXD is still active and monitors activity on the bus line.

Shutdown Mode (CA-IF1034S)

When the EN pin is low, the device will turn off all drivers and receivers, unable to communicate, and will not accept bus wake-up requests. In Shutdown mode, the bus is biased to ground.

9.1.2. CA-IF1033S/ZS operating mode

Table 9- 3 operating mode

SHDN	STB	Operating Mode	DRIVER	RECEIVER
L[1]	L[1] or Floating	Normal	Enalble	Enabled
L[1]	H[1]	Standby	OFF	Low-power receive channel is enabled and monitor the bus line.
H[1]	X[1]	Shutdown	OFF	OFF

Note:1. X =Don't Care, H =High-Level, L = Low-Level;

Normal Mode

When the SHDN pin is low level, pull down or float the STB pin, and the device is in normal operating mode. In this mode, the CAN driver and receiver are fully operational and CAN communication is bi-directional. The driver translates a digital input on TXD to a differential output on CANH and CANL. The receiver translates the differential signal from CANH and CANL to a single-ended output on RXD.

Standby Mode

When the SHDN pin is low level, pull up the STB pin for standby mode, which switches the transmitter off and disables the main receiver. The low-power receive channel is enabled and put the device to a low current and low-speed state. Thus the supply current is reduced during standby mode. The bus line is monitored by a low-power differential comparator to detect and recognize a wakeup event on the bus line

Shutdown Mode

When the SHDN pin is high level, the device will turn off all drivers and receivers, unable to communicate, and will not accept bus wake-up requests. In Shutdown mode, the bus is biased to ground.

9.2. CAN Bus Status

In normal/Silent mode, the CAN bus has two operating states: dominant and implicit, as shown in Figure9- 1.

The TXD pin is low, bus differential output, and RXD output is low in the dominant state. TXD is high, the bus is biased to the common mode voltage point by internal resistance, and RXD output is high in the recessive state.

For CA-IF1033S/ZS devices, when the SHDN pin is set to high level, the chip will enter low-power standby mode, and the bus will be biased to ground by internal resistance, as shown Figure9- 2.

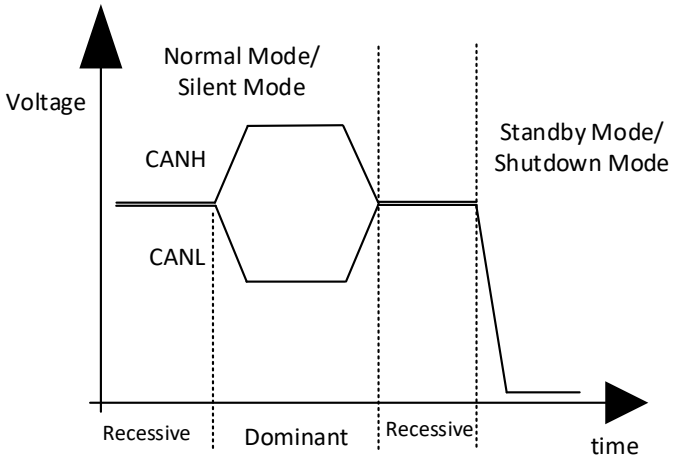


Figure9- 1 Bus Logic State Voltage Definition

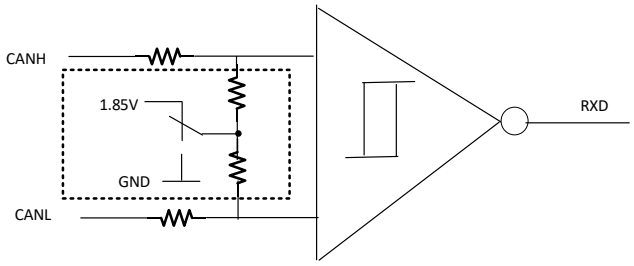


Figure9- 2 Receiver Input/Transmitter Output Bias Circuit

9.2.1. Transmitter

In normal operating mode, when the TXD input is high or floating, the bus output is in a positive state. When the TXD input is low, the bus output is in a dominant state.

Table 9- 4 Transmitter Truth Table

Device	INPUT	OUTPUT		Bus driver state
	TXD	CANH	CANL	
Normal Mode	L[1]	High	Low	Dominant
	High or Open	High-Z	High-Z	Recessive
Silent Mode (CA-IF1030S/ CA-IF1034S)	X[1]	High-Z	High-Z	Recessive
Standby Mode(CA-IF1033S/ZS)	X[1]	High-Z	High-Z	Weak pull-down to GND
Shutdwon Mode (CA-IF1033S/ZS、CA-IF1034S)	X[1]	High-Z	High-Z	Weak pull-down to GND

Note： 1. X =Don't Care, H =High-Level, L = Low-Level; Low level hold time not exceeding t_{DTO}

9.3. Receiver

The receiver of CA-IF103x family of devices includes a main receiver to support normal bi-directional communication. and CA-IF1033S/ZS has a low-power receiving channel for monitoring the bus and detecting wake-up events on the bus during standby mode

In normal/Silent operation, the main receiver reads the differential input from the bus line (CANH and CANL) and transfers this data as a single-ended output RXD to the CAN controller. The internal comparator senses the difference voltage V_{DIFF} = (V_{CANH}-V_{CANL}), with respect to an internal threshold. If V_{DIFF} > 0.9V, a logic-low is present on RXD; If V_{DIFF} < 0.5V, a logic-high is present. The CANH and CANL common-mode range is ±18V in normal mode.

Drive the CA-IF1033S/ZS STB pin high, in this case, the main receiver is disabled and the low-power receive channel is enabled. This switches the receiver to a low current and low-speed state. The bus line is monitored by a low-power differential comparator to detect and recognize a wakeup event on the bus line. The RXD logic High until a valid wake-up is received. Once a valid remote wake-up event occurred, RXD transition to logic Low.

The RXD is a logic-high when CANH and CANL are shorted or floating and un-driven see Table 9- for more details about the receiver truth table.

Table 9- 5 Receiver Truth Table

DEVICE MODE	$V_{ID} = V_{CANH}-V_{CANL}$	BUS STATE	RXD
Normal /Silent	$V_{ID} \geq 0.9V$	Dominant	Low
	$0.5V < V_{ID} < 0.9V$	Indeterminate	Indeterminate
	$V_{ID} \leq 0.5V$	Recessive	High
Standby	$V_{ID} > 1.15V$	Dominant	Low if a remote wake event occurred, otherwise output High.
	$0.4V < V_{ID} < 1.15V$	Indeterminate	Indeterminate
	$V_{ID} \leq 0.4V$	Recessive	High
Shutdown	X[1]	Recessive	High

Note： 1. X =Don't Care,

9.4. Transmitter-Dominant Timeout

The CA-IF103x family of devices features a transmitter-dominant timeout (t_{DOM}) that prevents erroneous CAN controllers from clamping the bus to a dominant level by maintaining a continuous low TXD signal. When TXD remains in the dominant state (low) for greater than t_{DOM}, the transmitter is disabled, releasing the bus to a recessive state. After a dominant timeout fault, the transmitter is re-enabled when receiving a rising edge at the TXD. The transmitter-dominant timeout limits the minimum possible data rate to 6.25kbps.

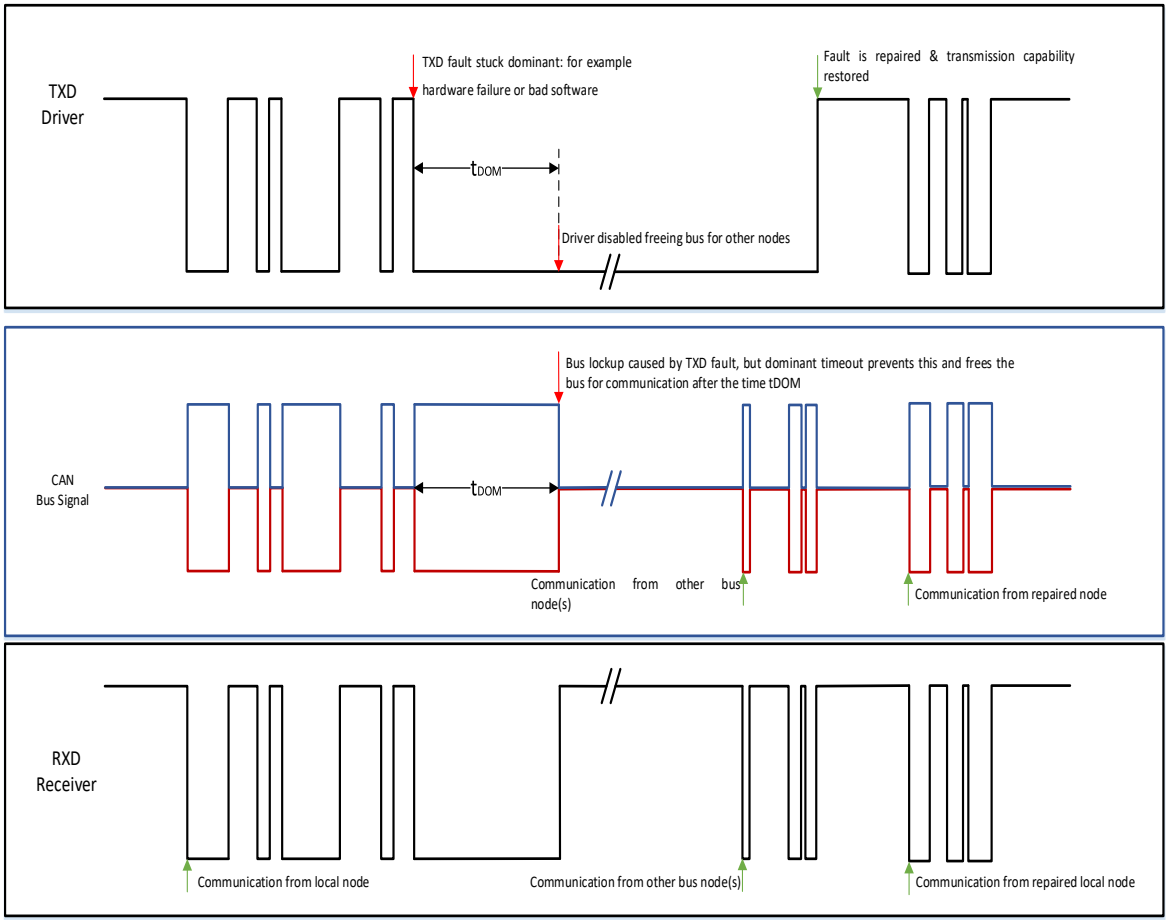


Figure9- 3 Transmitter-Dominant Timeout Protection

9.5. Undervoltage Lockout

The CA-IF103x devices have undervoltage detection on V_{CC} supply terminal, that place the device in protected mode during an undervoltage event on V_{CC}.

If the supply voltage V_{CC} is less than UV_{VCC}-, will put the device into protected state and leave the bus in high-impedance as shown in Table 9- 2. Once an undervoltage condition is cleared on V_{CC} and the supply voltage has returned to a valid level.

Table 9- 2 Undervoltage Lockout

V_{CC}	Device state	BUS Output[1]	RXD
>UVvcc+	Normal	Per TXD	Mirrors Bus
<UVvcc-	Protected mode	High-Z	High-Z

Note: 1. The table only lists the status of BUS Output in normal mode to introduce the undervoltage protection function.

9.6. Fault Protection

The CA-IF103x devices has an internal ±18V overvoltage protection circuit on the driver output and receiver input to protect the devices from accidental shorts between a local power supply and the data lines of the transceivers. This level of protection is present whether the transceiver is powered or un-powered.

9.7. Thermal Shutdown

If the junction temperature of the devices exceeds the thermal shutdown threshold T_{TSD} (170°C), the device turns off the CAN driver circuits thus blocking the TXD-to-bus transmission path. The CAN bus terminals are biased to the recessive level during a thermal shutdown, and the receiver-to-RXD path remains operational. The shutdown condition is cleared when the junction temperature drops at least the thermal shutdown hysteresis temperature below the thermal shutdown threshold.

9.8. Unpowered Device

The device is designed to be 'ideal passive' or 'no load' to the CAN bus if it is unpowered. The bus terminals (CANH, CANL) have extremely low leakage currents when the device is unpowered to avoid loading down the bus.

9.9. Input Pins Floating Terminals

When the TXD pin is floating, the device is pulled up to the power supply internally, causing the bus output to be in a hidden state;

When the enable EN (CA-IF1034S) pin is floating, the device is pulled up to the power supply internally, causing the device to be in an enabled state;

When the enable EN (CA-IF1033S/CA-IF1033ZS) pin is floating, the device is pulled up to the power supply internally, causing the device to be in an enabled state;

When the S/STB pin is floating, the device is pulled down to GND internally, causing the device to be in normal mode.

9.10. Remote wakeup

To improve the system operation reliability and to prevent false wake-up, the CA-IF1033S/ZS devices' receiver features wake-up timeout detection and filtered dominant wake-up detection according to the ISO 11898-2:2016 standard. This means, for a dominant or recessive to be considered, the bus must be kept in that state for more than the t_{WK_FILTER} time. Also, for a remote wake-up event to successfully occur, a dominant bus level greater than t_{WK_FILTER} must be detected and received by the low-power receive channel within the timeout value $t \leq t_{WK\_TIMEOUT}$. Once the low-power receive channel detects a successful wake-up event, RXD pulls low. CAN controller can drive the STB low based on this wake-up signal from RXD for normal operation. RXD is high until a valid wake-up is received during standby mode, see Figure 9-4 for more details.

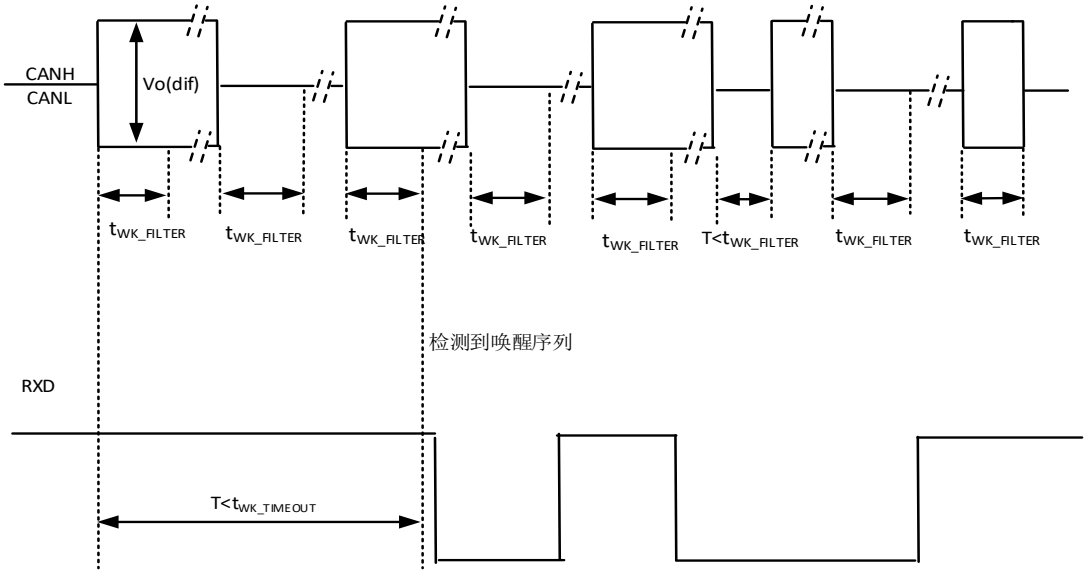


Figure9- 4 Wake-up Detection

10. Application Information

The CA-IF103x CAN transceivers are typically used in applications with a host microprocessor or FPGA that includes the data link layer portion of the CAN protocol. The V_{CC} power supply of CA-IF103x is directly connected to the power supply of MCU,as shown in Figure10- 1 and Figure10- 2.

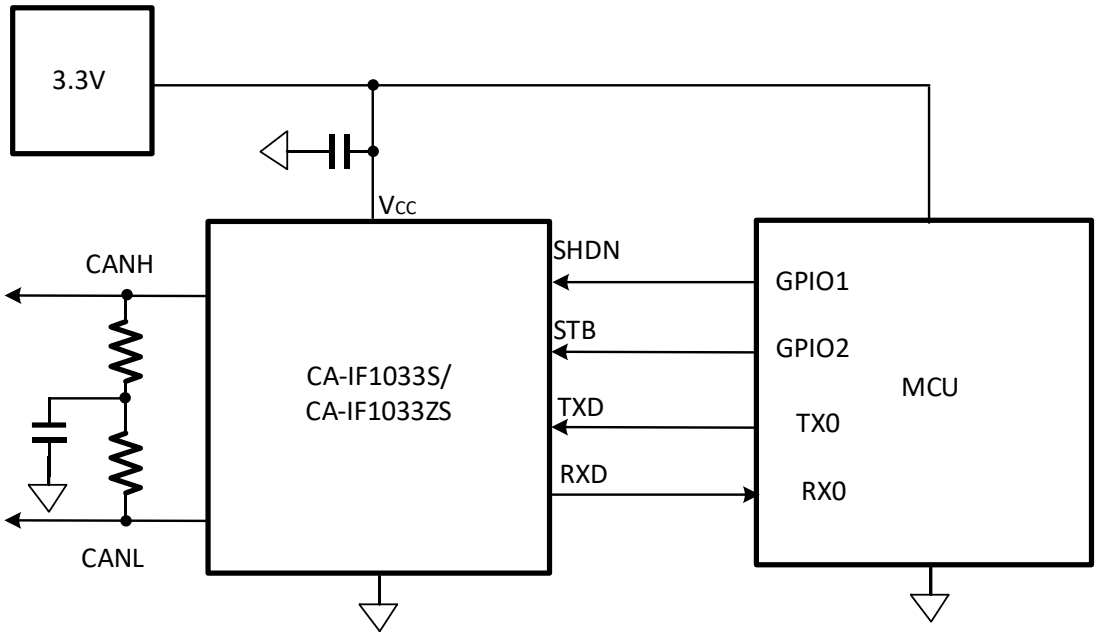


Figure10- 1 Typical Application Circuit for the CA-IF1033S/ZS-Q1

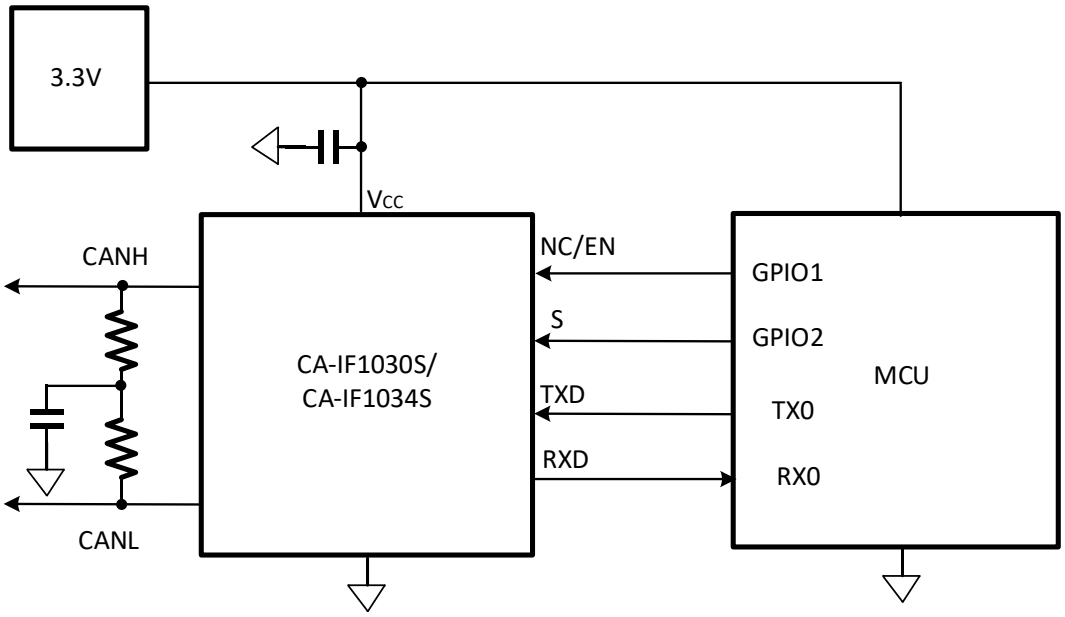
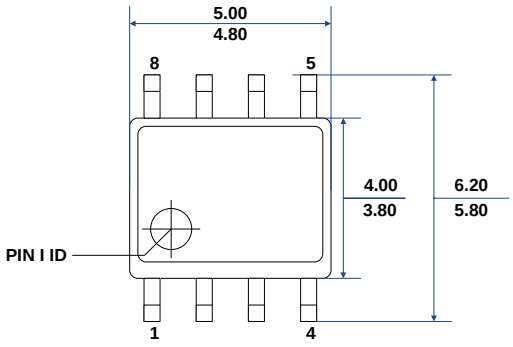


Figure10- 2 Typical Application Circuit for the CA-IF1030S/CA-IF1034S

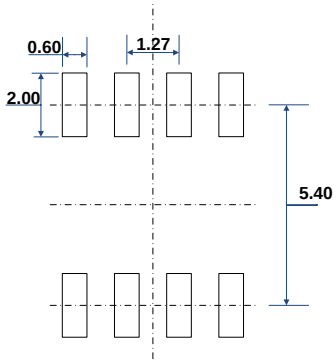
11. Package Information

11.1. SOIC8 Package Outline

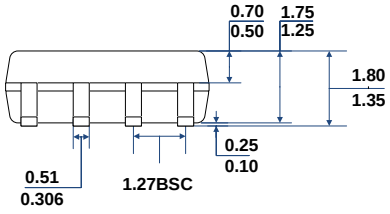
Package size diagram of SOT23-8, dimensions in millimeters.



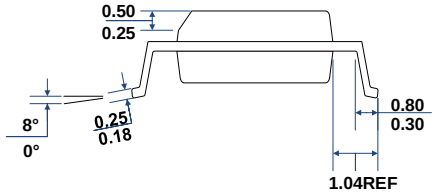
TOP VIEW



RECOMMENDED LAND PATTERN



FRONT VIEW



LEFT-SIDE VIEW

Note:

1. Controlling dimensions are in millimeters.

Figure 11-1 SOIC8 Package Outline

11.2. SOT23-8 Package Outline

Package size diagram of SOT23-8, dimensions in millimeters.

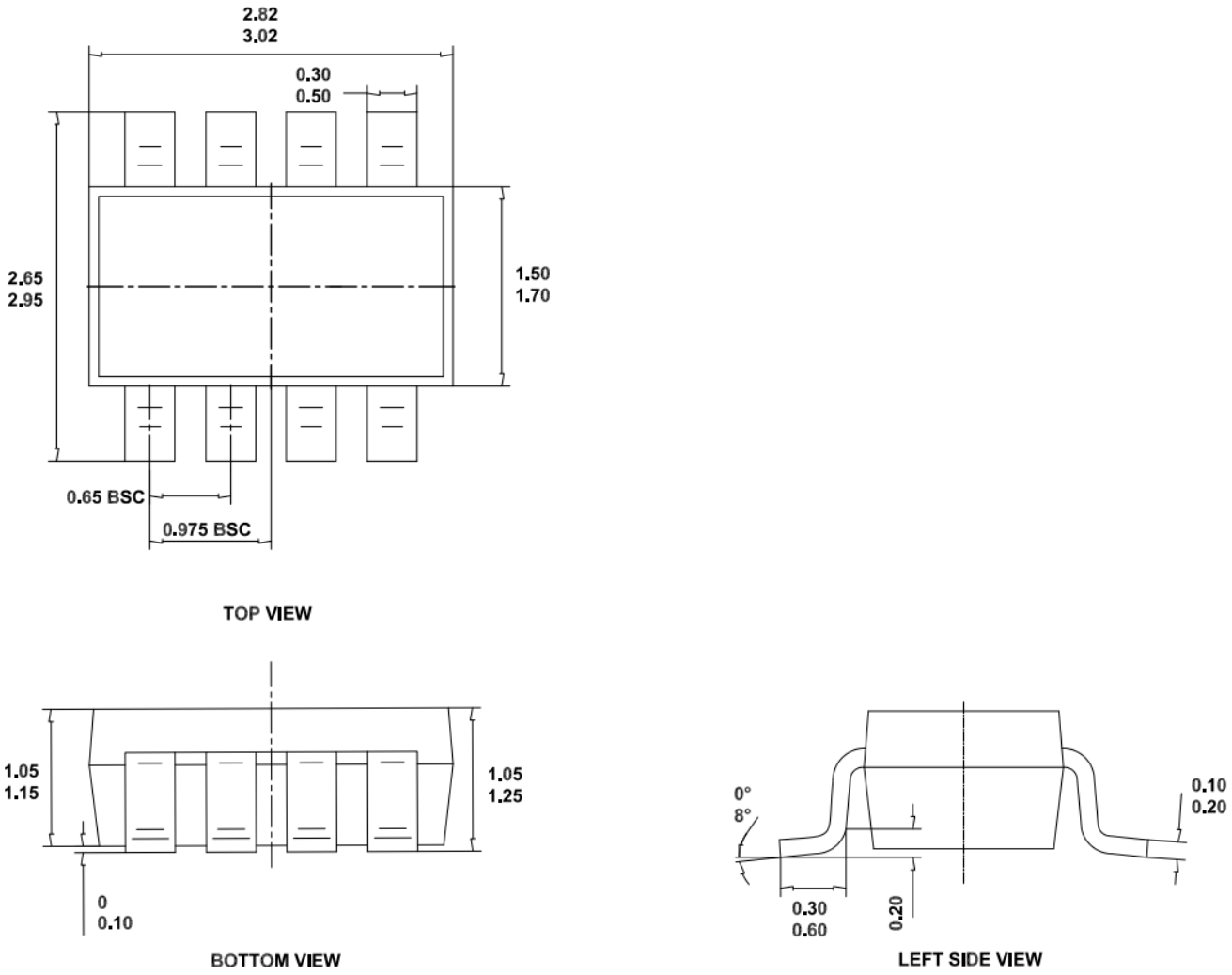


Figure 11-2 SOT23-8 Package Outline

12. Soldering Temperature (reflow) Profile

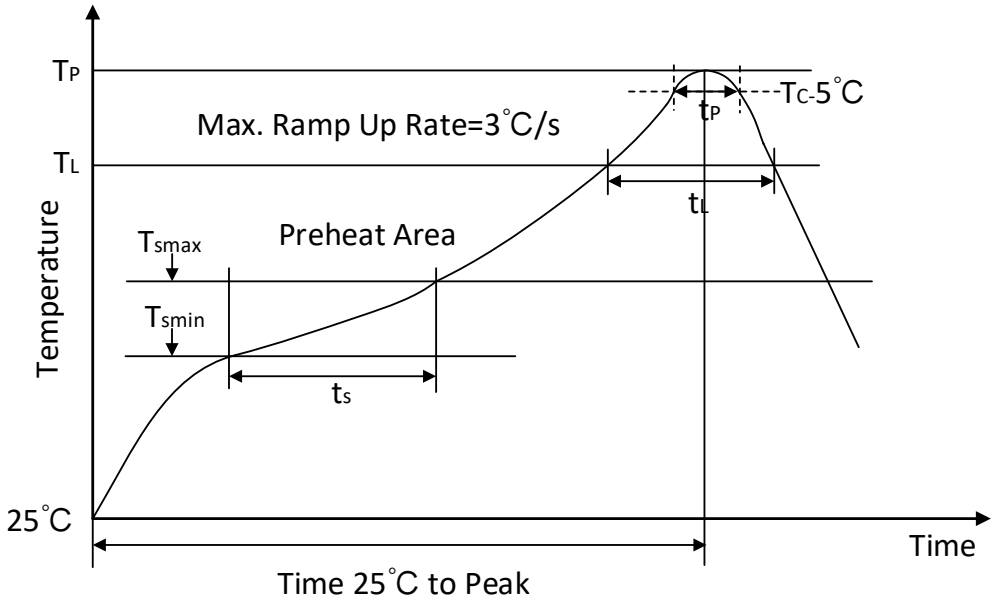


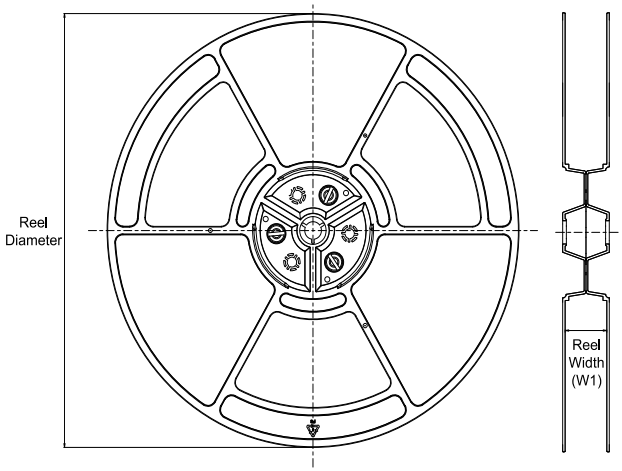
Figure 12- 1 Soldering Temperature (reflow) Profile

Table12- 1 Soldering Temperature Parameter

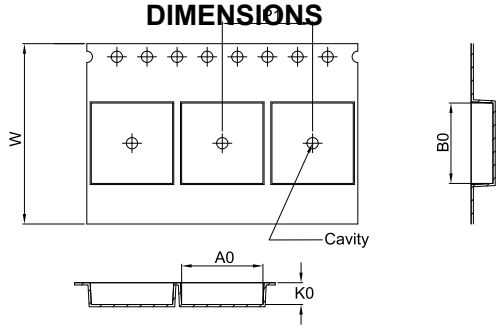
Profile Feature	**Pb-Free Assembly**
Average ramp-up rate(217 ℃ to Peak)	3℃/second max
Time of Preheat temp(from 150 ℃ to 200 ℃	60-120 second
Time to be maintained above 217 ℃	60-150 second
Peak temperature	260 +5/-0 ℃
Time within 5 ℃of actμAl peak temp	30 second
Ramp-down rate	6 ℃/second max.
Time from 25℃ to peak temp	8 minutes max

13. Tape and Reel Information

REEL DIMENSIONS

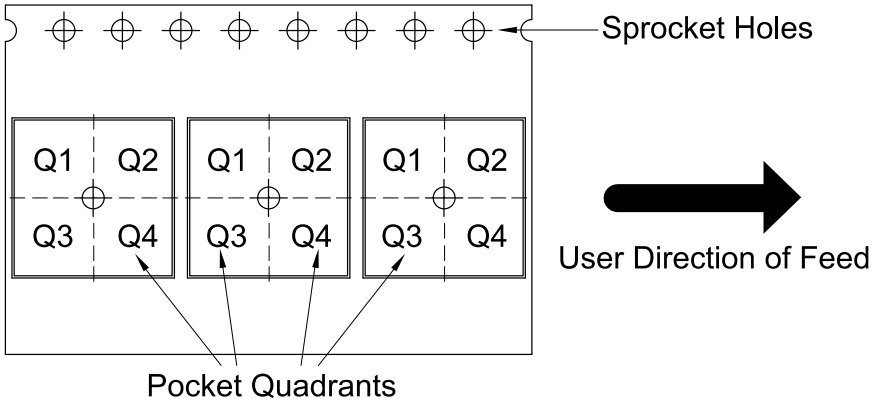


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 QμAdrant
CA-IF1030S	SOIC	S	8	2500	330	12.4	6.4	5.4	2.1	8.0	12.0	Q1
CA-IF1033S	SOIC	S	8	2500	330	12.4	6.4	5.4	2.1	8.0	12.0	Q1
CA-IF1033ZS	SOT23	ZS	8	3000	178	9.5	3.23	3.17	1.37	4.0	8.0	Q3
CA-IF1034S	SOIC	S	8	2500	330	12.4	6.4	5.4	2.1	8.0	12.0	Q1

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