15A Sink/Source, Single-Channel, Reinforced Isolated SiC/IGBT Gate Driver

1. Features

- Up to 33V Output Drive Supply Range(V_{DD}-V_{EE}) with 12V VDD UVLO Detection
- 15A Sink/Source Peak Current
- Drive High-power SiC MOSFET and IGBT with up to 2121 V_{PK} Operating Voltage
- Feature selections:
  - Integrated Miller Clamp (CA-IS3213MCG)
  - UVLO refer to COM (CA-IS3213VCG)
  - Split output (CA-IS3213SCG)
- Propagation Delay:
  - 130ns propagation delay (maximum)
  - 30ns pulse width distortion (maximum)
  - 30ns part to part skew (maximum)
- Robust Galvanic Isolation:
  - High lifetime: >40 years
  - Up to 5.7kV_{RMS} isolation rating
  - CMTI > ±150kV/μs
- 8-pin Wide-body SOIC Package with Creepage and Clearance >8mm
- Operating Temperature (T_J): -40°C to +150°C
- Safety regulatory approvals:
  - VDE Reinforced isolation per DIN EN IEC 60747-17 (VDE 0884-17): 2021-10
  - UL certification per UL 1577 for 1 minute
  - CQC certification per GB 4943.1-2022

2. General Description

The CA-IS3213 is a series of capacitive isolation based single-channel gate drivers for driving SiC, IGBT and MOSFET devices. The devices offer excellent dynamic performance and high reliability, as well as Sink/Source peak current capability up to ±15A.

The devices are electrically isolated from the control and driver sides by SiO_2 capacitive isolation technology, supporting an isolated operating voltage of 1.5kV_{RMS}, 12.8kV_{PK} surge immunity, and a rated gate life of more than 40 years at rated operating voltages, as well as good device consistency and common-mode transient immunity (CMTI) of >150kV/μs.

The device controls and drives side power UVLOs while being optimized for SiC and IGBT switching behavior and improved reliability. In addition, the CA-IS3213MCG has a built-in 4A peak current active Miller clamp; the CA-IS3213VCG has an external COM pin for easy isolation of the positive and negative driver-side power supplies; and the CA-IS3213SCG utilizes a split output configuration of OUTH and OUTL.

The entire series is packaged in a SOIC8-WB wide body package with creepage and clearance distances greater than 8mm.

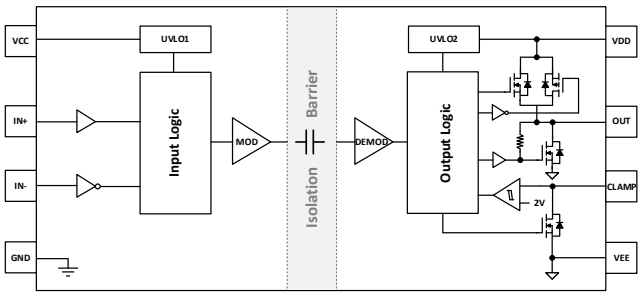
3. Applications

- UPS and PSU
- Solar Inverters
- Motor Drives

Device Information

Part Number	Package	Package Size (Nominal Value)
CA-IS3213MCG	SOIC8-WB(G)	7.5mm x 5.85mm
CA-IS3213VCG	SOIC8-WB(G)	7.5mm x 5.85mm
CA-IS3213SCG	SOIC8-WB(G)	7.5mm x 5.85mm

Simplified Schematic



4. Ordering Information

Table 4-1. Ordering Information

Part Number	Function selections	Package
CA-IS3213MCG	Integrated 4A active miller clamp	SOIC8-WB(G)
CA-IS3213VCG	UVLO refer to COM, Suitable for positive and negative power supplies	SOIC8-WB(G)
CA-IS3213SCG	Split gate output (OUTH and OUTL)	SOIC8-WB(G)

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5. Revision History

Revision Number	Description	Revised Date	Page Changed
Version 1.0	N/A	2024.08.22	N/A

6. Pin Configuration and Description

6.1. CA-IS3213MCG Pin Configuration

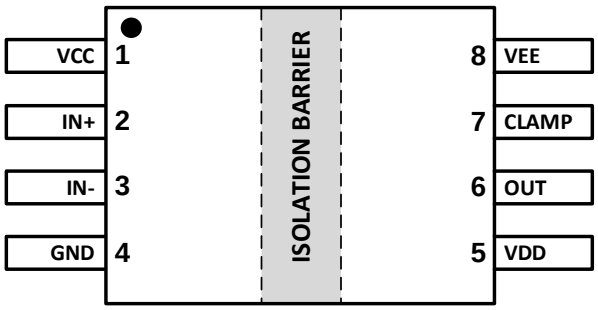


Figure 6-1. CA-IS3213MCG Pin Configuration

Table 6-1. CA-IS3213MCG Pin Description

Pin Name	Pin Number	Type[1]	Description
VCC	1	P	3.0V o 5.5V power supply input for control-side. Bypass VCC to GND with at least 1μF ceramic capacitor as close as possible to VCC pin.
IN+	2	I	Non-inverting driver input on control-side. It has internal pulldown to GND.
IN–	3	I	Inverting driver input on control-side. It has internal pullup to VCC.
GND	4	G	Ground reference for control-side.
VDD	5	P	Positive power supply input for gate driver. Bypass VDD to COM with at least 10μF capacitor as close as possible to the pin VDD.
OUT	6	O	Gate drive output.
CLAMP	7	I	Internal active Miller clamp input. Connect CLAMP to the gate of the power MOSFET.
VEE	8	P	Negative power supply input for gate driver. Bypass VEE to COM with at least 10μF capacitor as close as possible to the pin VEE.

Note:
1. P = power supply, G = GND, I = input, O = output

6.2. CA-IS3213VCG Pin Configuration

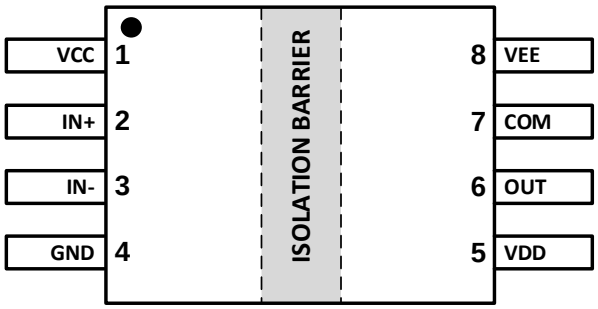


Figure 6-2. CA-IS3213VCG Pin Configuration

Table 6-2. CA-IS3213VCG Pin Description

Pin Name	Pin Number	Type[1]	Description
VCC	1	P	3.0V o 5.5V power supply input for control-side. Bypass VCC to GND with at least 1μF ceramic capacitor as close as possible to VCC pin.
IN+	2	I	Non-inverting driver input on control-side. It has internal pulldown to GND.
IN–	3	I	Inverting driver input on control-side. It has internal pullup to VCC.
GND	4	G	Ground reference for control-side.
VDD	5	P	Positive power supply input for gate driver. Bypass VDD to COM with at least 10μF capacitor as close as possible to the pin VDD.
OUT	6	O	Gate drive output.
COM	7	P	Reference Ground at drive side.
VEE	8	P	Negative power supply input for gate driver. Bypass VEE to COM with at least 10μF capacitor as close as possible to the pin VEE.

Note:
2. P = power supply, G = GND, I = input, O = output

6.3. CA-IS3213SCG Pin Configuration

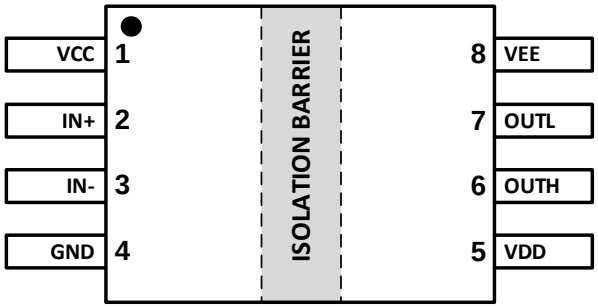


Figure 6-3. CA-IS3213SCG Pin Configuration

Table 6-3. CA-IS3213SCG Pin Description

Pin Name	Pin Number	Type[1]	Description
VCC	1	P	3.0V o 5.5V power supply input for control-side. Bypass VCC to GND with at least 1μF ceramic capacitor as close as possible to VCC pin.
IN+	2	I	Non-inverting driver input on control-side. It has internal pulldown to GND.
IN–	3	I	Inverting driver input on control-side. It has internal pullup to VCC.
GND	4	G	Ground reference for control-side.
VDD	5	P	Positive power supply input for gate driver. Bypass VDD to COM with at least 10μF capacitor as close as possible to the pin VDD.
OUTH	6	O	Gate drive pull-up output.
OUTL	7	O	Gate drive pull-down output.
VEE	8	P	Negative power supply input for gate driver. Bypass VEE to COM with at least 10μF capacitor as close as possible to the pin VEE.

Note:

3. P = power supply, G = GND, I = input, O = output

7. Specifications

7.1. Absolute Maximum Ratings[1]

Over operating free-air temperature range unless otherwise specified.

Parameters		Minimum	Maximum	Unit
VCC	VCC–GND	–0.3	6	V
VDD	VDD–COM	–0.3	36	V
VEE	VEE–COM	–17.5	0.3	V
V_{MAX}	VDD–VEE	–0.3	36	V
IN+, IN–	DC	GND–0.3	VCC	V
OUTH, OUTL, CLAMPI	DC	VEE–0.3	VDD	V
T_J	Junction temperature	–40	150	°C
T_{stg}	Storage temperature	–65	150	°C

Notes:

1. The stresses listed under "Absolute Maximum Ratings" are stress ratings only, not for functional operation condition. Exposure to absolute maximum rating conditions for extended periods may cause permanent damage to the device.
2. Bench test result.

7.2. ESD Ratings

		Value	Unit
V_{ESD} Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001	±3000	V
	Charged device model (CDM), per JESD22-C101 (All Pins)	±2000	

7.3. Recommended Operating Conditions

Over operating free-air temperature range unless otherwise specified.

Parameters			Minimum	Maximum	Unit
VCC	VCC–GND		3.0	5.5	V
VDD	VDD–COM		13	33	V
VMAX	VDD–VEE		–	33	V
IN+, IN–	Referenced to GND.	Logic-high input	$0.7xV_{CC}$	V_{CC}	V
		Logic-low input	0	$0.3×V_{CC}$	
T_A	Junction temperature		–40	125	°C
T_J	Ambient temperature		–40	150	°C

7.4. Thermal Information

Thermal Metric		SOIC8-WB	Unit
$R_{\theta JA}$	Junction-to-ambient thermal resistance	110.1	°C/W

7.5. Power Ratings

Parameters		Test Conditions	Typical Value	Unit
P_D	Maximum input and output power dissipation	VCC=5V, VDD–COM=20V, COM–VEE=5V, IN+/IN– = 5V, 150kHz square wave with 50% duty cycle, C_L = 10Nf, T_A=25°C	982.5	mW
P_{D1}	Maximum input power dissipation		17.5	mW
P_{D2}	Maximum output power dissipation		965	mW

7.6. Insulation Specifications

Parameters		Test Conditions	Specifications	Unit
			G	
CLR	External clearance	Shortest terminal-to-terminal distance through air	8	mm
CPG	External creepage	Shortest terminal-to-terminal distance across the package surface	8	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	> 24	μm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11)； IEC 60112	> 600	V
	Material group	According to IEC 60664-1	I	
	IEC 60664-1 over-voltage category	Rated mains voltage ≤ 300 V_{RMS}	I-IV	
		Rated mains voltage ≤ 600 V_{RMS}	I-IV	
		Rated mains voltage ≤ 1000 V_{RMS}	I-III	
DIN V VDE V 0884-11:2021-10[1]				
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	2121	V_{PK}
V_{IOWM}	Maximum operating isolation voltage	AC voltage; time-dependent dielectric breakdown (TDDB) test	1500	V_{RMS}
		DC voltage	2121	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t=60 s (qualification);	8000	V_{PK}
		$V_{TEST} = 1.2 \times V_{IOTM}$, t=1 s (100% product test)	9600	
V_{IOSM}	Maximum surge isolation voltage[2]	Test method per IEC 62368-1, 1.2/50 μs waveform, $V_{TEST} = 1.6 \times V_{IOSM}$	8000	V_{PK}
q_{pd}	Apparent charge[3]	Method a, after input/output safety tests subgroup 2/3, $V_{ini} = V_{IOTM}$, t_{ini} = 60s; $V_{pd(m)} = 1.2 \times V_{IORM}$, t_m = 10s	≤5	pC
		Method a, after environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, t_{ini} = 60s; $V_{pd(m)} = 1.6 \times V_{IORM}$, t_m = 10s	≤5	
		Method b1, at routine test (100% production test) and preconditioning (sample test) $V_{ini} = 1.2 \times V_{IOTM}$, t_{ini} = 1s; $V_{pd(m)} = 1.875 \times V_{IORM}$, t_m = 1s	≤5	
C_{IO}	Barrier capacitance, input to output[4]	V_{IO} = 0.4 × sin (2πft), f = 1 MHz	~1	pF
R_{IO}	Isolation resistance , input to output[4]	V_{IO} = 500 V, T_A = 25°C	$>10^{12}$	Ω
		V_{IO} = 500 V, 100°C ≤ T_A ≤ 125°C	$>10^{11}$	
		V_{IO} = 500 V at T_S = 150°C	$>10^{9}$	
	Pollution degree		2	
	Climatic category		40/125/21	
UL 1577				
V_{ISO}	Maximum isolation voltage	$V_{TEST} = V_{ISO}$, t = 60 s (certified) $V_{TEST} = 1.2 \times V_{ISO}$, t = 1 s (100% production test)	5700	V_{RMS}

Notes:

1. This coupler is suitable for “safe electrical insulation” only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
2. Devices are immersed in oil during surge characterization.
3. The characterization charge is discharging charge (pd) caused by partial discharge.
4. Capacitance and resistance are measured with all pins on field-side and logic-side tied together.

7.7. Safety-Related Certifications

VDE	UL	CQC
Certified according to DIN EN IEC 60747-17 (VDE 0884-17):2021-10; EN IEC 60747-17: 2020+AC:2021	Certified according to UL 1577 Component Recognition Program	Certified according to GB4943.1-2022
Reinforced isolation(SOIC8-WB): Maximum transient isolation voltage: 8000V_{pk} Maximum repetitive-peak isolation voltage: 2121 V_{pk} Maximum surge isolation voltage: 8000V_{pk}	Protection voltage: - 5700V_{RMS} for SOIC8-WB packages	Reinforced insulation for SOIC8-WB
Certificate number: 40057278	Certificate number: Pending	Certificate number: CQC23001406424

7.8. Safety Limits

Parameters		Test Conditions	Minimum	Typical	Maximum	Unit
I_S	Safety input, output or supply current	$R_{\theta JA}$=110.1°C/W, VDD=15V, VEE=–5V, T_J=150°C, T_A=25°C			56	mA
		$R_{\theta JA}$=110.1°C/W, VDD=20V, VEE=–5V, T_J=150°C, T_A=25°C			45	
P_S	Safety power dissipation	$R_{\theta JA}$=110.1°C/W, VDD=20V, VEE=–5V, T_J=150°C, T_A=25°C			1135	mW
T_S	Maximum safety temperature				150	℃

7.9. Electrical Characteristics

V_{CC} = 3.3V or 5V, connect a 1μF bypass capacitor between VCC and GND; VDD-COM = 20V, 18V or 15V; COM–VEE=0V, 5V, 8V or 15V; C_L=100pF; -40°C < T_J < +150°C, unless otherwise noted. Typical values are at T_A = +25°C, unless otherwise noted.[1, 2]

Parameters		Test Conditions	Minimum	Typical	Maximum	Unit
VCC UVLO threshold and delay						
V_{VCC_ON}	VCC raising	VCC–GND	2.55	2.7	2.85	V
V_{VCC_OFF}	VCC falling		2.35	2.5	2.65	
V_{VCC_HYS}	Undervoltage-lockout threshold hysteresis			0.2		
t_{VCCFIL}	VCC UVLO detection deglitch time			5		μs
$t_{VCC+ \text{ to } OUT}$	VCC power up delay, UVLO raising to output high	IN+=VCC, IN–=GND		30	70	
$t_{VCC- \text{ to } OUT}$	VCC power down delay, UVLO falling to output low			7	15	
VDD UVLO threshold and delay						
V_{VDD_ON}	VDD raising	VDD–COM	11.0	12.0	13.0	V
V_{VDD_OFF}	VDD falling		10.0	11.0	12.0	
V_{VDD_HYS}	Undervoltage-lockout threshold hysteresis			1.0		
t_{VDDFIL}	VDD UVLO detection deglitch time			5		μs
$t_{VDD+ \text{ to } OUT}$	VDD power up delay, UVLO raising to output high	IN+=VCC, IN–=GND		7	15	
$t_{VDD- \text{ to } OUT}$	VDD power down delay, UVLO falling to output low			7	15	
VCC, VDD supply current						
I_{VCCQ}	V_{CC} quiescent current	OUT(H)=high	1.4	2.3	3.5	mA
		OUT(L)=low	0.8	1.5	2.3	
I_{VDDQ}	V_{DD} quiescent current	OUT=high/low	2.5	3.7	5.3	
Logic input: IN+, IN–						
V_{INH}	Logic-high input voltage	VCC=3.3V		1.85	2.31	V
V_{INL}	Logic-low input voltage		0.99	1.52		V
V_{INHYS}	Input hysteresis			0.33		V
I_{IH}	Logic-high input leakage	V_{IN}=VCC	70	90	110	μA
I_{IL}	Logic-low input leakage	V_{IN}=GND	–110	–90	–70	μA
R_{IND}	Input pulldown resistance	IN+ refer to GND	42	55	68	kΩ
R_{INU}	Input pullup resistance	IN– refer to VCC	42	55	68	kΩ
t_{INFIL}	IN+, IN–, input deglitch time (rising or falling)	f =50kHz, see Figure 8-3, Figure 8-4		40		ns
Gate driver						
I_{OUTH}	Peak sourcing current	C_{VDD}=10μF, C_L=0.18μF, f_S=1kHz	10	15		A
I_{OUTL}	Peak sink current	C_{VEE}=10μF, C_L=0.18μF, f_S=1kHz	10	15		A
R_{OUTH}	Pullup resistance	I_{OUT}=–0.1A		1.6		Ω
R_{OUTL}	Pulldown resistance	I_{OUT}=0.1A		0.23		Ω
V_{OUTH}	Output high voltage	I_{OUT}=–0.2A, VDD=18V		17.6		V
V_{OUTL}	Output low voltage	I_{OUT}=0.2A		50		mV
Active pulldown						
V_{OUTPD}	Active pulldown, OUTH, OUTL	I_{OUTL} =1A, VDD=OPEN, VEE=COM		2.0		V

Notes:

1. Inflow current is positive and outflow current is negative.

All voltage is referenced to COM unless otherwise noted.

Electrical Characteristics (continued)

V_{CC} = 3.3V or 5V, connect a 1μF bypass capacitor between VCC and GND; VDD-COM = 20V, 18V or 15V; COM–VEE=0V, 5V, 8V or 15V; C_L=100pF; -40°C < T_J < +150°C, unless otherwise noted. Typical values are at T_A = +25°C, unless otherwise noted. [1, 2]

Parameters		Test Conditions	Minimum	Typical	Maximum	Unit
Internal active Miller clamp (CA-IS3213MCG only)						
$V_{CLAMPTH}$	Miller clamp threshold	Referenced to VEE	1.5	2.0	2.5	V
V_{CLAMP}	Low-level output clamp voltage	I_{CLAMPI} =1A		VEE+0.4		V
I_{CLAMP}	Low-level output clamp current	V_{CLAMPI}=0V, VEE=–4V		4		A
R_{CLAMPI}	Miller clamp pulldown resistance	I_{CLAMPI} =0.2A		0.4		Ω
$t_{DCLAMPI}$	Miller clamp delay time	C_L=1.8nF, see Figure 8-5		20		ns
Short-circuit clamp						
$V_{CLP - OUT}$	$V_{OUT(H)}$ – VDD	OUT = High, $I_{OUT(H)}$ = 500mA, t_{CLP} = 10μs		0.73		V
$V_{CLP - CLAMP}$	V_{CLAMP} – VDD	OUT = High, I_{CLAMP} = 500mA, t_{CLP} = 10μs		1.3		V

Notes:
1. Inflow current is positive and outflow current is negative.
2. All voltage is referenced to COM unless otherwise noted.

7.10. Switching Characteristics

V_{CC} = 3.3V or 5V, connect a 1μF bypass capacitor between VCC and GND; VDD-COM = 20V, 18V or 15V; COM–VEE=0V, 5V, 8V or 15V; C_L=100pF; -40°C < T_J < +150°C, unless otherwise noted. Typical values are at T_A = +25°C, unless otherwise noted.

Parameters		Test Conditions	Minimum	Typical	Maximum	Unit
t_{PDHL}	Propagation delay, high to low	See Figure 8-1, Figure 8-2	60	90	130	ns
t_{PDLH}	Propagation delay, low to high		60	90	130	
PWD	Pulse width distortion |t_{PDHL}-t_{PDLH}|	See Figure 8-1, Figure 8-2			30	
t_{sk-pp}	Part to part skew	Propagation delay(rising and falling)			30	
t_r	Driver output rise time	C_L=10nF, see Figure 8-1		30		
t_f	Driver output fall time	C_L=10nF, see Figure 8-1		30		
f_{MAX}	Maximum switching frequency				1	MHz
CMTI	Common mode noise immunity	IN+=High, IN-=Low, see Figure 8-8, Figure 8-9, Figure 8-10	150			kV/μs
		IN+=Low, IN-=Low, see Figure 8-8, Figure 8-9, Figure 8-10	150			

Notes:
1. Inflow current is positive and outflow current is negative.
2. All voltage is referenced to COM unless otherwise noted.

7.11. Typical Characteristics

V_{CC} = 3.3V or 5V, connect a 1μF bypass capacitor between VCC and GND; VDD-COM = 20V, 18V or 15V; COM–VEE=0V, 5V, 8V or 15V; C_L=100pF; -40°C < T_J < +150°C, unless otherwise noted. Typical values are at T_A = +25°C, unless otherwise noted.

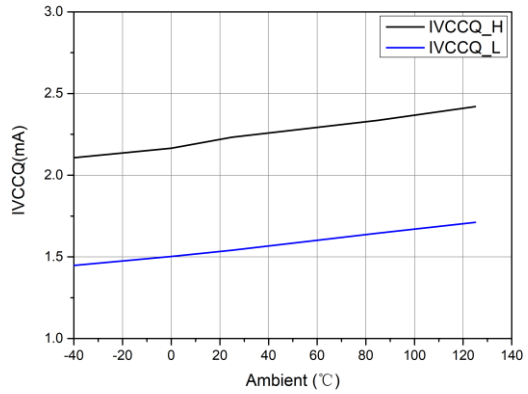


Figure 7-1. VCC quiescent current vs. temperature

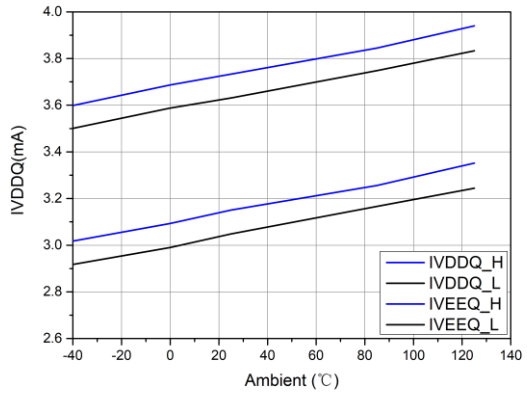


Figure 7-2. VDD & VEE quiescent current vs. temperature

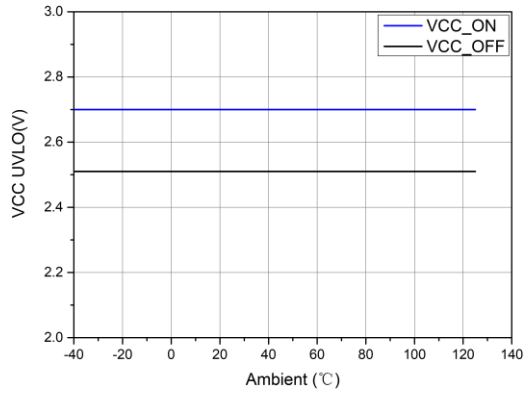


Figure 7-3. VCC UVLO vs. temperature

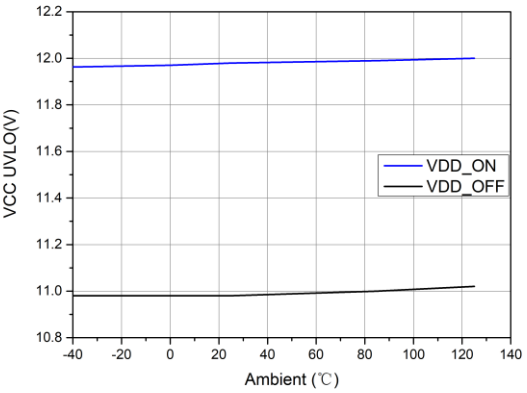


Figure 7-4. VDD UVLO vs. temperature

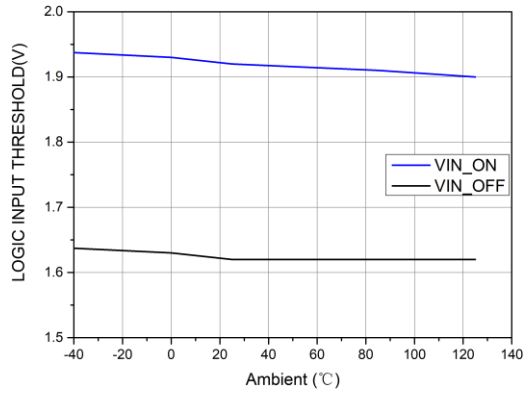


Figure 7-5. Logic input threshold vs. temperature

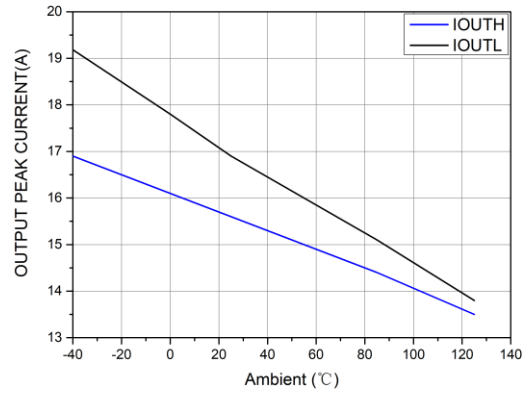


Figure 7-6. Output peak current vs. temperature (C_L=180nF)

（Continued）

V_{CC} = 3.3V or 5V, connect a 1μF bypass capacitor between VCC and GND; VDD-COM = 20V, 18V or 15V; COM–VEE=0V, 5V, 8V or 15V; C_L=100pF; -40°C < T_J < +150°C, unless otherwise noted. Typical values are at T_A = +25°C, unless otherwise noted.

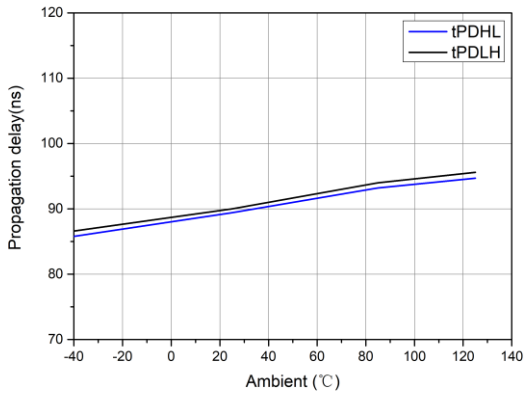


Figure 7-7. Propagation delay vs. temperature

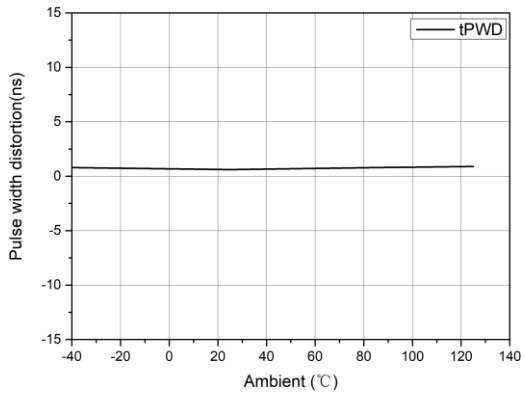


Figure 7-8. PWD vs. temperature

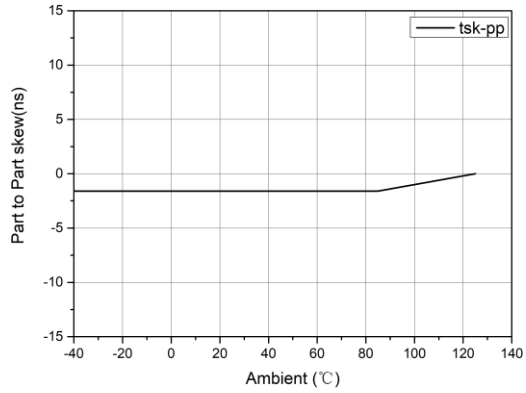


Figure 7-9. Delay matching vs. temperature

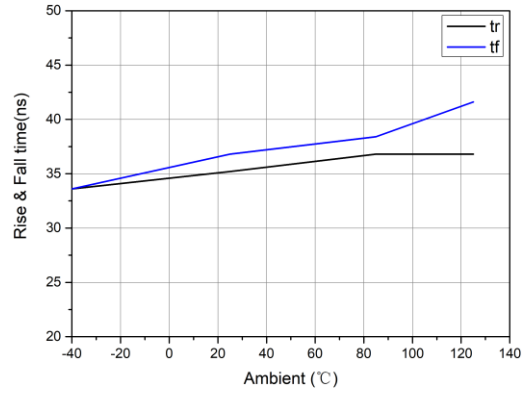


Figure 7-10. Rise & Fall time vs. temperature

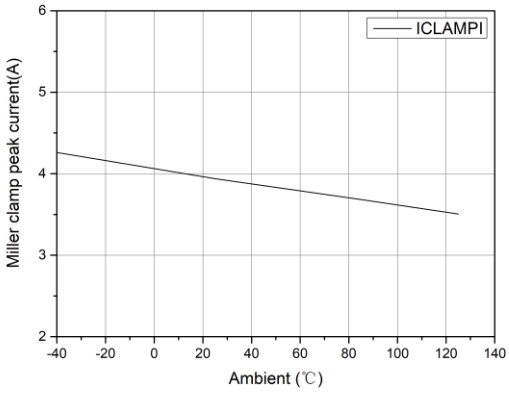


Figure 7-11. Miller clamp current vs. temperature

8. Parameter Measurement Information

8.1. Propagation Delay

Figure 8-1 shows the definition and measurement for the non-inverting input propagation delay (t_{PDLH}, t_{PDHL}). Figure 8-2 shows the definition and measurement for the inverting input propagation delay.

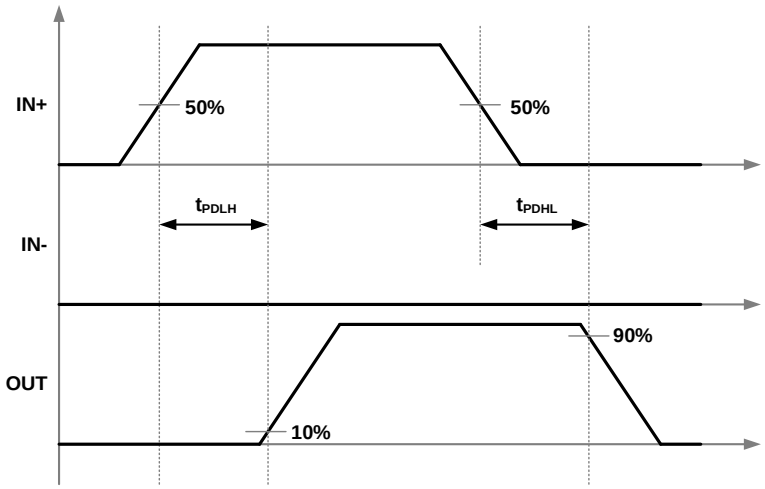


Figure 8-1 Noninverting input propagation delay measurement

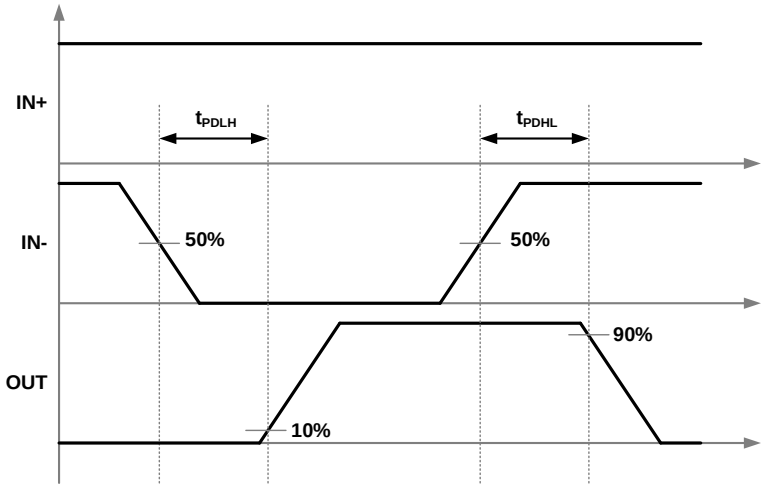


Figure 8-2 Inverting input propagation delay measurement

8.2. Input Glitch Filter

Fast common-mode transients and accidental small pulses can inject noise and glitches on the control inputs (IN+, IN– pins) because of parasitic coupling. In order to increase the robustness of gate driver, the CA-IS3213 devices feature a 40ns glitch filter per control input to reduce glitches and noise at the input, and make sure there is no wrong output responses or accidental driver operation. For example, if the IN+ or IN- PWM pulse width is lease than t_{INFIL}, the input signal will be filtered out and there will be no responses on gate driver output. Figure 8-3 shows the ON/OFF pulse deglitch filter effect on IN+ input; Figure 8-4 shows the ON/OFF pulse deglitch filter effect on IN- input.

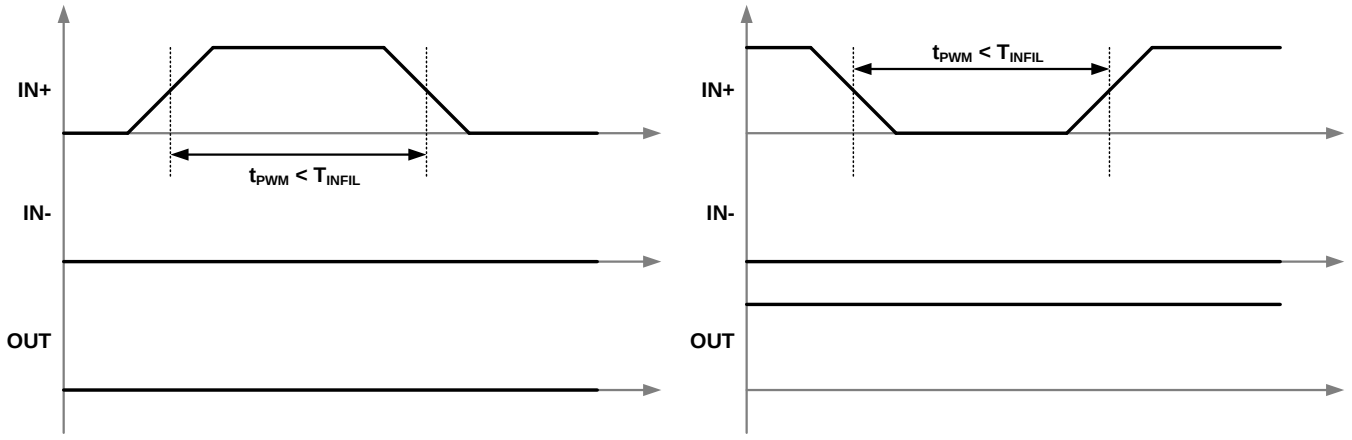


Figure 8-3 IN+ ON/OFF deglitch filter

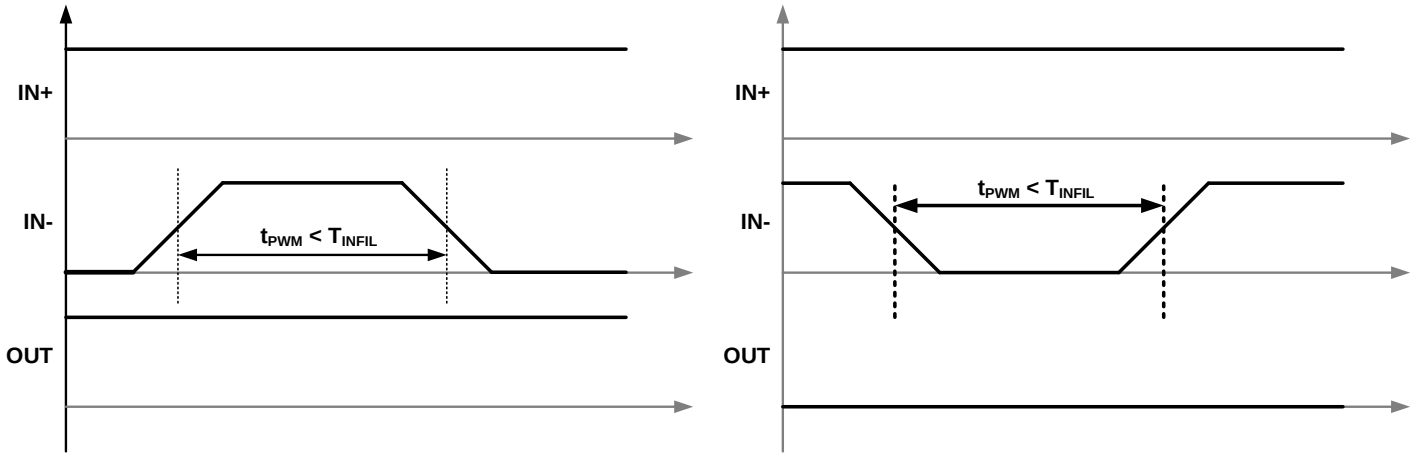


Figure 8-4 IN– ON/OFF filter

8.3. Active Miller Clamp

For the gate driver with single supply or dual supplies with small negative turn-off voltage on driver-side, the active Miller clamp circuit provides a very low-impedance path to direct the Miller current. This configuration can prevent the power transistors from unintentionally turning-on because of high dV/dt current induced from the Miller effect, see Figure 8-5 for a Miller clamp timing diagram.

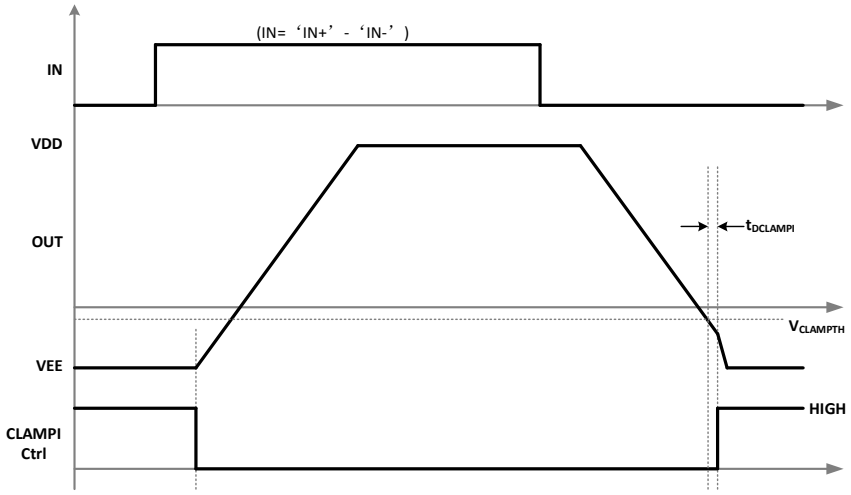


Figure 8-5 Internal active Miller clamp timing diagram

8.4. Power-up UVLO Delay

The VCC and VDD supplies are both internally monitored for undervoltage conditions. UVLO is a key protection function. It can prevent the power transistors from unintentionally turning-on when control-side or driver-side supply is in UVLO condition during power-up, power-down, or during normal operation due to a sagging supply voltage.

8.4.1. VCC UVLO

Figure 8-6 shows the behavior of the outputs during power-up and power-down, including UVLO ON/OFF threshold, deglitch filter, response time, and RDY timing diagram.

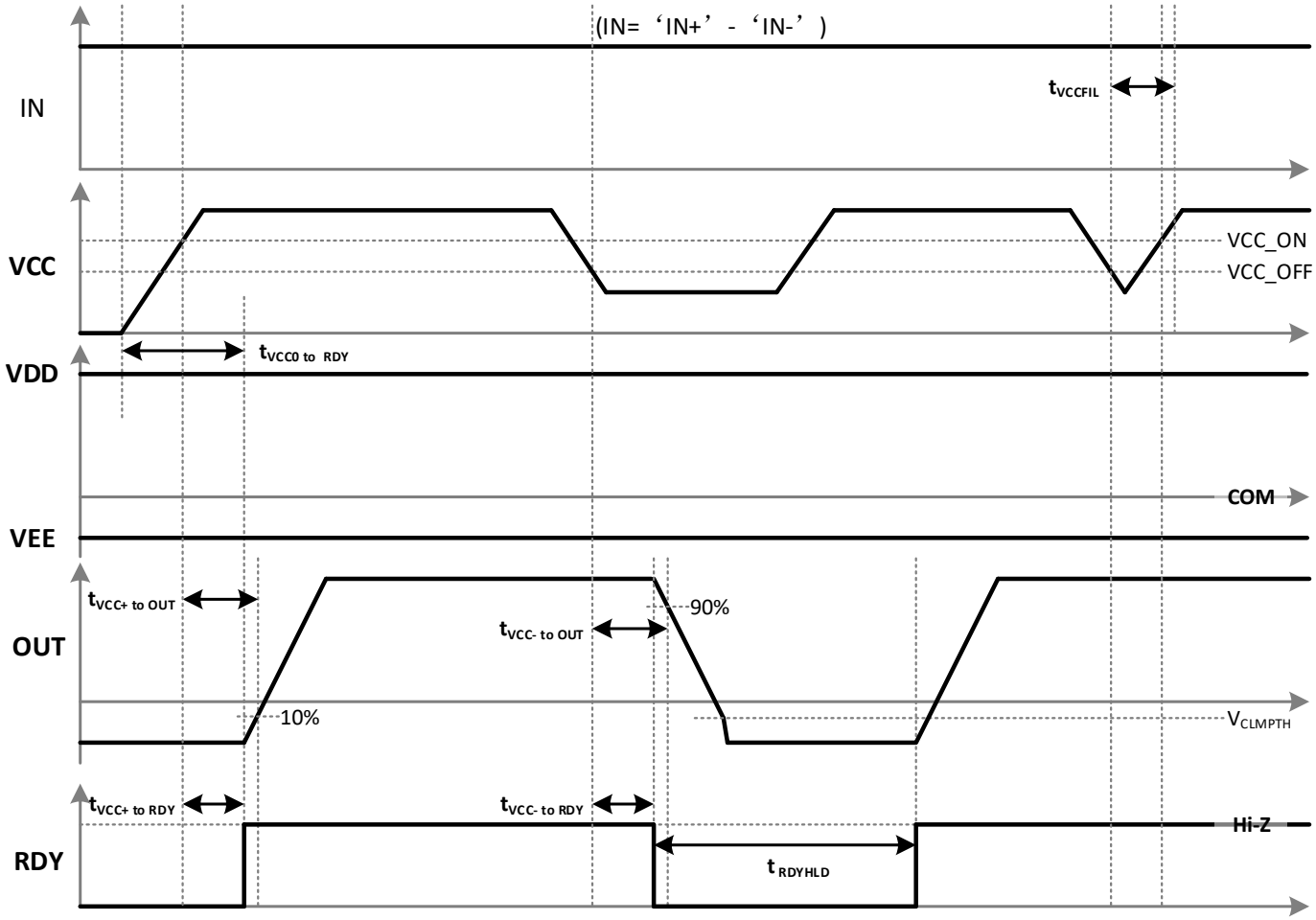


Figure 8-6 VCC UVLO timing diagram

8.4.2. VDD UVLO

Figure 8-7 shows the behavior of the outputs during power-up and power-down, including UVLO ON/OFF threshold, deglitch filter, response time, and RDY timing diagram.

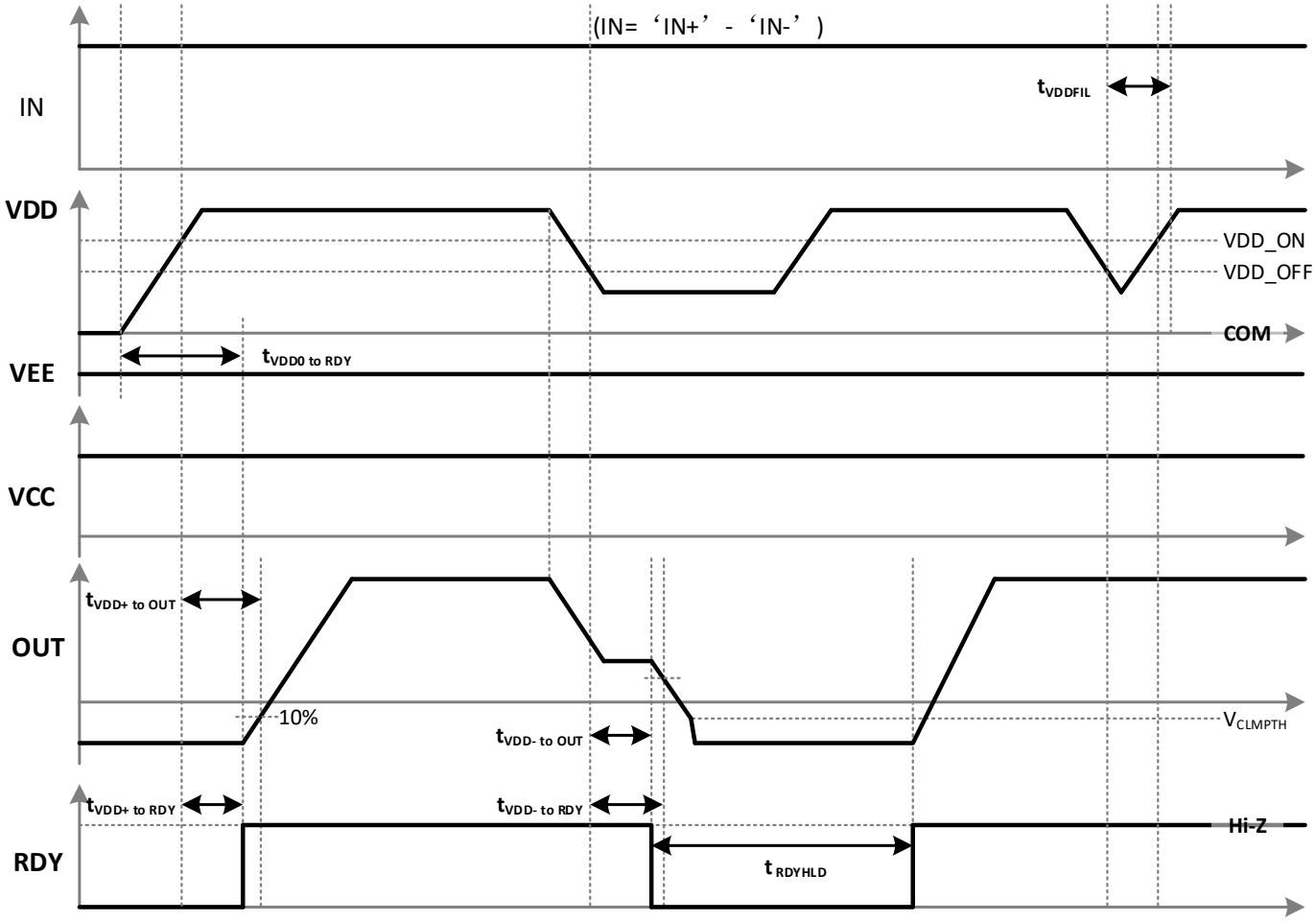


Figure 8-7 VDD UVLO timing diagram

8.5. CMTI Test Circuit

Figure 8-8, Figure 8-9 and Figure 8-10 are the CMTI test configuration for the CA-IS3213 products.

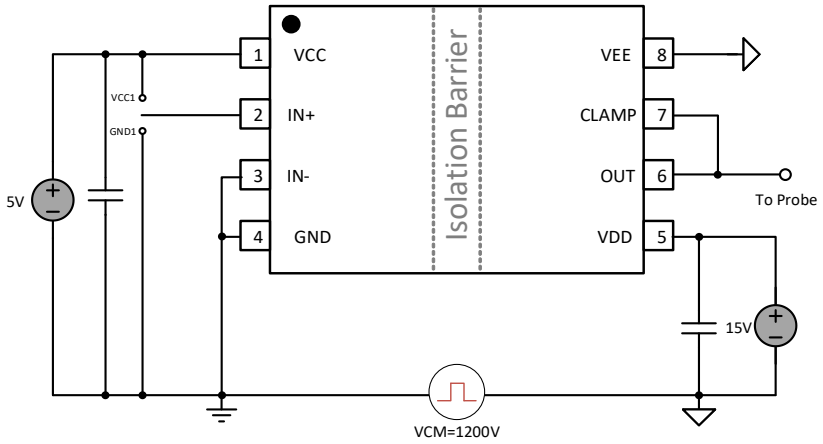


Figure 8-8 CMTI test setup（CA-IS3213MCG）

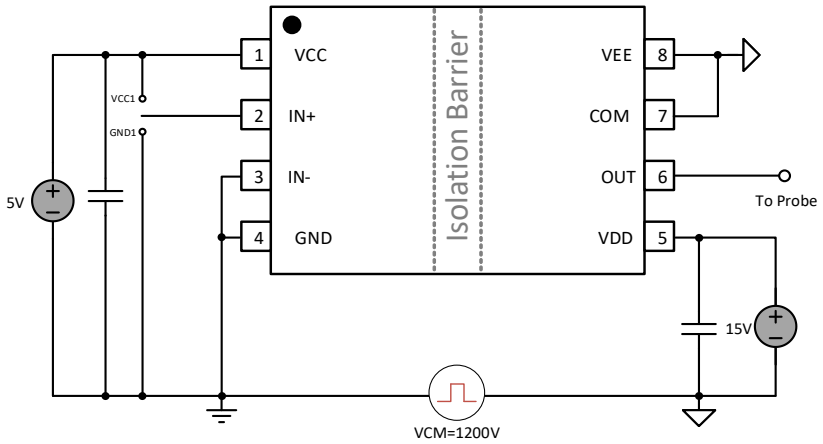


Figure 8-9 CMTI test setup（CA-IS3213VCG）

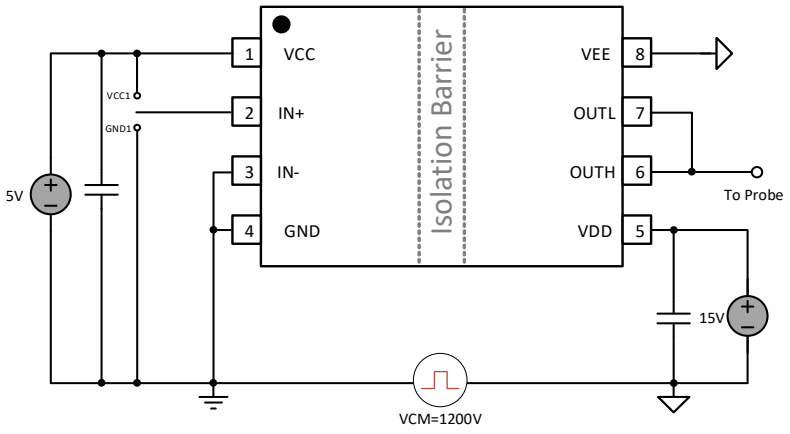


Figure 8-10 CMTI test setup（CA-IS3213SCG）

9. Detailed Description

9.1. Overview

The CA-IS3213 is a series of capacitive isolation based single-channel gate drivers for driving SiC, IGBT and MOSFET devices. The devices offer excellent dynamic performance and high reliability, along with sink/souce current capability up to ±15A peak. The device controls and drives the side supply UVLO while optimized for SiC and IGBT switching behavior and improved reliability. In addition, the CA-IS3213MCG has a built-in 4A peak current active Miller clamp; the CA-IS3213VCG has an external COM pin for easy isolation of the positive and negative driver-side power supplies; and the CA-IS3213SCG has an OUTH and OUTL split output configuration.

The entire series is available in SOIC8-WB wide body packages with creepage and clearance distances greater than 8mm.

9.2. Functional Block Diagram

Their operations are described separately in the following sections.

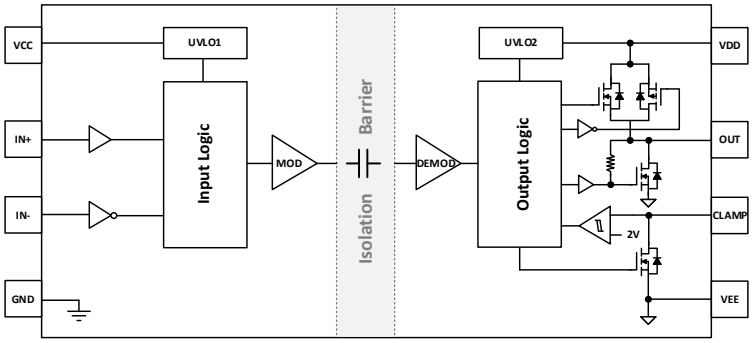


Figure 9-1 CA-IS3213M functional block diagram

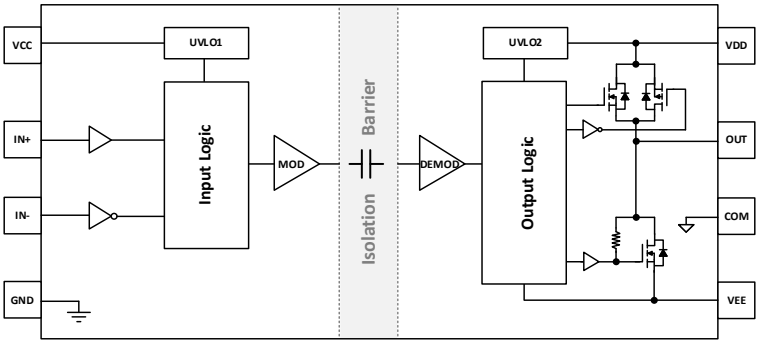


Figure 9-2 CA-IS3213V functional block diagram

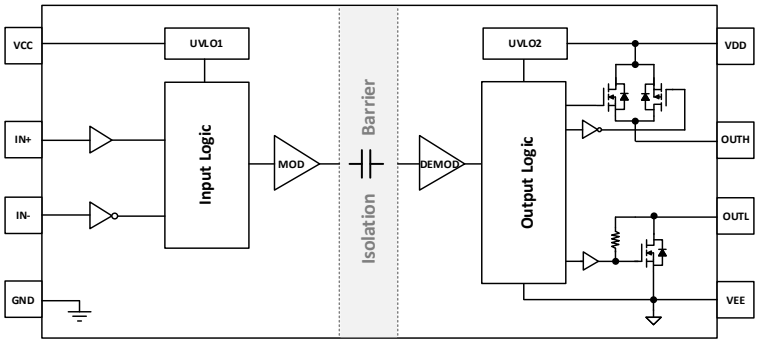


Figure 9-3 CA-IS3213S functional block diagram

9.3. Functions description

9.3.1. Power supply

The control-side power supply VCC of the CA-IS3213 supports a wide voltage range of 3V to 5.5V. The driver side supports both unipolar and bipolar power supplies, and VDD to VEE supports a wide voltage range of 13V to 33V. In SiC and IGBT applications, the fast dV/dt and Miller effect may lead to power tube mis-conductivity, and negative voltage shutdown of power devices can improve reliability. Therefore, negative voltage power supply is also particularly important.

9.3.2. Output stage

With ±15A peak drive capability, the CA-IS3213 is capable of directly driving SiC MOSFET modules, IGBT modules, or discrete devices in parallel without the need for additional buffer stages. OUT or OUTH/OUTL is pulled low when the input pin is in the idle state to prevent power tubes from turning on by mistake. The driver's output separation configuration allows flexibility in setting the drive resistors, as shown in Figure 9-4 and Figure 9-5. The driver internally realizes rail-to-rail outputs through a hybrid pull-up structure with a combination of PMOS and NMOS, and a pull-down structure with NMOS. The pull-up NMOS has the same structure as the pull-down NMOS, so the on-resistance RNMOS and ROL are also the same. The pull-up NMOS provides fast peak current in the Miller region during power device turn-on until the voltage difference between the OUTH voltage and the VDD voltage is less than 3 V. The pull-up NMOS stops working and the pull-up PMOS pulls the OUTH voltage to the VDD. hybrid pull-up structure can provide the highest peak current pulling capability during turn-on transient, which can shorten the charging time to the input capacitance of the power tubes and reduce the conduction losses.

The pull-down structure of the driver is realized by a single pull-down NMOS only. the ROL of the N-channel MOSFET is detailed in the parameters in the electrical characteristics. this MOSFET ensures that the OUTL voltage is pulled down to VEE. the low pull-down impedance not only achieves large sink current capability and reduces turn-off time, but also contributes to the immunity to interference in the presence of the Miller Effect.

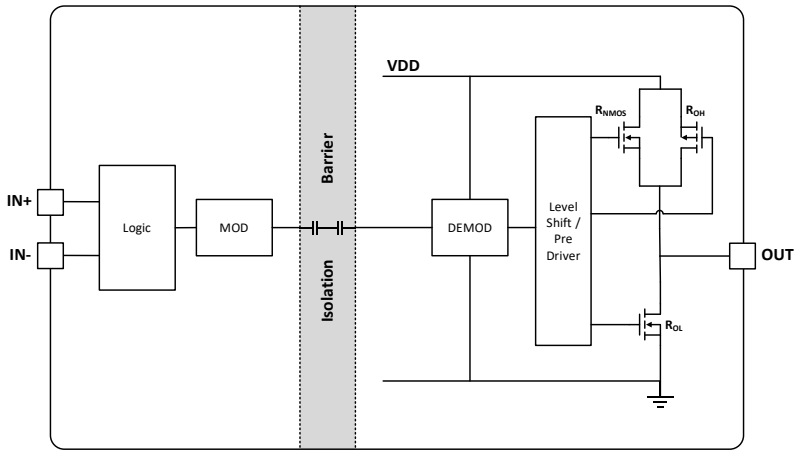


Figure 9-4 Gate-driver output stage (CA-IS3213M/V)

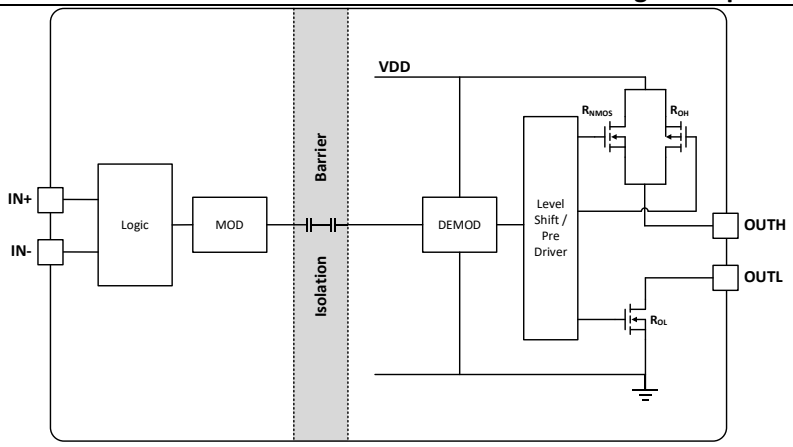


Figure 9-5 Gate-driver output stage (CA-IS3213S)

9.3.3. VCC and VDD UVLO

The CA-IS3213 implements an internal UVLO protection function for the control-side supply VCC and the driver-side supply VDD. When the supply voltage is below the threshold voltage, the driver output remains low. The output can only go high when both VCC and VDD are above the UVLO threshold state. The UVLO protection function both reduces the power consumption of the driver itself under low supply voltage conditions and improves the efficiency of the power stage. The VDD has a UVLO threshold voltage of 12V with a 1V hysteresis.

Both VCC and VDD of CA-IS3213 have built-in anti-spike pulse filters. When the power supply voltage may drop suddenly and briefly at the moment the power supply is turned on or off, the filter can effectively filter out some power supply noise interference and prevent the chip from malfunctioning.

Figure 8-6 and Figure 8-7 show the timing diagrams of the UVLO function of VCC and VDD.

9.3.4. Active Pulldown

The CA-3213 has an active pulldown function to turn-off the external power transistor when VDD is open and prevent the external power transistor from falsely turning-on before the device is back to control. See Figure 9-6, when the driver output stages are in power-off or VDD is open, the OUTH/OUTL pins are placed in high-impedance and clamped to VEE.

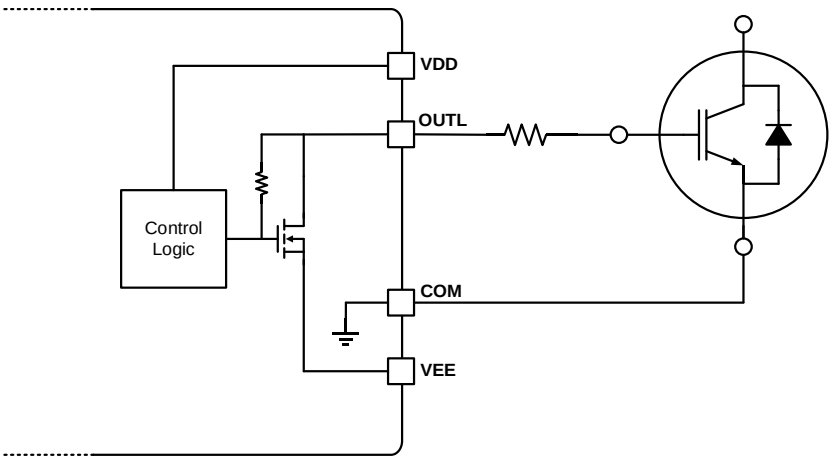


Figure 9-6 Active pulldown

9.3.5. Short-Circuit Clamping

As shown in Figure 9-7, when a short-circuit occurs in a power device, the Miller capacitance may cause current to be poured into the OUTH/OUTL/CLAMP pin, and a high dV/dt may pull up the OUTH/OUTL/CLAMP voltage. The short-circuit clamp function of the CA-IS3213 clamps the OUTH/OUTL/CLAMP pin voltage to a diode voltage slightly higher than that of VDD, thus protecting the power device from gate-source or gate-emitter overvoltage breakdown. This protects the power device from gate-source or gate-emitter overvoltage breakdown. This function is realized by the internal diode from OUTH/OUTL/CLAMP to VDD.

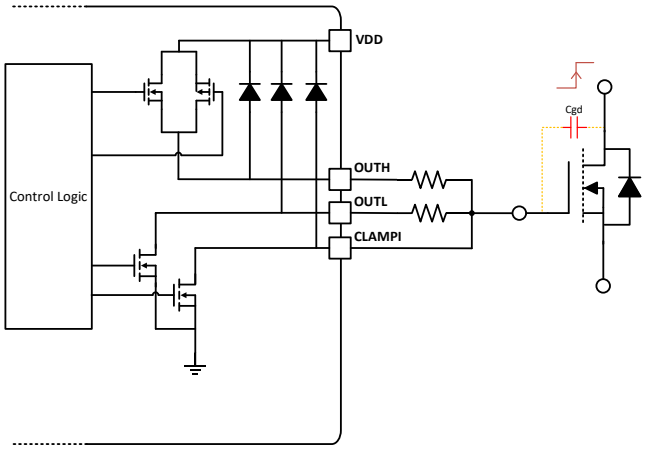


Figure 9-7 Short-circuit clamping

9.3.6. Active Miller Clamp

In high dV/dt applications, due to the presence of the Miller capacitance effect, the moment the other power tubes are turned on, the gate will be shunted by the CGD and CGS capacitive couplings, and if this voltage is greater than the threshold voltage of the gate, it may cause a false conduction phenomenon, which can damage the power tubes. It is important to provide a drain circuit for this current.

The CA-IS3213M has an internal independent pull-down NMOS that provides a 4A peak pull-down capability to hold the gate to VEE. The CLAMP pin is connected to the gate of the power device to provide a bleeder circuit for this current. When the gate voltage falls below VCLAMPTH, i.e., 2V above VEE, the pull-down NMOS will turn on and establish a low impedance path to avoid false turn-on of the power switch. Figure 9-8 shows the built-in active Miller clamp function.

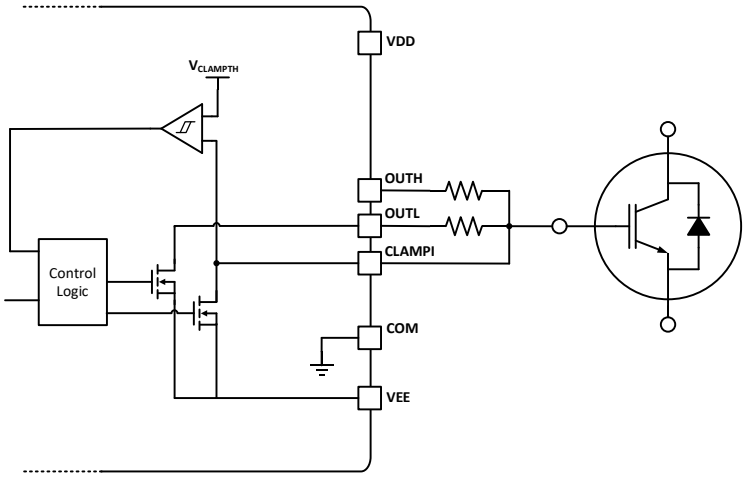


Figure 9-8 Active Miller clamp

9.4. Device Functional Modes

Table 9-1 shows the CA-IS3213 devices functional modes.

Table 9-1 CA-IS3213 Inputs vs. Output Truth Table

VCC	VDD	VEE	IN+	IN-	OUTH	OUTL	CLAMP
PU	PU	PU	Low	Low	HiZ	Low	Low
PU	PU	PU	High	Low	High	HiZ	HiZ
PU	PU	PU	Low	High	HiZ	Low	Low
PU	PU	PU	High	High	HiZ	Low	Low
PD	PU	PU	X	X	HiZ	Low	Low
PU	PD	PD	X	X	HiZ	Low	Low

Notes:

1. X = don't care; HiZ = high-impedance.
2. PU = power up (VCC≥ 2.7V, VDD≥12V, VEE≤0V); PD = power down (VCC≤2.5V, VDD≤11V).

10. Application and Implementation

10.1. Typical Application

CA-IS3213 is characterized by strong driving capability, high isolation level, excellent CMTI and high reliability, etc. It is widely used in the fields of motor drives, photovoltaic inverters, energy storage converters, power modules for charging piles, and industrial power supplies.

See the Figure 10-1 CA-IS3213 typical application circuits for IGBT driving.

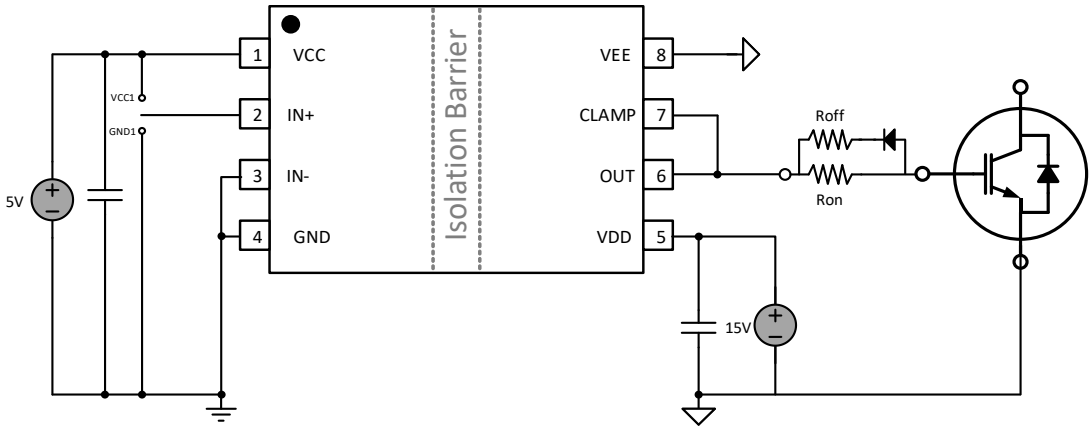


Figure 10-1 The CA-IS3213 typical application circuit

10.2. Power design

When the OUT switching, the peak source and sink current are provided by the VDD and VEE power supplies. To ensure a stable power supply and provide ±15A peak drive capability, a 10uF/50V decoupling capacitor is recommended for VDD to COM and VEE to COM. A 1μF decoupling capacitor is recommended between VCC and GND on the control side. At the same time, it is recommended to use an additional 0.1μF bypass capacitor per power supply to filter out high-frequency noise. The recommended capacitors must be low ESR and ESL to avoid high-frequency noise, and should be as close as possible to the VCC, VDD, and VEE pins to prevent parasitic coupling noise caused by the PCB layout.

10.3. Input Filters

The CA-IS3213 gate drivers feature differential PWM inputs (IN+ and IN-). The differential inputs reject input glitches and prevent false turn-on of the output. The internal filter can keep driver output in the previous state when a glitch or short pulse (<40ns, typical) is detected on either input(IN+, IN–). The IN+, IN– pins can not leave float if not used. For single-ended input configuration, apply PWM input at IN+ and connect IN- to GND.

10.4. Interlock configuration

The IN+ and IN- pins of the CA-IS3213 have an internal PWM interlock to prevent in-phase bridge breakdown problems. As shown in Table 9-1, when both IN+ and IN- are logic high, the drive output is logic low. As shown in Figure 10-2, PWMA is the PWM signal to the high-side switch and PWMB is the PWM signal to the low-side switch. For the high-side gate drive, the PWMA signal is given the IN+ pin, while the PWMB signal is given the IN- pin; for the low-side gate drive, the PWMB signal is given the IN+ pin, while the PWMA signal is given the IN- pin. When both the PWMA and PWMB signals are high, the outputs of both gate drivers are low to prevent the high-side switch and the low-side switch from conducting at the same time.

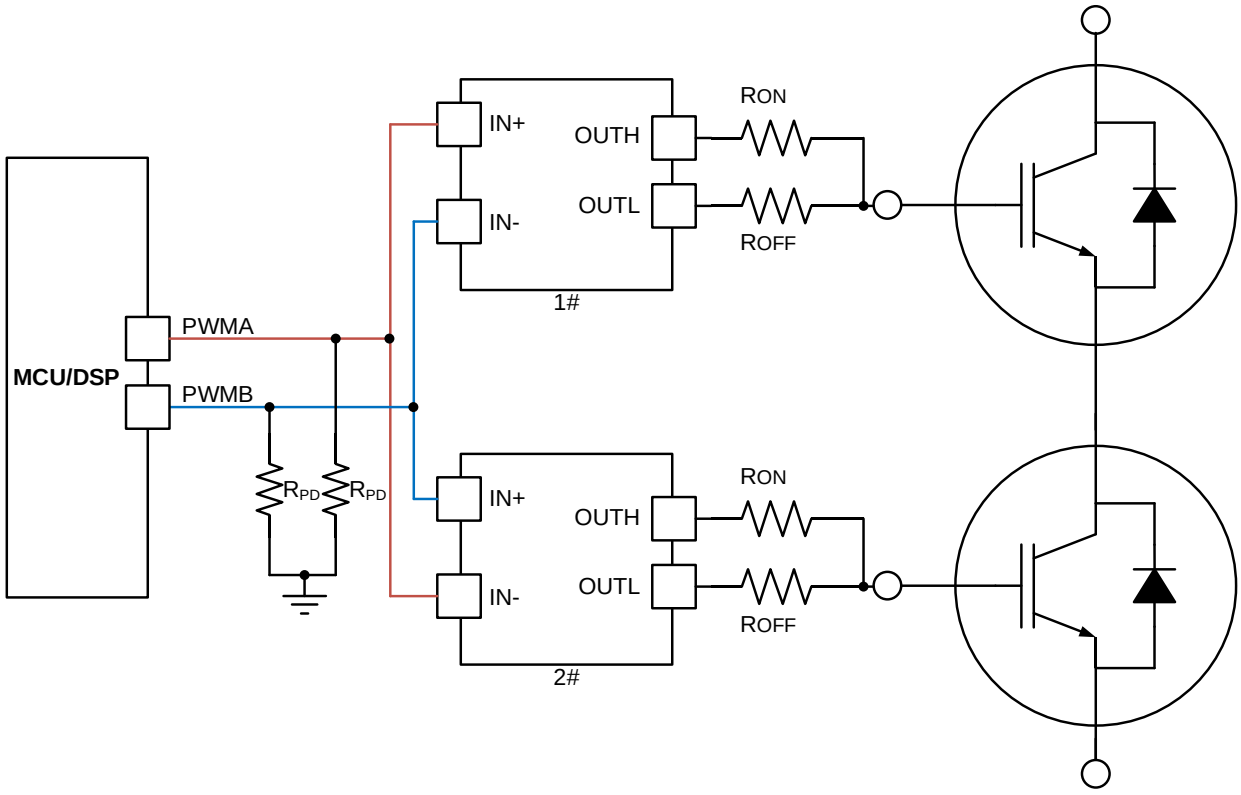


Figure 10-2 The CA-IS3213 half-bridge interlock configuration

10.5. Gate Driver Resisters Selection

The CA-IS3213 separates the outputs into OUTH and OUTL, allowing independent control of on and off switching speeds. External gate drive resistors are especially critical to power tube design, where parasitic inductance, parasitic capacitance, high dv/dt and di/dt, and diode reverse recovery time can cause undesirable behavior or EMI problems when the power tube is switched on and off. The gate drive resistor has an impact on three main areas: drive current, switching losses, and rise and fall times. Therefore, designers need to balance the comprehensive performance parameters of the program when selecting the drive resistor.

The peak pull and sink currents are calculated as follows:

I_{OUTH} peak source current:

$$I_{OUTH} = \min\left[15A, \frac{VDD - VEE}{\left(R_{OH\_EFF} + R_{GON} + R_{GFET_{int}}\right)}\right]$$

I_{OUTL} peak sink current:

$$I_{OUTL} = \min\left[15A, \frac{VDD - VEE}{\left(R_{OUTL} + R_{GOFF} + R_{GFET_{int}}\right)}\right]$$

Where:

- R_{GON} is the external turn-on resistance;
- R_{GOFF} is the external turn-off resistance;
- R_{OH_EFF} is internal resistance of pull-up structure, about $2\times R_{OL}$ (0.7Ω);
- R_{OUTL} is internal pulldown resistance, about 0.23Ω;
- R_{GEFT_Int} is the gate resistance of the external power transistor, this number is available from power transistor data sheet.

11. PCB Layout Guidelines

Due to the powerful driving capability of the CA-IS3213, careful consideration must be given to the following points in the PCB design:

- The driver should be located as close as possible to the power device to minimize parasitic inductance due to PCB alignment.

- Decoupling capacitors for the control side and driver side power supplies should be as close as possible to the power supply pins. Peak currents generated at each switching instant can lead to high di/dt and voltage spikes on the PCB lead parasitic inductance.

- The driver COM pin connection to the SiC MOSFET source or IGBT emitter should be a Kelvin connection. If the power device does not have a separated Kelvin source or emitter, the COM pin should be connected as close as possible to the source or emitter of the power device package in order to separate the gate loop from the high power switching loop.

- Use a ground layer on the control side to shield the input signal. Input signals can be distorted by high-frequency noise generated by switching moments on the drive side. The ground layer provides a low-inductance filter for the return current.

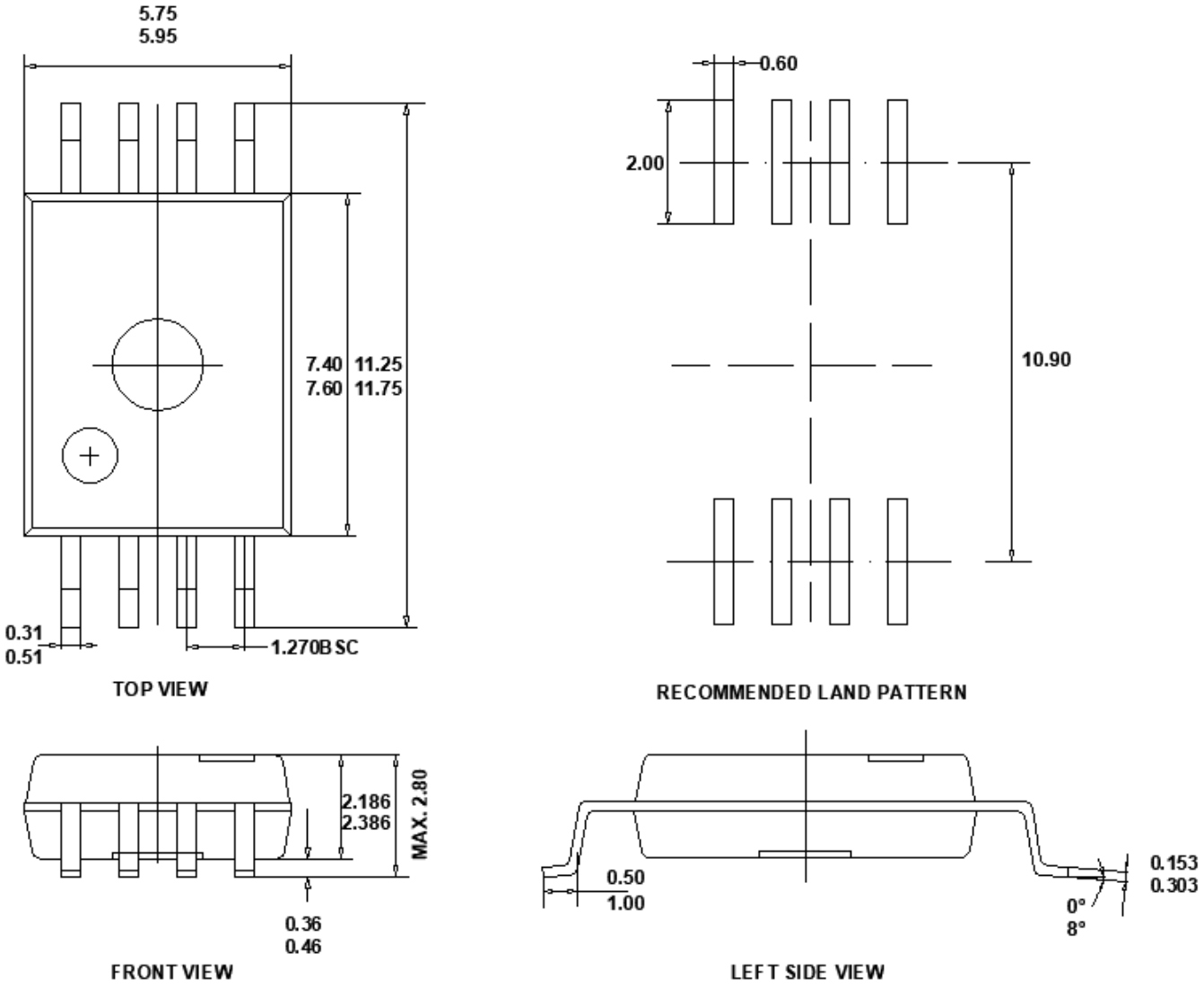
- If the gate driver is connected to a low-side switch on the negative side of the DC bus with a COM pin, use the ground layer on the driver side to shield the output signal from noise generated by the switch node; if the gate driver is connected to a high-side switch on the switch node with a COM pin, use of the ground layer is not recommended.

- No PCB printed wires or copper overlays are allowed under the gate driver. PCB cutouts are recommended to avoid any possible contamination between the control side and the driver side increasing the noise coupling of the gate.

12. Package Information

8-Pin Wide Body SOIC Package

The following diagrams provide the package details and the recommended land pattern details for the CA-IS3213 isolated gate driver in 8-pin wide body SOIC package. All values for the dimensions are shown in millimeters.



Note:

1. All dimensions are in millimeters, angles are in degrees.

13. Soldering Temperature (reflow) Profile

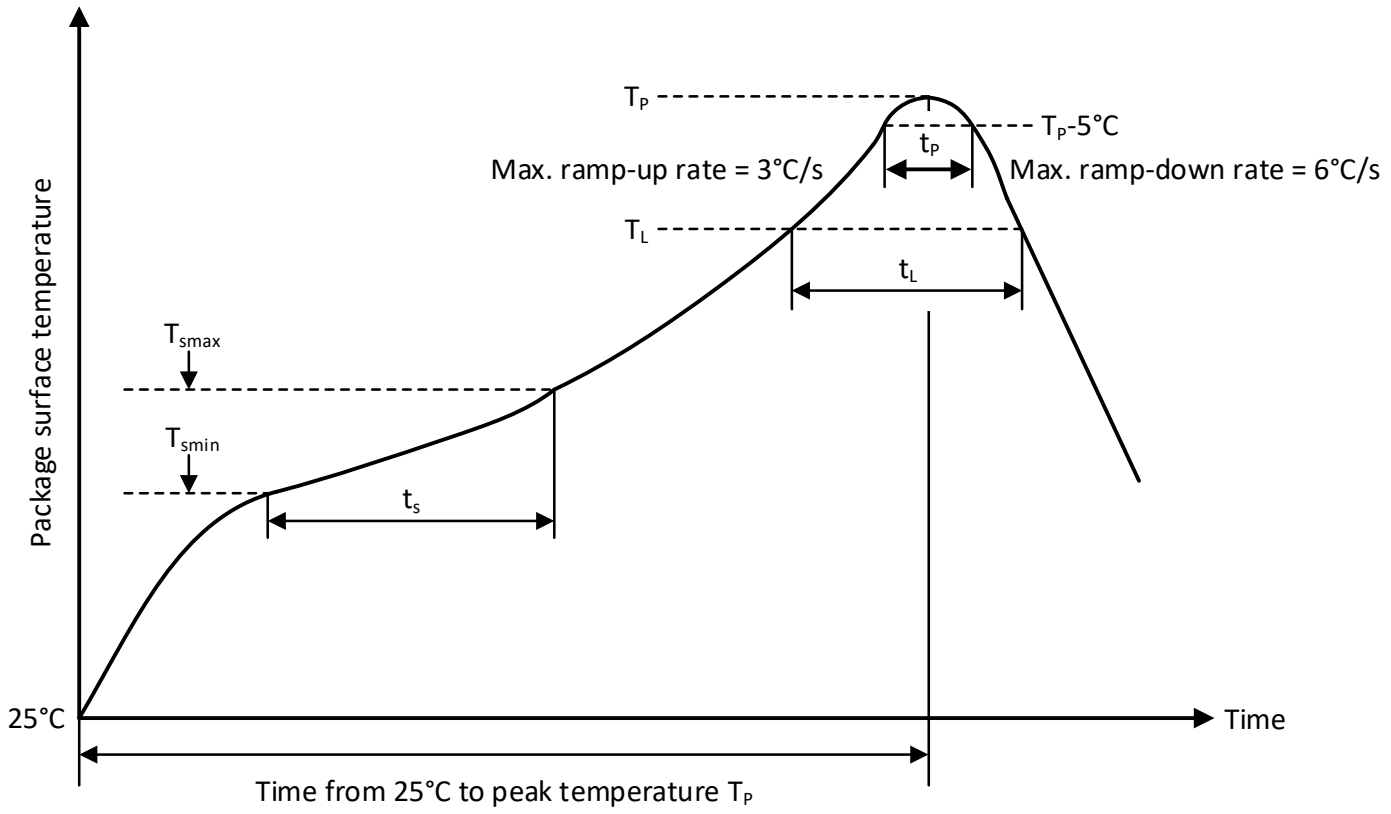


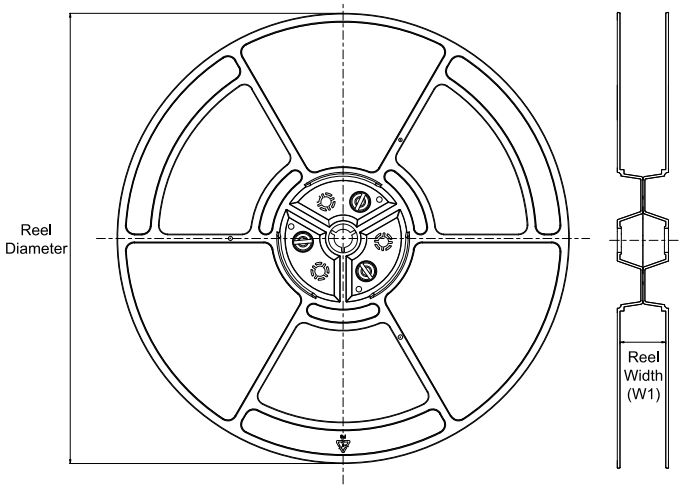
Figure 13-1. Soldering Temperature (reflow) Profile

Table 13-1. Soldering Temperature Parameter

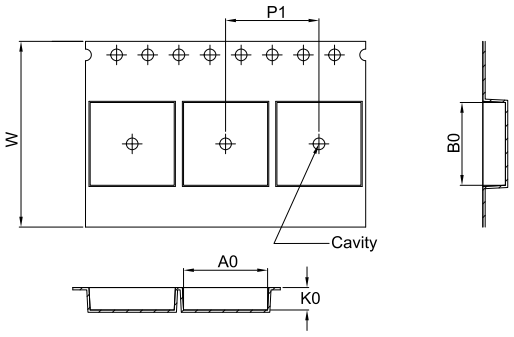
Profile Feature	**Pb-Free Assembly**
Average ramp-up rate(217°C to Peak)	3°C /second max
Time of Preheat temp(from 150°C to 200°C	60-120 second
Time to be maintained above 217 °C	60-150 second
Peak temperature	260 +5/-0°C
Time within 5°C of actual peak temp	30 second
Ramp-down rate	6 °C /second max.
Time from 25℃ to peak temp	8 minutes max

14. Tape and Reel Information

REEL DIMENSIONS

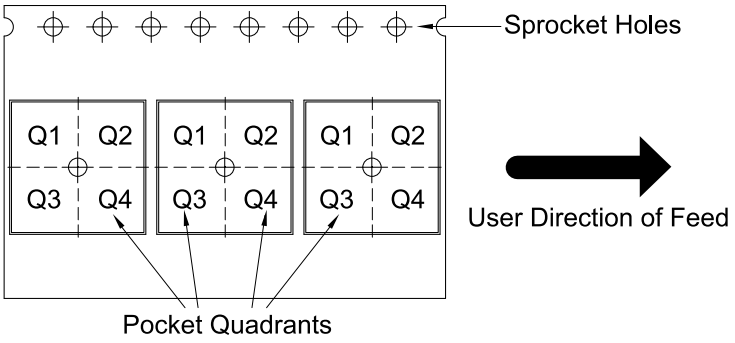


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CA-IS3213MCG	SOIC	G	8	1000	330	16.40	11.95	6.15	3.20	16.0	16.0	Q1
CA-IS3213SCG	SOIC	G	8	1000	330	16.40	11.95	6.15	3.20	16.0	16.0	Q1
CA-IS3213VCG	SOIC	G	8	1000	330	16.40	11.95	6.15	3.20	16.0	16.0	Q1

15. Important statement

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