

CA-IF4988S 3V to 5.5V Half-Duplex RS-485 Transceiver with $\pm 30\text{kV}$ ESD Rating, $\pm 65\text{V}$ Fault Protection, $\pm 40\text{V}$ CMR and Bus Polarity Control

1 Key Features

- Meets or Exceeds the Requirements of the TIA/EIA-485A Standard
- Low EMI 2Mbps Data Rate
- 3V to 5.5V Supply Voltage
- Polarity Control Pin: POL
 - Driving POL to Low, Default Bus Polarity
 - Driving POL to High, Bus Polarity is Swapped
- Driver with Current Limiter and Thermal Shutdown Protection
- Bus Pins ESD Protection
 - $\pm 30\text{kV}$ HBM ESD
 - $\pm 6\text{kV}$ IEC 61000-4-2 Contact Discharge
- 1/8 Unit Load (Up to 256 Bus Nodes)
- Open, Short and Idle Bus Failsafe Protection
- Hot Plug-in Protection
- Extended Industrial Temperature Range: -40°C to 125°C
- $\pm 65\text{V}$ Fault Protection on Bus Pins
- $\pm 40\text{V}$ Common Mode Range on Bus Pins
- Standard SOIC8 Narrow Body Package

2 Applications

- HVAC
- Home and Building Automation
- Motion Controllers
- Industrial Automation
- Elevator Control
- Video Surveillance
- Power Grid Infrastructure

3 Description

The CA-IF4988S is the high-performance half-duplex RS-485 transceiver which could be used in harsh industrial and home-appliance environments. The bus pins could withstand high-level ESD events to protect internal circuit without damage.

This device has $\pm 65\text{V}$ fault protection on bus pins, and the common-mode range (CMR) could be extended to $\pm 40\text{V}$

when V_{CC} ranges from 4.5V to 5.5V, which is suitable for long-cable communication applications. Each device contains one driver and one receiver, supporting the power supply range from 3V to 5.5V. This device could select the polarity of bus pins A/B by the polarity control pin (POL), allowing for software correction of cross-wired field cables through the external controller.

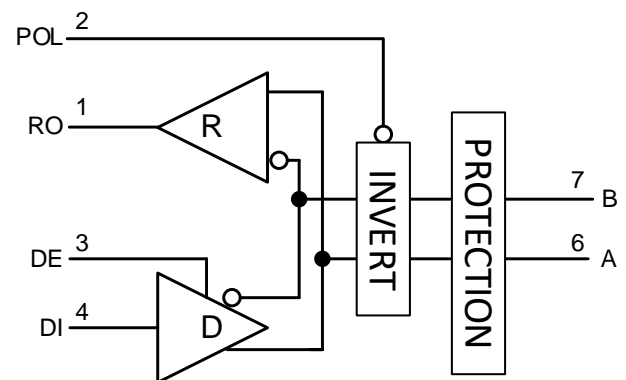
The CA-IF4988S features slew-rate-limited driver for low EMI and data rates up to 2Mbps. This device integrates failsafe circuit to guarantee a logical high on the receiver output when the bus inputs are open, short or on idle state (POL is low). This device features a 1/8 unit load impedance, allowing up to 256 transceivers on a bus.

The CA-IF4988S devices are packaged in narrow body, 8-pin SOIC packages and specified over ambient free-air temperature range of -40°C to 125°C .

Device Information

PART NUMBER	PACKAGE	BODY SIZE (NOM)
CA-IF4988S	SOIC8 (S)	3.9mm × 4.9mm

Simplified Schematic



4 Ordering Guide

Table 4-1 Ordering Guide for Valid Ordering Part Number

Part Number	Full/Half-Duplex	Date Rate (Mbps)	Package
CA-IF4988S	Half-Duplex	2	SOIC8 (S)

Table of Contents

1	Key Features	1			
2	Applications.....	1			
3	Description	1			
4	Ordering Guide	2			
5	Revision History	3			
6	Pin Descriptions and Functions.....	4			
7	Specifications.....	5			
	7.1 Absolute Maximum Ratings ¹	5			
	7.2 ESD Ratings.....	5			
	7.3 Recommended Operating Conditions	5			
	7.4 Thermal Information	5			
	7.5 Electrical Characteristics	6			
	7.6 Timing Characteristics	7			
	7.7 Typical Characteristics	8			
8	Parameter Measurement Information	10			
9	Detailed Description	12			
			9.1	Device Feature Description	12
			9.1.1	±65V fault protection on Bus Pins	12
			9.1.2	±40V Common-Mode Range	12
			9.1.3	Bus Failsafe Protection	12
			9.1.4	Hot Plug-in Protection.....	12
			9.1.5	Thermal Shutdown Protection	12
			9.2	Device Function Mode	12
			9.2.1	Driver	12
			9.2.2	Receiver	13
			10	Application and Implementation	14
			10.1	Typical Application	14
			10.2	Power Supply Recommendation.....	14
			11	Package Information	15
			11.1	SOIC8 (S) Package.....	15
			12	Soldering Information	16
			13	Tape and Reel Information	17
			14	Important Notice	18

5 Revision History

Revision	Description	Date	Page
Version 1.00	NA	2024.06.30	NA

6 Pin Descriptions and Functions

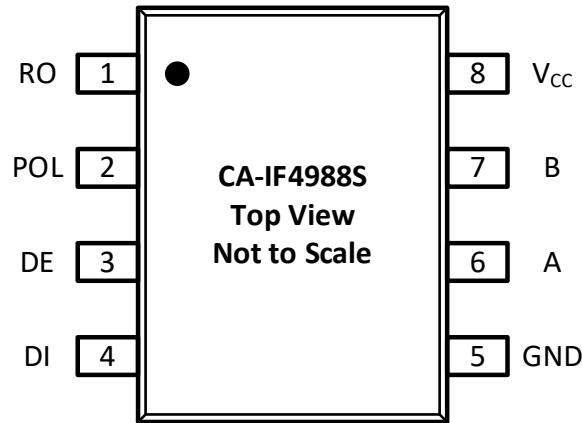


Figure 6-1 CA-IF4988S Pin Configuration

Table 6-1 CA-IF4988S Pin Description and Functions

NAME	PIN NUMBER	TYPE	DESCRIPTION
RO	1	Digital Output	Receiver data output.
POL	2	Digital Input	Bus polarity control, pulled down internally: 1. When POL is low or open, bus polarity is default; 2. When POL is high, bus polarity inverts.
DE	3	Digital Input	Driver enable control, pulled down internally: 1. When DE is high, driver is enabled; 2. When DE is low or open, driver is disabled.
DI	4	Digital Input	Driver data input, pulled up internally.
GND	5	Ground	Ground.
A	6	Bus Input/Output	Noninverting driver output/receiver input.
B	7	Bus Input/Output	Inverting driver output/receiver input.
V _{CC}	8	Power	Power supply input, bypass V _{CC} to GND with 0.1μF and at least 1μF capacitors as close as possible to the device.

7 Specifications

7.1 Absolute Maximum Ratings¹

PARAMETER		MIN	MAX	UNIT
V _{CC}	Supply voltage ²	-0.5	7	V
V _{IO}	Bus voltage of A and B ²	-65	65	V
V _{IO}	Input logical voltage of DI, DE and POL	-0.3	V _{CC} + 0.3 ³	V
V _{IO}	Output logical voltage of RO	-0.3	V _{CC} + 0.3 ³	V
T _J	Junction Temperature		150	°C
T _{STG}	Storage Temperature	-65	150	°C

NOTE:

- Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- All voltage values are with respect to the ground terminal and are peak voltage values.
- Maximum voltage must not exceed 7V.

7.2 ESD Ratings

			VALUE	UNIT	
V _{ESD}	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001	Bus pins to GND	±30	kV
			All other pins	±4	
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins		±2	kV
		Contact discharge, per IEC 61000-4-2		±6	

7.3 Recommended Operating Conditions

PARAMETER		MIN	NOM	MAX	UNIT
V _{CC}	Supply voltage, with respect to GND	3.0	5.0	5.5	V
V _{IN}	Bus input voltage	-40		40	V
V _{IH}	High-level input voltage of DI, DE and POL	2.0		V _{CC}	V
V _{IL}	Low-level input voltage of DI, DE and POL	0		0.8	V
R _L	Differential load resistance	54			Ω
1/t _{UI}	Data Rate			2	Mbps
T _A	Ambient Temperature	-40		125	°C
T _J	Junction Temperature	-40		150	°C

7.4 Thermal Information

THERMAL METRIC		SOIC8 (S)	UNIT
R _{θJA}	Junction-to-ambient thermal resistance	120	°C/W

7.5 Electrical Characteristics

 Over recommended operating temperature range (unless otherwise noted). All typical specifications are at $T_A = 25^\circ\text{C}$ and $V_{CC} = 5\text{V}$.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Driver						
V _{OD}	Differential output voltage	R _L = 60Ω, -40V ≤ V _{test} ≤ 40V, see Figure 8-1	1.2	2.8		V
		R _L = 60Ω, -40V ≤ V _{test} ≤ 40V, 4.5V ≤ V _{CC} ≤ 5.5V, see Figure 8-1	2	2.8		V
		R _L = 100Ω, C _L = 50pF, see Figure 8-2	1.7	3.5		V
		R _L = 54Ω, C _L = 50pF, see Figure 8-2	1.2	2.8		V
Δ V _{OD}	Change in magnitude of differential-output voltage	R _L = 100Ω or 54Ω, C _L = 50pF, see Figure 8-2	-200		200	mV
V _{OC}	Common-mode output voltage		1		3.2	V
ΔV _{OC(SS)}	Change in magnitude of steady-state common-mode output voltage		-100		100	mV
I _{OSD}	Driver short-circuit output current	DE = V _{CC} , -65V ≤ V _O ≤ 65V ¹ , or A pin shorted to B pin	-200		200	mA
Receiver						
I _I	Bus input current	DE = 0V, V _{CC} = 0V or 5.5V	V _I = 12V		125	μA
			V _I = -7V	-100		
			V _I = 40V		410	
			V _I = -40V	-400		
R _I	Bus input resistance	Over V _{CM} range	96			kΩ
V _{CM}	Common mode voltage range	3V ≤ V _{CC} ≤ 3.6V	-25		25	V
		4.5V ≤ V _{CC} ≤ 5.5V	-40		40	
V _{TH+}	Positive-going receiver differential-input voltage threshold	Over V _{CM} range, POL = 0V, see Table 9-2			-20	mV
V _{TH-}	Negative-going receiver differential-input voltage threshold		-200			mV
V _{HYS} ²	Receiver differential-input voltage threshold hysteresis, V _{TH+} - V _{TH-}			30		mV
V _{OH}	High-level output voltage	I _{OH} = -3mA	V _{CC} - 0.4	V _{CC} - 0.25		V
V _{OL}	Low-level output voltage	I _{OL} = 3mA		0.2	0.4	V
I _{OSR}	Receiver short-circuit output current	POL = DE = 0V, see Figure 8-3			95	mA
Input Logic (DI, DE, POL)						
I _{IN}	Input Current	0V ≤ V _{IN} ≤ V _{CC} , after hot-swap protection delay for DE	-10		10	μA
V _{IH}	High-level input voltage		2.0		V _{CC}	V
V _{IL}	Low-level input voltage		0		0.8	V
Supply						
I _{CC}	Quiescent supply current	DE = V _{CC} , empty load, no switching		2.2	3.5	mA
TSD	Thermal shutdown threshold			185		°C
	Thermal shutdown hysteresis			20		°C
NOTE:						
1. In the case of high ambient temperature, when pin A or pin B applies a voltage with a high absolute value, overtemperature protection may be triggered. At this time, the driver outputs become high-impedance, and the short-circuit output current would be greatly reduced.						
2. Under any specific conditions, V _{TH+} is specified to be at least V _{HYS} higher than V _{TH-} .						

7.6 Timing Characteristics

 Over recommended operating temperature range (unless otherwise noted). All typical specifications are at $T_A = 25^\circ\text{C}$ and $V_{CC} = 5\text{V}$.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Driver						
t_{DR}, t_{DF}	Differential output rise and fall time	$R_L = 54\Omega, C_L = 50\text{pF}$, see Figure 8-4		55	200	ns
t_{DPHL}, t_{DPLH}	Driver propagation delay			80	250	ns
t_{DSKEW}	Driver pulse skew, $ t_{DPHL} - t_{DPLH} $			1	100	ns
t_{DZH}, t_{DLZ}	Driver disable time	See Figure 8-5 and Figure 8-6		100	250	ns
t_{DZH}, t_{DZL}	Driver enable time			110	450	ns
Receiver						
t_{RPHL}, t_{RPLH}	Receiver propagation delay time	$C_L = 15\text{pF}^1$, see Figure 8-7		135	220	ns
t_{RSKEW}	Receiver pulse skew, $ t_{RPHL} - t_{RPLH} $			1	30	ns
NOTE:						
1. C_L includes probe and fixture capacitance.						

7.7 Typical Characteristics

All typical specifications are at $T_A = 25^\circ\text{C}$ and $V_{CC} = 5\text{V}$ (unless otherwise noted).

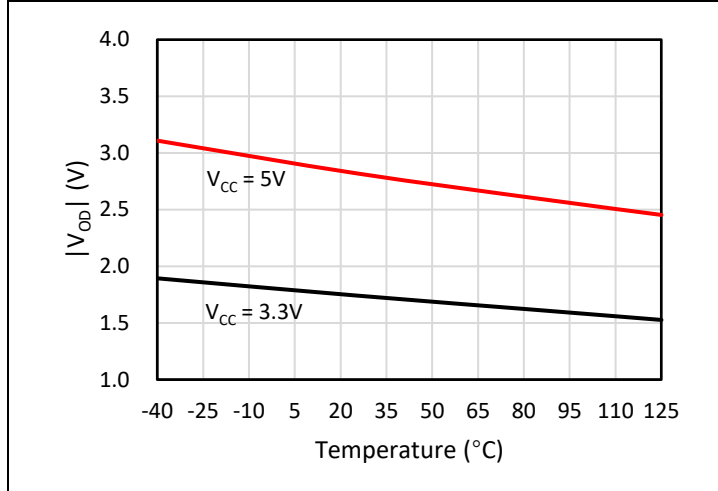


Figure 7-1 Differential Output Voltage vs Temperature @ $R_L = 54\Omega$

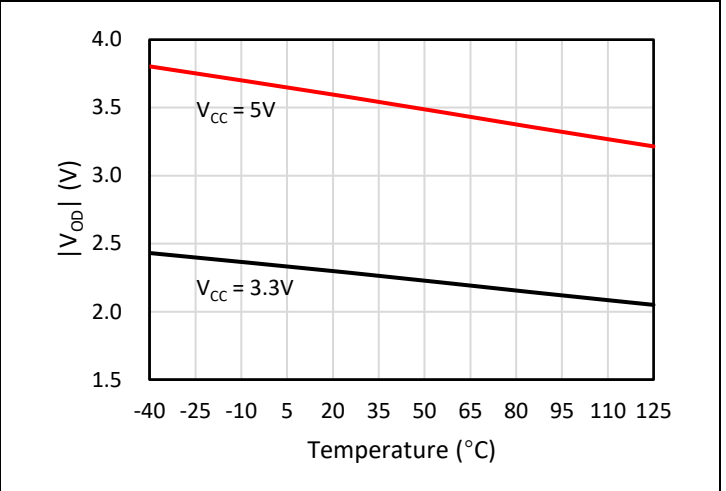


Figure 7-2 Differential Output Voltage vs Temperature @ $R_L = 100\Omega$

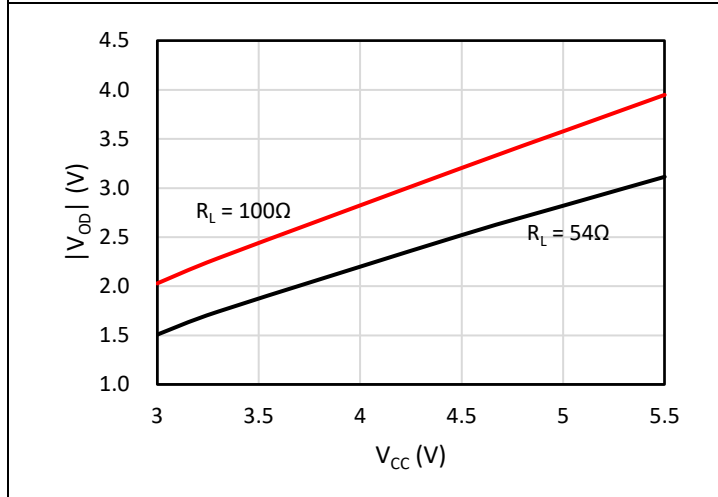


Figure 7-3 Differential Output Voltage vs Supply Voltage

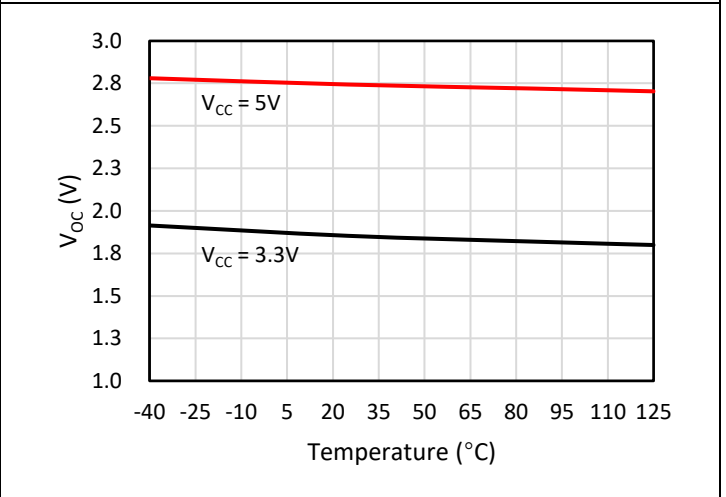


Figure 7-4 Common-Mode Output Voltage vs Temperature

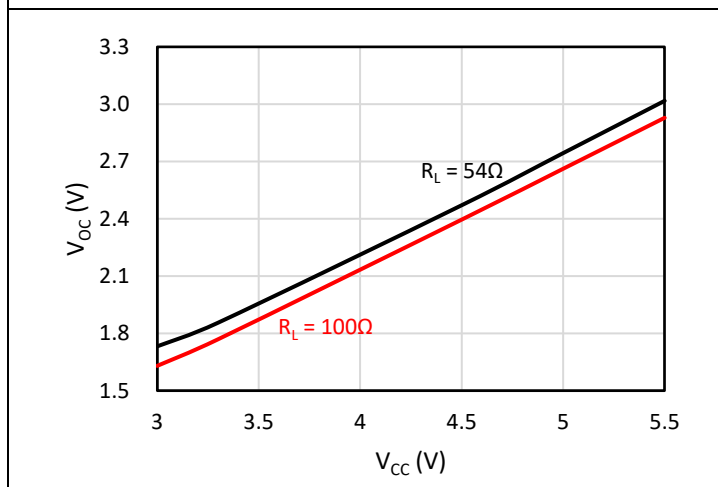


Figure 7-5 Common-Mode Output Voltage vs Supply Voltage

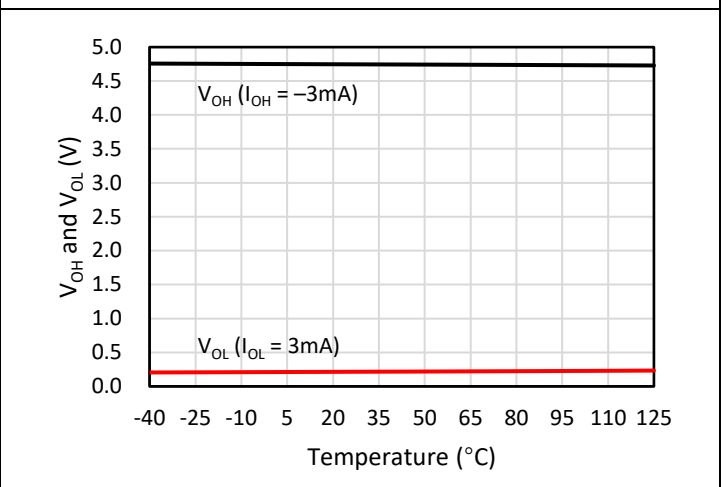


Figure 7-6 High- or Low-Level Output Voltage of RO vs Temperature

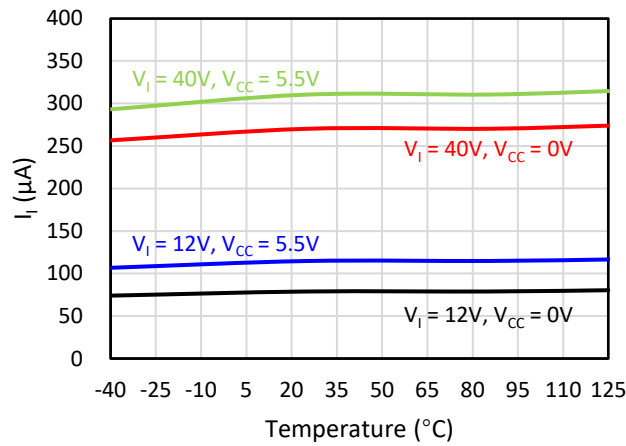


Figure 7-7 Bus Input Current vs Temperature @ $V_I = 12V$ or $40V$

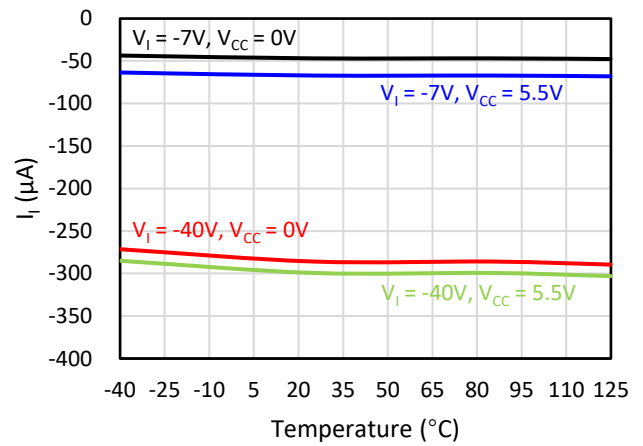


Figure 7-8 Bus Input Current vs Temperature @ $V_I = -7V$ or $-40V$

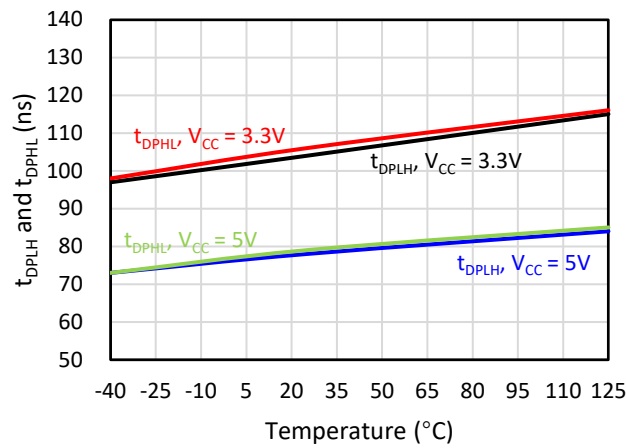


Figure 7-9 Driver Propagation Delay vs Temperature

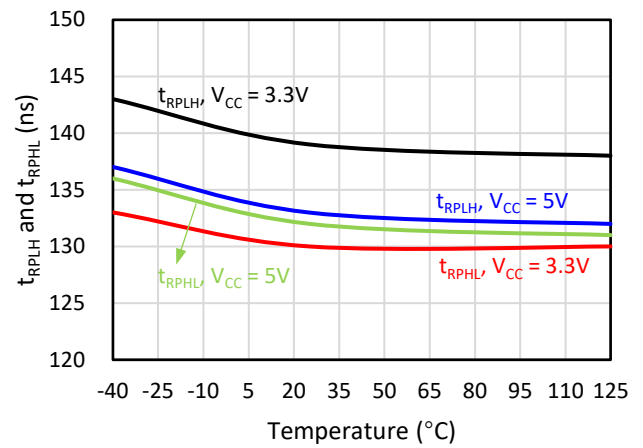


Figure 7-10 Receiver Propagation Delay vs Temperature

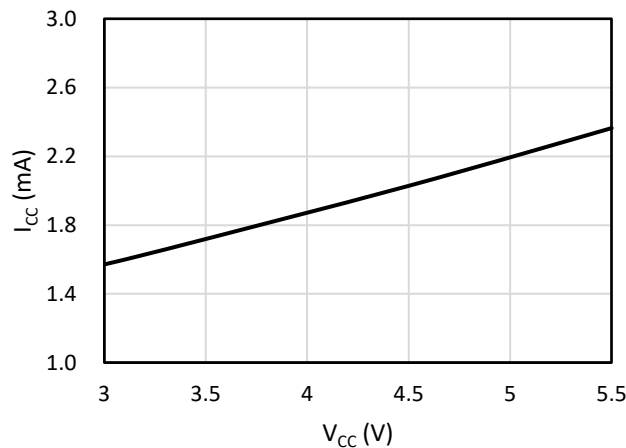


Figure 7-11 Quiescent Supply Current vs Supply Voltage

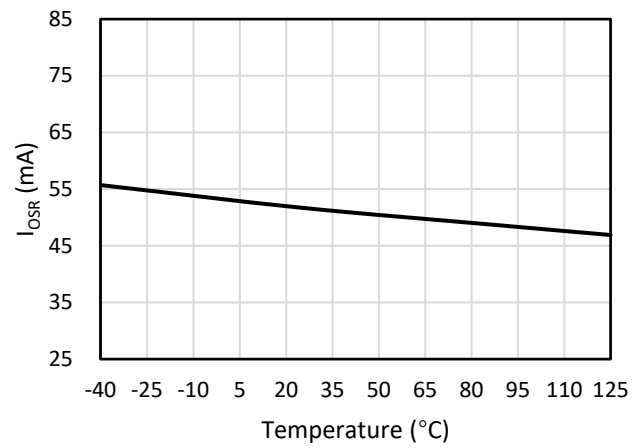


Figure 7-12 Receiver Short-Circuit Output Current vs Temperature

8 Parameter Measurement Information

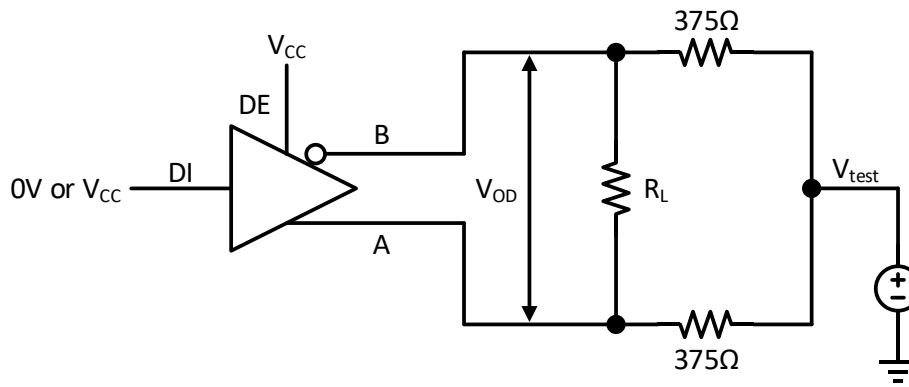


Figure 8-1 Measurement of Driver Differential Output Voltage With Common-Mode Load

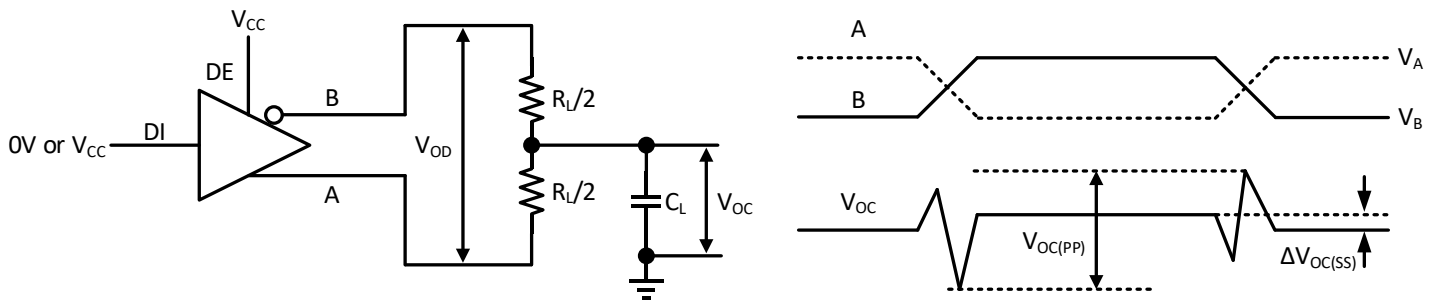


Figure 8-2 Measurement of Driver Differential and Common-Mode Output Voltage With RS-485 Load

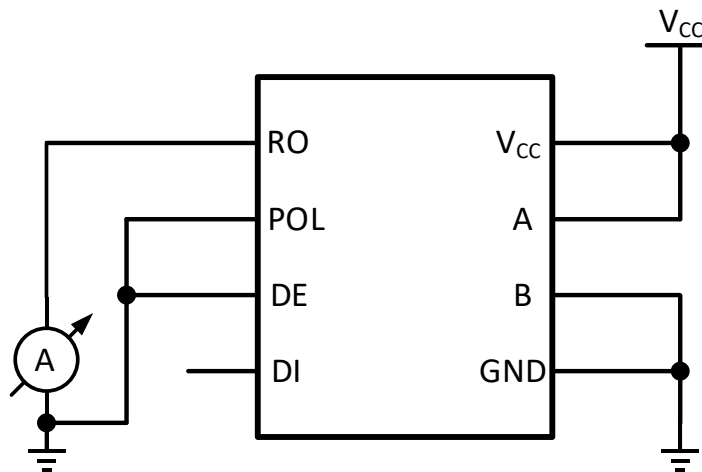


Figure 8-3 Measurement of Receiver Output Short Circuit Current

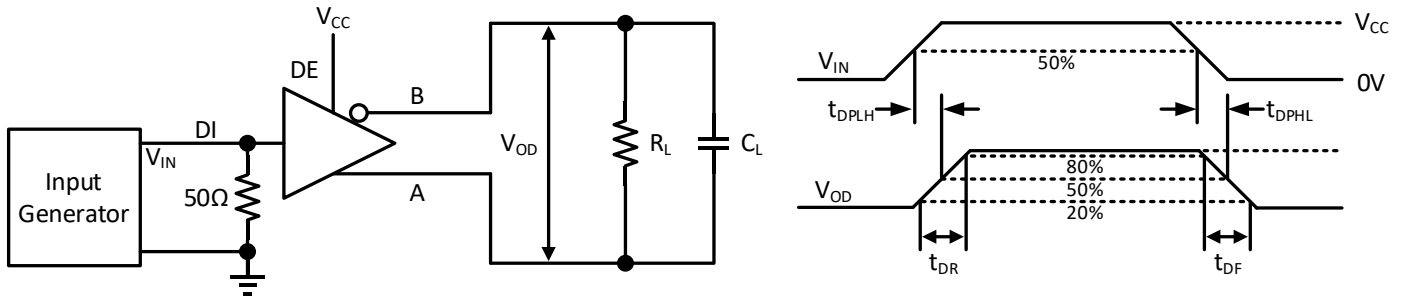


Figure 8-4 Measurement of Driver Output Rise and Fall Time and Propagation Delay

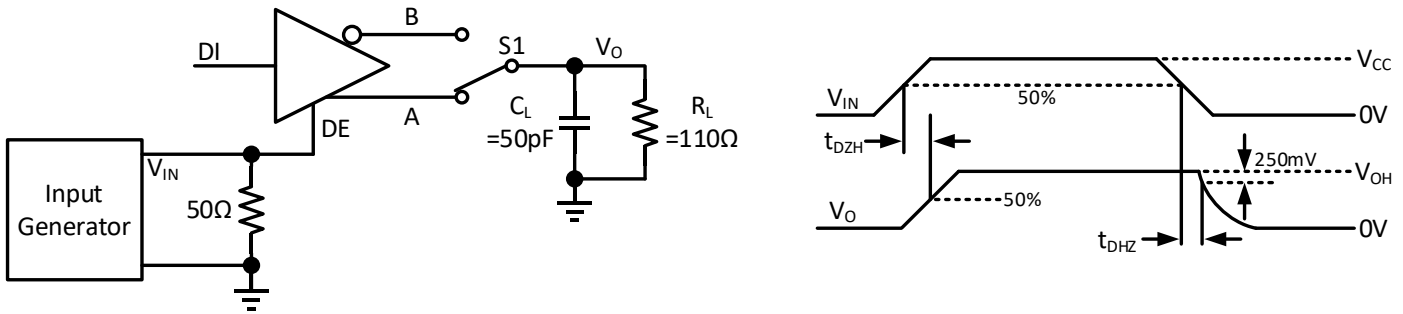


Figure 8-5 Measurement of Driver Enable and Disable Time With Active High Output and Pull-Down Load

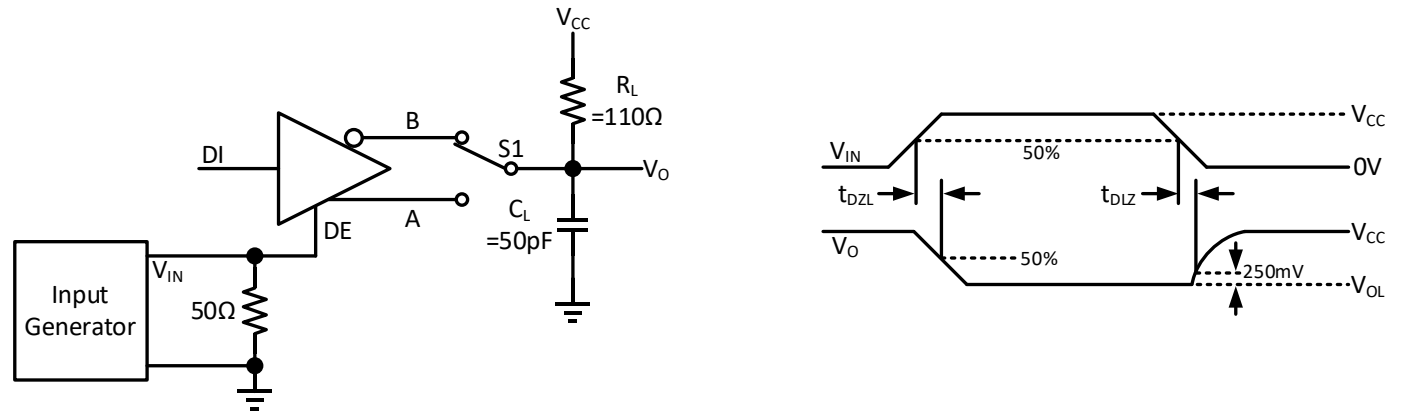


Figure 8-6 Measurement of Driver Enable and Disable Time With Active Low Output and Pull-Up Load

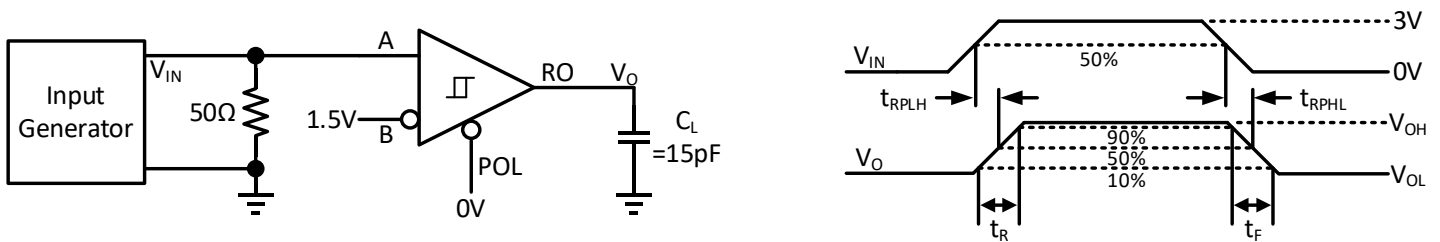


Figure 8-7 Measurement of Receiver Output Rise and Fall Time and Propagation Delay

9 Detailed Description

9.1 Device Feature Description

9.1.1 $\pm 65\text{V}$ fault protection on Bus Pins

The bus pins of transceivers connected to a RS-485 network often experience faults when shorted to voltages that exceed the -7V to 12V input range specified in the EIA/TIA-485 standard. Under such circumstances, ordinary RS-485 transceivers generally require costly external protection devices which can compromise the performance. To reduce system complexity and the requirements of external protection devices, The CA-IF4988S has $\pm 65\text{V}$ fault protection on bus pins with respect to ground whenever this device is under enabled, disabled or power-down mode. When the driver is enabled and the bus pins are short-circuited, the driver would limit the output short-circuit current within a certain range by the built-in current limiter firstly. If the absolute value of the bus pin's fault voltage is large, the device's junction temperature could increase rapidly to trigger the thermal shutdown protection. Once the device's junction temperature rises above the thermal shutdown temperature, the driver would be disabled and the outputs become high-impedance, resulting in the reduction of power consumption and thus avoiding further thermal damage.

9.1.2 $\pm 40\text{V}$ Common-Mode Range

RS-485 standards define the common-mode range as -7V to 12V for the receiver. However, the common-mode range of the CA-IF4988S exceeds the standard with $\pm 40\text{V}$ for both the driver and receiver. This feature was specifically designed for systems where there is a large common-mode voltage present due to either nearby electrically noisy equipment or large ground differences due to earth ground loop. Compared with ordinary RS-485 transceivers, $\pm 40\text{V}$ common-mode range could ensure that the CA-IF4988S communicates correctly in a broader range of applications.

9.1.3 Bus Failsafe Protection

The input threshold of the CA-IF4988S's receiver ranges from -20mV to -200mV when POL is held to low, which guarantees a logical high on the receiver output when the bus inputs are open, short or on idle state.

9.1.4 Hot Plug-in Protection

Inserting circuit boards into a powered backplane may cause voltage transients on DE and bus input pins that can lead to data errors. For example, upon initial circuit board insertion, the processor undergoes a power-up sequence. During this period, the high-impedance state of the output drivers makes them unable to drive the DE input to a defined logic level. Meanwhile, coupling noise from V_{CC} or GND could cause the input of DE to drift to an indeterminate logic state. The internal hot plug-in protection circuit on DE pin could avoid unwanted driver activation during hot-swap situations. The basic working principle of this circuit is to strongly pull down the input of DE at least $15\mu\text{s}$ when detecting the rising from low voltage of the power supply. After the power-up sequence, this hot plug-in protection circuit is bypassed and DE could receive the normal control signal from outside.

9.1.5 Thermal Shutdown Protection

The CA-IF4988S integrates thermal shutdown protection circuit. When the junction temperature rises above 185°C (typical value), the output of driver is disabled and the output of RO is high-impedance. When the junction temperature falls below 165°C (typical value), the output of both driver and receiver is re-enabled.

9.2 Device Function Mode

9.2.1 Driver

When the enable pin DE of driver is logical high, the differential outputs of A and B follow with the data input DI, as well as influenced by logical level at POL pin, which is shown in [Table 9-1](#).

When DE is logical low or open, the driver is disabled, the outputs of A and B are high-impedance and are irrelevant to the state at DI pin. DI pin is weakly pulled up to V_{CC} internally, the output of A is high while B is low when driver is enabled, DI's input is open and POL is logical low.

Table 9-1 Truth Table of Driver¹

POL ²	DE ³	DI ⁴	A	B
L	H	L	L	H
L	H	H	H	L
H	H	L	H	L
H	H	H	L	H
X	L	X	High-Z	High-Z

NOTE:

- H = high level, L = low level, X = irrelevant, High-Z = high impedance.
- POL is weakly pulled down to GND internally.
- DE is weakly pulled down to GND internally.
- DI is weakly pulled up to V_{CC} internally.

9.2.2 Receiver

After V_{CC} is powered up, the receiver is always enabled in normal operation, but would be disabled when the device triggers thermal shutdown. RO is high-impedance under thermal shutdown conditions.

The truth table of receiver is shown in [Table 9-2](#).

When POL is logical low and the bus differential input voltage V_{ID} is greater than or equal to -20mV, receiver output RO is logical high. When V_{ID} is less than or equal to -200mV, receiver output RO is logical low. When V_{ID} is between -20mV and -200mV, receiver output RO is indeterminate.

When POL is logical high and the bus differential input voltage V_{ID} is greater than or equal to 200mV, receiver output RO is logical low. When V_{ID} is less than or equal to 20mV, receiver output RO is logical high. When V_{ID} is between 20mV and 200mV, receiver output RO is indeterminate.

When POL is logical low and the bus inputs are open, short or on idle state, a failsafe logic high output at RO pin is achieved. Under such conditions while POL is logical high, a failsafe logic low output at RO pin is achieved.

Table 9-2 Truth Table of Receiver

POL	V _{ID} = (V _A - V _B)	RO
L	≥ -20mV	H
	-200mV < V _{ID} < -20mV	?
	≤ -200mV	L
H	≤ 20mV	H
	20mV < V _{ID} < 200mV	?
	≥ 200mV	L
L	Open/Short/Idle	H
H	Open/Short/Idle	L

NOTE: H = high level, L = low level, ? = indeterminate.

10 Application and Implementation

10.1 Typical Application

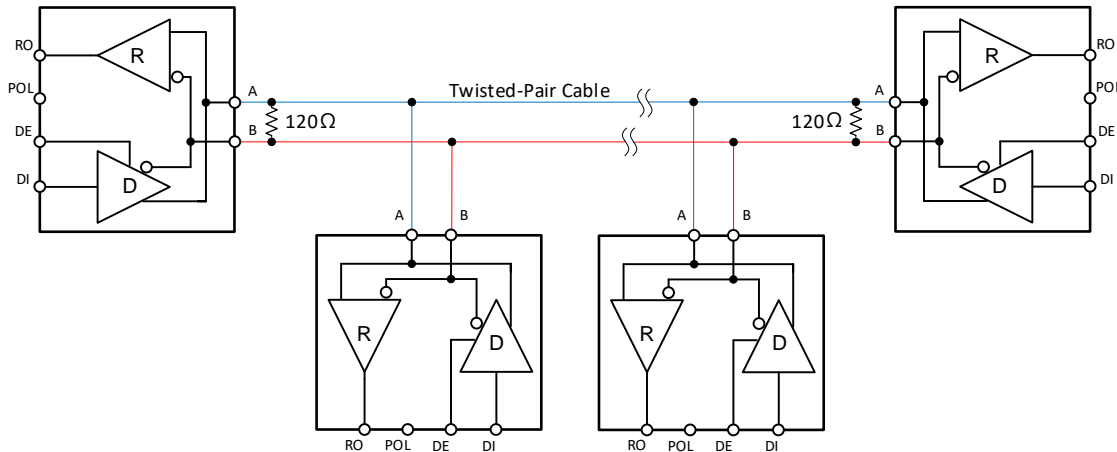


Figure 10-1 Typical RS-485 Network

The typical RS-485 network consists of multiple transceivers connecting in parallel to a bus cable. To eliminate the line reflection, both ends of the cable terminate a termination resistor R_T which should be matched to the characteristic impedance Z_0 of the cable. At the same time, please keep the stub lengths off the main line as short as possible. This parallel termination method could achieve higher data rates over longer cable length. The typical RS-485 network utilizing CA-IF4988S is shown in [Figure 10-1](#).

If certain node's transceiver is cross-wired in field cables which results in inverting bus polarity, it could be corrected to set POL to high by controller allowing for software correction.

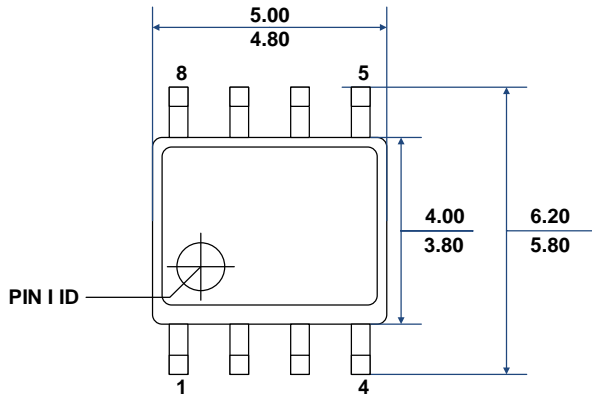
10.2 Power Supply Recommendation

To ensure reliable operation at all data rates and supply voltages, each supply should be decoupled with 0.1 μ F and at least 1 μ F ceramic capacitors located as close as possible to the supply pins. This helps to reduce supply voltage ripple present on the outputs of switched-mode power supplies and also helps to compensate for the resistance and inductance of the PCB power planes. At the same time, please keep the voltage in V_{CC} pin with respect to GND pin is below 5.5V.

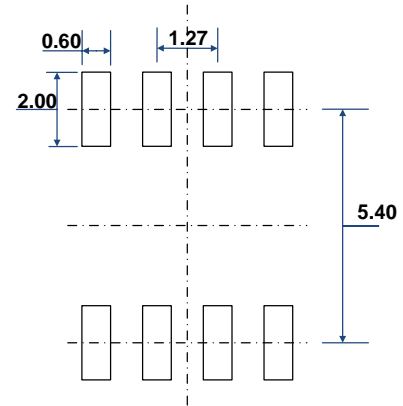
11 Package Information

11.1 SOIC8 (S) Package

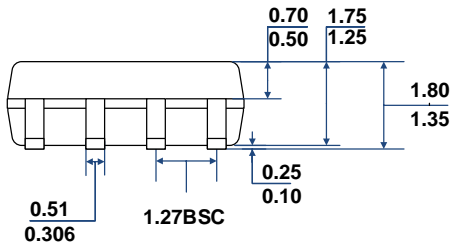
The values for the dimensions are shown in millimeters.



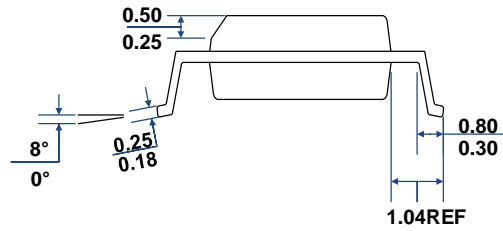
TOP VIEW



RECOMMENDED LAND PATTERN



FRONT VIEW



LEFT-SIDE VIEW

12 Soldering Information

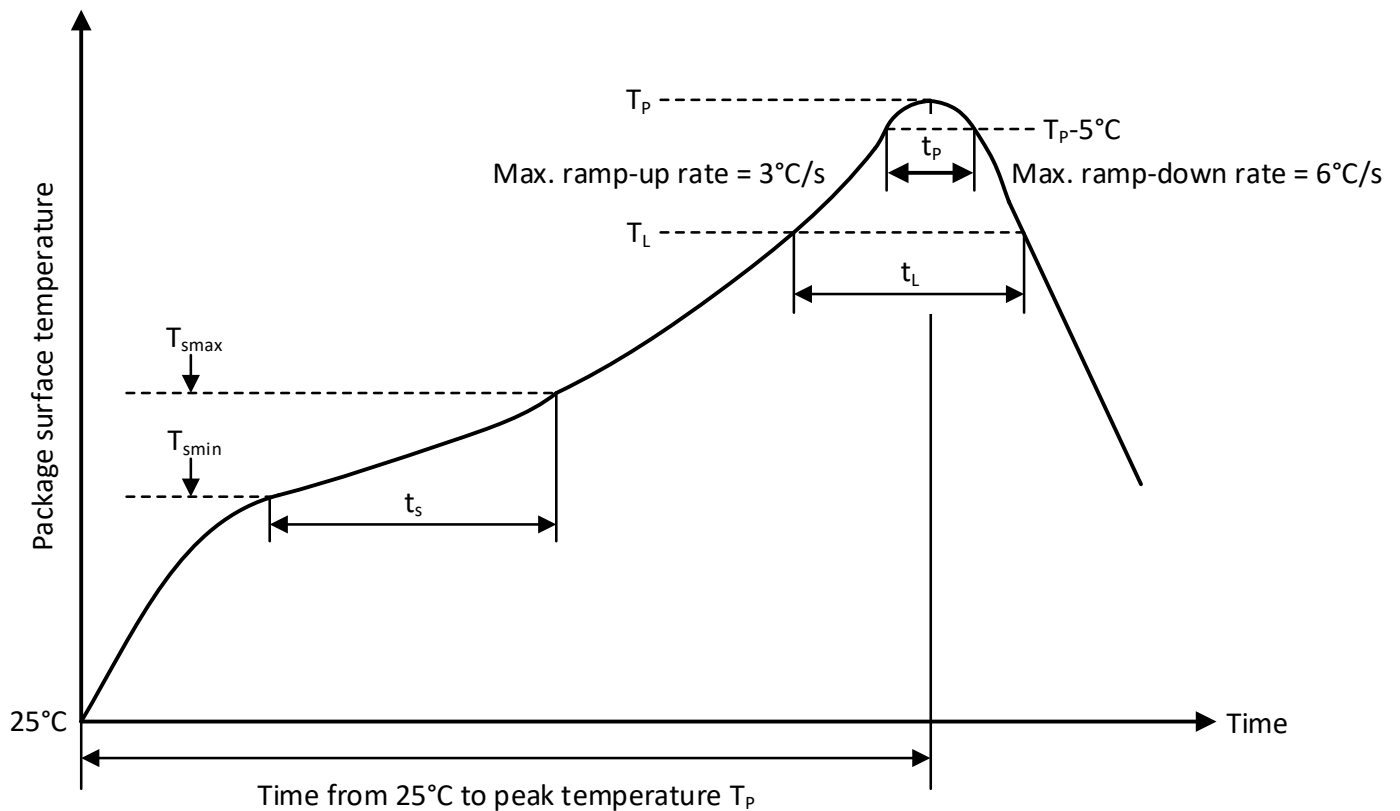


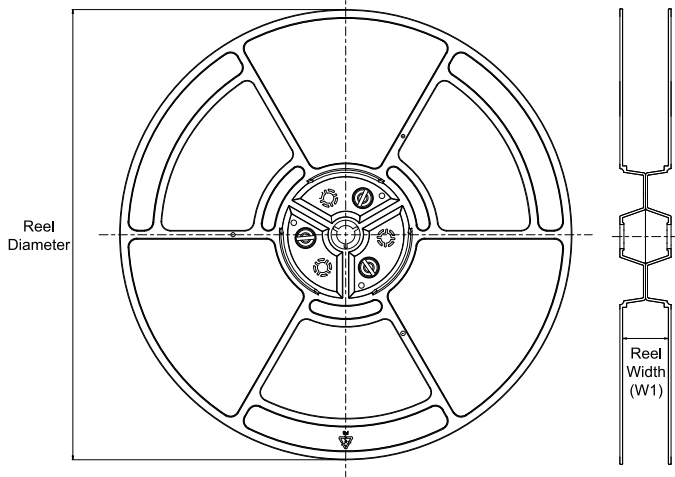
Figure 12-1 Soldering Temperature Curve

Table 12-1 Soldering Temperature Parameters

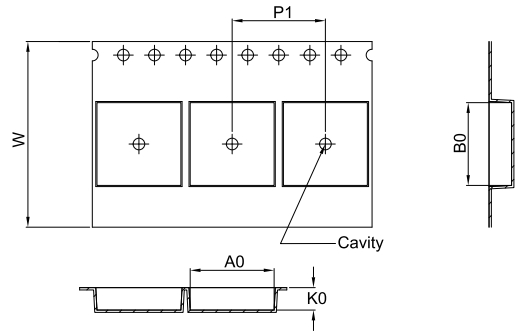
Profile Feature	Pb-Free Soldering
Ramp-up rate ($T_L = 217^\circ\text{C}$ to peak T_p)	3°C/s max
Time t_s of preheat temp ($T_{smin} = 150^\circ\text{C}$ to $T_{smax} = 200^\circ\text{C}$)	60~120 seconds
Time t_L to be maintained above 217°C	60~150 seconds
Peak temperature T_p	260°C
Time t_p within 5°C of actual peak temp	30 seconds max
Ramp-down rate (peak T_p to $T_L = 217^\circ\text{C}$)	6°C/s max
Time from 25°C to peak temperature T_p	8 minutes max

13 Tape and Reel Information

REEL DIMENSIONS

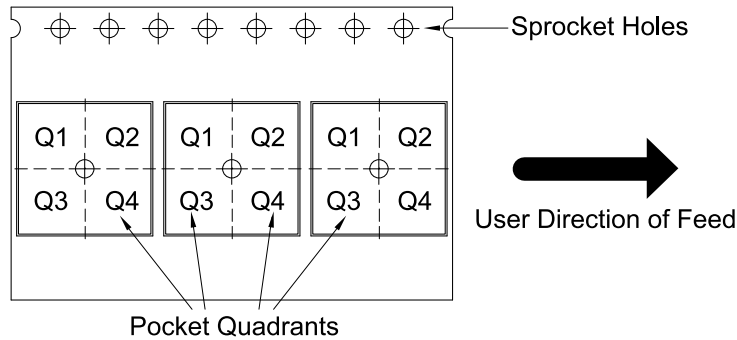


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CA-IF4988S	SOIC	S	8	2500	330	12.4	6.5	5.4	2.1	8.0	12.0	Q1

14 Important Notice

The above information is for reference only and is used to assist Chipanalog customers in design and development. Chipanalog reserves the right to change the above information due to technological innovation without prior notice.

Chipanalog products are all factory tested. The customers shall be responsible for self-assessment and determine whether it is applicable for their specific application. Chipanalog's authorization to use the resources is limited to the development of related applications that the Chipanalog products involved in. In addition, the resources shall not be copied or displayed. And Chipanalog shall not be liable for any claim, cost, and loss arising from the use of the resources.

Trademark Information

Chipanalog Inc. ®, Chipanalog® are trademarks or registered trademarks of Chipanalog.



<http://www.chipanalog.com>