CA-IS302x Low Power Bidirectional I2C Isolator Test Board Instructions

General Description

This document outlines the instructions for utilizing the CA-IS302x test board, which includes an overview of the chip, a schematic diagram, a PCB wiring diagram, a bill of materials, and a portion of the test data, among other things. The CA-IS302x evaluation board can be used to assess the performance of the chip's parameters for the forward and reverse channels, among other applications.

CA-IS302x Introduction

The CA-IS302x series is a comprehensive, bidirectional, dual-channel digital isolator offering 3.75kVRMS (narrow body package), 5kVRMS (wide body package), and 7.5kV (ultra-wide body package) galvanic isolation, with typical CMTIs up to ±150kV/μs. All devices feature Schmitt triggers, which enhance immunity. Each isolated channel features digital inputs and outputs separated by a silicon dioxide (SiO_2) insulating layer, ensuring high EMI rejection and low EMI characteristics. The highly integrated design requires only two external VDDA, VDDB bypass capacitors and pull-up resistors to form an I2C isolated interface, offering customers a simple and cost-effective solution.

The CA-IS302x series is capable of supporting DC to 2.0MHz transfer rates. The CA-IS3020 offers two bi-directional, open-drain output isolation channels, ideal for bi-directional isolation applications such as multi-homed I2C, where bi-directional transfer of data or clocks on the same bus is required. The CA-IS3021 provides one uni-directional and one bi-directional isolation channel, making it suitable for single-homed I2C isolation applications. The CA-IS3021 offers a single unidirectional and one bidirectional isolation channel, ideal for single host I2C isolation applications. The unidirectional channel is designed for clock (SCL) isolation, while the bidirectional channel is optimized for data (SDA) isolation.

The CA-IS3020x series comprises seven models, as detailed in the table below. In this article, we will use the CA-IS3020G as an example to demonstrate the use of the CA-IS3020x beta version.

Table 1. Device information

Part #	Bidirectional isolated channel	One-way isolated channel	Galvanic Isolation (kV_{RMS})	Output type	package
CA-IS3020S	2	0	3.75	open-drain output	SOIC8(S)
CA-IS3020G	2	0	5	open-drain output	SOIC8-WB (G)
CA-IS3020W	2	0	5	open-drain output	SOIC16-WB (W)
CA-IS3020WG	2	0	7.5	open-drain output	SOIC8-WWB (WG)
CA-IS3021S	1	1	3.75	open-drain output	SOIC8(S)
CA-IS3021G	1	1	5	open-drain output	SOIC8-WB (G)
CA-IS3021W	1	1	5	open-drain output	SOIC16-WB (W)

CA-IS302x EVM Board

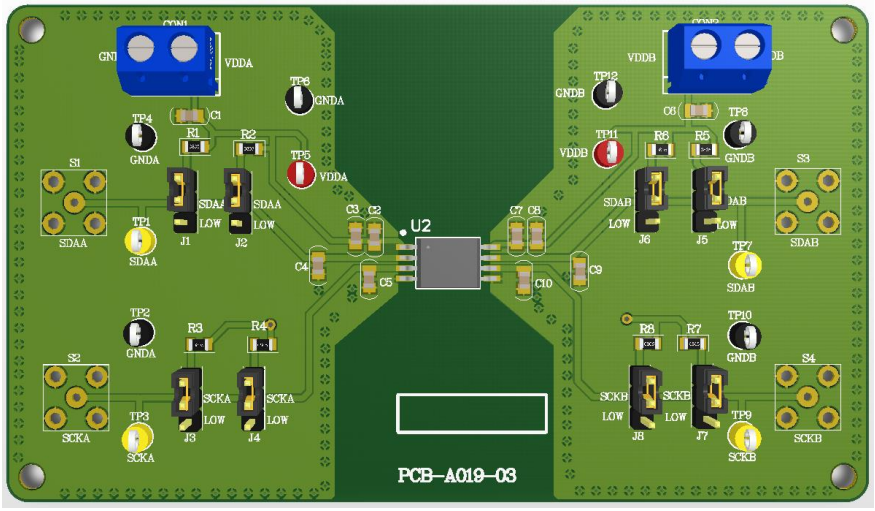

Figure 1. The CA-IS3020G PCB

CA-IS302x EVM Schematic

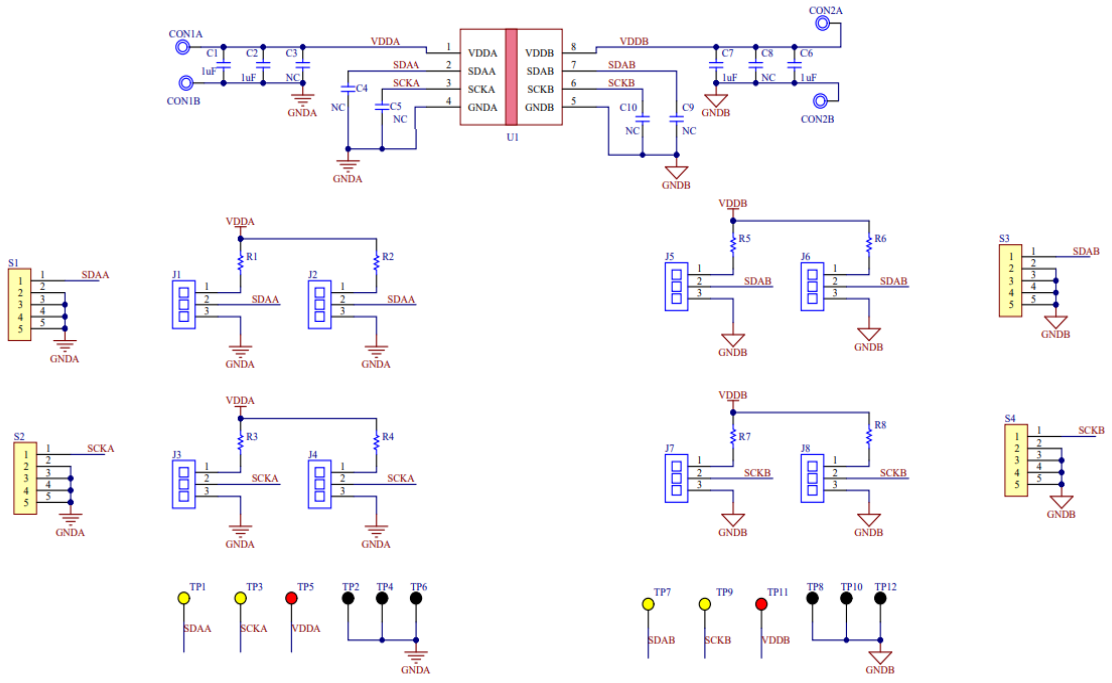

Figure 2. CA-IS3020G EVM Schematic

CA-IS302x EVM PCB Layouts

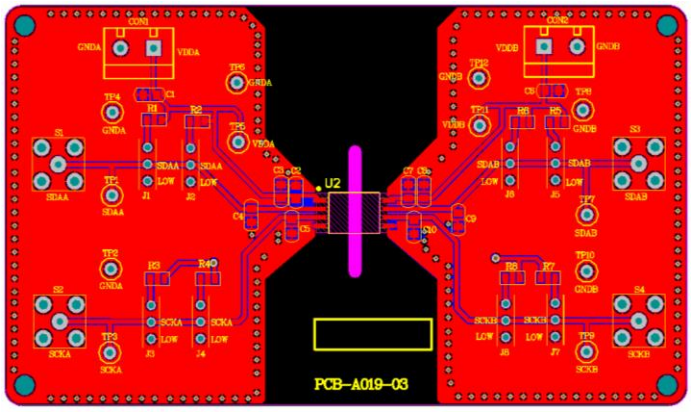

Figure 3. The CA-IS3020G EVM PCB Layout_ Top

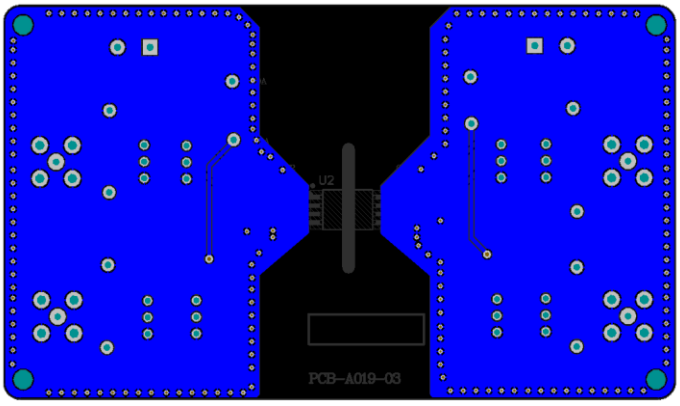

Figure 4. The CA-IS3020G EVM PCB Layout_ Bottom

EVM Bill of Materials

Item	Ref Des	Qty	Description	Package	MFR	PN.
1	CON1, CON2	2	CONN, 5.08mm, Rising Cage Clamp	KF301-5.0-2P	-	-
2	C1, C2, C6, C7	4	MLCC, 1μF/10V, X7R	0805	-	Standard
3	C3, C4, C5, C8, C9, C10	6	NA	-	-	-
4	R1, R3	2	Resistor, 1.43kΩ, 1%	0805	-	Standard
5	R2, R4	2	Resistor, 953Ω, 1%	0805	-	Standard
6	R5, R7	2	Resistor, 143Ω, 1%	0805	-	Standard
7	R6, R8	2	Resistor, 95.3Ω, 1%	0805	-	Standard
8	S1, S2, S3, S4	4	SMA Connect, 2.54mm	-	-	Standard
9	U1	1	CA-IS3020G	SOIC8-WB	Chipanalog	
10	TP5, TP11	2	Test Point, Red, Through Hole, 1mm	-	Keystone	5000
11	TP1, TP3, TP7, TP9	4	Test Point, Yellow, Through Hole, 1mm	-	Keystone	5009
12	TP2, TP4, TP6, TP8, TP10, TP12,	6	Test Point, Black, Through Hole, 1mm	-	Keystone	5001
13	J1, J2, J3, J4, J5, J6, J7, J8	8	Header, 3 pin, 2.54mm	-	-	Standard

Test Equipment

- Power Supplies
- 500MHz Wideband Oscilloscope (Agilent DSOX3054T)
- Signal Generator

Hardware Setup

Please find below an example of the input from SDAB and the corresponding output from SDAA.

1. Connect the two voltages from the DC voltage source to CON1 and CON2;
2. Output a signal of a certain frequency and amplitude from a signal generator and connect it to the S3 terminal (i.e., the SDAB pin of the CA-IS3020G);
3. Observe the waveforms on terminals S3 and S1 (i.e., SDAA pin of the CA-IS3020G) with an oscilloscope;
4. You may also pass the jumper cap J5/J6, directly pull down to GNDB or through the pull-up resistor R3/R4 of VDDB;
5. It is possible to refer to the signaling from SCKB to SCKA, another channel of the CA-IS3020G, in the same way as the signaling from SDAB to SDAA.

Please note the following specifications of the CA-IS3020G product:

1. Both channels of the CA-IS3020G product are bi-directional data transmission, allowing for input from either the A or B side.
2. The data transfer between SCKA and SCKB of the CA-IS3021G is unidirectional, with the signal only able to be input from SCKA and output from SCKB.

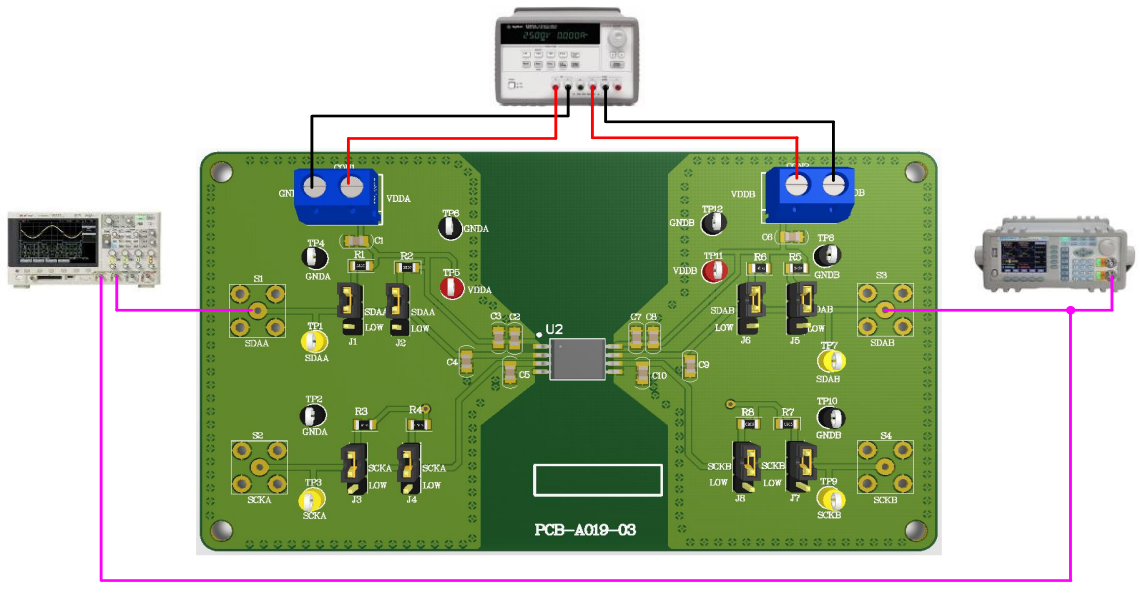

Figure 5. Hardware Setup Diagram

Typical Characteristics

The following illustration depicts a typical waveform of the transmission from channel SDAB to SDAA of the CA-IS3020G.

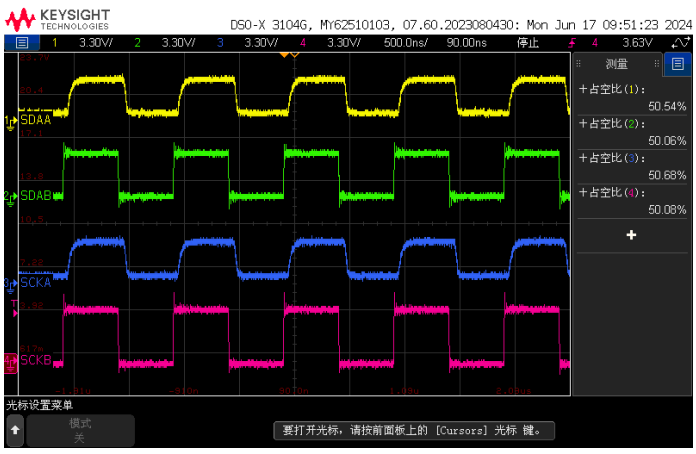

Figure 6.
SDAB->SDAA Typical communication rate waveform
VDDA=VDDB=3.3V

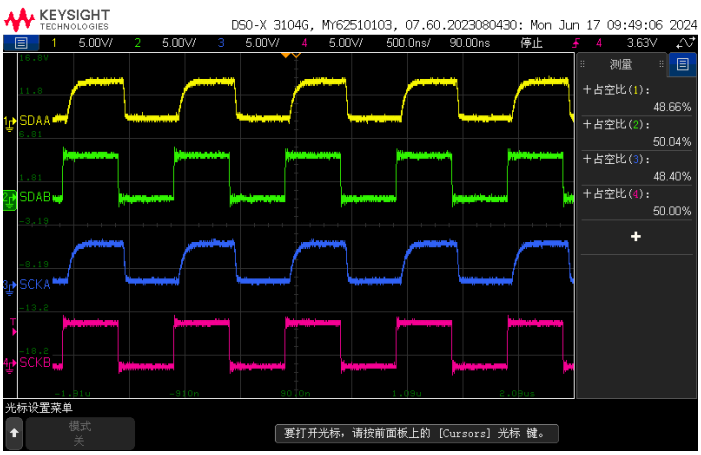

Figure 7.
SDAB->SDAA Typical communication rate waveform
VDDA=VDDB=5V

Revision History

Revision Number	Revision Date	Description
Rev1.0	Jan. 2021	Preliminary-Datasheet
Rev1.1	Sep. 2024	Updated PCB and schematic, changed measurement data and waveforms, added table 1.

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