Reliability Test Report

Product Name: CA-IS38XX

Report Version: V1.2

Contents

1. Overview

Reliability testing of microelectronic products is a risk mitigation process designed to ensure the service life of device in customer applications. Semiconductor wafer manufacturing process and package-level reliability can be assessed in a variety of ways and may include accelerated environmental test conditions. Chipanalog evaluates manufacturability of the device to verify a robust silicon and assembly flow to ensure continuity of supply to customers. Chipanalog qualifies new devices, significant changes, and product families based on JEDEC JESD47. CA-IS38XX series chips are packaged with the same wafer. The differences between part numbers are the package and bonding diagram. The data shown is representative of the material sets, processes, and manufacturing sites used by the device family.

2. Part Number List

Package Type	Part Number
SOIC16-WB(W)	CA-IS3830LW/CA-IS3830HW/CA-IS3831LW/CA-IS3831HW/CA-IS3840LW/ CA-IS3840HW/CA-IS3841LW/CA-IS3841HW/CA-IS3842LW/CA-IS3842HW/ CA-IS3860LW/CA-IS3860HW/CA-IS3861LW/CA-IS3861HW/CA-IS3862LW/ CA-IS3862HW/CA-IS3863LW/CA-IS3863HW
SOIC16-WWB(WW)	CA-IS3821LWW/CA-IS3821HWW/CA-IS3830LWW/CA-IS3830HWW/CA-IS3831LWW/ CA-IS3831HWW/CA-IS3840LWW/CA-IS3840HWW/CA-IS3841LWW/CA-IS3841HWW/ CA-IS3842LWW/CA-IS3842HWW

Note: JEDEC specification is designed to also qualify a family of similar components utilizing the same fabrication process, design rules, and similar circuits. The family qualification may also be applied to a package family where the construction is the same and only the size and number of leads differs.

3. Product Information

3.1. Wafer Information

Wafer ID	TAIYI
Die Tech	BCDXXX

3.2. Package Information

Assembly site	JCET-D8	JCET-D8
FT site	JCET-D8	JCET-D8
Package	SOIC16-WB	SOIC16-WWB
Lead frame	Cu	Cu
Bond wire	20um Au	20um Au
MSL level	MSL3	MSL3

4. Reliability Qualification Plan

4.1. Device Qualification Test Requirements

Stress	Ref.	Abbv.	Conditions	Duration /Accept
Electrical Parameter Assessment	JESD86	ED	Per Datasheet	Per Datasheet
High Temperature Operating Life	JESD22-A108, JESD85	HTOL	$T_J \geq 125°C$ $V_{CC} \geq V_{CC}$ max	1000 hrs/0 Fail
Human Body Model ESD	JS-001	ESD-HBM	$T_A = 25°C$	Classification
Charged Device Model ESD	JS-002	ESD-CDM	$T_A = 25°C$	Classification
Latch-Up	JESD78	LU	Class I or Class II	Classification

4.2. Nonhermetic Package Qualification Test Requirements

Stress	Ref.	Abbv.	Conditions	Duration /Accept
MSL Preconditioning	JESD22-A113	PC	Per appropriate MSL level per J-STD-020	Electrical Test (optional)
High Temperature Storage	JESD22-A103 & A113	HTSL	150°C, 1000 hrs	1000 hrs/0 Fail
Temperature Humidity Bias	JESD22-A101	THB	85°C, 85% RH, V_{CC} max	1000 hrs/0 Fail
Highly Accelerated Temperature and Humidity Stress	JESD22-A110	HAST	130°C/110°C, 85% RH, V_{CC} max	96/264 hrs/0 Fail
Temperature Cycling	JESD22-A104	TC	-65°C to 150°C	500 cycles/0 Fail
Unbiased Temperature/Humidity	JESD22-A102	AC	121°C, 100% RH, 29.7psia	96 hrs/0 Fail
Bond Pull Strength	M2011	BPS	Characterization, Pre Encapsulation	Ppk≥1.66 or Cpk≥1.33
Bond Shear	JESD22-B116	BS	Characterization, Pre Encapsulation	Ppk≥1.66 or Cpk≥1.33
Solderability	JESD22-B102	SD	Characterization	95% coverage

Note: Either HAST or THB may be chosen.

5. Reliability Test Results

5.1. Device Reliability Test Results

Stress	Condition	Duration	Sample Size	Result	Classification
ED	Per Datasheet	/	10*3 lot	Pass	/
HTOL[1]	Ta=125°C，Vcc=5.5V	1000hrs	77*3 lot	Pass	/
HTOL[2]	T_A = 125°C, V_{CC} = 5.5V	1000hrs 2000hrs 3000hrs	77*1 lot	Pass	/
ESD-HBM	T_A = 25°C	/	3*1 lot	Pass	Class 3B
ESD-CDM	T_A = 25°C	/	3*1 lot	Pass	Class C3
LU	T_A = 25°C	/	3*1 lot	Pass	Class I A

Note1：3 lot HTOL data refers to generic data of the same product family CA-IS37XX.

Note2：1 lot HTOL data comes from CA-IS3841HW qual data and T2000 and T3000 are performed with customer special requirement.

5.2. Package Reliability Test Results

Package Type: SOIC16-WB				
Stress	**Condition**	**Duration**	**Sample size**	**Results**
PC	MSL 3	/	231*3 lot	Pass
HTSL	T_A = 150°C	1000 hrs	77*3 lot	Pass
HAST	130°C, 85% RH, 5.5V	96 hrs	77*3 lot	Pass
TC	-65°C to 150°C	500 cycles	77*3 lot	Pass
AC	121°C, 100% RH, 29.7 psia	96 hrs	77*3 lot	Pass
BS	JESD22-B116	/	30 bonds/5 ea.	Pass
BPS	M2011	/	30 bonds/5 ea.	Pass
SD	Steam aging, 245°C dipping	5s	22 leads*3 lot	Pass
Package Type: SOIC16-WWB				
Stress	**Condition**	**Duration**	**Sample size**	**Results**
PC	MSL 3	/	231*1 lot	Pass
HTSL	T_A = 150°C	1000 hrs	77*1 lot	Pass
HAST	130°C, 85% RH, 5.5V	96 hrs	77*1 lot	Pass
TC	-65°C to 150°C	500 cycles	77*1 lot	Pass
AC	121°C , 100% RH, 29.7 psia	96 hrs	77*1 lot	Pass
BS	JESD22-B116	/	30 bonds/5 ea.	Pass

BPS	M2011	/	30 bonds/5 ea.	Pass
SD	Steam aging, 245°C dipping	5s	22 leads*1 lot	Pass

6. Conclusion

CA-IS38XX series products are qualified with JEDEC standards.

Disclaimer

This information is provided to assist customers in design and development. It could change for technology innovation without notice.

The devices are shipped after passing final test. Customers are responsible to conduct sufficient engineering and additional qualification testing to determine whether a device is suitable for use in their applications.

License to customers to use the information is limited to the development of applications using the device. Apart from above, the information shall not be reproduced or displayed, and Chipanalog shall not be liable for any claims, compensation, costs, losses or liabilities arising out of the use of the information.

Trademarks

Chipanalog Inc.®、Chipanalog® are trademarks of Chipanalog.

Revision History

Revision	Change Log	Date
V0.5	Preliminary release	Mar, 2023
V1.0	HTOL pass 1000hrs	Apr, 2023
V1.1	1. HTOL pass 3000hrs 2. Complete HAST & AC test condition information	Oct, 2023
V1.2	Add HTOL and W package qualification lot information	Jan, 2024