AEC-Q100 Qualification Report

Product Series： CA-IF1021LS-Q1

Report Version： V 1.0

Reference Doc.： AEC-Q100-REV-H

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Contents

1. Overview 3

2. Part Number List 3

3. Production Information 3

   3.1. Wafer information 3

   3.2. Package information 3

4. Reliability Qualification Plan 4

5. Reliability Test Results 6

6. MTBF&FIT 7

7. Conclusion 7

Appendix 1: EMC Test Results 9

Appendix 2: SAT Test Results 10

1. Overview

Reliability testing of microelectronic products is a risk mitigation process designed to ensure the service life of device in customer applications. Semiconductor wafer manufacturing process and package-level reliability can be assessed in a variety of ways and may include accelerated environmental test conditions. Chipanalog evaluates manufacturability of the device to verify a robust silicon and assembly flow to ensure continuity of supply to customers. Chipanalog qualifies new devices, significant changes, and product families based on AEC-Q100.

2. Part Number List

Package Type	Part Number
SOIC8-NB(S)	CA-IF1021LS-Q1

Note： AECQ-100 provides the guideline for the use of generic data to accelerate and streamline the qualification process. Products sharing the same major product, process and materials elements may be categorized in a product qualification family.

3. Production Information

3.1. Wafer information

Fab site	SMIC
Wafer	LYNX
Fab Process	18BCDA

3.2. Package information

Assembly site	JCET
FT site	JCET
Package	SOIC8-NB(S)
Lead Frame	Cu
Bond wire	20um Au
MSL level	MSL1
Operation Temp.	Grade 1(-40°C - 125°C)

4. Reliability Qualification Plan

<table>
<tr><th colspan="6">Test Group A–Accelerated Environment Stress Tests</th></tr>
<tr><th>Group</th><th>Item</th><th>Refer.</th><th>Test condition</th><th>QTY</th><th>Remark</th></tr>
<tr><td>A1</td><td>PC</td><td>J-STD-020
JESD22-A113</td><td>Test @ Rm, SMD only, Moisture Preconditioning before THB/BHAST, AC/UHAST, TC, and PTC stress, MSL = 1, Peak Reflow Temp = 260°C</td><td>77 pcs*3 lots</td><td></td></tr>
<tr><td>A2</td><td>BHAST</td><td>JESD22-A110</td><td>BHAST: 130°C, 85% RH, V_{cc1}= 27V, V_{cc2}= 5.5V, 96 hrs (Test @ Rm/Hot)</td><td>77 pcs*3 lots</td><td></td></tr>
<tr><td>A3</td><td>UHAST</td><td>JESD22-A101</td><td>UHAST: 130°C, 85% RH, 96 hrs (Test @ Rm)</td><td>77 pcs*3 lots</td><td></td></tr>
<tr><td>A4</td><td>TC</td><td>JESD22-A104</td><td>-65°C-150°C, 500 cycles (Test @Rm/ Hot)</td><td>77 pcs*3 lots</td><td></td></tr>
<tr><td>A5</td><td>PTC</td><td>JESD22-A105</td><td>-40°C-125°C, 1000 cycles (Test @ Rm/Hot)</td><td>NA</td><td>△T<40℃</td></tr>
<tr><td>A6</td><td>HTSL</td><td>JESD22-A103</td><td>T_a = 150°C, 1000 hrs (Test @ Rm/Hot)</td><td>45 pcs*1 lot</td><td></td></tr>
<tr><th colspan="6">Test Group B–Accelerated Lifetime Simulation Tests</th></tr>
<tr><th>Group</th><th>Item</th><th>Refer.</th><th>Test condition</th><th>QTY</th><th>Remark</th></tr>
<tr><td>B1</td><td>HTOL</td><td>JESD22-A108</td><td>T_a = 125°C, V_{cc1}= 27V, V_{cc2}= 5.5V, 1000 hrs (Test @ Rm/Cold/Hot)</td><td>77 pcs*3 lots</td><td></td></tr>
<tr><td>B2</td><td>ELFR</td><td>AEC-Q100-008</td><td>T_a = 125°C, V_{cc1}= 27V, V_{cc2}= 5.5V, 48 hrs (Test @ Rm/Hot)</td><td>800 pcs*3 lots</td><td></td></tr>
<tr><td>B3</td><td>EDR</td><td>AEC-Q100-005</td><td>Test @ Rm/Hot</td><td>NA</td><td>Not memory</td></tr>
<tr><th colspan="6">Group C–Package Assembly Integrity Tests</th></tr>
<tr><th>Group</th><th>Item</th><th>Refer.</th><th>Test condition</th><th>QTY</th><th>Remark</th></tr>
<tr><td>C1</td><td>WBS</td><td>AEC-Q100-001
AEC-Q003</td><td>Cpk > 1.67, T0 samples</td><td>30 bonds from 5 pcs</td><td></td></tr>
<tr><td>C2</td><td>WBP</td><td>MIL-STD883
AEC-Q003</td><td>Cpk > 1.67, T0 samples</td><td>30 bonds from 5 pcs</td><td></td></tr>
<tr><td>C2</td><td>WBP</td><td>MIL-STD883
AEC-Q003</td><td>0 fails, post-TC samples</td><td>30 bonds from 5 pcs</td><td></td></tr>
<tr><td>C3</td><td>SD</td><td>J-STD-002</td><td>> 95% coverage, 8hr steam aging prior to testing</td><td>15 pcs*1 lot</td><td></td></tr>
<tr><td>C4</td><td>PD</td><td>JESD22-B100
JESD22-B108
AEC-Q003</td><td>Cpk > 1.67</td><td>10 pcs*3 lots</td><td></td></tr>
<tr><td>C5</td><td>SBS</td><td>AEC-Q100-010
AEC-Q003</td><td>Cpk > 1.67, 5 balls from min. of 10 devices</td><td>NA</td><td>No solder ball</td></tr>
<tr><td>C6</td><td>LI</td><td>JESD22-B105</td><td>10 leads from each of 5 devices</td><td>NA</td><td>SMD</td></tr>
</table>

Test Group D–Die Fabrication Reliability Tests

Group	Item	Refer.	Test condition	QTY	Remark
D1	EM	JESD61	---	---	Done by Fab
D2	TDDB	JESD35	---	---	Done by Fab
D3	HCI	JESD60 & 28	---	---	Done by Fab
D4	BTI	JESD90	---	---	Done by Fab
D5	SM	JESD61, 87, & 202	---	---	Done by Fab

Group E-Electrical Verification Tests

Group	Item	Refer.	Test condition	QTY	Remark
E1	TEST	per datasheet	Pre and Post Stress Electrical Test	All	
E2	HBM	AEC Q100-002	±500V， ±1KV， ±2KV， ±8KV (Test @ Rm/Hot)	3 pcs*1 lot	
E3	CDM	AEC-Q100-011	±250V， ±500V， ±750V， ±2KV (Test @ Rm/Hot)	3 pcs*1 lot	
E4	LU	AEC-Q100-004	125℃, I-trigger ±200mA(Test @ Rm/Hot)	3 pcs*1 lot	
E5	ED	AEC-Q100-009	CPK＞1.67(Test @ Rm/Cold/Hot)	30 pcs*3 lots	
E9	EMC	SAE J1752/3	Electromagnetic Compatibility (Radiated Emissions)	1 pcs*1 lot	
E10	SC	AEC-Q100-012	/	NA	Not smart power
E11	SER	JESD89-1/-2/-3	/	NA	Analog device
E12	LF	AEC-Q005	/	2 pcs*3 lots	

Group S-Special Requirement Tests

S1	BLR-Bending	JESD22-B113	Align with customer	NA	
S2	BLR-Drop	JESD22-B11	Align with customer	NA	
S3	BLR-TC	IPC-9701	Refer test requirement	NA	
S4	BLR-Vibration	JESD22-B103	Refer test requirement	NA	

Note：Group E6, E7 and Group F are not reliability related items. Group G are not applicable to non-hermetic packaged devices.

5. Reliability Test Results

Test Group A–Accelerated Environment Stress Test

Group	Item	Test Condition	QTY	Lot NO.	Result
A1	PC	Test @ Rm, SMD only, Moisture Preconditioning before BHAST, UHAST, TC stress, MSL = 1, Peak Reflow Temp = 260°C	240 pcs*3 lots	2349A	Pass
				2350A	Pass
				2351A	Pass
A2	BHAST	130°C, 85% RH, 96 hrs, V_{cc1}= 27V, V_{cc2}= 5.5V,	80 pcs*3 lots	2349A	Pass
				2350A	Pass
				2351A	Pass
A3	UHAST	130°C, 85% RH, 96 hrs	80 pcs*3 lots	2349A	Pass
				2350A	Pass
				2351A	Pass
A4	TC	-65°C-150°C, 500 cycles	80 pcs*3 lots	2349A	Pass
				2350A	Pass
				2351A	Pass
A6	HTSL	T_a = 150°C, 1000 hrs	50 pcs*1 lot	2349A	Pass

Test Group B–Accelerated Lifetime Simulation Tests

Group	Item	Test Condition	QTY	Lot NO.	Result
B1	HTOL	T_a = 125°C, 1000 hrs, V_{cc1}= 27V, V_{cc2}= 5.5V, input f = 10kHz	77 pcs*3 lots	2349A	Pass
				2350A	Pass
				2351A	Pass
B2	ELFR	T_a = 125°C, 48 hrs, V_{cc1}= 27V, V_{cc2}= 5.5V, input f = 10kHz	800 pcs*3 lots	2349A	Pass
				2350A	Pass
				2351A	Pass

Group C–Package Assembly Integrity Tests

Group	Item	Test Condition	QTY	Lot NO.	Result
C1	WBS	Cpk > 1.67, Each bonder used, T0 samples	30 bonds from 5 pcs	2349A	CPK=2.39
C1	WBS	0 fails, Each bonder used, post-TC samples	30 bonds from 5 pcs	2349A	Pass
C2	WBP	Cpk > 1.67, each bonder used, T0 samples	30 bonds from 5 pcs	2349A	CPK=2.31
C2	WBP	0 fails, Each bonder used, post-TC samples	30 bonds from 5 pcs	2349A	Pass
C3	SD	>95% coverage, 8 hrs steam aging prior to testing	15 pcs*1 lot	2349A	Pass
C4	PD	Cpk > 1.67	10 pcs*3 lots	2349A	Pass
				2350A	Pass
				2351A	Pass

TEST GROUP D–Die Fabrication Reliability Tests

Group	Item	Test Condition	ADDITIONAL REQUIREMENTS
D1	EM	---	The Die Fabrication Reliability Tests are carried out by every fabrication site. The data, test method, calculations and internal criteria are available to the customer upon request.
D2	TDDB	---	
D3	HCI	---	
D4	NBTI	---	
D5	SM	---	

Group E-Electrical Verification Tests

Group	Item	Test Condition	QTY	Lot NO.	Result
E1	TEST	Pre and Post Stress Electrical Test	All	All	Pass
E2	HBM	±500V, ±1KV, ±2KV, ±8KV (Test @ Rm/Hot)	3 pcs*1 lot	2349A	3B
E3	CDM	±250V, ±500V, ±750V, ±2KV (Test @ Rm/Hot)	3 pcs*1 lot	2349A	C3
E4	LU	125℃, I-trigger ±200mA, Over Voltage 40V(Test @ Rm/Hot)	3pcs*1 lot	2349A	Class II A
E5	ED	Test @ Rm/Cold/Hot	30pcs*3 lots	2349A	Pass
				2350A	
				2351A	
E9	EMC	Electromagnetic Compatibility (Radiated Emissions)	1 pcs*1 lot	2349A	Class O
E12	LF	SOIC8-NB	Refer to JCET SOP8 Tin Whisker report		

6. MTTF&FIT

Supporting Data (Ea = 0.7 eV, Confidence Level = 60%)							MTTF (hrs)	FIT
Test Temp.	Test Voltage	Duration	QTY	Fail QTY	Operation Temp.	Operation Voltage		
125℃	27V/5.5V	1000 hrs	231	0	55℃	27V/5.5V	2.94E+07	33.96
125℃	27V/5.5V	48 hrs	2400	0	55℃	27V/5.5V		

Note: The FIT data is generated based on Arrhenius model and voltage acceleration model.

7. Conclusion

CA-IF1021LS-Q1 series products are qualified according to AEC-Q100 standard.

Disclaimer

This information is provided to assist customers in design and development. It could change for technology innovation without notice.

The devices are shipped after passing final test. Customers are responsible to conduct sufficient engineering and additional qualification testing to determine whether a device is suitable for use in their applications.

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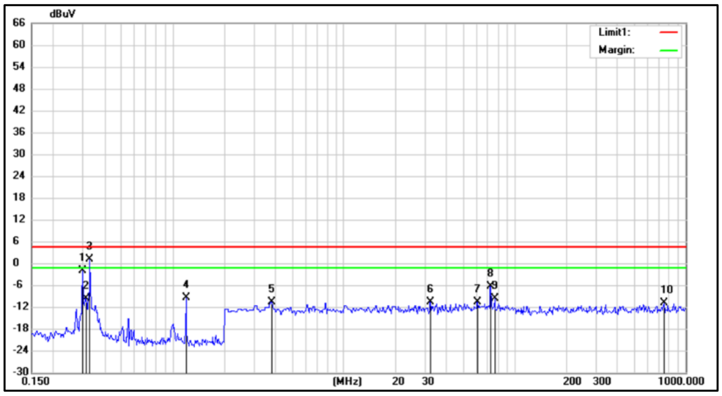
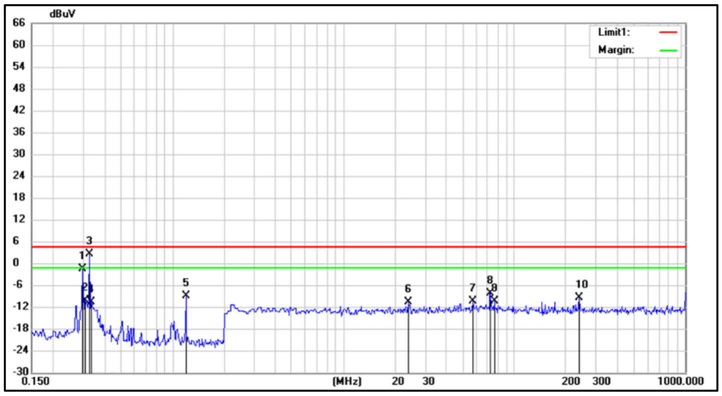
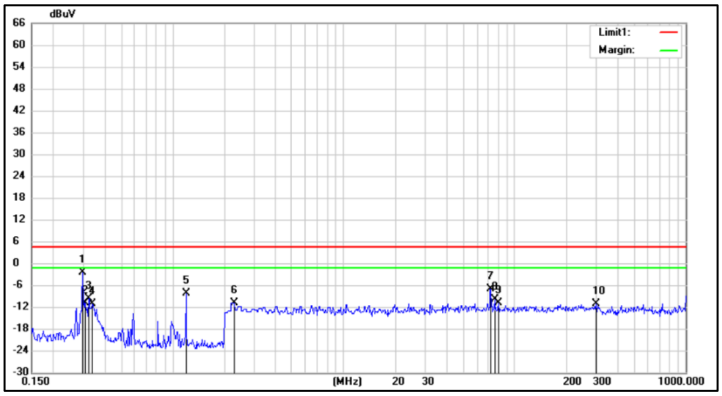
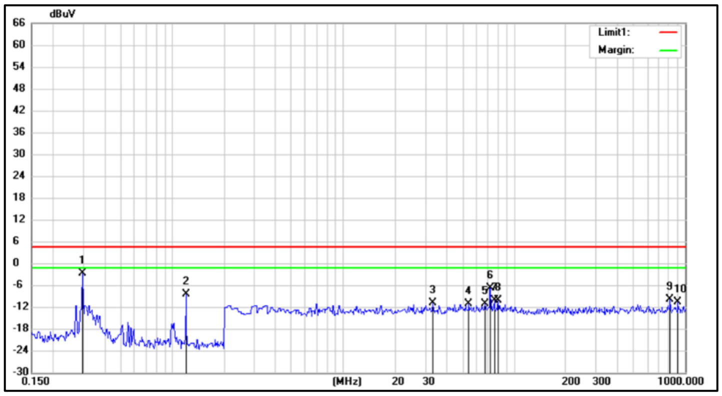
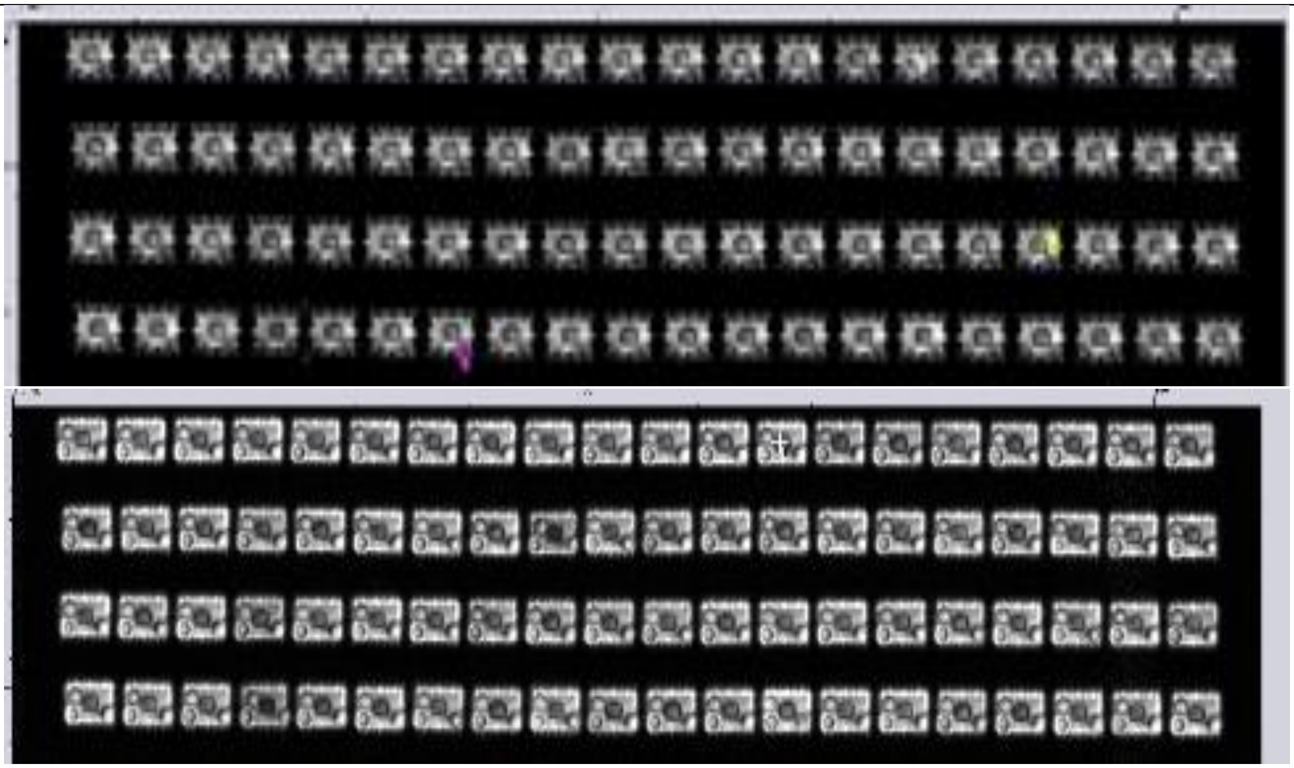
Revision History

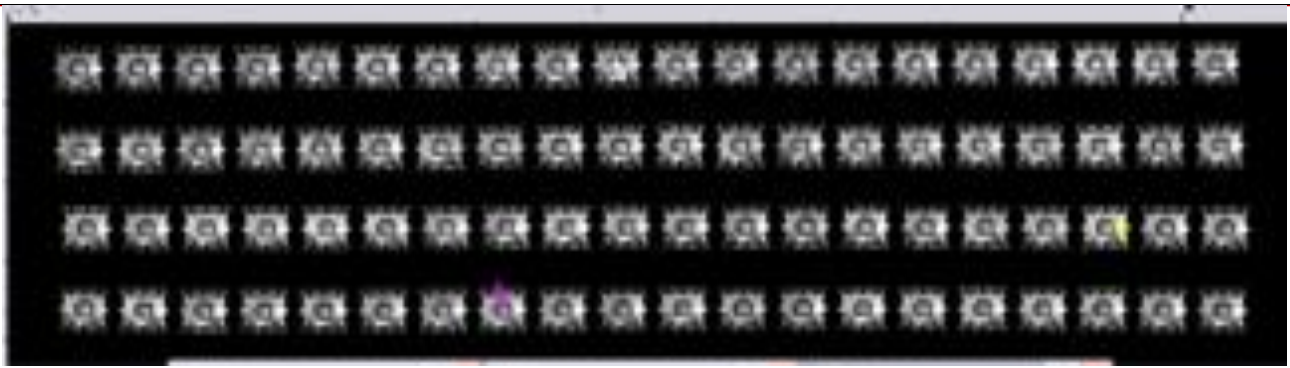
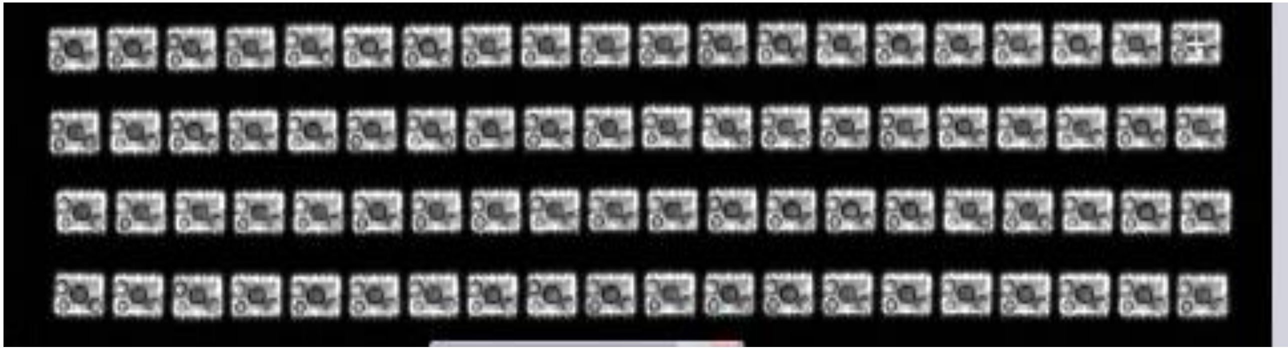
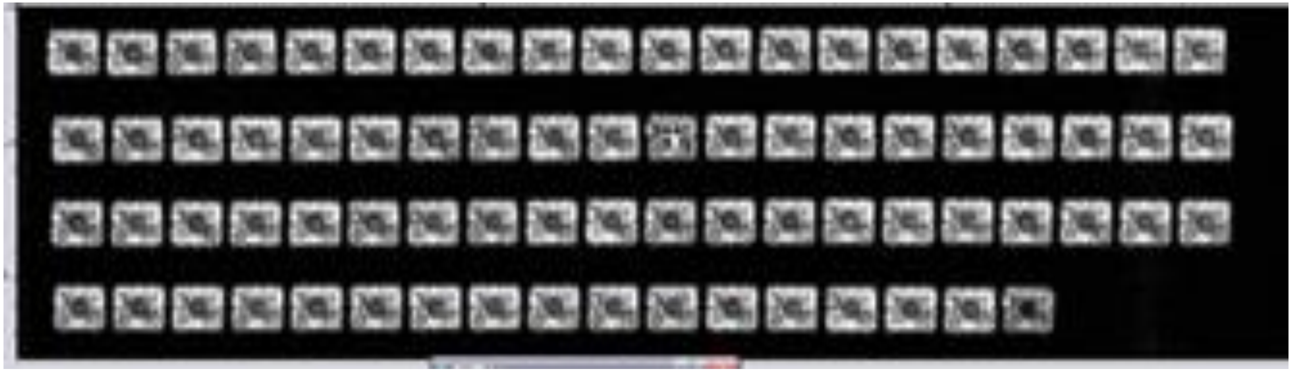
Revision	Change Log	Date
V1.0	Initial release	2024/06/04

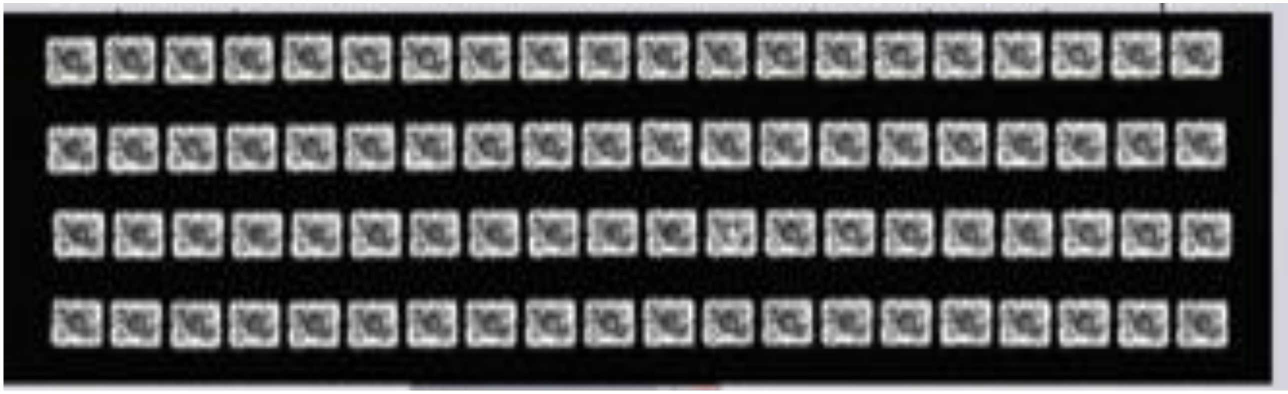
Appendix 1: EMC Test Results

VCC1=27V, VCC2=5V, TTL Input 10kHz, orientation 0°	VCC1=27V, VCC2=5V, TTL Input 10kHz, orientation 90°
	
VCC1=27V, VCC2=5V, TTL Input 10kHz, orientation 180°	**VCC1=27V, VCC2=5V, TTL Input 10kHz, orientation 270°**
	

Appendix 2: SAT Test Results

Lot 1 pre-MSL	
Lot 1 post-MSL	

Lot 2 pre-MSL	 
Lot 2 post-MSL	 

Lot 3 pre-MSL	 
Lot 3 post-MSL