

4. Ordering Information

Table 4-1 Ordering Information

Part #	Output	UVLO (V)	Isolation Rating (V _{PK})	Package
CA-IS3211SCWG	Split output, OUTH & OUTL	12	10600	SOIC8-WWB (WG)

Table of Contents

1. Features	1	7.2. I_{OH} and I_{OL}	11
2. Applications	1	7.3. CMTI Test Circuit	12
3. General Description	1	8. Detailed Description	13
4. Ordering Information	2	8.1. Overview	13
5. Pin Configuration and Description	4	8.2. Input Stage	14
5.1. CA-IS3211SCWG Pin Configuration and Description.....	4	8.3. Driver Output Stage	14
6. Specifications	5	8.4. Undervoltage Lockout (UVLO).....	15
6.1. Absolute Maximum Ratings ¹	5	9. Application and Implementation	16
6.2. ESD Ratings.....	5	9.1. Typical Application Circuit	16
6.3. Recommended Operating Conditions	5	9.2. Interlock configuration.....	17
6.4. Thermal Information	5	9.3. Input Current Limit.....	19
6.5. Power Ratings.....	5	9.4. Driver Output Resisters Selection	19
6.6. Insulation Specifications.....	6	9.5. PCB Layout	20
6.7. Safety-Related Certifications	7	10. Package Information	21
6.8. Safety Limits	7	10.1. 8-Pin Super Wide Body (SOIC8-WWB) Package Outline 21	
6.9. Electrical Characteristics.....	8	11. Soldering Information	22
6.10. Switching Characteristics.....	8	12. Tape and Reel Information	23
6.11. Typical Operating Characteristics	9	13. Revision History	24
7. Parameter Measurement Information	11	14. Important Statement	25
7.1. Propagation Delay and Rising time/Falling time	11		

5. Pin Configuration and Description

5.1. CA-IS3211SCWG Pin Configuration and Description



Figure 5-1 The CA-IS3211SCWG Pin Configuration

Table 5-1 The CA-IS3211SCWG Pin Description

Pin Name	Pin Number	Type	Description
ANODE	2	Input	Driver input, the anode of input diode.
CATHODE	3	Input	Driver input, the cathode of input diode.
NC	1, 4	---	No internal connection.
VEE	5	Power Supply	Negative Power supply input for output-side, it's the negative output supply rail. For bipolar operation, bypass VEE to output-side ground with 0.1μF 10μF capacitors as close as possible to the device. For single supply operation, connect VEE to GND on the output-side.
OUTL	6	Output	Gate driver pull-down output.
OUTH	7	Output	Gate driver pull-up output.
VCC	8	Power Supply	Positive Power supply input for output-side, it's the positive output supply rail. Bypass VCC to output-side ground with 0.1μF 10μF capacitors as close as possible to the device.

6. Specifications

6.1. Absolute Maximum Ratings¹

over operating free-air temperature range unless otherwise specified. ¹

Parameters		Minimum	Maximum	Unit
$I_{F(AVG)}$	Average input current	-	25	mA
$I_{F(TRAN)} < 1\mu s \text{ pulse, } 300ps$	Peak transient input current		1	A
$V_{R(MAX)}$	Reverse input voltage		7.0	V
$V_{CC} - V_{EE}$	Output-side supply voltage range	-0.3	32	V
V_{OUTH}, V_{OUTL}	Driver output voltage	$V_{EE} - 0.3$	$V_{CC} + 0.3$	V
T_J^2	Junction temperature	-40	150	°C
T_{stg}	Storage temperature	-65	150	°C

Notes:

- The stresses listed under “Absolute Maximum Ratings” are stress ratings only, not for functional operation condition. Exposure to absolute maximum rating conditions for extended periods may cause permanent damage to the device.
- To maintain the recommended operating junction temperature conditions, see Thermal Information.

6.2. ESD Ratings

			Value	Unit
V_{ESD}	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001.	±4000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101.	±2000	

6.3. Recommended Operating Conditions

Over operating free-air temperature range unless otherwise specified.

Parameters			Minimum	Typical	Maximum	Unit
V_{CC}	Driver output voltage ($V_{CC} - V_{EE}$)	12V UVLO version	14		30	V
$I_{F(ON)}$	Input diode turn-on: diode forward current		7		16	mA
$V_{F(OFF)}$	Input diode turn-off: anode voltage - cathode voltage		-5.5		0.9	V
T_J	Junction temperature		-40		150	°C
T_A	Ambient temperature		-40		125	°C

6.4. Thermal Information

Thermal Metric		SOIC8-WWB	Unit
		(WG)	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	113.3	°C/W
$R_{\theta JC(top)}$	Junction-to-Case (top) thermal resistance	34.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	64.2	°C/W

6.5. Power Ratings

Parameters		Test Conditions	Minimum	Typical	Maximum	Unit
P_D	Maximum input and output power dissipation (derate 6mW/°C above +25°C)	$V_{CC} = 20V, I_F = 10mA, 10kHz$ square wave with 50% duty cycle, $C_L = 180nF, T_A = 25^\circ C$			750	mW
P_{D1}	Maximum input power dissipation ¹				10	mW
P_{D2}	Maximum output power dissipation				740	mW

Note:

- The maximum $P_{D1} = 40mW$ and the absolute maximum rating of P_{D1} is 55mW.

6.6. Insulation Specifications

Parameters		Test Conditions	Specifications	Unit
			WG	
CLR	External clearance ¹	Shortest terminal-to-terminal distance through air	>15	mm
CPG	External creepage ¹	Shortest terminal-to-terminal distance across the package surface	>15	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	>28	μm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	>600	V
	Material group	According to IEC 60664-1	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 300 V _{RMS}	I-IV	
		Rated mains voltage ≤ 600 V _{RMS}	I-IV	
		Rated mains voltage ≤ 1000 V _{RMS}	I-III	
DIN EN IEC 60747-17 (VDE 0884-17)²				
V _{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	2828	V _{PK}
V _{IOWM}	Maximum operating isolation voltage	AC voltage; time-dependent dielectric breakdown (TDDB) test	2000	V _{RMS}
		DC voltage	2828	V _{DC}
V _{IOTM}	Maximum transient isolation voltage	V _{TEST} = V _{IOTM} , t = 60 s (qualification); V _{TEST} = 1.2 × V _{IOTM} , t = 1 s (100% production test)	10600	V _{PK}
V _{IMP}	Maximum impulse voltage	1.2/50-μs waveform per IEC 62368-1	9846	V _{PK}
V _{IOSM}	Maximum surge isolation voltage ³	V _{IOSM} ≥ 1.3 × V _{IMP} ; Tested in oil (qualification) 1.2/50-μs waveform per IEC 62368-1	12800	V _{PK}
q _{pd}	Apparent charge ⁴	Method a, After input/output safety tests subgroup 2/3, V _{ini} = V _{IOTM} , t _{ini} = 60s; V _{pd(m)} = 1.2 × V _{IORM} , t _m = 10s	≤5	pC
		Method a, After environmental tests subgroup 1, V _{ini} = V _{IOTM} , t _{ini} = 60s; V _{pd(m)} = 1.6 × V _{IORM} , t _m = 10s	≤5	
		Method b1, At routine test (100% production test) and preconditioning (sample test) V _{ini} = 1.2 × V _{IOTM} , t _{ini} = 1s; V _{pd(m)} = 1.875 × V _{IORM} , t _m = 1s;	≤5	
C _{IO}	Barrier capacitance, input to output ⁵	V _{IO} = 0.4 × sin(2πft), f = 1 MHz	~0.5	pF
R _{IO}	Isolation resistance, input to output ⁴	V _{IO} = 500 V, T _A = 25°C	>10 ¹²	Ω
		V _{IO} = 500 V, 100°C ≤ T _A ≤ 125°C	>10 ¹¹	
		V _{IO} = 500 V at T _S = 150°C	>10 ⁹	
	Pollution degree		2	
	Climatic category		40/125/21	
UL 1577				
V _{ISO}	Maximum isolation voltage	V _{TEST} = V _{ISO} , t = 60 s (qualification) V _{TEST} = 1.2 × V _{ISO} , t = 1 s (100% production test)	7500	V _{RMS}
Notes: <ol style="list-style-type: none"> Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications. This coupler is suitable for safe electrical insulation only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits. Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier. Apparent charge is electrical discharge caused by a partial discharge (pd). All pins on each side of the barrier tied together creating a two-terminal device. 				

6.7. Safety-Related Certifications

VDE (Pending)	UL (Pending)	CQC (Pending)	TUV (Pending)
Certified according to DIN EN IEC 60747-17 (VDE 0884-17):2021-10; EN IEC 60747-17:2020+AC:2021	Certified according to UL 1577 Component Recognition Program	Certified according to GB4943.1-2022	Certified according to EN 61010-1 and EN 62368-1
Reinforced isolation: Maximum transient isolation voltage: 10600V _{pk} Maximum repetitive-peak isolation voltage: 2828V _{pk} Maximum surge isolation voltage: 12800V _{pk}	Single protection: - 7.5kV _{RMS} for SOIC8-WWB packages	Reinforced insulation 7.5kV _{RMS} for SOIC8-WWB packages (Altitude ≤ 5000m)	EN 61010-1 SOIC8-WWB: 7500V _{RMS} EN 62368-1 SOIC8-WWB: 7500V _{RMS}
Certification Number: Pending	Certification Number: Pending	Certification Number: Pending	Client reference number: 2253313

6.8. Safety Limits

Parameters		Test Conditions	Minimum	Typical	Maximum	Unit
I _s	Safety output supply current	R _{qJA} ¹ = 113.3°C/W, V _I = 15V, T _J = 150°C, T _A = 25°C			50	mA
		R _{qJA} ¹ = 113.3°C/W, V _I = 30V, T _J = 150°C, T _A = 25°C			25	
P _s	Safety power dissipation	R _{qJA} ¹ = 113.3°C/W, T _J = 150°C, T _A = 25°C			750	mW
T _s	Maximum safety temperature ²				150	°C

Note:

1. The R_{qJA} values in this safety limit are used the SOIC8-WWB package.

2. $T_{J(max)} = T_S = T_A + R_{\theta JA} * P_S$, where T_{J(max)} is the maximum allowed junction temperature. $P_S = I_s * V_{IN}$, where V_{IN} is the maximum supply voltage.

6.9. Electrical Characteristics

All minimum/maximum specs are at $T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{CC} = 15\text{V}$ to 30V , $V_{EE} = \text{GND}$, $I_{F(\text{on})} = 7\text{mA}$ to 16mA , $V_{F(\text{off})} = -5\text{V}$ to 0.8V , unless otherwise noted. Typical values are at $T_A = +25^{\circ}\text{C}$, $V_{CC} - V_{EE} = 15\text{V}$, $V_{EE} = \text{GND}$, unless otherwise noted.

Parameters		Test Conditions	Minimum	Typical	Maximum	Unit
Input						
I_{FLH}	Input diode forward threshold: low to high	$V_{out} > 5\text{V}$, $C_g = 1\text{nF}$	1.5	2.8	4	mA
V_F	Input diode forward voltage	$I_F = 10\text{mA}$	1.8	2.1	2.4	V
V_{F_HL}	Input voltage threshold: high to low	$V < 5\text{V}$, $C_g = 1\text{nF}$	0.9			V
$\Delta V_F/\Delta T$	Temp coefficient of V_F	$I_F = 10\text{mA}$		1.5	1.8	mV/ $^{\circ}\text{C}$
V_R	Input reverse breakdown voltage	$I_R = 10\mu\text{A}$	7			V
C_{IN}	Input Capacitance	$F = 0.5\text{MHz}$		15		pF
Output						
I_{OH}	High level Output Peak current	$I_F = 10\text{mA}$, $V_{CC} = 15\text{V}$, $C_{LOAD} = 0.18\mu\text{F}$, $C_{VDD} = 10\mu\text{F}$, Pulse width $< 10\mu\text{s}$, see Figure 7-2	3	5.0		A
I_{OL}	Low level Output Peak current	$V_F = 0\text{V}$, $V_{CC} = 15\text{V}$, $C_{LOAD} = 0.18\mu\text{F}$, $C_{VDD} = 10\mu\text{F}$, Pulse width $< 10\mu\text{s}$, see Figure 7-2	3.5	6.0		A
V_{OH}	Output high voltage	$I_F = 10\text{mA}$, $I_O = -20\text{mA}$ (respect to V_{CC})	0.07	0.11	0.36	V
		$I_F = 10\text{mA}$, $I_O = 0\text{mA}$		V_{CC}		V
V_{OL}	Output low voltage	$V_F = 0\text{V}$, $I_O = 20\text{mA}$		10	25	mV
I_{CC_H}	Output supply current (e-diode turn on)	$I_F = 10\text{mA}$, $I_O = 0\text{mA}$		1.13	2.2	mA
I_{CC_L}	Output supply current (e-diode turn off)	$V_F = 0\text{V}$, $I_O = 0\text{mA}$		1.05	2	mA
Undervoltage-Lockout Threshold (12V UVLO)						
$UVLO_R$	UVLO threshold (V_{CC} rising)	$I_F = 10\text{mA}$	10.9	12.1	13.3	V
$UVLO_F$	UVLO threshold (V_{CC} falling)	$I_F = 10\text{mA}$	9.9	11.1	12.3	V
$UVLO_{HYS}$	Undervoltage-lockout threshold hysteresis			1.0		V

6.10. Switching Characteristics

All minimum/maximum specs are at $T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{CC} = 15\text{V}$ to 30V , $V_{EE} = \text{GND}$, $I_{F(\text{on})} = 7\text{mA}$ to 16mA , $V_{F(\text{off})} = -5\text{V}$ to 0.8V , unless otherwise noted. Typical values are at $T_A = +25^{\circ}\text{C}$, $V_{CC} - V_{EE} = 30\text{V}$, $V_{EE} = \text{GND}$, unless otherwise noted.

Parameters		Test Conditions	Minimum	Typical	Maximum	Unit
t_r	Output rise time	$C_g = 1\text{nF}$, $F_{SW} = 20\text{kHz}$ with 50% duty-cycle; $V_{CC} = 15\text{V}$, see Figure 7-1		6	28	ns
t_f	Output fall time			4	25	ns
t_{PLH}	Propagation delay, low to high		40	70	105	ns
t_{PHL}	Propagation delay, high to low		40	60	105	ns
t_{PWD}	Pulse width distortion $ t_{PHL} - t_{PLH} $			10	35	ns
$t_{sk(pp)}$	Part to part propagation delay matching	$C_g = 1\text{nF}$, $F_{SW} = 20\text{kHz}$ with 50% duty-cycle; $V_{CC} = 15\text{V}$, $I_F = 10\text{mA}$			25	ns
t_{UVLO_rec}	UVLO recovery time	V_{CC} rising from 0V to 15V , see Figure 8-3		70	100	μs
$CMTI_H$	CMTI (output high)	$I_F = 10\text{mA}$, $V_{CM} = 1500\text{V}$, $V_{CC} = 30\text{V}$, $T_A = 25^{\circ}\text{C}$, see Figure 7-3	100	150		kV/ μs
$CMTI_L$	CMTI (output low)	$V_F = 0\text{V}$, $V_{CM} = 1500\text{V}$, $V_{CC} = 30\text{V}$, $T_A = 25^{\circ}\text{C}$, see Figure 7-3	100	150		kV/ μs

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6.11. Typical Operating Characteristics

All values are at $V_{CC} = 15V$, $C_{LOAD} = 1nF$ for timing specs and $C_{LOAD} = 180nF$ for IOH, IOL specs; $T_A = -40^{\circ}C$ to $+125^{\circ}C$, $V_{EE} = GND$, bypass V_{CC} to V_{EE} with $1\mu F$ capacitor, unless otherwise noted.

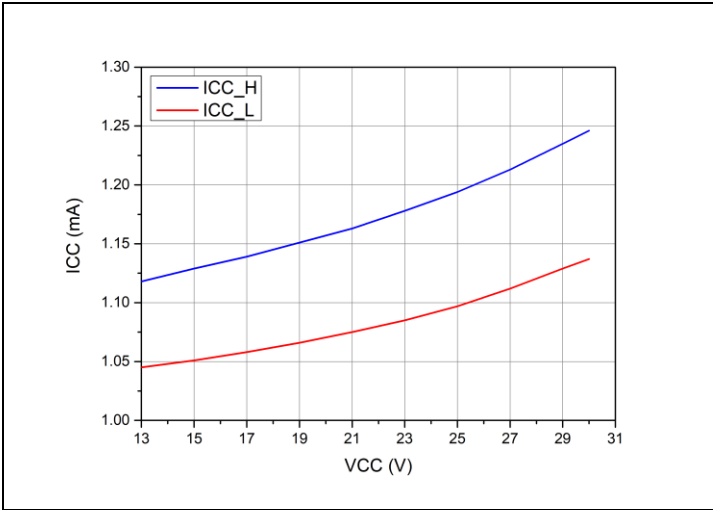


Figure 6-1 V_{CC} supply current vs. V_{CC} supply voltage

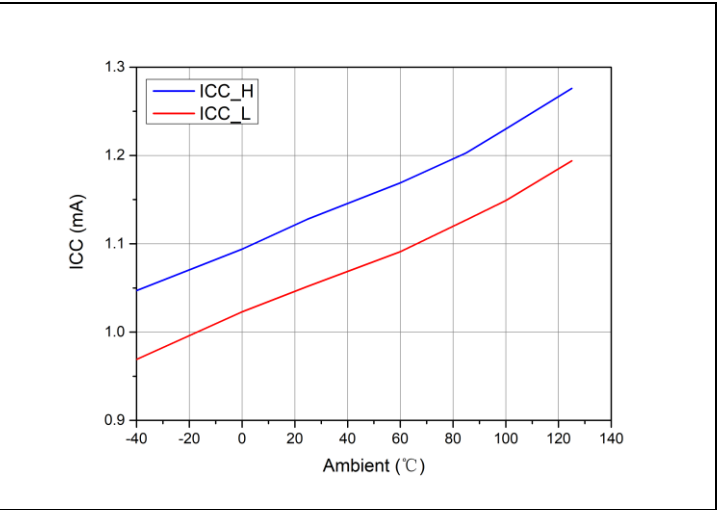


Figure 6-2 V_{CC} supply current vs. Temperature

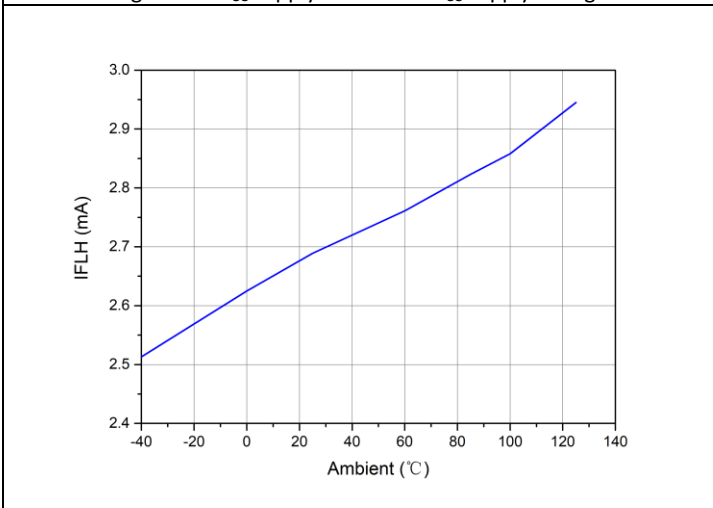


Figure 6-3 Input diode forward threshold vs. Temperature

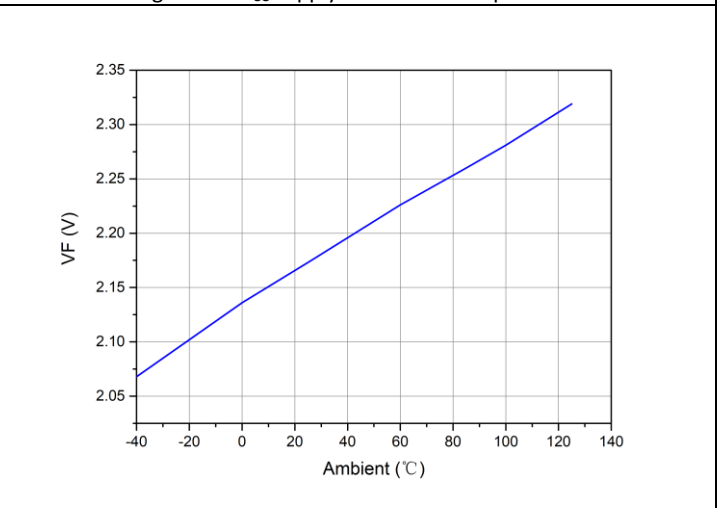


Figure 6-4 Input diode forward voltage vs. Temperature (I_f=10mA)

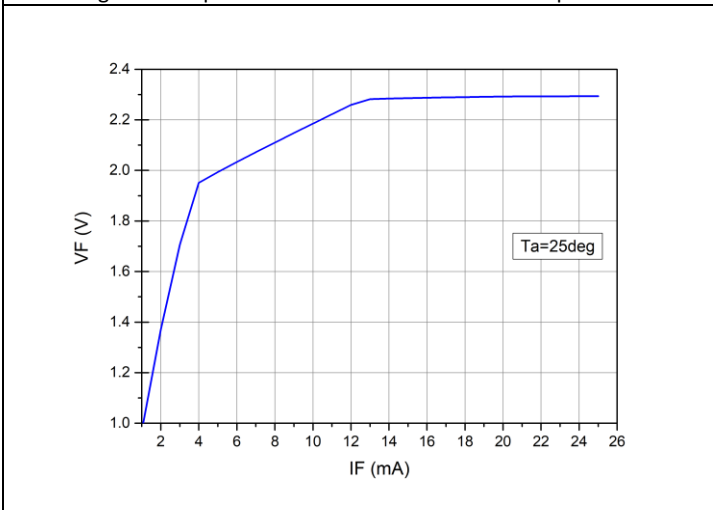


Figure 6-5 Input diode forward voltage vs. Forward current

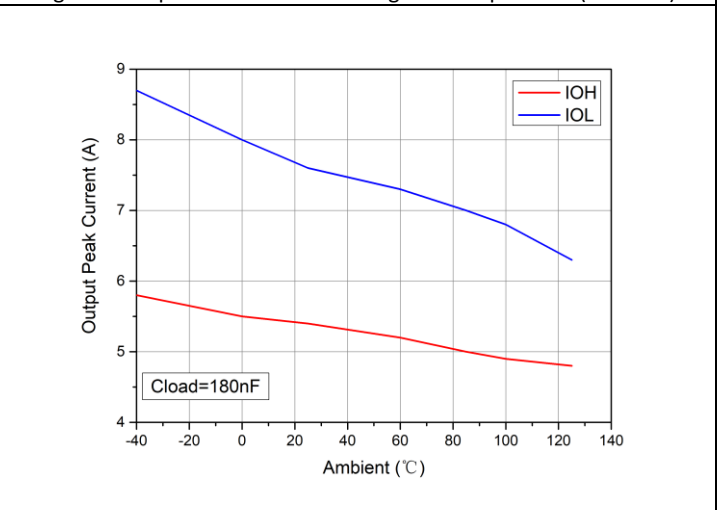


Figure 6-6 Output peak current vs. Temperature

(Continued from above)

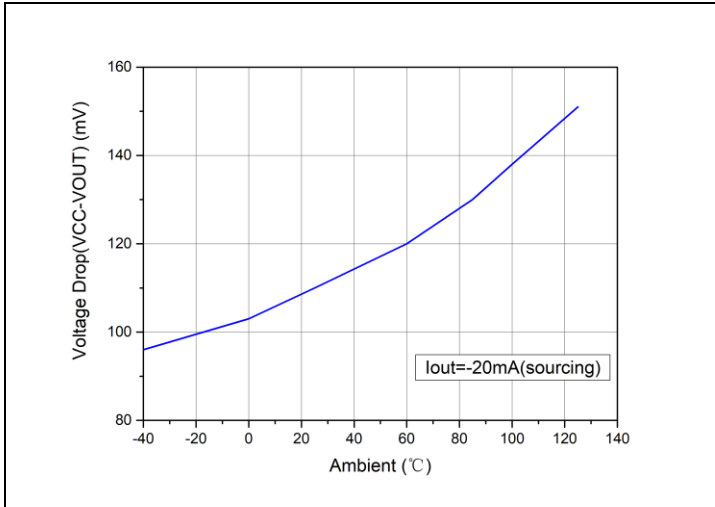


Figure 6-7 V_{OH} vs. Temperature (20mA load current)

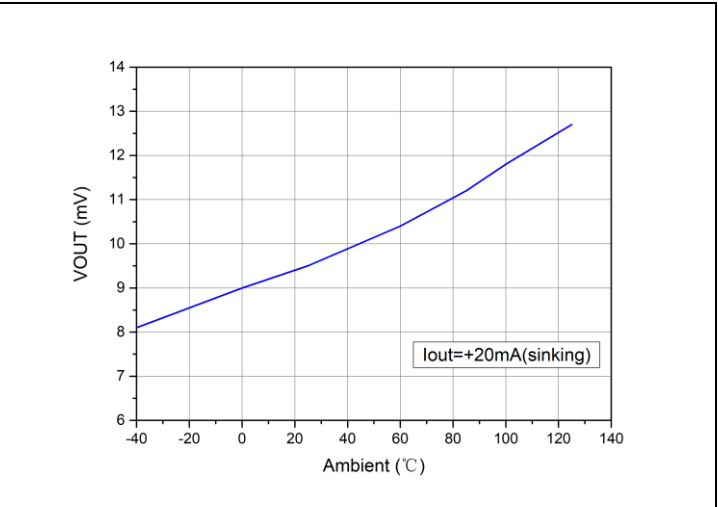


Figure 6-8 V_{OL} vs. Temperature (20mA load current)

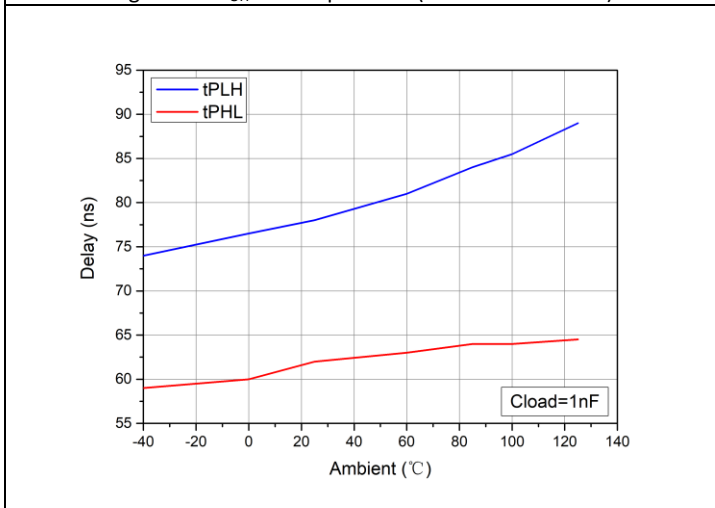


Figure 6-9 Propagation delay vs. Temperature

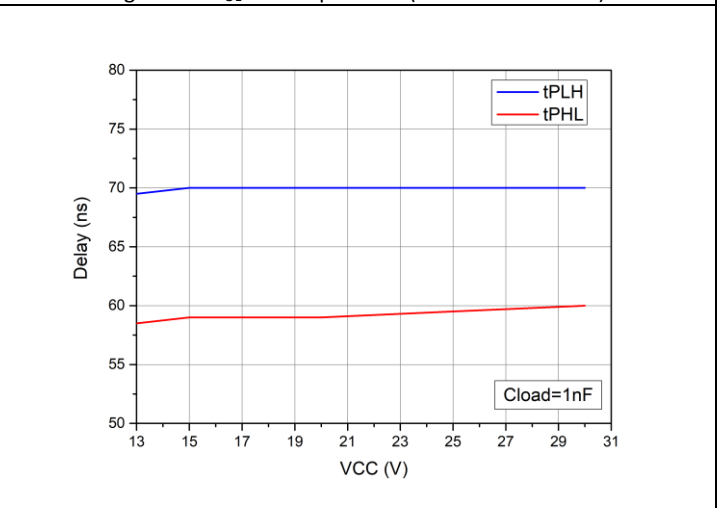


Figure 6-10 Propagation delay vs. V_{CC} supply voltage

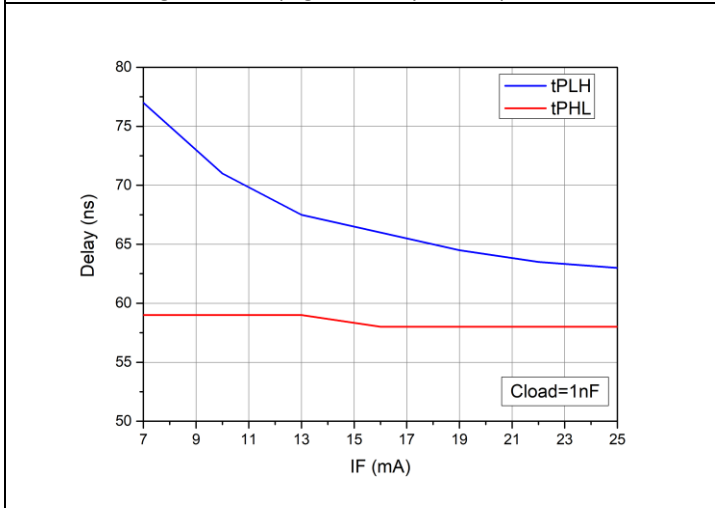


Figure 6-11 Propagation delay vs. Input diode forward current

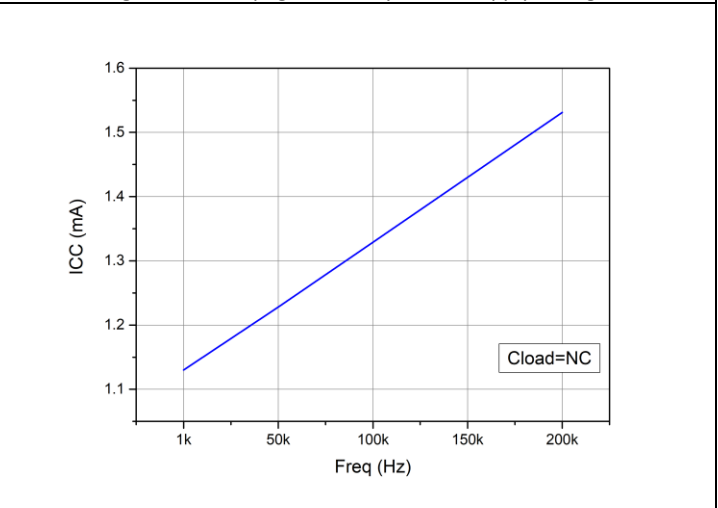


Figure 6-12 V_{CC} operating current vs. Frequency

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7. Parameter Measurement Information

7.1. Propagation Delay and Rising time/Falling time

Figure 7-1 shows the definition and measurement for the propagation delay t_{PLH} , t_{PHL} , and rising time (t_r), falling time (t_f).

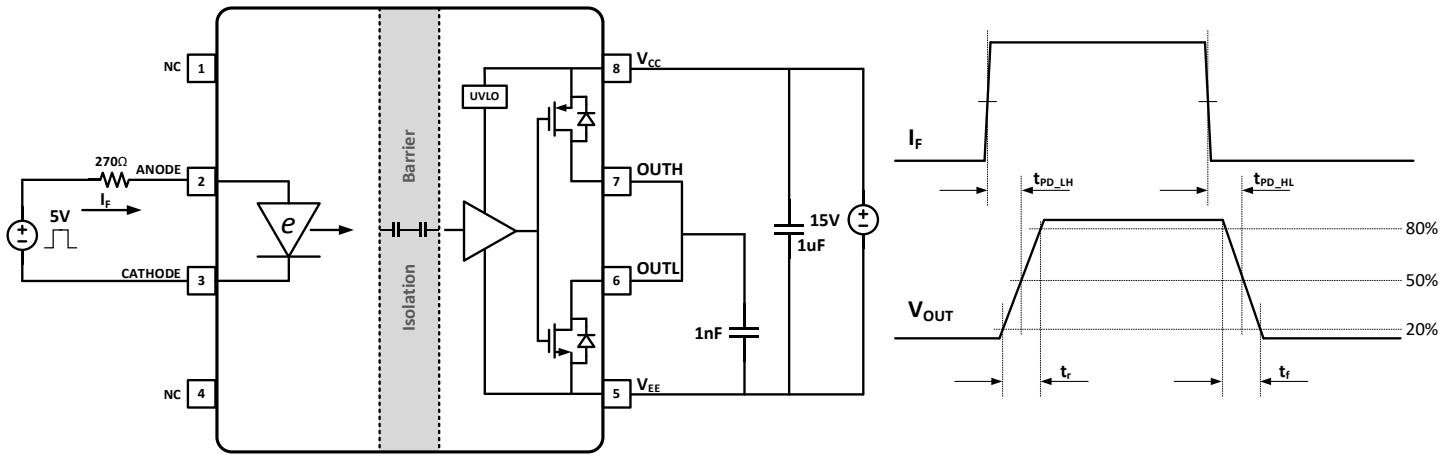


Figure 7-1 Propagation delay and rise time/fall time measurement

7.2. I_{OH} and I_{OL}

Figure 7-2 shows the measurement of output driving current I_{OH} and I_{OL} . In Figure 8-2, $C_{OUT} = 180nF$. The peak dV/dt of capacitor voltage is measured to determine gate driver's peak sourcing and sinking current.

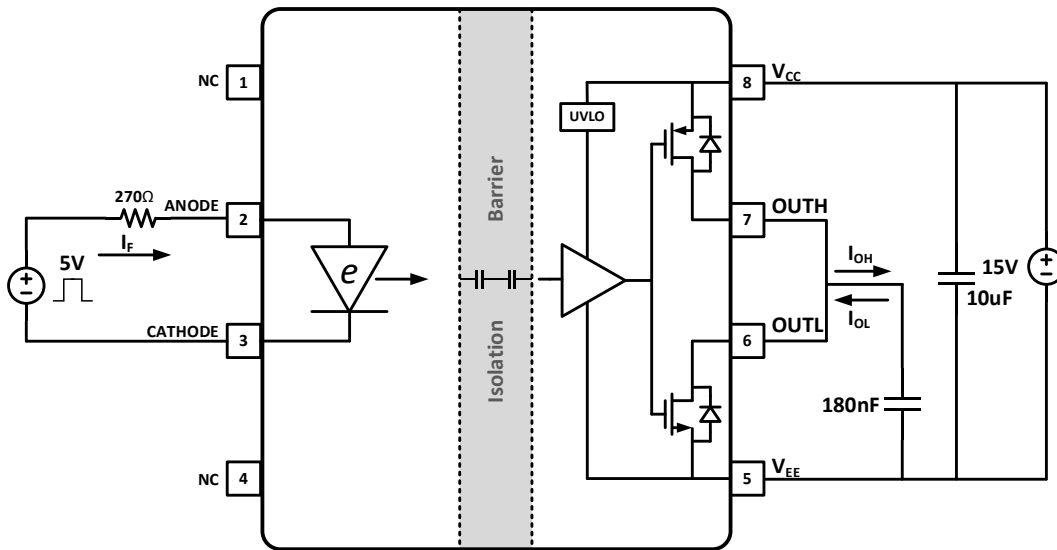


Figure 7-2 I_{OH} and I_{OL} test circuit

7.3. CMTI Test Circuit

Figure 7-3 is the CMTI test configuration for the CA-IS3211.

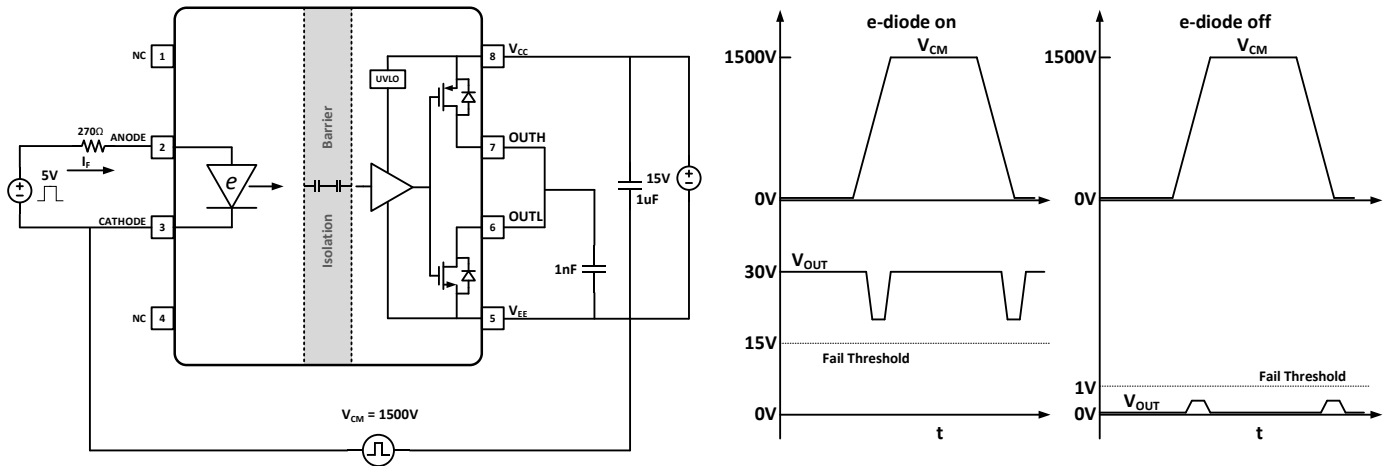


Figure 7-3 Common-mode transient immunity test circuit and waveform

8. Detailed Description

8.1. Overview

The CA-IS3211 is a family of single-channel, opto-compatible reinforced isolated gate driver capable of sinking 6A and sourcing 5A currents, that can be used to replace industry standard optocoupler-based gate drivers with pin-to-pin compatibility while providing high CMTI, low propagation delay, small pulse width distortion and small part-to-part skew to achieve the fast switching frequency, and better jitter and propagation delay performance. As the input stage uses an emulated diode (analog diode), these gate drivers offer long term reliability and excellent aging characteristics. The CA-IS3211 devices operate with dual supplies or a single supply of 14V to 30V (12V UVLO parts) wide voltage range of $V_{CC} - V_{EE}$, support unbalanced dual supplies operation, making them ideal to drive power MOSFET, IGBT or silicon-carbide (SiC) transistors in various inverter, power supply or motor drive applications. The CA-IS3211Sx offers dual separate output: OUTH and OUTL. All devices can be configured as low-side and high-side drivers. The driver output is pulled to low state to turn-off external power transistors when V_{CC} supply input is either not powered or is in UVLO. Undervoltage lockout (UVLO) with hysteresis is integrated on V_{CC} supply which ensure robust system performance under noisy conditions.

The CA-IS3211 devices are available either in 8-pin super wide-body SOIC packages with 15mm of creepage and clearance. All devices are rated for operation at -40°C to $+150^{\circ}\text{C}$ junction temperature. Higher operation temperature range extends gate driver designs in industrial and automotive applications with the high temperature environment that can not supported by optocoupler-based isolator. Figure 8-1 provides a conceptual block diagram of the CA-IS3211 reinforced isolated gate driver. It shows the main elements of CA-IS3211, including input stage, output stage, V_{CC} UVLO, digital isolator functional groups. Their operations are described separately in the following sections.

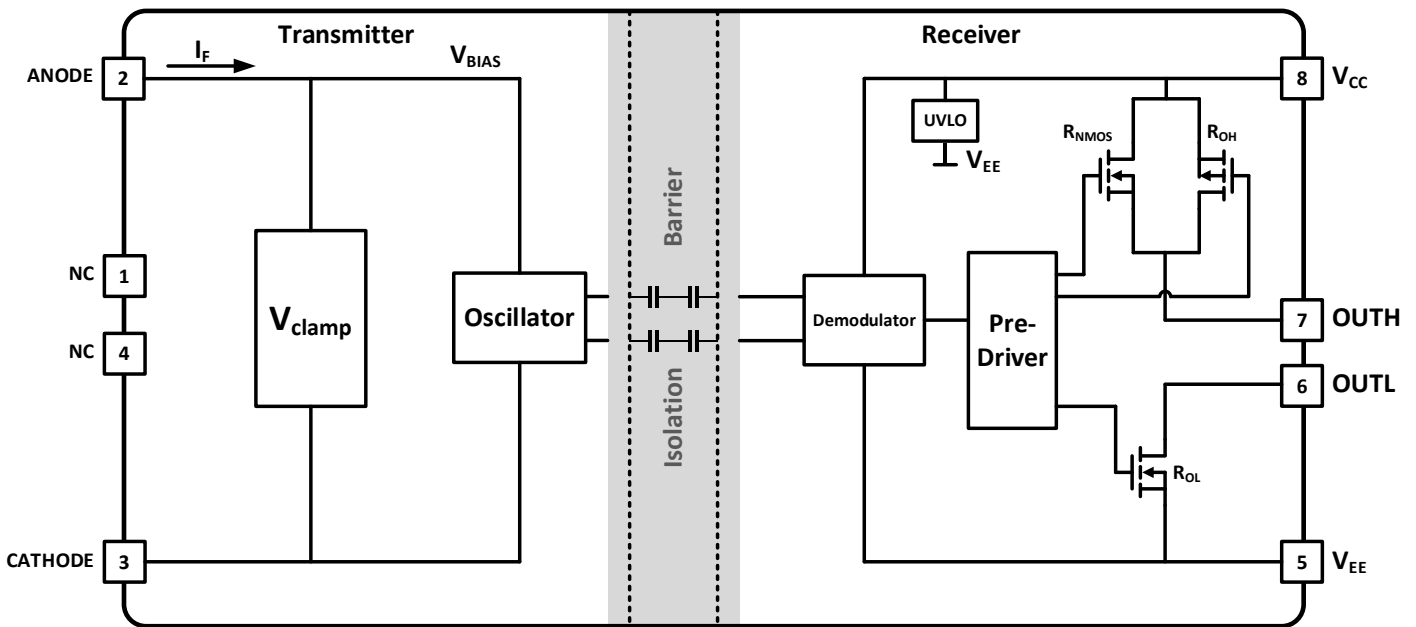


Figure 8-1 Functional block diagram

The CA-IS3211 devices have an ON-OFF keying (OOK) modulation scheme to transfer digital signals across the SiO_2 based isolation barrier between circuits with different power domains. The isolation transmitter sends a high frequency carrier across the barrier to represent one digital state and sends no signal to represent the other digital state. The isolation receiver demodulates the signal and recovery input signal at output-side through a buffer stage. With Chipanalog's full differential OOK capacitive isolation technology, the CA-IS3211 builds a robust data transmission path between different power domains and the wide-body package parts support up to $7.5\text{kV}_{\text{RMS}}$ galvanic isolation between input-side and output-side, also features up to

100kV/ μ s common mode transient immunity, 2000V_{RMS} working voltage, up to 12.8kV_{PK} surge rating. This enables efficient signal transmission in noisy environments. The advanced full differential techniques can maximize CMTI performance and minimize the radiated emissions due the high frequency carrier and driver switching.

8.2. Input Stage

The input stage of CA-IS3211 integrated an analog diode with anode and cathode pins. There is no power supply and ground pins on the input-side. Applying a positive voltage between the anode and cathode, the analog diode is forward biased and a forward current I_F flows into the diode. The analog diode features 2.1V typical forward voltage. Like optocoupler-based gate drivers, an external resistor (R_{EXT} in the typical application circuits) is needed to limit the forward current. For the CA-IS3211 devices, the operating forward current range is 7mA to 16mA. If $I_F > I_{FLH}$ (2.8mA, typ.), the isolation transmitter sends a high frequency carrier across the SiO₂ barrier and the isolation receiver demodulates this high-frequency signal and drive output high; If the anode voltage drops below V_{F_HL} (0.9V, min.), or reverse biased, the gate driver output is put to low state. The reverse breakdown voltage of the CA-IS3211 input diode is >7V. Refer to Table 8-1 for the inputs vs. output truth table of the CA-IS3211.

Table 8-1 The CA-IS3211 Inputs vs. Output Truth Table

Input diode	V _{CC}	V _{OUT}
Turn off ($I_F < I_{FLH}$)	UVLO _R to 30V	Low
Turn on ($I_F > I_{FLH}$)	UVLO _R to 30V	High
X	0V to UVLO _R , UVLO _F to 0V	Low

As an opto-compatible reinforced isolated gate driver, the CA-IS3211 family of products can be used as drop-in replacement for the industry standard optocoupler-based gate drivers. The key features and characteristics of the CA-IS3211 also bring significant performance and reliability improvement over opto-based gate drivers as flowing list:

1. High reliability and stability, since the analog diode does not use light emission for its operation, the operating point of input stage is very stable and predictable over operating temperature range. The dynamic impedance of the CA-IS3211 input diode is very small (<1.0 Ω) and the temperature coefficient of the forward voltage drop is less than 1.5mV/ $^{\circ}$ C. These advanced features lead to excellent stability of the forward current I_F across all operating conditions, provide better reliability and stability over full temperature range and life-time, also offer better part to part matching.
2. Smaller propagation delay and skew, due to Chipanalog's proprietary process technology, the CA-IS3211 drivers feature smaller pulse width distortion and less part to part propagation skew. The part-to-part propagation delay is matched within 25ns over the junction temperature range of -40 $^{\circ}$ C to +150 $^{\circ}$ C.
3. More robust, the CA-IS3211 silicon-based gate drivers can operate at higher ambient temperature range(up to 125 $^{\circ}$ C), while most of opto-isolated gate drivers only operate up to 105 $^{\circ}$ C. They also feature higher common mode transient immunity than opto isolated gate drivers.

8.3. Driver Output Stage

The output driver stage of the CA-IS3211 integrates a pull-up structure and a pull-down structure. They have distinct current sourcing/sinking capabilities to control the external transistors. Figure 9-2 shows the output stage circuit, in the output stage, a p-channel MOSFET and an additional n-channel MOSFET in parallel combined into the pull-up structure. The n-channel MOSFET only turns on for a short period of time during the output low-to-high transition and provides a boost current to enable the fast turn-on of the device. The on-resistance of this n-channel MOSFET (R_{NMOS}) is about 0.8 Ω when activated. In Figure 8-2 , R_{OH} (5.5 Ω , typ.) is the on-resistance of the P-channel MOSFET only. This is because the n-channel MOSFET is placed in off state in DC condition and is turned on only for a very short time when the output is changing from low to high. Thus, the effective on-resistance($R_{NMOS} // R_{OH}$) of the output pull-up stage during NMOS turn-on phase is much lower than R_{OH} .

The pull-down circuit of CA-IS3211 is simply composed of an n-channel MOSFET. R_{OL} in Figure 9-2 is the on-resistance of the pull-down n-channel MOSFET, the typical value of R_{OL} is 0.5 Ω . Because of the very low turn-on impedance of the output

stage MOSFETs, the CA-IS3211 reinforced isolated gate drivers provide rail-to-rail outputs (output voltage swings between V_{CC} and V_{EE}). Also, the CA-IS3211 family offers different output option, the CA-IS3211Sx offers split output terminals: OUTH and OUTL.

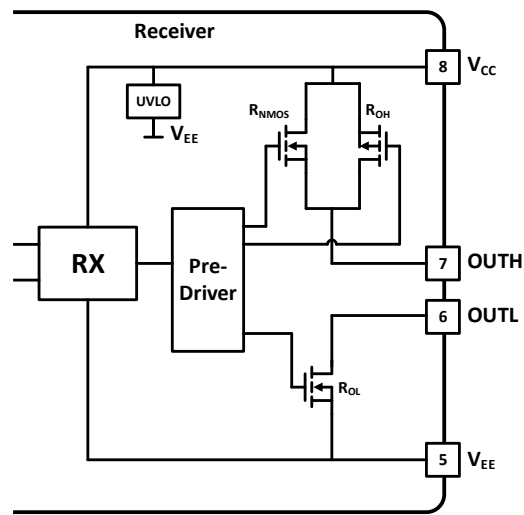


Figure 8-2 Driver output stage

When the V_{CC} supply is in power-off or UVLO condition, the high-side p-channel MOSFET and n-channel MOSFET are held off while the low-side n-channel MOSFET gate is connected to the driver output through a clamp resistor (about 500k Ω). This active clamp circuit holds driver outputs to the threshold voltage of the lower n-channel MOSFET (less than 2.0V) or low state, to turn off the external power transistors when no power is connected to the V_{CC} supply. This prevents the external power transistors from falsely turning on during V_{CC} power off or UVLO.

The output stage of the CA-IS3211 also features short-circuit clamping function that clamp the driver output voltage and pull the V_{OUT} slightly higher than V_{CC} supply during short-circuit conditions. This protects the external transistors from overvoltage breakdown. The internal conduction diode can support up to 500mA @10 μ s pulse current and 20mA continuous current. An external diode can be used to provide larger current conduction capability.

8.4. Undervoltage Lockout (UVLO)

The CA-IS3211 supply ($V_{CC}-V_{EE}$) is internally monitored for undervoltage conditions. The supply terminal V_{CC} undervoltage detection places the driver output in low state (default state) during an undervoltage event: $V_{CC} < UVLO_R$ during power on, or $V_{CC} < UVLO_F$ during power-down or during normal operation due to a sagging supply voltage. Low state output turn off the external power transistor regardless of the state of the input to avoid under-driven condition on IGBTs and MOSFETs, see Figure 9-3 for more details. The V_{CC} UVLO has hysteresis to avoid chattering when there is ground noise from the power supply, also allows the device to accept small drops in supply voltage and ensures stable operation. Table 9-1 illustrate the output behavior during V_{CC} undervoltage conditions.

Note that before the device enters normal operation and get ready to provide driver output correctly, there is a power-up delay from UVLO rising edge to driver output. This delay time is defined as t_{UVLO_rec} as shown in Figure 8-3. Designers need to leave proper margin before sending PWM signal to gate driver after the V_{CC} supply is ready.

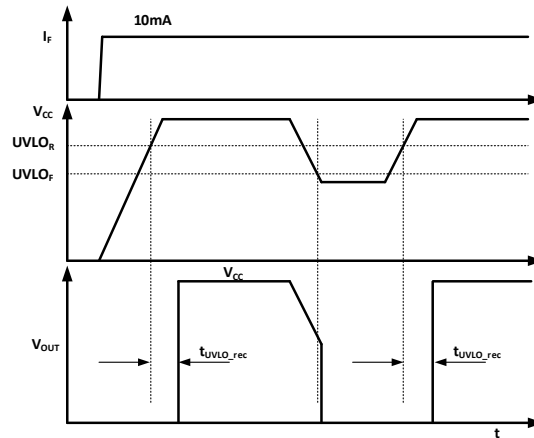


Figure 8-3 UVLO timing diagram

9. Application and Implementation

9.1. Typical Application Circuit

The CA-IS3211 reinforced isolated gate drivers are designed to drive power MOSFET, IGBT or silicon-carbide (SiC) transistors in various power supply systems to optimize system cost and efficiency. This family of devices can be configured as low-side and high-side drivers. The default-low output keeps the output in low state when V_{CC} supply is in UVLO or power off. The high CMTI rating of $100\text{kV}/\mu\text{s}$ (min) @ at 1500V common mode voltages, UVLO detection and the propagation delay matching of 25ns (max) part to part make the CA-IS3211 devices ideal to drive high-power transistors in motor drives, industrial inverters, isolated power supply etc. high reliability applications. Figure 9-1 and Figure 9-2 provide the CA-IS3211 typical application circuits for IGBT driving.

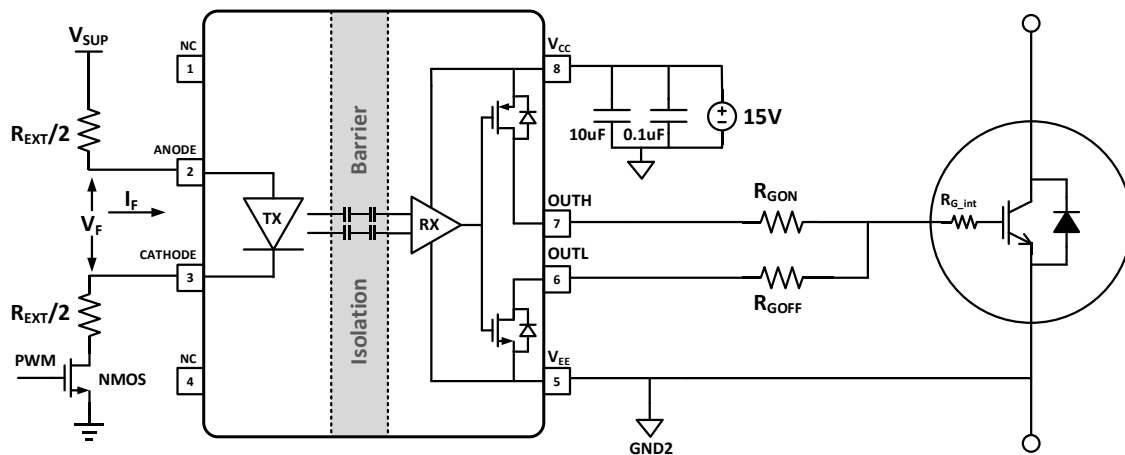


Figure 9-1 Typical application circuit with NMOS & current limit resistor at input side

The gate driver is typically placed between micro-controller (that is MCU or FPGA) and power transistors. As the CA-IS3211 input stage requires 7mA to 16mA forward current to drive the anode to turn-on input diode, most MCUs are not capable of providing enough forward current for this design, an external buffer is needed between the MCU output and CA-IS3211 input in the typical applications, see Figure 10-2. Usually, the buffer power supply is 3.3V or 5.0V, while the forward voltage drop of input diode is typically 2.1V (1.8V to 2.4V) with $1.5\text{mV}/^\circ\text{C}$ tempco, need to add a resistor R_{EXT} before the CA-IS3211 input to limit the forward current. For the input resistor selection, see the Input Current Limit section for more details.

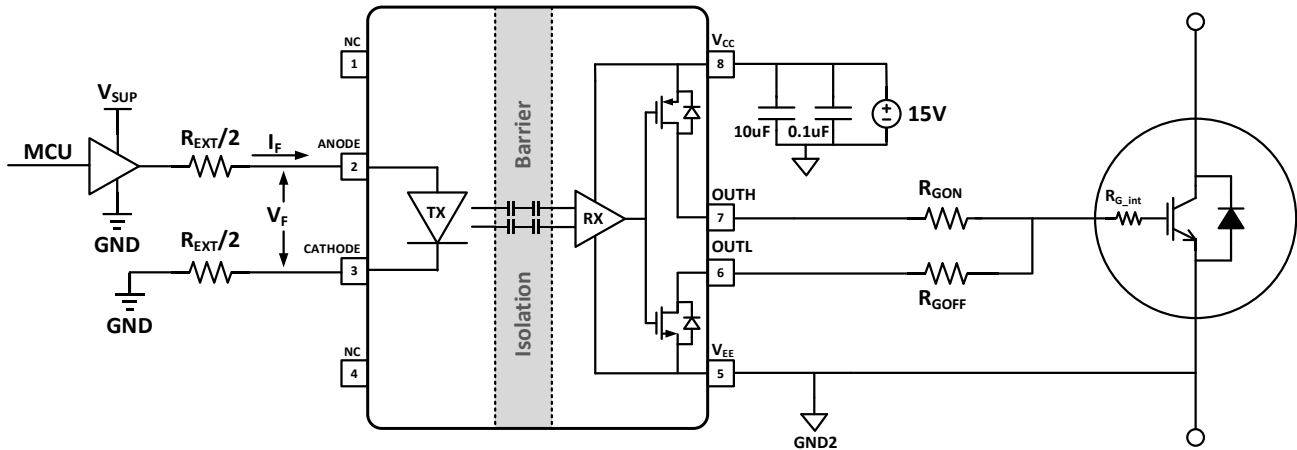


Figure 9-2 Typical application circuit with input buffer and current limit resistor

On the output-side, the power supply V_{CC} can be as high as 30V (32V abs max). The V_{CC} supply can be a single isolated supply up to 30V or isolated bipolar supply such that $V_{CC}-V_{EE}$ does not exceed 30V, or it can be bootstrapped with external diode and capacitors if the system uses a single power supply respected to the power ground. For most operation with single supply, the V_{CC} pin is connected to 15V with respect to ground for IGBT driver, and 20V for SiC MOSFET driver; connect the V_{EE} pin to GND.

For most operation with dual-supplies, the power transistors are turned off with a negative voltage on the gate with respect to the emitter or source. This configuration can prevent the power transistors from unintentionally turning on because of current induced from the Miller effect. The typical supply voltage of the V_{CC} and V_{EE} for bipolar operation are 15V and -8V with respect to GND for IGBT driver, and 20V and -5V for SiC MOSFET driver. Bypass V_{CC} and V_{EE} (for bipolar operation) with at least 10 μ F/50V low-ESR and low-ESL capacitors to GND. An additional 0.1 μ F /50V capacitor in parallel with the device biasing capacitor for high frequency filtering. To ensure the best performance, place the decoupling capacitors as close to the power-supply pin as possible.

9.2. Interlock configuration

In the typical applications, the gate drivers are used to drive high-side and low-side power transistors. The MCU generates complementary PWM pulses during normal operation. However, MCU failures or software faults can cause both the high-side and low-side PWM signals from the MCU to latch high. Interlock configuration can be used to prevent the output from being high at same time even both high-side and low-side inputs are pulled high. As shown in Figure 9-3, the anode of the high-side driver's input diode is connected to the cathode of the low-side driver's input diode. The cathode of the high-side driver's input diode is connected to the anode of the low-side driver's input diode. This architecture prevents both the input diodes from being "ON" at the same time, preventing shoot through in the external power transistors.

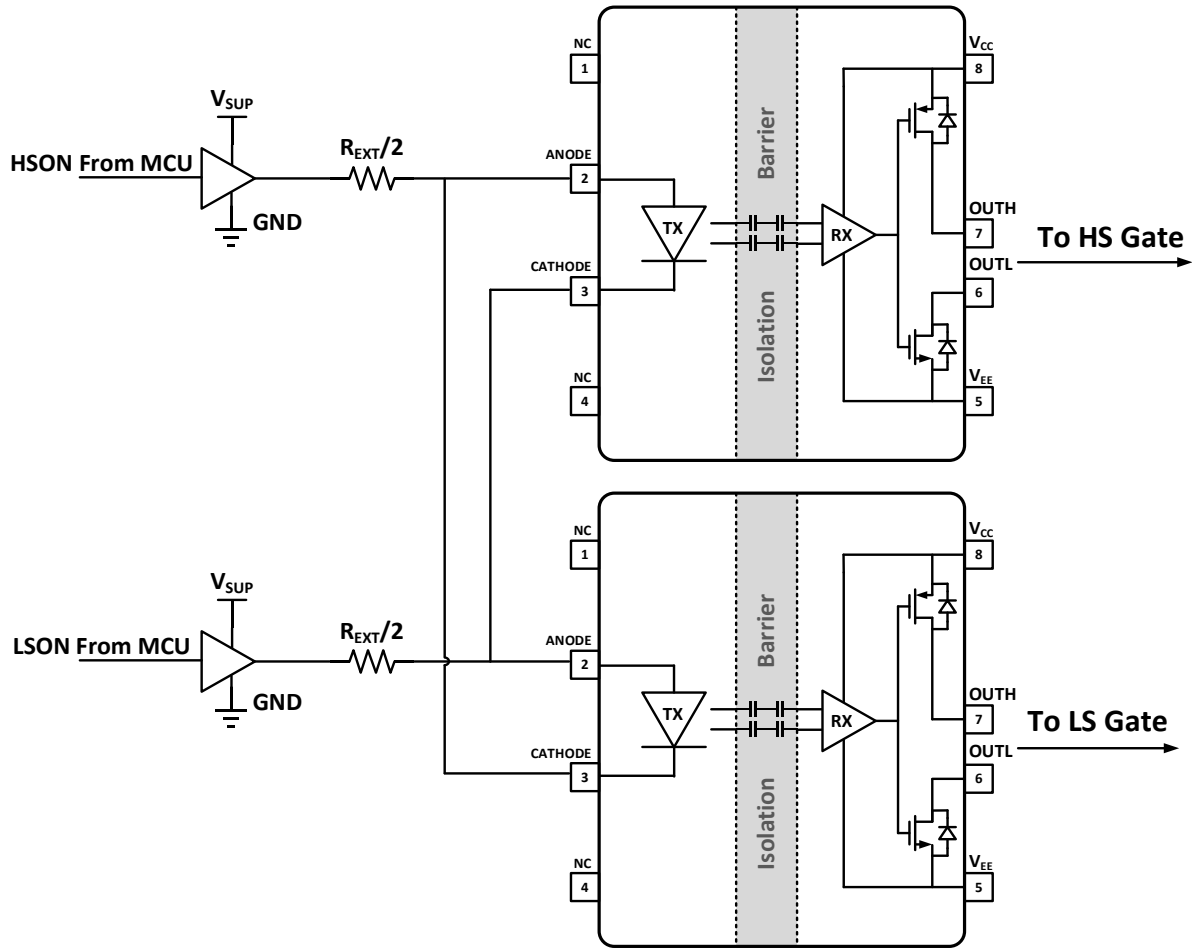


Figure 9-3 Interlock configuration

9.3. Input Current Limit

It is important to select a suitable resistor R_{EXT} to keep the diode forward current within 7mA to 16mA, and must be less than 16mA over the temperature range. The typical value of input diode forward threshold (I_{FLH}) is 2.8mA. In Figure 9-2 application circuit, the R_{EXT} is determined as follows:

$$R_{EXT} = \frac{V_{SUP} - V_F}{I_F} - R_{OH_buf}$$

Where,

- I_F is input forward current, the typical value is 10mA, with 7mA minimum value and 16mA maximum value;
- V_{SUP} is the supply voltage of the buffer, typical value is 5V, with 4.75V minimum value and 5.25V maximum value;
- V_F is the forward voltage drop of input diode, typical value is 2.1V (1.8V minimum value and 2.4V maximum value);
- R_{OH_buf} is the buffer's output resistances, typical value is 18Ω (13Ω minimum value and 22Ω maximum value).

Calculate the external resistor R_{EXT} using the above equation,

$$R_{EXT} = 272\Omega \text{ (typ)}, \text{ or from } 204\Omega \text{ to } 310\Omega$$

To turn the input diode off, the voltage between anode and cathode should be less than 0.8V, or $I_F < I_{FLH}$. The input diode can also be reverse biased up to 7V to turn it off and put the gate driver output low.

9.4. Driver Output Resistors Selection

In the typical application circuits Figure 9-1 and Figure 9-2, there are two external gate driver resistors: R_{GOFF} and R_{GON} , R_{GOFF} is the external turn-off resistance; R_{GON} is the external turn-on resistance. These two resistors are chosen to limit the ringing caused by fast switching and parasitic inductances and capacitances, reduce EMI, also can be used to fine-tune gate drive strength and optimize the switching loss. Use the following equations to estimate R_{GOFF} and R_{GON} resistor values,

I_{OH} peak current calculation:

$$I_{OH} = \min \left[5A, \frac{V_{CC} - V_{EE}}{(R_{NMOS} || R_{OH} + R_{GON} + R_{GFET_{int}})} \right]$$

Where $R_{GFET_{int}}$ is the gate resistance of the external power transistor, this number is available from power transistor data sheet. R_{NMOS} is 0.8ohm. R_{OH} is 5.5ohm.

I_{OL} peak current calculation:

$$I_{OL} = \min \left[6A, \frac{V_{CC} - V_{EE}}{(R_{OL} + R_{GOFF} + R_{GFET_{int}})} \right]$$

Where $R_{GFET_{int}}$ is the gate resistance of the external power transistor, this number is available from power transistor data sheet. R_{OL} is 0.5ohm.

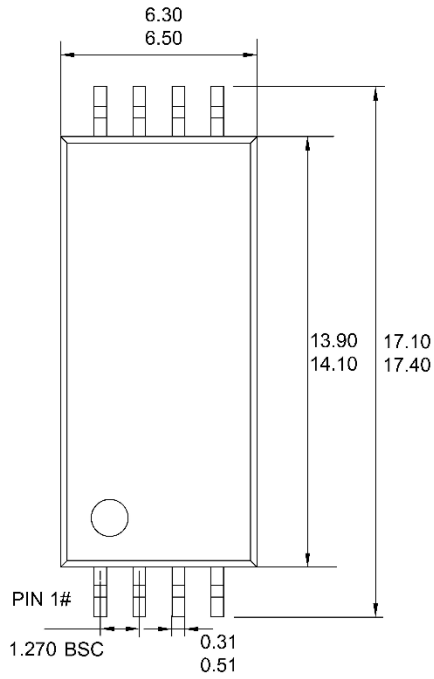
9.5. PCB Layout

Due to high current levels and fast switching (high dv/dt and di/dt) that radiate noise, proper PCB layout is essential. Follow these guidelines for good PCB layout:

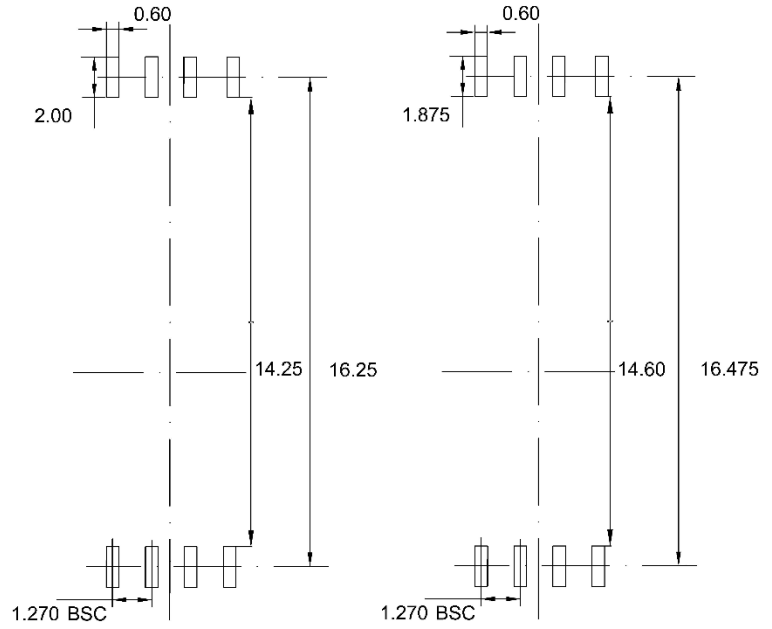
- To ensure the best performance and keep lower supply ripple, place the decoupling capacitors as close to the power-supply pin as possible. We recommend to use low ESR, low ESL MLCC capacitors.
- VOUT connections carrying pulsed currents must be very short and as wide as possible. The inductance of these connections must be kept to an absolute minimum due to the high di/dt of the currents in high-frequency-switching operation. This implies that the VOUT loop areas should be minimized. Additionally, small current loop areas reduce radiated EMI. Place the external transistor as close to the gate driver as possible.
- Connect the supply pins (V_{CC} , V_{EE}) to as large a copper pour or plane area as possible for best heat-sinking.
- To ensure isolation performance between the primary side and secondary side, on the top layer and bottom layer keep the space under the CA-IS3211 device free from traces, vias, and pads to maintain maximum creepage distance.
- For the multiple layers design, it is recommended to connect the V_{CC} and V_{EE} pins to internal ground or power planes through multiple vias. These vias should be located close to the IC pins to maximize thermal conductivity, also keep lower parasitic value.

10. Package Information

10.1. 8-Pin Super Wide Body (SOIC8-WWB) Package Outline

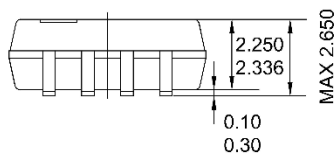


TOP VIEW

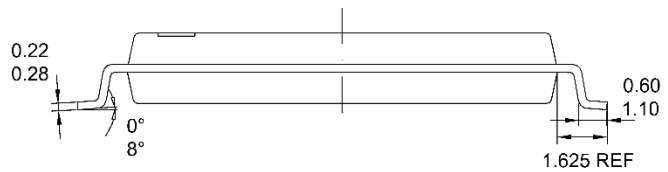


STANDARD

PCB CLEARANCE & CREEPAGE OPTIMIZED



FRONT VIEW



SIDE VIEW

Note:

1. All dimensions are in millimeters, angles are in degrees.

11. Soldering Information

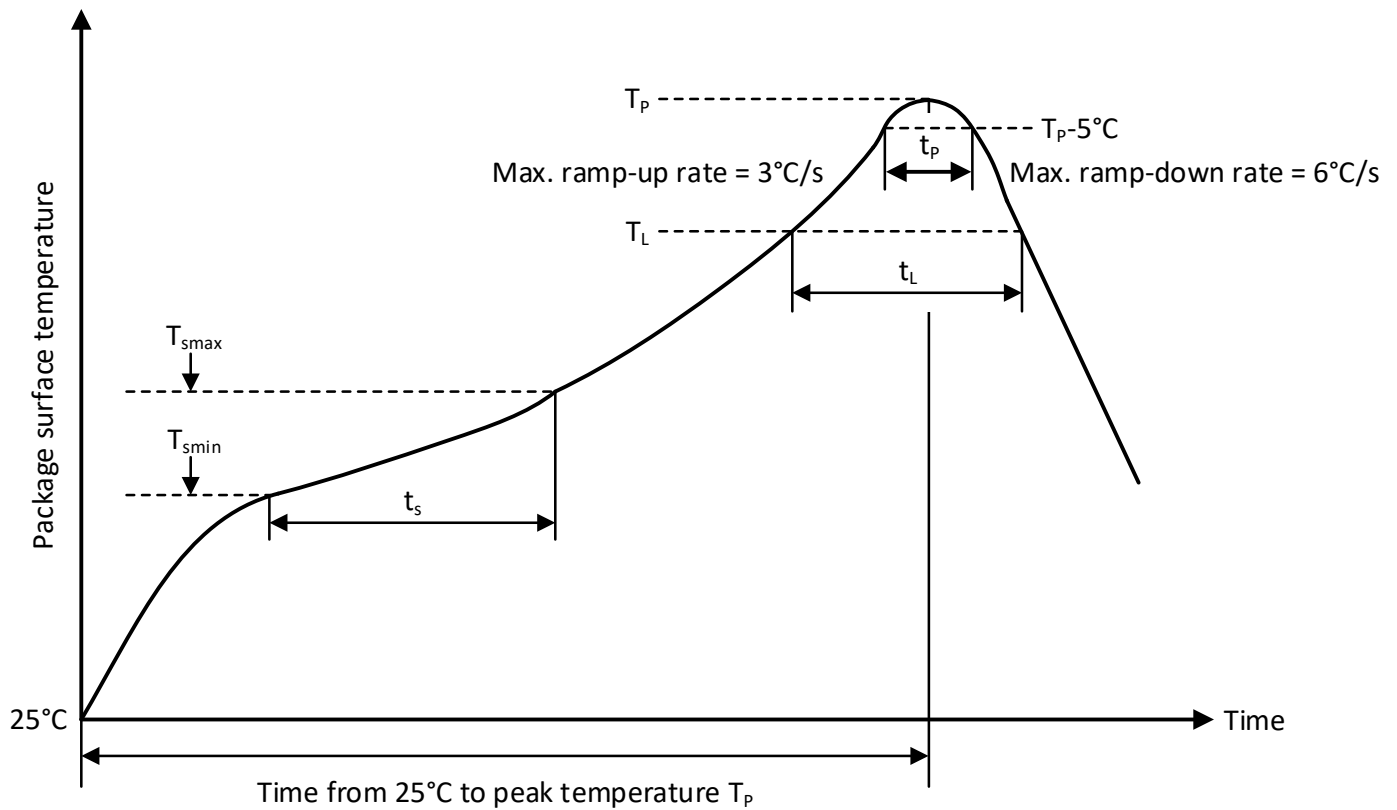


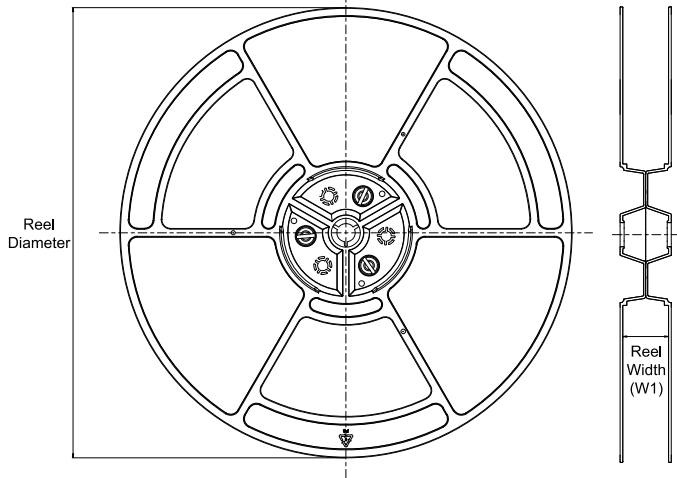
Figure 11-1 Soldering Temperature (reflow) Profile

Table 11-1 Soldering Temperature Parameter

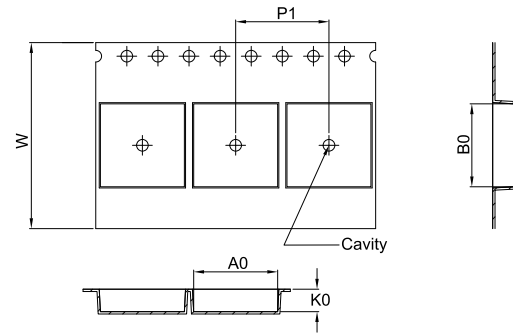
Profile Feature	Pb-Free Soldering
Ramp-up rate ($T_L = 217^\circ\text{C}$ to peak T_p)	3°C/s max
Time t_s of preheat temp ($T_{smin} = 150^\circ\text{C}$ to $T_{smax} = 200^\circ\text{C}$)	60~120 seconds
Time t_L to be maintained above 217°C	60~150 seconds
Peak temperature T_p	260°C
Time t_p within 5°C of actual peak temp	30 seconds max
Ramp-down rate (peak T_p to $T_L = 217^\circ\text{C}$)	6°C/s max
Time from 25°C to peak temperature T_p	8 minutes max

12. Tape and Reel Information

REEL DIMENSIONS

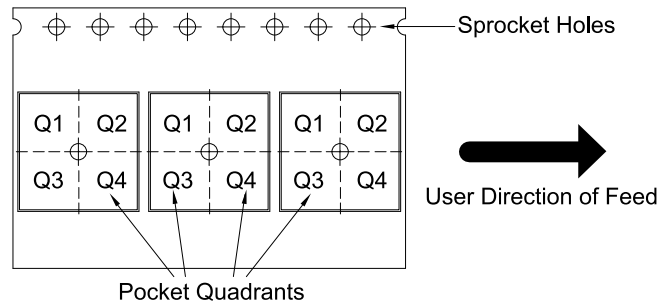


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CA-IS3211SCWG	SOIC	WG	8	500	330	16.4	17.70	6.80	2.80	24.00	16.00	Q1

13. Revision History

Revision Number	Description	Revised Date	Page Changed
Version 1.00	Initial publish	2025/01/20	NA

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