



# AEC-Q100 Qualification Report

Product Series: CA-IS3417WT-Q1

Report Version: V1.1

Reference Doc.: AEC-Q100-REV-J

Prepare	Review	Approve
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## 1. Overview

Reliability testing of microelectronic products is a risk mitigation process designed to ensure the service life of device in customer applications. Semiconductor wafer manufacturing process and package-level reliability can be assessed in a variety of ways and may include accelerated environmental test conditions. Chipanalog evaluates manufacturability of the device to verify a robust silicon and assembly flow to ensure continuity of supply to customers. Chipanalog qualifies new devices, significant changes, and product families based on AEC-Q100.

## 2. Part Number List

Package Type	Part Number
SOIC12-WB(WT)	CA-IS3417WT-Q1

## 3. Production Information

### 3.1. Wafer information

Fab site	DBH
Wafer	KUN
Fab Process	18BCD

### 3.2. Package information

Assembly site	UNIMOS
FT site	UNIMOS
Package	SOIC12-WB(WT)
Lead Frame	Cu
Bond wire	20um Au
MSL level	MSL3
Operation Temp.	Grade 1(-40°C - 125°C)

#### 4. Reliability Qualification Plan

Test Group A-Accelerated Environment Stress Tests					
Group	Item	Refer.	Test condition	QTY	Remark
A1	PC	J-STD-020 JESD22-A113	Test @ Rm, SMD only, Moisture Preconditioning before THB/BHAST, AC/UHAST, TC, and PTC stress, MSL = 3, Peak Reflow Temp = 260°C	77 pcs*3 lots	
A2	BHAST	JESD22-A110	BHAST: 130°C, 85% RH, $V_{cc1}= 5.5V$ , $V_{cc2}= 40V$ , 96 hrs (Test @ Rm/Hot)	77 pcs*3 lots	
A3	UHAST	JESD22-A101	UHAST: 130°C, 85% RH, 96 hrs (Test @ Rm)	77 pcs*3 lots	
A4	TC	JESD22-A104	-65°C-150°C, 500 cycles (Test @Rm/Hot)	77 pcs*3 lots	
A4	TC-SAT	J-STD-020	Check delamination in die attach or wire bonding surface areas via AM after TC	3 pcs*3 lots	
A5	PTC	JESD22-A105	-40°C-125°C, 1000 cycles (Test @ Rm/Hot)	NA	
A6	HTSL	JESD22-A103	$T_a = 150°C$ , 1000 hrs (Test @ Rm/Hot)	45pcs*1 lot	
Test Group B-Accelerated Lifetime Simulation Tests					
Group	Item	Refer.	Test condition	QTY	Remark
B1	HTOL	JESD22-A108	$T_a = 125°C$ , $V_{cc}= 40V$ , 1000 hrs (Test @ Rm/Cold/Hot)	77 pcs*3 lots	
B2	ELFR	AEC-Q100-008	$T_a = 125°C$ , $V_{cc}= 40V$ , 48 hrs (Test @ Rm/Hot)	800 pcs*3 lots	
B3	EDR	AEC-Q100-005	Test @ Rm/Hot	NA	
Group C-Package Assembly Integrity Tests					
Group	Item	Refer.	Test condition	QTY	Remark
C1	WBS	AEC-Q100-001 AEC-Q003	Cpk > 1.67, T0 samples	30 bonds from 5 pcs	
C2	WBP	MIL-STD883 AEC-Q003	Cpk > 1.67, T0 samples	30 bonds from 5 pcs	
C2	WBP	MIL-STD883 AEC-Q003	0 fails, post-TC samples	30 bonds from 5 pcs	
C3	SD	J-STD-002	> 95% coverage, 8hr steam aging prior to testing	15 pcs*1 lot	
C4	PD	JESD22-B100 JESD22-B108 AEC-Q003	Cpk > 1.67	10 pcs*3 lots	
C5	SBS	AEC-Q100-010 AEC-Q003	Cpk > 1.67, 5 balls from min. of 10 devices	NA	

C6	LI	JESD22-B105	10 leads from each of 5 devices	5pcs*1 lot	
<b>Test Group D–Die Fabrication Reliability Tests</b>					
Group	Item	Refer.	Test condition	QTY	Remark
D1	EM	JESD61	---	---	Done by Fab
D2	TDDDB	JESD35	---	---	Done by Fab
D3	HCI	JESD60 & 28	---	---	Done by Fab
D4	BTI	JESD90	---	---	Done by Fab
D5	SM	JESD61, 87, & 202	---	---	Done by Fab
<b>Group E-Electrical Verification Tests</b>					
Group	Item	Refer.	Test condition	QTY	Remark
E1	TEST	per datasheet	Pre and Post Stress Electrical Test	All	
E2	HBM	AEC Q100-002	$\pm 500V$ , $\pm 1KV$ , $\pm 2KV$ , $\pm 3KV$ (Test @ Rm/Hot)	3 pcs*1 lot	
E3	CDM	AEC-Q100-011	$\pm 250V$ , $\pm 500V$ , $\pm 750V$ , $\pm 2KV$ (Test @ Rm/Hot)	3 pcs*1 lot	
E4	LU	AEC-Q100-004	125°C, I-trigger $\pm 200mA$ (Test @ Rm/Hot)	6 pcs*1 lot	
E9	EMC	SAE J1752/3	Electromagnetic Compatibility (Radiated Emissions)	1 pcs*1 lot	
E10	SC	AEC-Q100-012	/	NA	
E11	SER	JESD89-1/-2/-3	/	NA	
E12	LF	AEC-Q005	/	2 pcs*3 lots	
<b>Group S-Special Requirement Tests</b>					
S1	BLR-Bending	JESD22-B113	Align with customer	NA	
S2	BLR-Drop	JESD22-B11	Align with customer	NA	
S3	BLR-TC	IPC-9701	Refer test requirement	NA	
S4	BLR-Vibration	JESD22-B103	Refer test requirement	NA	

**Note:** Group E5, E6, E7 and Group F are not reliability related items. Group G are not applicable to non-hermetic packaged devices.

## 5. Reliability Test Results

<b>Test Group A–Accelerated Environment Stress Test</b>					
<b>Group</b>	<b>Item</b>	<b>Test Condition</b>	<b>QTY</b>	<b>Lot NO.</b>	<b>Result</b>
A1	PC	Test @ Rm, SMD only, Moisture Preconditioning before BHAST, UHAST, TC stress, MSL = 3, Peak Reflow Temp = 260°C	240 pcs*3 lots	2345D	Pass
				2346D	Pass
				2347D	Pass
A2	BHAST	130°C, 85% RH, 96 hrs, $V_{cc1}= 5.5V$ , $V_{cc2}= 40V$	80 pcs*3 lots	2345D	Pass
				2346D	Pass
				2347D	Pass
A2	BHAST-Robust	130°C, 85% RH, 192 hrs, $V_{cc1}= 5.5V$ , $V_{cc2}= 40V$	80 pcs*1 lots	2347D	Pass
A3	UHAST	130°C, 85% RH, 96 hrs	80 pcs*3 lots	2345D	Pass
				2346D	Pass
				2347D	Pass
A3	UHAST-Robust	130°C, 85% RH, 192 hrs	80 pcs*1 lots	2345D	Pass
A4	TC	-65°C-150°C, 500 cycles	80 pcs*3 lots	2345D	Pass
				2346D	Pass
				2347D	Pass
A4	TC-SAT	Check delamination in die attach or wire bonding surface areas via AM after TC	80 pcs*3 lots	2345D	Pass
				2346D	Pass
				2347D	Pass
A4	TC-Robust	-65°C-150°C, 1000 cycles	70 pcs*1 lots	2346D	Pass
A4	TC-Robust-SAT	Check delamination in die attach or wire bonding surface areas via AM after TC	70 pcs*1 lots	2346D	Pass
A6	HTSL	$T_a = 150^\circ C$ , 1000 hrs	50 pcs*1 lot	2347D	Pass
A6	HTSL-Robust	$T_a = 150^\circ C$ , 2000 hrs	50 pcs*1 lot	2347D	Pass
<b>Test Group B–Accelerated Lifetime Simulation Tests</b>					
<b>Group</b>	<b>Item</b>	<b>Test Condition</b>	<b>QTY</b>	<b>Lot NO.</b>	<b>Result</b>
B1	HTOL	$T_a = 125^\circ C$ , 1000 hrs, $V_{cc1}= 3.3V$ (input f = 1kHz), $V_{cc2}=40V$	80 pcs*3 lots	2345D	Pass
				2346D	Pass
				2347D	Pass
B1	HTOL-Robust	$T_a = 125^\circ C$ , 2000 hrs, $V_{cc1}= 3.3V$ (input f = 1kHz), $V_{cc2}=40V$	80 pcs*1 lots	2347D	Pass
B2	ELFR	$T_a = 125^\circ C$ , 48 hrs, $V_{cc} = 3.3V$ , (input f = 1kHz), $V_{cc2}=40V$	800 pcs*3 lots	2345D	Pass
				2346D	Pass
				2347D	Pass
<b>Group C–Package Assembly Integrity Tests</b>					

Group	Item	Test Condition	QTY	Lot NO.	Result
C1	WBS	Cpk > 1.67, each bonder used, T0 samples	30 bonds from 5 pcs	2345D	Pass, CPK=8.381
C1	WBS	0 fails, each bonder used, post-TC samples	30 bonds from 5 pcs	2345D	Pass, CPK=5.722
C2	WBP	Cpk > 1.67, each bonder used, T0 samples	30 bonds from 5 pcs	2345D	Pass, CPK=3.491
C2	WBP	0 fails, each bonder used, post-TC samples	30 bonds from 5 pcs	2345D	Pass, CPK=3.723
C3	SD	>95% coverage, 8 hrs steam aging prior to testing	15 pcs*1 lot	2345D	Pass
C4	PD	Cpk > 1.67	10 pcs*3 lots	2345D	Pass
				2346D	Pass
				2347D	Pass

### TEST GROUP D–Die Fabrication Reliability Tests

Group	Item	Test Condition	ADDITIONAL REQUIREMENTS
D1	EM	---	The Die Fabrication Reliability Tests are carried out by every fabrication site. The data, test method, calculations and internal criteria are available to the customer upon request.
D2	TDDDB	---	
D3	HCI	---	
D4	NBTI	---	
D5	SM	---	

### Group E-Electrical Verification Tests

Group	Item	Test Condition	QTY	Lot NO.	Result
E1	TEST	Pre and Post Stress Electrical Test	All	All	Pass
E2	HBM	Drain 1 to Drain 2 Pass $\pm 3KV$ , Other Pins Pass $\pm 8KV$	3 pcs*1 lot	2345D	2
E3	CDM	$\pm 250V$ , $\pm 500V$ , $\pm 750V$ , $\pm 2KV$	3 pcs*1 lot	2345D	C3
E4	LU	125°C, I-trigger $\pm 200mA$	6 pcs*1 lot	2345D	Class II A
E9	EMC	Electromagnetic Compatibility (Radiated Emissions)	1 pcs*1 lot	2345D	L11
E12	LF	SOIC12-WB	Refer to UNIMOS SOIC16-WB Tin Whisker report		

## 6. MTTF&FIT

Supporting Data (Ea = 0.7 eV, Confidence Level = 60%)							MTTF (hrs)	FIT
Test Temp.	Test Voltage	Duration	QTY	Fail QTY	Operation Temp.	Operation Voltage	3.70E7	27.01
125°C	3.3V	1000 hrs	160	0	55°C	3.3V		
125°C	3.3V	2000 hrs	80	0	55°C	3.3V		
125°C	3.3V	48 hrs	2400	0	55°C	3.3V		

**Note:** The FIT data is generated based on Arrhenius model and voltage acceleration model.

## **7. Conclusion**

CA-IS3417WT-Q1 product is qualified according to AEC-Q100 standard.



## Disclaimer

This information is provided to assist customers in design and development. It could change for technology innovation without notice.

The devices are shipped after passing final test. Customers are responsible to conduct sufficient engineering and additional qualification testing to determine whether a device is suitable for use in their applications.

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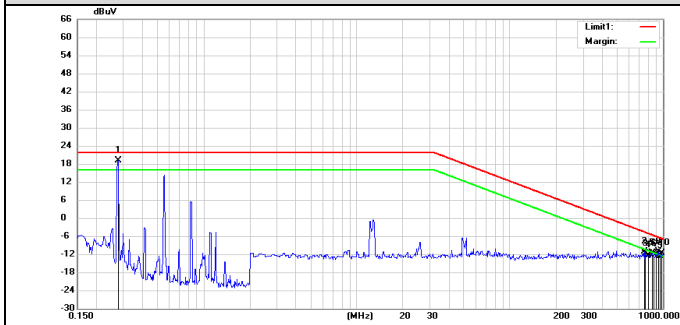
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## Revision History

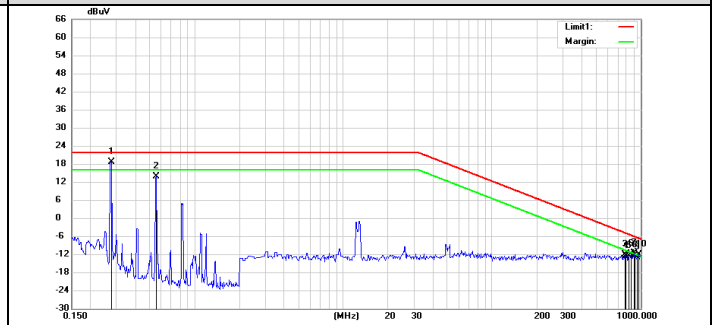
Revision	Change Log	Date
V1.0	Initial	May. 2024
V1.1	Add 1lot HTOL 2000hrs Result Add 1lot BHAST 192hrs Result Add 1lot UHAST 192hrs Result Add 1lot TCT 1000cycles Result Add 1lot HTSL 2000hrs Result	Jun. 2024

## Appendix 1: EMC Test Results

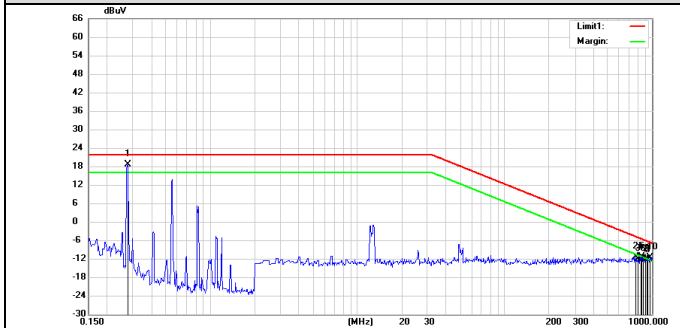
**Vcc1= 3.3V(input f = 1kHz), Vcc2=40V,  
orientation 0°**



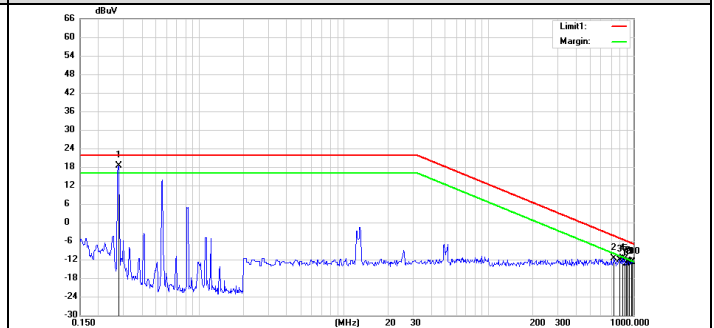
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orientation 90°**



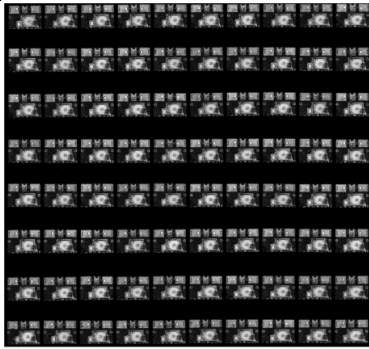
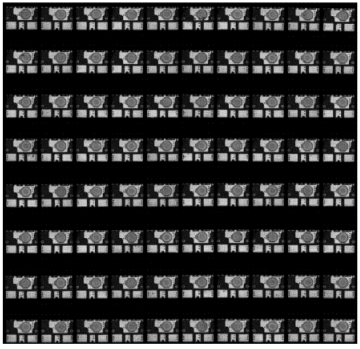
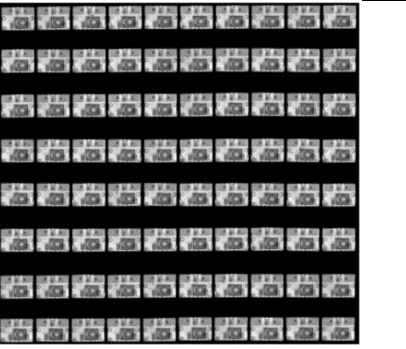
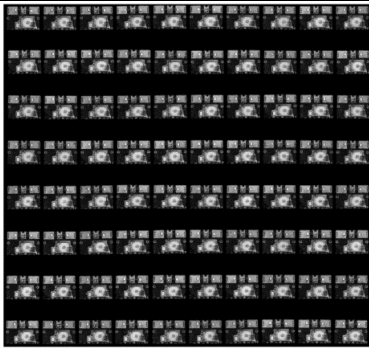
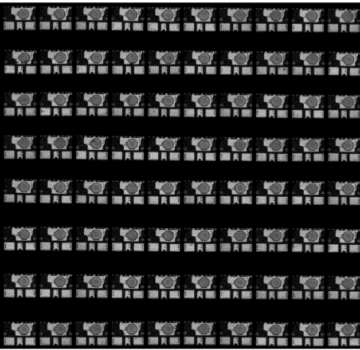
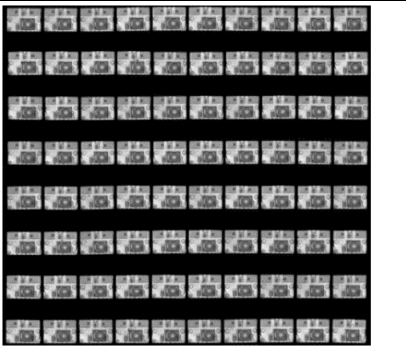
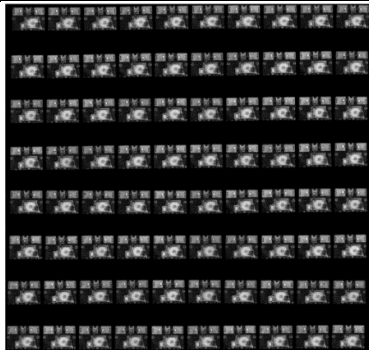
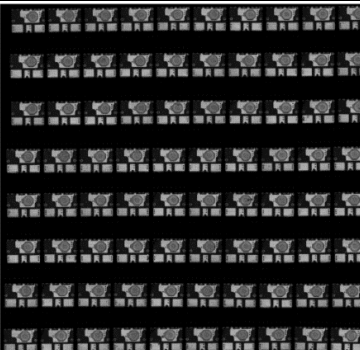
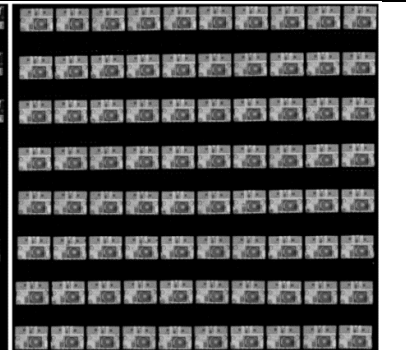
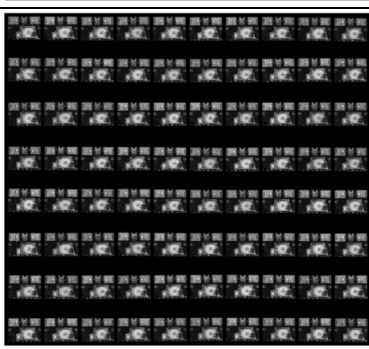
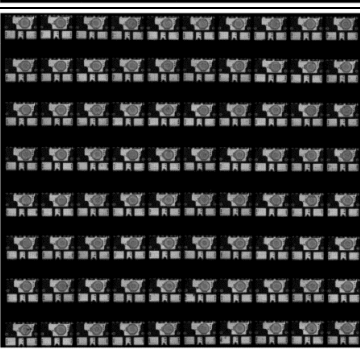
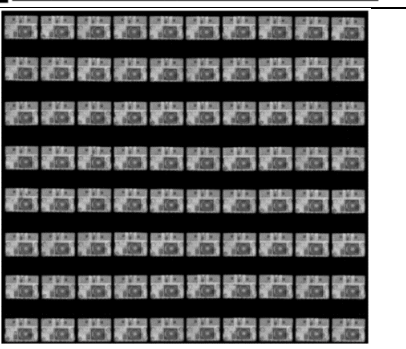
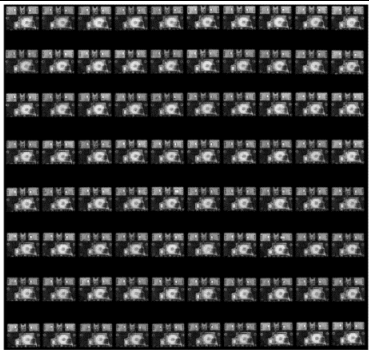
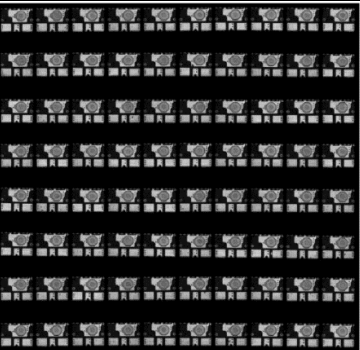
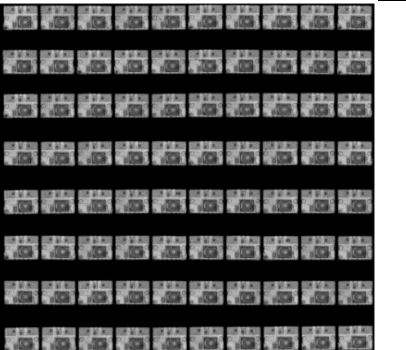
**Vcc1= 3.3V(input f = 1kHz), Vcc2=40V,  
orientation 180°**

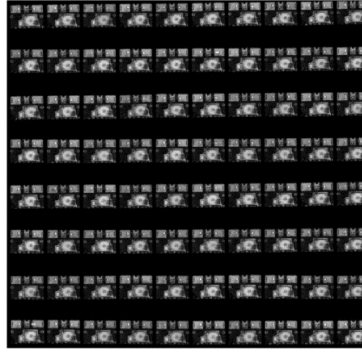
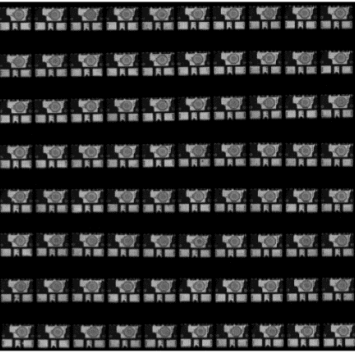
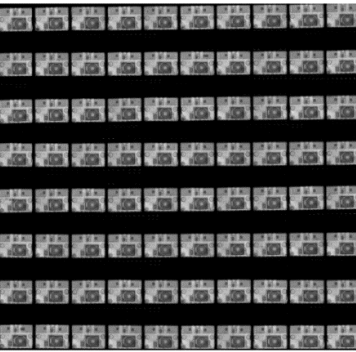
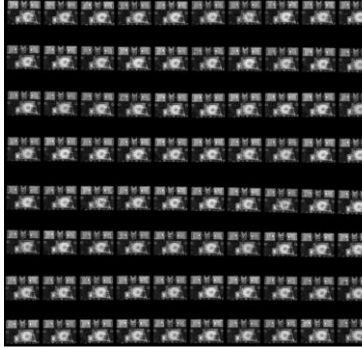
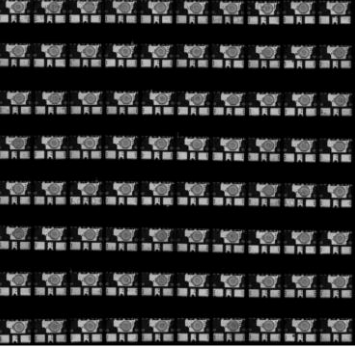
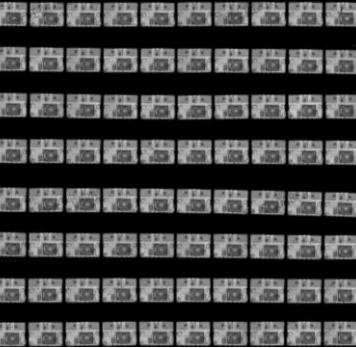

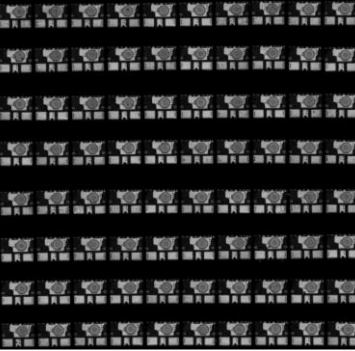
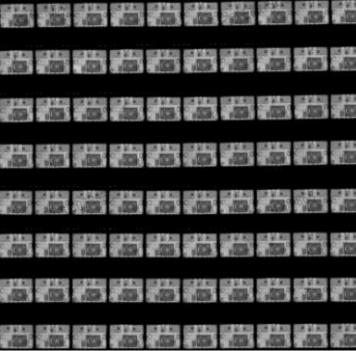


**Vcc1= 3.3V(input f = 1kHz), Vcc2=40V,  
orientation 270°**



## Appendix 2: SAT Test Results

<p><b>Lot 1 pre-MSL</b></p>			
<p><b>Lot 1 post-MSL</b></p>			
<p><b>Lot 2 pre-MSL</b></p>			
<p><b>Lot 2 post-MSL</b></p>			
<p><b>Lot 3 pre-MSL</b></p>			

<p><b>Lot 3 post-MSL</b></p>			
<p><b>Lot1 TC500</b></p>			
<p><b>Lot2 TC500</b></p>			
<p><b>Lot3 TC500</b></p>	