CA-IS2062A 2.5kV$_{RMS}$ Isolated CAN Transceivers With Integrated DC-DC Converter

1 Key Features

- Meet the ISO 11898-2:2016 Physical Layer Standard
- Support Classic CAN up to 1Mbps and CAN FD (Flexible Data Rate) up to 5Mbps
- Integrate DC-DC Converter to Generate 5V Isolated Power Supply for the Bus Side
- Integrated Protection Functions to Support Reliable Data Communications
  - DC Bus Fault Protection Voltage: ±42V
  - Bus Input Common-Mode Voltage Range: ±24V
  - Driver Dominant Timeout (DTO) to Prevent Bus Lockup, Allowing Minimum Data Rate to 4.4kbps
  - Thermal Shutdown Protection and Current Limiting Protection of Bus Pins
  - Ideal Passive and High Impedance Bus Terminals When Unpowered
  - UVLO Protection of VDDP and VDDL
- Logic-side Supply VDDL Range: 2.5V to 5.5V
- Wide Operating Temperature Range: –40°C to 125°C
- High CMTI: ±150kV/μs (typ)
- Low Loop Delay: 165ns (typ), 255ns (max)
- Ultra-Compact Package: LGA16
- >40-year Life at Rated Working Voltage
- 2.5-kV$_{RMS}$ Isolated Voltage Rating for 60s
- Safety-Related Certifications:
  - UL certification according to UL 1577
  - CQC certification according to GB4943.1-2022
  - TUV certification

2 Applications

- Industrial Controls
- Building Automation
- Battery Charging and Management
- Energy Storage
- Solar System
- Medical Equipment
- Telecom Equipment

3 Description

The CA-IS2062A is a galvanically-isolated CAN transceiver with a built-in isolated DC-DC converter, which eliminates the need of an external isolated power supply to save the system space and simplify the design. The internal logic input and output buffer are separated by a silicon oxide (SiO_2) insulation barrier that provides up to 2.5-kV$_{RMS}$ (60s) galvanic isolation as well as typical CMTI of ±150kV/μs. The isolation barrier helps to ensure the correct transmission of data by breaking the ground loops and reducing the noise where there are large differences in ground potential between ports.

The CA-IS2062A operates from a single 5V supply VDDP on the logical side, and the logical supply VDDL ranges from 2.5V to 5.5V. VDDL and VDDP could be separated and powered by different voltages, which is convenient to interface with the low-voltage controller. VDDL could also share the same 5V power supply with VDDP. An integrated DC-DC converter generates the 5V output voltage VISO$_{OUT}$ for the bus side to supply the VISO$_{IN}$ which is the power supply pin of CAN transceiver. It needs to connect VISO$_{OUT}$ to VISO$_{IN}$ directly in applications.

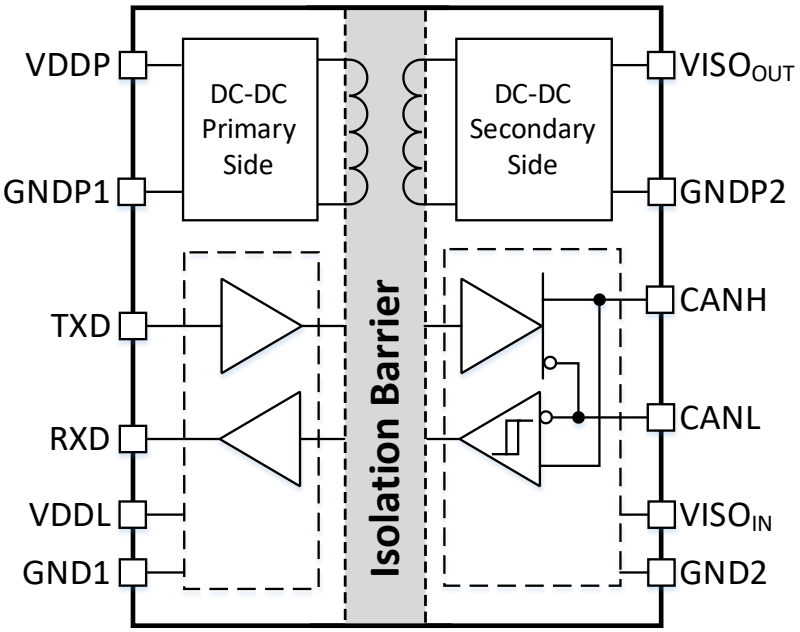
The transceiver in CA-IS2062A supports CAN FD up to 5Mbps and features integrated protection for robust communication, including current limiting on bus pins (CANH/CANL), thermal shutdown protection, and up to ±42V bus fault protection voltage. The dominant timeout (DTO) detection prevents bus lockup caused by controller error or by a fault on the TXD input. Furthermore, this device offers up to ±24V input common-mode range (CMR), which far exceeds the ISO 11898-2 specification of –2V to +7V, supporting reliable data communication.

The CA-IS2062A devices are packaged in ultra-compact LGA16 packages, which could save PCB space significantly. This device is specified over the extended industrial temperature range of –40°C to 125°C.

Device Information

PART NUMBER	PACKAGE	BODY SIZE (NOM)
CA-IS2062A	LGA16	5.2mm × 4.65mm

Simplified Schematic



4 Ordering Guide

Table 4-1 Ordering Guide for Valid Ordering Part Number

Part Number	VDDP	VDDL	Data Rate	Isolation Rating	Package
CA-IS2062A	4.5~5.5	2.5~5.5	5Mbps	2.5kV$_{RMS}$	LGA16

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5 Revision History

Revision	Description	Date	Page
Version 1.00	Initial version	2024.08.01	NA
Version 1.01	Updated TUV certification Updated UL certification Updated Figure 10-1 and Figure 10-3: connect $VISO_{OUT}$ to $VISO_{IN}$	2025.03.25	1, 7 7 18, 20

6 Pin Descriptions and Functions

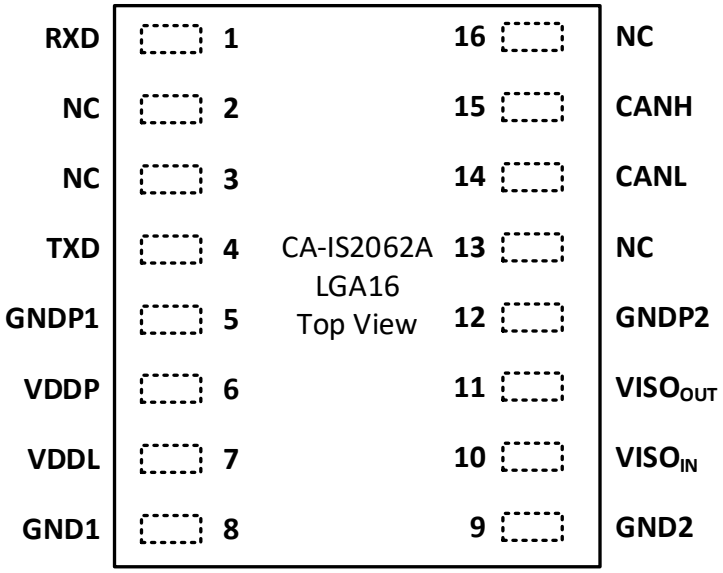


Figure 6-1 Pin Configuration

Table 6-1 Pin Description and Functions

NAME	PIN NUMBER	TYPE	DESCRIPTION
RXD	1	Digital Output	Receiver's output. RXD is high when the bus state is recessive. RXD is low when the bus state is dominant.
NC	2, 3	--	Logic-side no connection, leave them open.
TXD	4	Digital Input	Driver's data input. CANH and CANL are in the dominant state when TXD is low. CANH and CANL are in the recessive state when TXD is high.
GNDP1	5	Ground	Logic-side reference ground for DC-DC converter, connect to GND1 directly in layout.
$VDDP^{1}$	6	Power	Logic-side power supply for DC-DC converter, bypass VDDP to GNDP1 with 0.1μF and at least 10μF capacitors as close to the device as possible.
$VDDL^{1}$	7	Power	Logic-side power supply for logical interface.
GND1	8	Ground	Logic-side reference ground for logical interface, connect to GNDP1 directly in layout.
GND2	9	Ground	Bus-side reference ground for CAN transceiver, connect to GNDP2 directly in layout.
$VISO_{IN}^{2}$	10	Power	Bus-side power supply for CAN transceiver, connect to $VISO_{OUT}$ directly in layout.
$VISO_{OUT}^{2}$	11	Power	Isolated DC-DC converter's output, connect to $VISO_{IN}$ directly in layout and bypass $VISO_{OUT}$ to GNDP2 with 0.1μF and at least 10μF capacitors as close to the device as possible.
GNDP2	12	Ground	Bus-side reference ground for DC-DC converter, connect to GND2 directly in layout.
NC	13, 16	--	Bus-side no connection, leave them open.
CANL	14	Bus I/O	Low-level CAN bus line.
CANH	15	Bus I/O	High-level CAN bus line.

NOTE:

1. VDDP and VDDL must exceed $VDDP_{ULVO+}$ and $VDDL_{ULVO+}$ respectively for the setup of $VISO_{OUT}$ to a normal output voltage.
2. $VISO_{IN}$ and $VISO_{OUT}$ must be connected together for the setup of $VISO_{OUT}$ to a normal output voltage.

7 Specifications

7.1 Absolute Maximum Ratings[1]

PARAMETER		MIN	MAX	UNIT
VDDP, VDDL	Logic-side power supply voltage[2]	–0.5	6.0	V
$VISO_{OUT}$, $VISO_{IN}$	Bus-side power supply voltage[2]	–0.5	6.0	V
V_I	Logic-side input voltage (TXD)	–0.5	VDDL + 0.5[3]	V
V_{BUS}	Voltage on bus pins (CANH, CANL), reference to GND2	–42	42	V
V_{BUS_DIFF}	Differential voltage on bus pins (CANH – CANL)	–42	42	V
I_O	Output current on RXD pin	–20	20	mA
T_J	Junction Temperature	–40	150	°C
T_{STG}	Storage Temperature	–65	150	°C

NOTE:

1. Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. All voltage values are with respect to the local ground terminal (GNDP1/GND1 or GNDP2/GND2) and are peak voltage values.
3. Maximum voltage must not exceed 6V.

7.2 ESD Ratings

			VALUE	UNIT
V_{ESD} Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001	Logic-side pins to GNDP1/GND1	±6	kV
		Bus-side pins to GNDP2/GND2	±6	
	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins		±2	

7.3 Recommended Operating Conditions

PARAMETER		MIN	NOM	MAX	UNIT
VDDP	Logic-side supply voltage for DC-DC converter	4.5	5	5.5	V
VDDL	Logic-side supply voltage for logical interface	2.5	3.3 or 5	5.5	V
V_{BUS}	Voltage on bus pins (separately or common mode)	–24		24	V
V_{IH}	Input high voltage on TXD pin	0.7 × VDDL		VDDL	V
V_{IL}	Input low voltage on TXD pin	0		0.3 × VDDL	V
I_{OH}	High-level output current on RXD pin	–4			mA
I_{OL}	Low-level output current on RXD pin			4	mA
T_A	Ambient Temperature	–40		125	°C
T_J	Junction Temperature	–40		150	°C

7.4 Thermal Information

THERMAL METRIC		PACKAGE	UNIT
		LGA16 (A)	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	133.8	°C/W

7.5 Insulation Specifications

PARAMETR		TEST CONDITIONS	VALUE	UNIT
CLR	External clearance[1]	Shortest terminal-to-terminal distance through air	3.45	mm
CPG	External creepage[1]	Shortest terminal-to-terminal distance across the package surface	3.45	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	18	µm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	> 400	V
	Material group	According to IEC 60664-1	II	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 150V_{RMS}	I-IV	
		Rated mains voltage ≤ 300V_{RMS}	I-III	
DIN EN IEC 60747-17 (VDE 0884-17)[2]				
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	566	V_{PK}
V_{IOWM}	Maximum working isolation voltage	AC voltage; Time dependent dielectric breakdown (TDDB) Test	400	V_{RMS}
		DC voltage	566	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t = 60s (qualification); $V_{TEST} = 1.2 \times V_{IOTM}$, t= 1s (100% production)	3535	V_{PK}
V_{IMP}	Maximum impulse voltage	1.2/50-µs waveform per IEC 62368-1	5000	V_{PK}
V_{IOSM}	Maximum surge isolation voltage[3]	1.2/50-µs waveform per IEC 62368-1, $V_{IOSM} \geq 1.3 \times V_{IMP}$; Tested in air (qualification test)	6500	V_{PK}
q_{pd}	Apparent charge[4]	Method a, After input/output safety test subgroup 2/3, $V_{ini} = V_{IOTM}$, t_{ini} = 60s; $V_{pd(m)} = 1.2 \times V_{IORM}$, t_m = 10s	≤ 5	pC
		Method a, After environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, t_{ini} = 60s; $V_{pd(m)} = 1.6 \times V_{IORM}$, t_m = 10s	≤ 5	
		Method b1, At routine test (100% production) and preconditioning (type test) $V_{ini} = 1.2 \times V_{IOTM}$, t_{ini} = 1s; $V_{pd(m)} = 1.875 \times V_{IORM}$, t_m = 1s	≤ 5	
C_{IO}	Barrier capacitance, input to output[5]	V_{IO} = 0.4 × sin(2πft), f = 1MHz	~ 3.5	pF
R_{IO}	Isolation resistance[5]	V_{IO} = 500V, T_A = 25°C	> 10^{12}	Ω
		V_{IO} = 500V, 100°C ≤ T_A ≤ 125°C	> 10^{11}	
		V_{IO} = 500V at T_S = 150°C	> 10^9	
	Pollution degree		2	
UL 1577				
V_{ISO}	Maximum withstanding isolation voltage	$V_{TEST} = V_{ISO}$, t = 60s (qualification), $V_{TEST} = 1.2 \times V_{ISO}$, t = 1s (100% production)	2500	V_{RMS}

NOTE:

1. Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications.
2. This coupler is suitable for safe electrical insulation only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
3. Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
4. Apparent charge is electrical discharge caused by a partial discharge (pd).
5. All pins on each side of the barrier tied together creating a two-terminal device.

7.6 Safety-Related Certifications

UL	CQC (Pending)	TUV
Recognized under UL 1577 Component Recognition Program	Certified according to GB4943.1-2022	Certified according to EN 61010-1 and EN 62368-1
Single protection 2500V_{RMS}	Basic insulation (Altitude ≤ 5000m)	EN 61010-1: 2500V_{RMS} EN 62368-1: 2500V_{RMS}
Certification Number: E511334	Certification Number:	Client reference number: 2253313

7.7 Electrical Characteristics

VDDP connects to VDDL, GNDP1 connects to GND1, $VISO_{OUT}$ connects to $VISO_{IN}$, GNDP2 connects to GND2, over recommended operating conditions (unless otherwise noted). All typical specifications are at VDDP = VDDL = 5V, T_A = 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Supply Current							
I_{DDP}	Logic-side supply current	TXD = 0V, dominant, R_L = 60Ω			105	150	mA
		TXD = VDDL, recessive			10	20	
Isolated Power Supply							
V_{ISO}	Isolated output voltage	I_{ISO} = 0 to 80mA, VDDP = VDDL = 5V, no load between CANH and CANL		4.5	5.0	5.5	V
$VDDP_{UVLO+}$	Rising under voltage lock-out	VDDP		2.5	2.7	2.9	V
$VDDP_{UVLO-}$	Falling under voltage lock-out			2.1	2.3	2.5	
$VDDP_{UVLO\_HYS}$	Hysteresis under voltage lock-out				0.4		
$VDDL_{UVLO+}$	Rising under voltage lock-out	VDDL		2.05	2.25	2.45	V
$VDDL_{UVLO-}$	Falling under voltage lock-out			1.9	2.1	2.3	
$VDDL_{UVLO\_HYS}$	Hysteresis under voltage lock-out				0.15		
Driver							
$V_{O(D)}$	Bus output voltage (dominant)	V_I = 0V, R_L = 60Ω; see Figure 8-1 and Figure 8-2	CANH	2.9		4.5	V
			CANL	0.5		2	
$V_{O(R)}$	Bus output voltage (recessive)	V_I = VDDL, R_L = 60Ω; see Figure 8-1 and Figure 8-2		2	2.5	3	V
$V_{OD(D)}$	Differential output voltage (dominant)	V_I = 0V, R_L = 60Ω; see Figure 8-1, Figure 8-2 and Figure 8-3		1.5		3	V
		V_I = 0V, R_L = 45Ω; see Figure 8-1 and Figure 8-2		1.3		3	
$V_{OD(R)}$	Differential output voltage (recessive)	V_I = VDDL, R_L = 60Ω; see Figure 8-1 and Figure 8-2		–80		80	mV
		V_I = VDDL, R_L = open; see Figure 8-1 and Figure 8-2		–50		50	
$V_{OC(D)}$	Common mode output voltage (dominant)	See Figure 8-4		2	2.5	3	V
I_{IH}	High-level input current on TXD pin	V_I = VDDL				20	µA
I_{IL}	Low-level input current on TXD pin	V_I = 0V		–20			µA
$I_{OS(SS)}$	Short-circuit steady-state output current	V_{CANH} = –24V, CANL open; see Figure 8-5		–105			mA
		V_{CANH} = 24V, CANL open; see Figure 8-5				5	
		V_{CANL} = –24V, CANH open; see Figure 8-5		–5			
		V_{CANL} = 24V, CANH open; see Figure 8-5				105	
CMTI	Common-mode transient immunity	V_{TEST} = ±1kV; see Figure 8-12		±100	±150		kV/µs
Receiver							
V_{IT}	Differential Input threshold voltage	V_{CM} = –20V to 20V		0.5		0.9	V
		V_{CM} = –24V to 24V		0.4		1.0	V
V_{HYS}	Hysteresis voltage for differential input threshold				120		mV
V_{OH}	High-level output voltage on RXD pin	I_{OH} = –4mA; see Figure 8-6		VDDL – 0.4	VDDL – 0.2		V
		I_{OH} = –20µA; see Figure 8-6		VDDL – 0.1	VDDL		
V_{OL}	Low-level output voltage on RXD pin	I_{OL} = 4mA; see Figure 8-6			0.2	0.4	V
		I_{OL} = 20µA; see Figure 8-6			0	0.1	
C_I	Single-ended input capacitance	CANH or CANL to GND2			24		pF
C_{ID}	Differential input capacitance	Between CANH and CANL			12		pF

R_{IN}	Single-ended input resistance	V_{TXD} = VDDL, CANH or CANL to GND2	10		40	kΩ
R_{ID}	Differential input resistance	V_{TXD} = VDDL, between CANH and CANL	20		80	kΩ
$R_{I(M)}$	Input resistance matching: (1 – [$R_{IN(CANH)}$/$R_{IN(CANL)}$])	V_{CANH} = V_{CANL}	–2%		2%	
CMTI	Common-mode transient immunity	V_{TXD} = 0V or VDDL, V_{TEST} = ±1kV; see Figure 8-12	±100	±150		kV/μs
Thermal Shutdown Protection						
TSD	Thermal shutdown temperature	Temperature rises		180		°C
TSD_{HYS}	Thermal shutdown hysteresis			15		°C

7.8 Timing Characteristics

VDDP connects to VDDL, GNDP1 connects to GND1, $VISO_{OUT}$ connects to $VISO_{IN}$, GNDP2 connects to GND2, over recommended operating conditions (unless otherwise noted). All typical specifications are at VDDP = VDDL = 5V, T_A = 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Transceiver							
t_{loop1}	Total loop delay (from TXD to RXD)	From recessive to dominant, R_L = 60Ω, C_{LD} = 100pF; see Figure 8-7			165	255	ns
t_{loop2}	Total loop delay (from TXD to RXD)	From dominant to recessive, R_L = 60Ω, C_{LD} = 100pF; see Figure 8-7			185	255	ns
Driver							
t_{PLH}	TXD propagation delay (recessive to dominant)	R_L = 60Ω, C_L = 100pF; see Figure 8-8			55	100	ns
t_{PHL}	TXD propagation delay (dominant to recessive)				65	110	
t_r	Differential driver output rise time				35	70	
t_f	Differential driver output fall time				50	100	
t_{TXD_DTO}[1]	TXD dominant timeout	R_L = 60Ω, C_L = 100pF; see Figure 8-9		2.5	6.8	10	ms
Receiver							
t_{PLH}	RXD propagation delay (dominant to recessive)	C_L = 15pF; see Figure 8-10			95	165	ns
t_{PHL}	RXD Propagation delay (recessive to dominant)				105	175	
t_r	RXD output rise time				2.5	6	
t_f	RXD output fall time				2.5	6	
Timing of CAN FD							
$T_{bit(BUS)}$	Bit time on CAN bus output pins	R_L = 60Ω, C_{LD} = 100pF, C_L = 15pF; see Figure 8-11	$T_{bit(TXD)}$ = 500ns	435		530	ns
			$T_{bit(TXD)}$ = 200ns	155		210	
$T_{bit(RXD)}$	Bit time on RXD output pins		$T_{bit(TXD)}$ = 500ns	400		550	ns
			$T_{bit(TXD)}$ = 200ns	120		220	
Δt_{rec}	Receiver timing symmetry: $T_{bit(RXD)}$ – $T_{bit(BUS)}$		$T_{bit(TXD)}$ = 500ns	–65		40	ns
			$T_{bit(TXD)}$ = 200ns	–45		15	

NOTE:

1. The TXD dominant timeout (DTO) disables the driver of the transceiver once the TXD has been dominant longer than (t_{TXD_DTO}) which releases the bus lines to recessive preventing a local failure from locking the bus dominant.

7.9 Typical Characteristics

VDDP connects to VDDL, GNDP1 connects to GND1, $VISO_{OUT}$ connects to $VISO_{IN}$, GNDP2 connects to GND2, VDDP = VDDL = 5V.

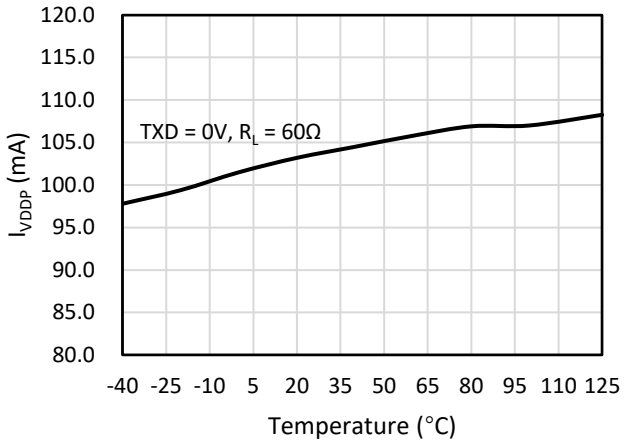


Figure 7-1 Logic-side Supply Current vs. Temperature @ Dominant

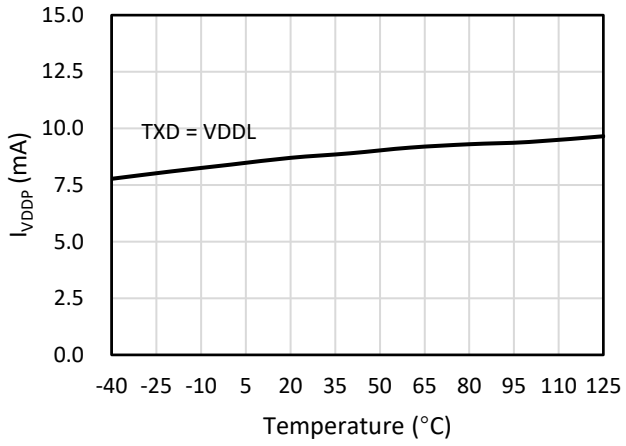


Figure 7-2 Logic-side Supply Current vs. Temperature @ Recessive

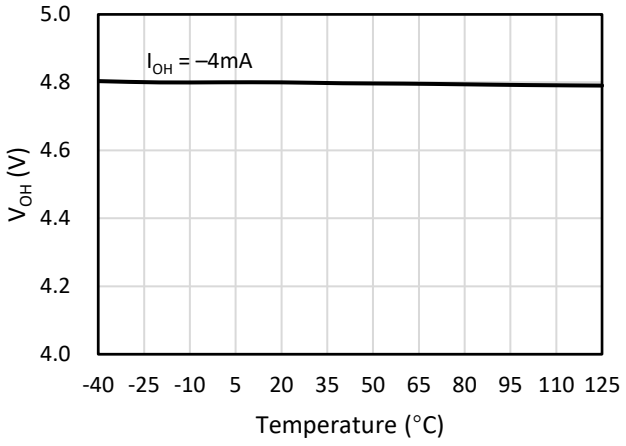


Figure 7-3 Output High Voltage of RO vs. Temperature

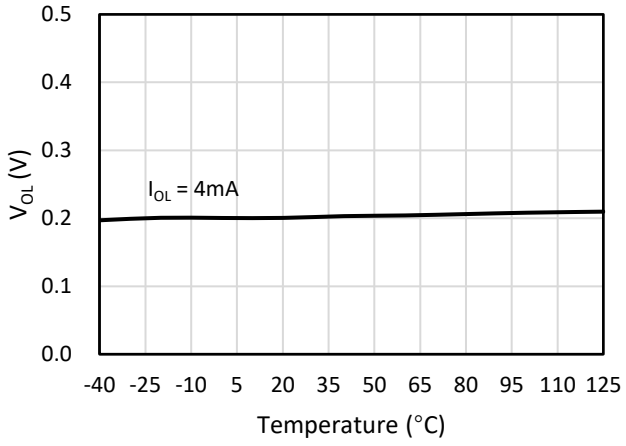


Figure 7-4 Output Low Voltage of RO vs. Temperature

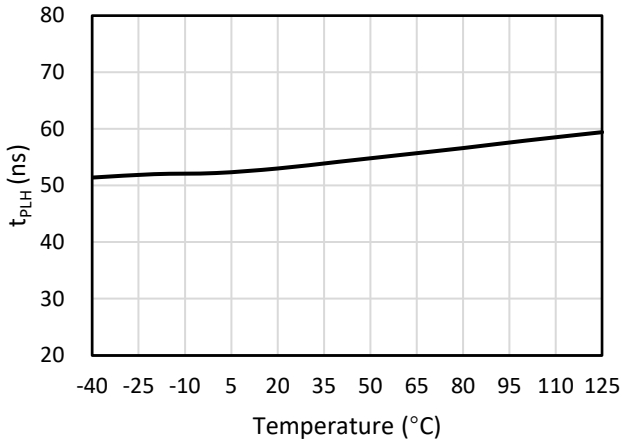


Figure 7-5 TXD Propagation Delay (R to D) vs. Temperature

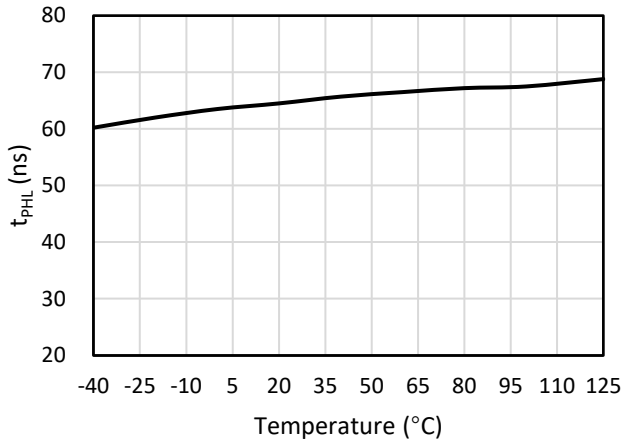


Figure 7-6 TXD Propagation Delay (D to R) vs. Temperature

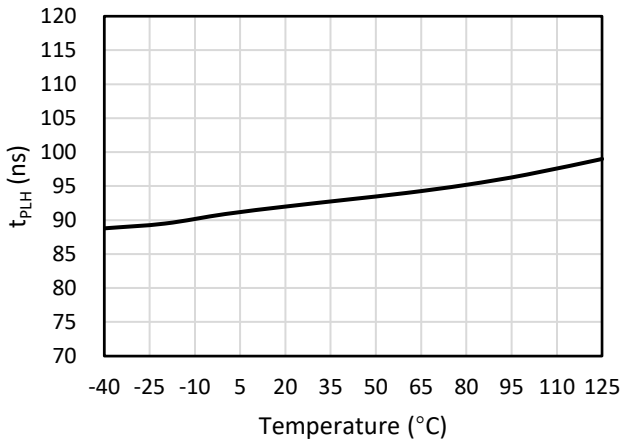


Figure 7-7 RXD Propagation Delay (D to R) vs. Temperature

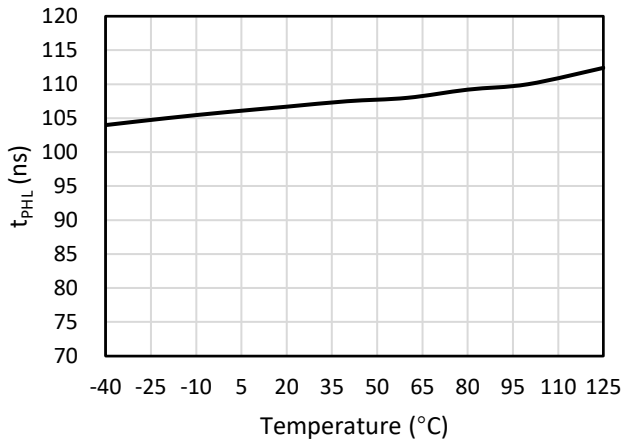


Figure 7-8 RXD Propagation Delay (R to D) vs. Temperature

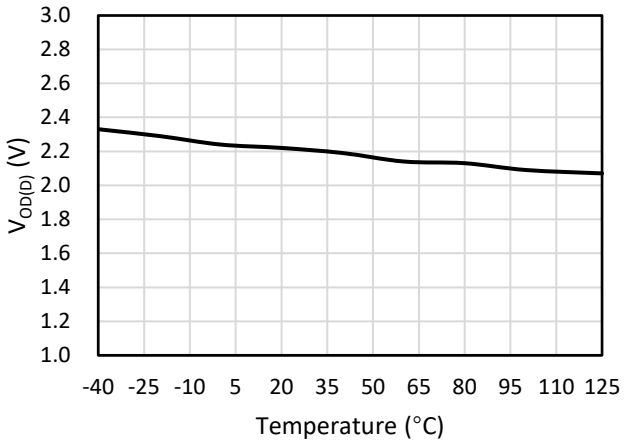


Figure 7-9 Differential Output Voltage (Dominant) vs. Temperature

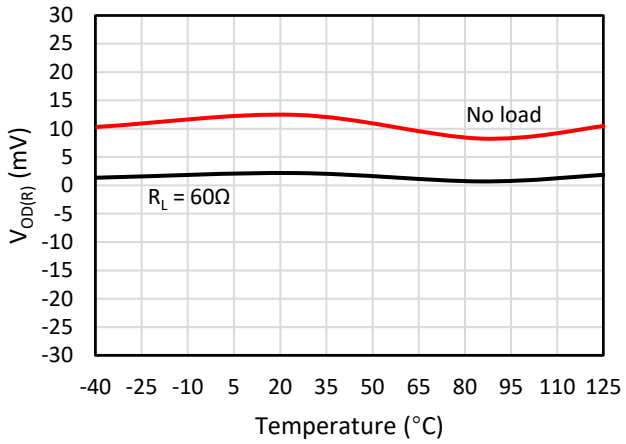


Figure 7-10 Differential Output Voltage (Recessive) vs. Temperature

8 Parameter Measurement Information

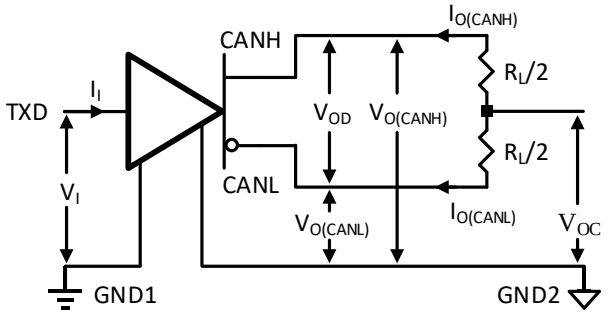


Figure 8-1 Driver Voltage, Current and Test Definitions

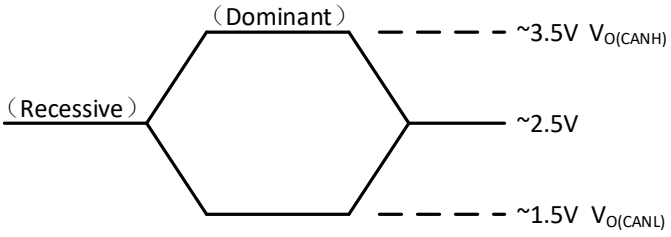


Figure 8-2 Bus Logic State Voltage Definition

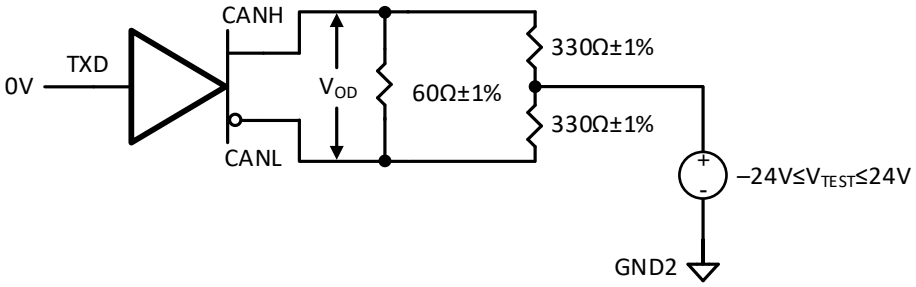


Figure 8-3 Driver's V_{OD} with Common Mode Load Test Circuit

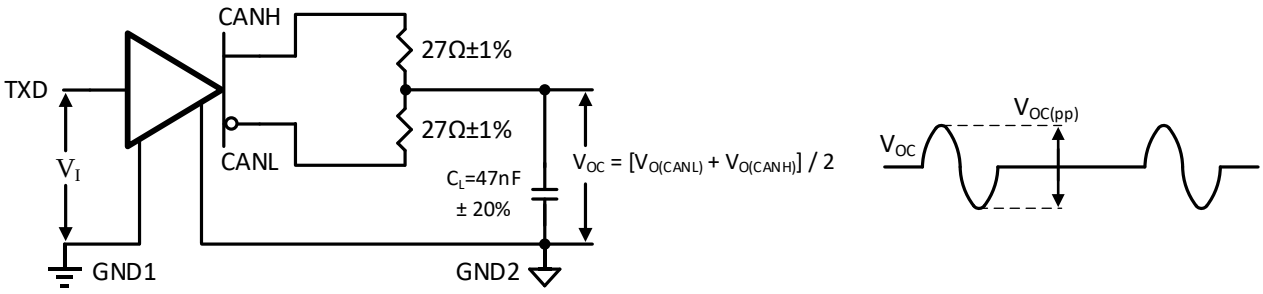


Figure 8-4 Driver's V_{OC} Test Circuit and Voltage Waveform

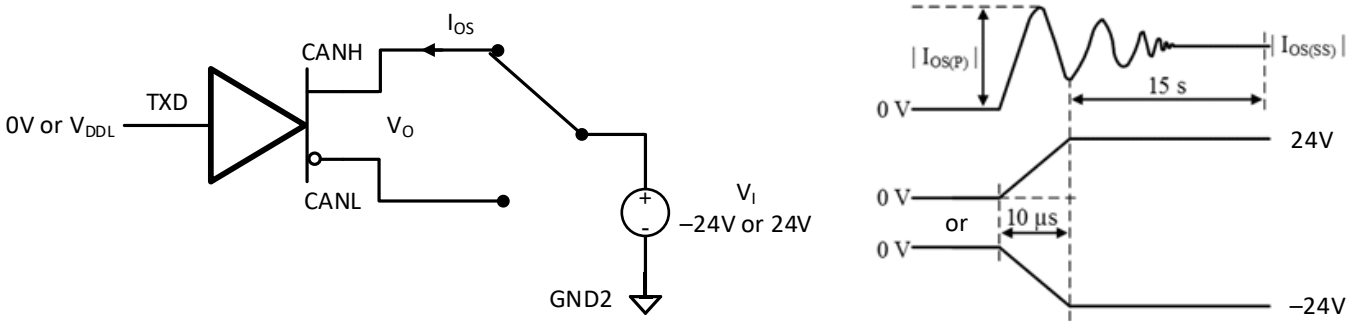


Figure 8-5 Driver Short Current Test Circuit and Waveforms

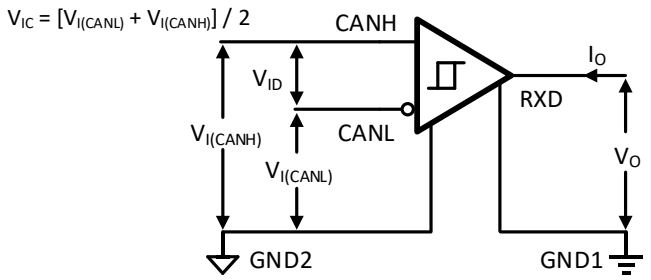


Figure 8-6 Receiver Voltage, Current and Test Definitions

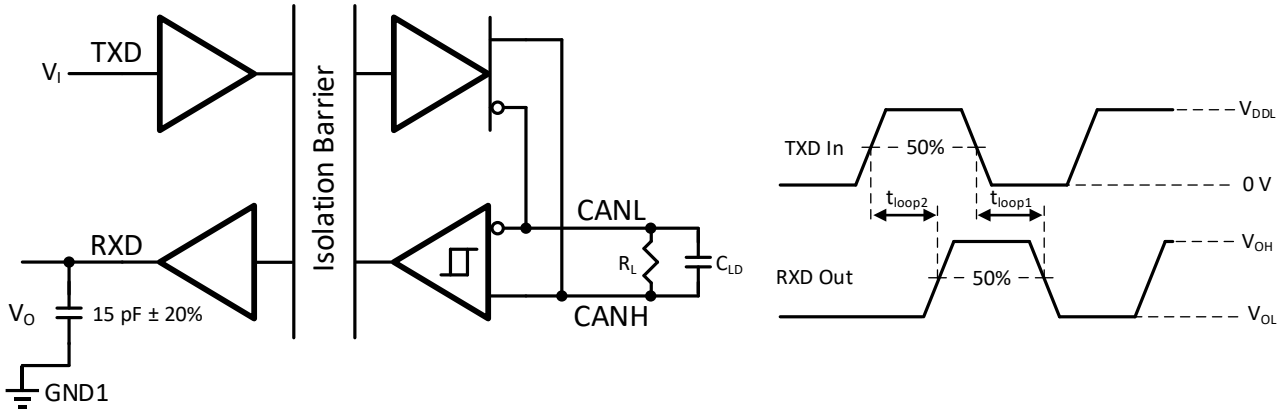
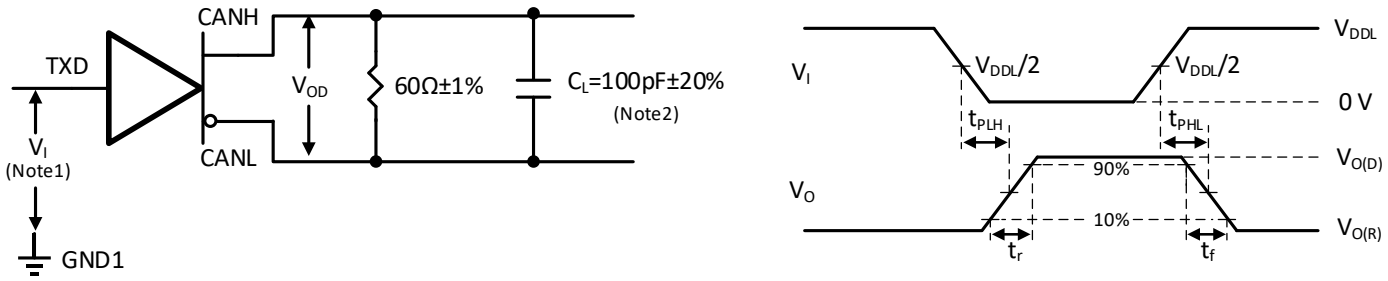


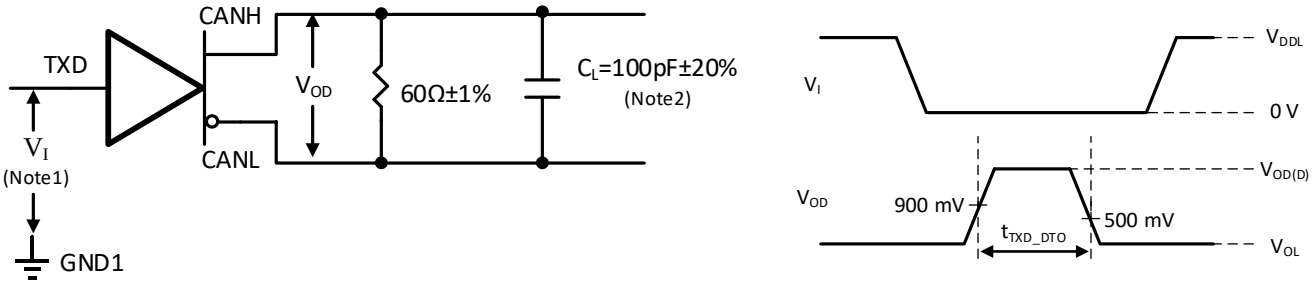
Figure 8-7 Loop Delay (from TXD to RXD) Test Circuit and Waveforms



Notes:

1. The input pulse is supplied by a generator with the characteristics: PRR ≤ 125kHz, 50% duty cycle, rise time t_r ≤ 6ns, fall time t_f ≤ 6ns, Z_O = 50Ω.
2. Load capacitance C_L includes external circuit (instrumentation and fixture etc.) capacitance.

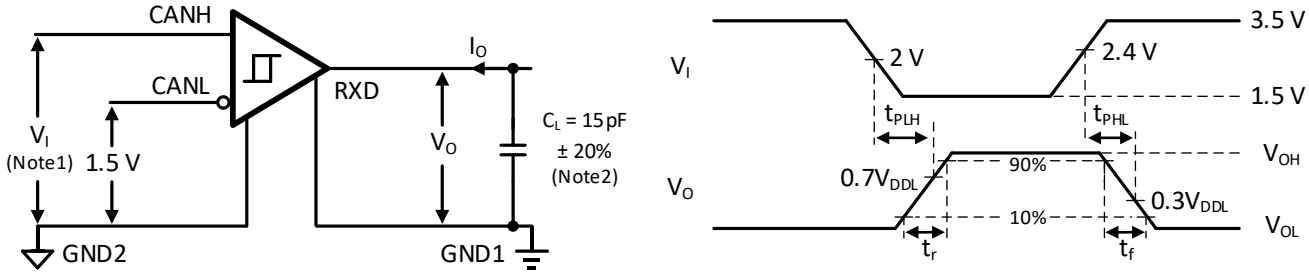
Figure 8-8 Driver Test Circuit and Waveforms



Notes:

1. The input pulse is supplied by a generator with the characteristics: PRR ≤ 125kHz, 50% duty cycle, rise time t_r ≤ 6ns, fall time t_f ≤ 6ns, Z_O = 50Ω.
2. Load capacitance C_L includes external circuit (instrumentation and fixture etc.) capacitance.

Figure 8-9 Driver Dominant Timeout (DTO) Timing Diagram



Notes:

1. The input pulse is supplied by a generator with the characteristics: PRR ≤ 125kHz, 50% duty cycle, rise time t_r ≤ 6ns, fall time t_f ≤ 6ns, Z_O = 50Ω.
2. Load capacitance C_L includes external circuit (instrumentation and fixture etc.) capacitance.

Figure 8-10 Receiver Test Circuit and Timing Diagram

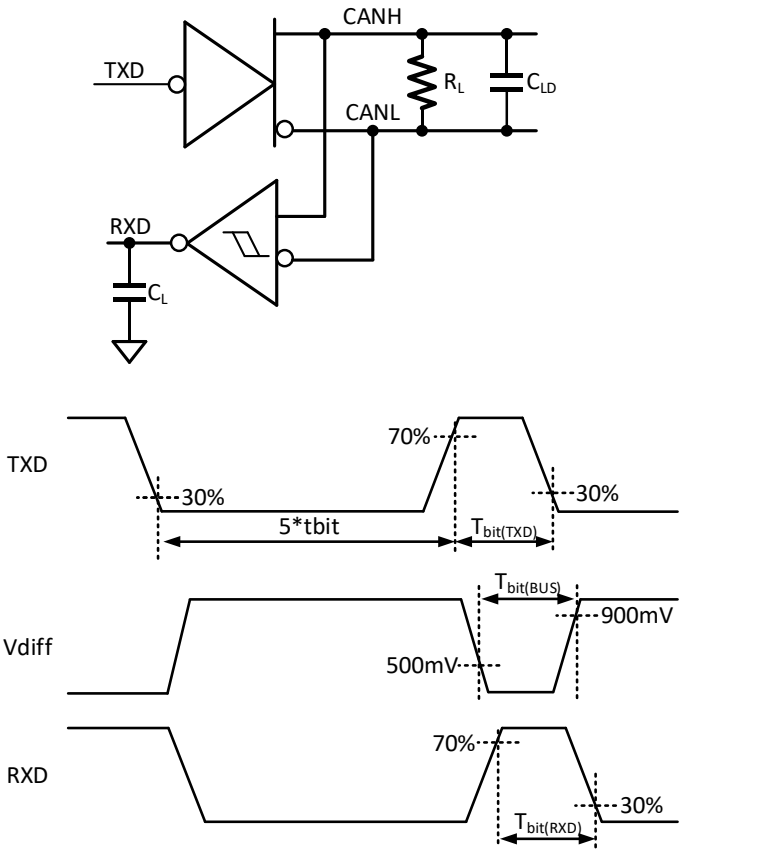


Figure 8-11 CAN FD Timing Diagram

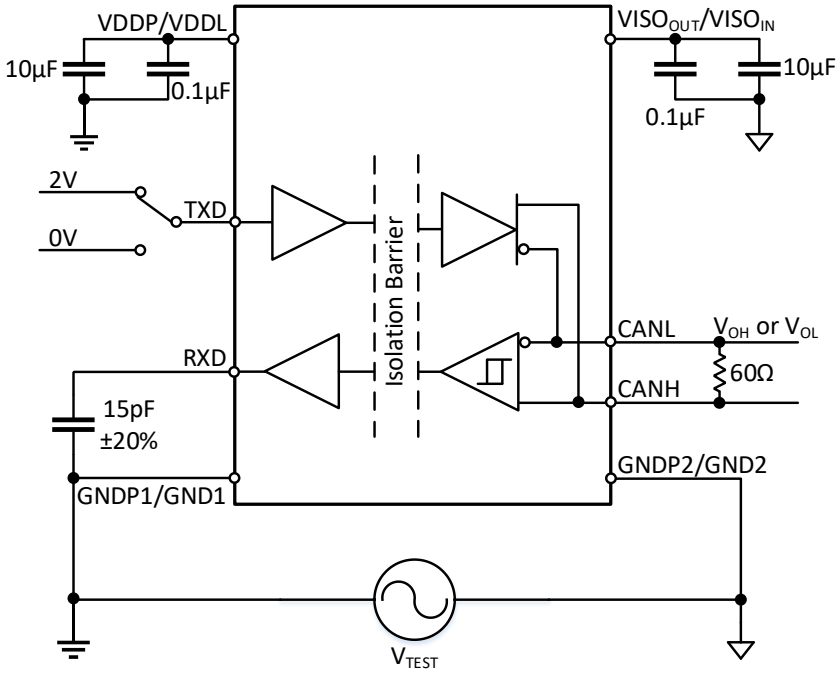


Figure 8-12 Common-Mode Transient Immunity Test Circuit

9 Detailed Description

9.1 Overview

The CA-IS2062A isolated CAN transceiver provides up to 2.5-kV_{RMS} galvanic isolation between the bus side and the logical side. This device features ±150-kV/μs common mode transient immunity (CMTI), allowing up to 5-Mbps data communication across the isolation barrier. The CA-IS2062A integrates isolated DC-DC converter to generate 5V supply voltage for the bus side, which eliminates the need of an external isolated power supply and could realize the complete isolated CAN interface with only several external bypass capacitors. Robust isolation characteristics and increased data rate enable efficient communication in noisy and harsh environments, making it ideal for communication with micro controllers in a wide range of applications such as industrial control, building automation, solar system and energy storage. The receiver of CA-IS2062A offers up to ±24V input common-mode range (CMR), which far exceeds the ISO 11898-2 specification of –2V to +7V. The fault tolerant voltage is up to ±42V for CANH and CANL, which provides efficient protection for system. Furthermore, the outputs of CANH and CANL are short-circuit current-limited, protected against excessive power dissipation by thermal shutdown circuitry which disables the $VISO_{OUT}$ and sets the driver outputs in a high-impedance state. The driver dominant timeout (DTO) detection prevents bus lockup caused by controller error or by a fault on the TXD input and releases the bus lines in time.

The CA-IS2062A devices are packaged in ultra-compact LGA16 packages, which could save PCB space significantly. This device is specified over the extended industrial temperature range of –40°C to 125°C.

9.2 CAN Bus States

The CAN bus has two states: dominant and recessive. In the dominant state (a zero bit, used to determine message priority), CANH – CANL is defined to be logic '0' when the voltage across them is between +1.5V and +3V (higher than 1V). In the recessive state (a 1-bit and the state of the idle bus), the driver is defined to be logic '1' when the differential voltage is between –80mV and +80mV, or when it is near zero (lower than 0.4V, depends on bus loading) and the bus is biased to a common mode of $VISO_{IN}$/2 by internal circuit. The CAN bus states are shown in Figure 8-2.

9.3 Device Protection Functions

9.3.1 Signal Isolation and Power Isolation

The CA-IS2062A devices integrate digital galvanic isolators using capacitive isolation technology based on the ON-OFF keying (OOK) modulation scheme and provide up to 2.5-kV_{RMS} galvanic isolation, allowing data transmission between the logic side and bus side of the transceiver with different power domains. Meanwhile, the power isolation is achieved with an integrated DC-DC convertor to generate a regulated 5V supply for the bus side, which simplifies the design of isolated interface.

9.3.2 Thermal Shutdown Protection

If the junction temperature of the CA-IS2062A device exceeds the thermal shutdown threshold TSD (180°C, typical value), output voltage $VISO_{OUT}$ as well as the output of CAN driver would be shut down. The shutdown condition is cleared when the junction temperature drops to normal operation temperature range (below 165°C, typical value). And then the $VISO_{OUT}$ as well as the output of CAN driver return to normal operation.

9.3.3 Current Limiting Protection

The CA-IS2062A device protects the driver's output stage against a short-circuit condition to a positive or negative voltage by limiting the driver output current. However, this would result in large supply current and power dissipation. Thermal shutdown further protects the device from excessive increase of temperature. The driver returns to normal operation once the short-circuit condition is removed.

9.3.4 TXD Dominant Timeout (DTO)

The CA-IS2062A devices feature a TXD dominant timeout (t_{TXD_DTO}) that prevents erroneous CAN controllers from clamping the bus to a dominant level by maintaining a continuous low-level TXD signal. When TXD remains in the dominant state (low level) for greater than t_{TXD_DTO}, the driver is disabled, releasing the bus line to a recessive state. After a dominant timeout fault, the driver is reenabled when receiving a rising edge on TXD pin.

The CAN protocol allows a maximum of eleven successive dominant bits in the worst case. Thus, the minimum transmitted data rate can be calculated as: 11bits / t_{TXD_DTO} = 11bits / 2.5ms = 4.4kbps. The TXD dominant timeout limits the minimum allowable data rate to 4.4kbps.

9.4 Device Functional Modes

9.4.1 Driver

The driver converts a single-ended input signal (TXD) from the local CAN controller to differential outputs for the bus lines CANH and CANL. The truth table for the driver is shown in Table 9-1. The outputs of CANH and CANL are short-circuit current limiting and are protected against excessive power dissipation by thermal shutdown circuitry, which disables the $VISO_{OUT}$ and sets the driver outputs in a high-impedance state.

Table 9-1 Truth Table of Driver[1]

VDDP and VDDL	INPUT	TXD LOW-LEVEL KEEP TIME	OUTPUT		BUS STATE
	TXD[2]		CANH	CANL	
Power Up	L	< t_{TXD_DTO}	H	L	Dominant
	L	> t_{TXD_DTO}	$VISO_{IN}$/2	$VISO_{IN}$/2	Recessive
	H or Open	X	$VISO_{IN}$/2	$VISO_{IN}$/2	Recessive
Power Down	X	X	Hi-Z	Hi-Z	Hi-Z

NOTE:
1. X = irrelevant, H = high level, L = low level, High-Z = high impedance.
2. TXD is weakly pulled up to VDDL internally.

9.4.2 Receiver

The receiver demodulates the differential input from the bus line (CANH and CANL) and transfers it as a single-ended output on RXD pin. The internal comparator senses the differential voltage $V_{ID} = (V_{CANH} - V_{CANL})$ from bus. If $V_{ID} \geq V_{IT+}$, a logical low is present on RXD pin; If $V_{ID} \leq V_{IT-}$, a logical high is present on RXD pin. RXD is a logical high when CANH and CANL are open, short or on idle state. The truth table for the receiver is shown in Table 9-2.

Table 9-2 Truth Table of Receiver

$V_{ID} = V_{CANH} - V_{CANL}$		BUS STATE	RXD
V_{CM} = –20V to 20V	V_{CM} = –24V to 24V		
$V_{ID} \geq 0.9V$	$V_{ID} \geq 1.0V$	Dominant	Low
0.5V < V_{ID} <0.9V	0.4V < V_{ID} <1.0V	Indeterminate	Indeterminate
$V_{ID} \leq 0.5V$	$V_{ID} \leq 0.4V$	Recessive	High
$V_{ID} \approx 0V$		Open, short or bus idle	High

10 Application and Implementation

10.1 Application Overview

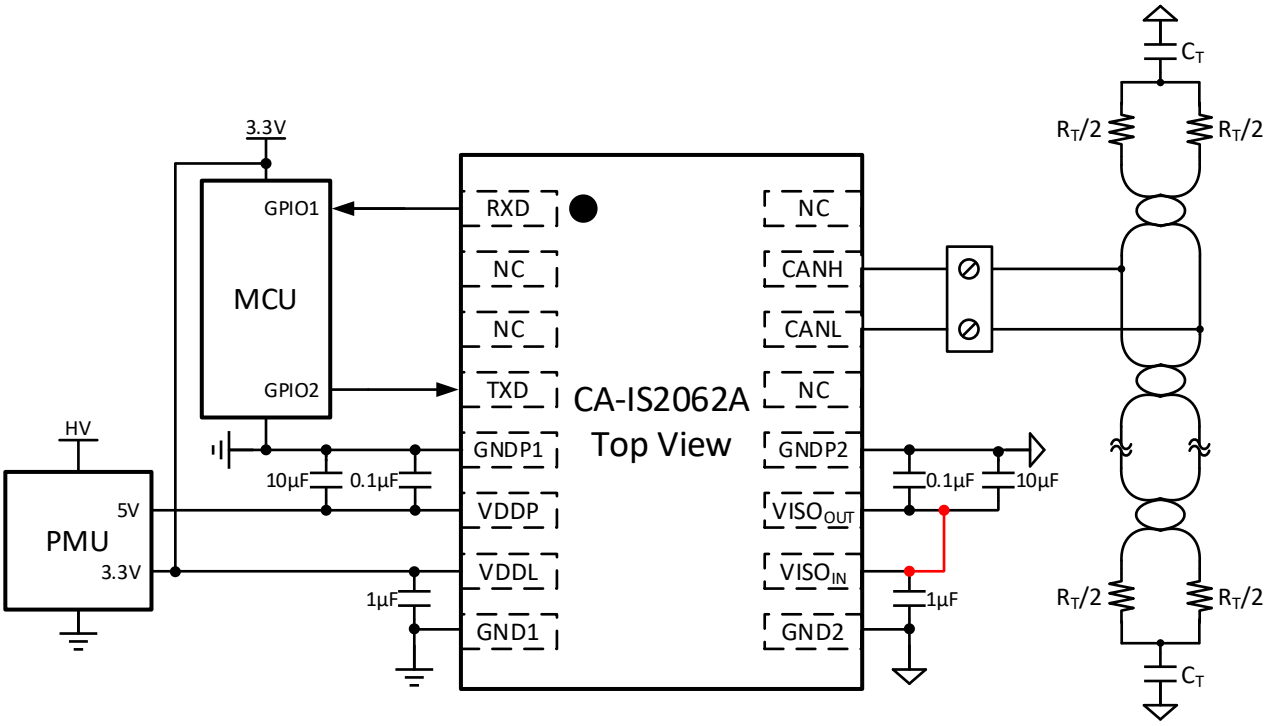


Figure 10-1 Typical Application Circuit

CAN interfaces have been widely used in the industrial and automotive applications due to their excellent prioritization and arbitration capabilities. In systems with different voltage domains, isolation is generally required to protect the low-voltage side from the high-voltage side in case of any faults. The CA-IS2062A could provide complete isolated CAN interface solution with only several external bypass capacitors for these kinds of applications, which contains both signal isolation and power isolation. The CA-IS2062A devices are packaged in ultra-compact LGA16 packages, which could save PCB space significantly. The typical application circuit is shown in Figure 10-1.

On logic side, VDDL and VDDP could be separated and powered by different voltages. VDDP is a single 5V supply for the integrated DC-DC converter to generate 5V output voltage $VISO_{OUT}$ for the bus side. VDDL could share the same power supply with the low-voltage CAN controller such as powered by 3.3V (minimum to 2.5V). Such configuration could eliminate the level shifters between low-voltage CAN controller and CAN transceiver for signal interaction and thus save BOM.

The CA-IS2062A devices support up to 5-Mbps data rate. However, the maximum data rate is limited by the bus loading, number of nodes, cable length, matching etc. factors. For CAN network design, margin must be given for signal loss across the system and cabling, parasitic loadings, timing, network imbalances, ground offsets and signal integrity thus a practical maximum data rate, number of nodes often lower. In practical applications, it could lower down the data rate of CAN FD according to actual situations.

Considering of the high input impedance of CA-IS2062A, up to 110 nodes are allowable on the same CAN bus with careful design and network layout.

10.2 Multi-Node Networking

In multi-node CAN network, it is important to maintain a single linear bus of uniform impedance that is properly terminated at each end. A star, ring, or tree configuration should never be used. Any deviation from the end-to-end wiring scheme creates a stub. High-speed data edges on a stub can create reflections back down to the bus. These reflections can cause data errors by

eroding the noise margin of the system. Although stubs are unavoidable in a multi-node system, care should be taken to keep these stubs (L_{stub} shown in Figure 10-2) as short as possible, especially when operating with high data rates. The typical CAN bus topology is shown in Figure 10-2. Both ends of the cable should terminate a termination resistor R_T which is matched to the characteristic impedance Z_O of the cable. The typical value of R_T is 120Ω. It is recommended to utilize the spilt termination with a 4.7-nF common-mode capacitor C_T to filter the common-mode voltage noise and improve the electromagnetic emissions behavior when data is transmitting.

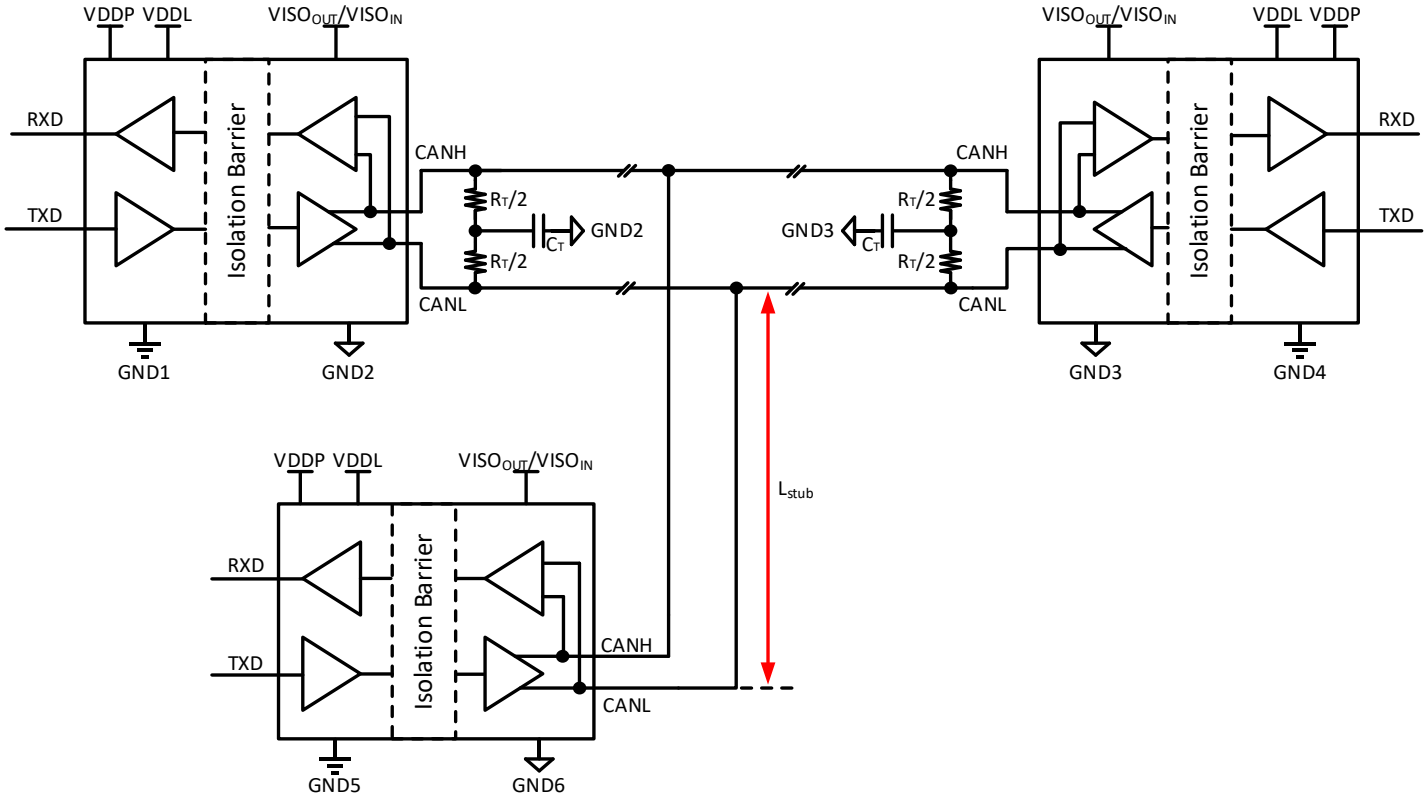


Figure 10-2 Typical CAN Bus Topology

10.3 PCB Layout Guidelines

To ensure reliable operation at all data rates, it is strongly recommended to bypass VDDP and $VISO_{OUT}$ with 0.1µF and at least 10µF low-ESR ceramic capacitors to GNDP1 and GNDP2 respectively. Place these bypass capacitors as close to the power supply input/output pins as possible, and keep the distance within 2mm.

For the logical supply input, we recommend to use a 1-µF ceramic capacitors with X5R or X7R type between VDDL and GND1. $VISO_{IN}$ is the power supply pin for CAN transceiver inside, we also recommend to use a 1-µF ceramic capacitors with X5R or X7R type between $VISO_{IN}$ and GND2. For harsh industrial environments, external protection might be necessary to protect the CAN transceiver during normal operation.

To meet with the system requirements in isolation rating, it is recommended to leave enough clearance and creepage between the logic side and bus side. Also, any top layer PCB routing underneath the body of the package should be avoided.

These mentioned bypass capacitors above should be placed on the same PCB layer with CA-IS2062A. It is forbidden to place capacitors and IC on different PCB layers and connect them by vias. The recommended PCB layout for power supply is shown in Figure 10-3.

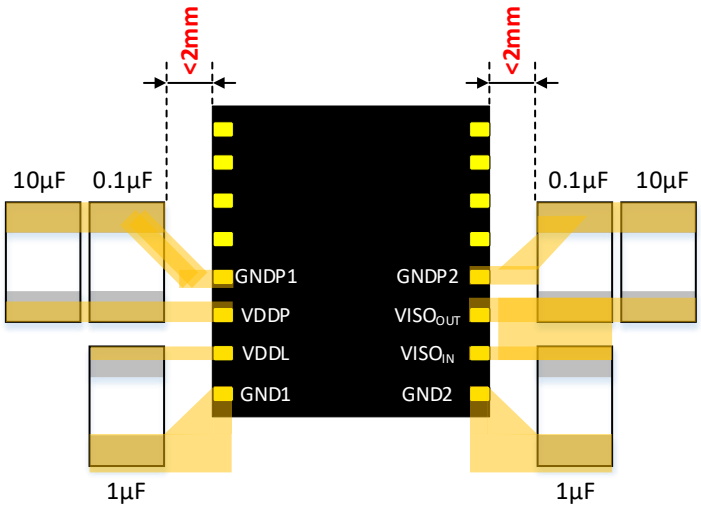


Figure 10-3 Recommended PCB Layout for Power Supply

10.4 Cautions

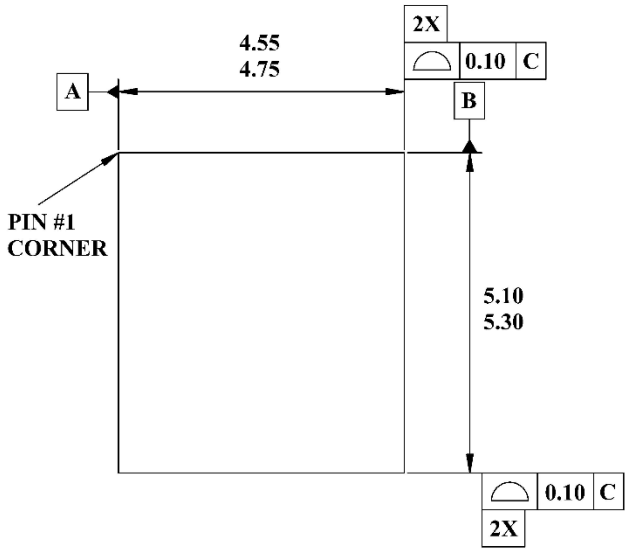
Please notice the following cautions in applications:

- VDDP and VDDL must exceed $VDDP_{ULVO+}$ and $VDDL_{ULVO+}$ respectively for the setup of $VISO_{OUT}$ to a normal output voltage.
- $VISO_{IN}$ and $VISO_{OUT}$ must be connected together for the setup of $VISO_{OUT}$ to a normal output voltage. It is forbidden to leave $VISO_{OUT}$ floating.

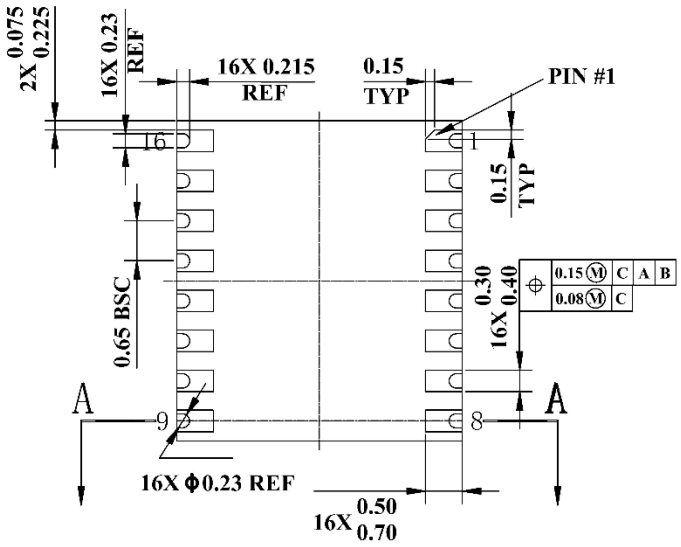
11 Package Information

11.1 LGA16 Package

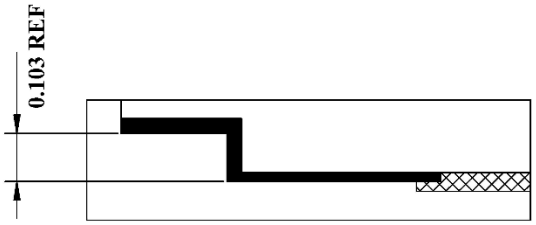
The values for the dimensions are shown in millimeters.



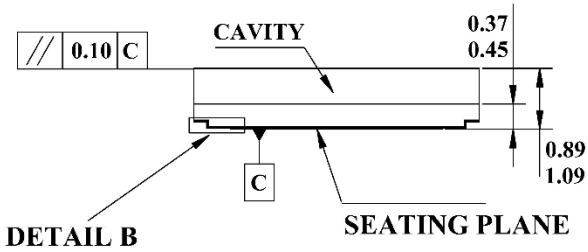
TOP VIEW



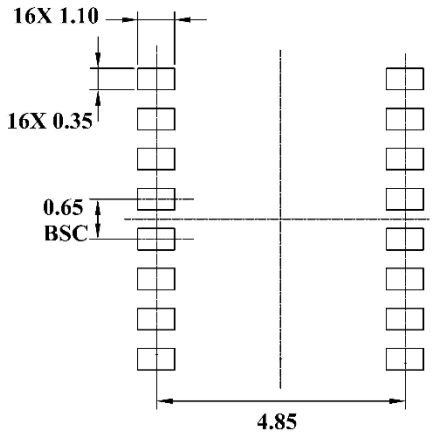
BOTTOM VIEW



DETAIL B
80:1



SECTION A-A



RECOMMEND LAND PATTERN

12 Soldering Information

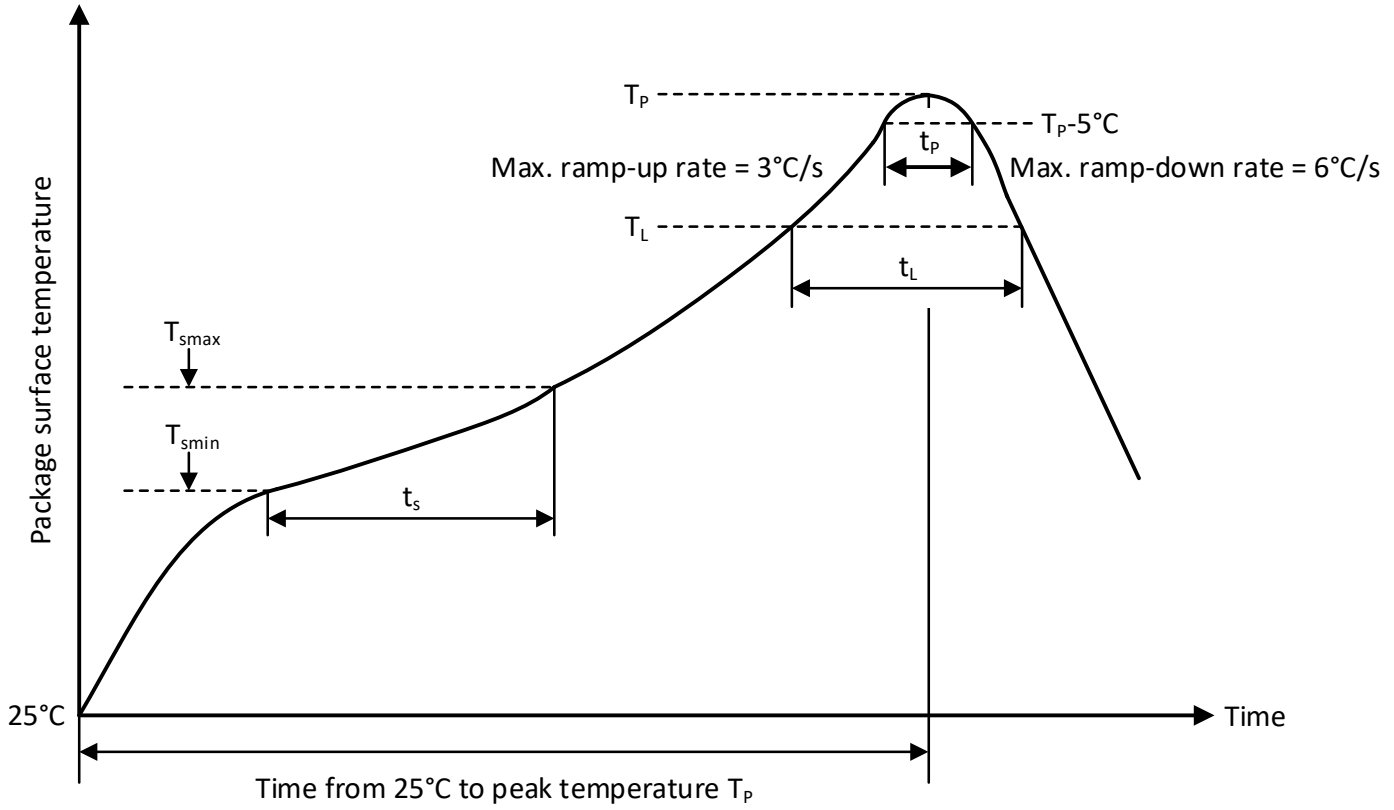


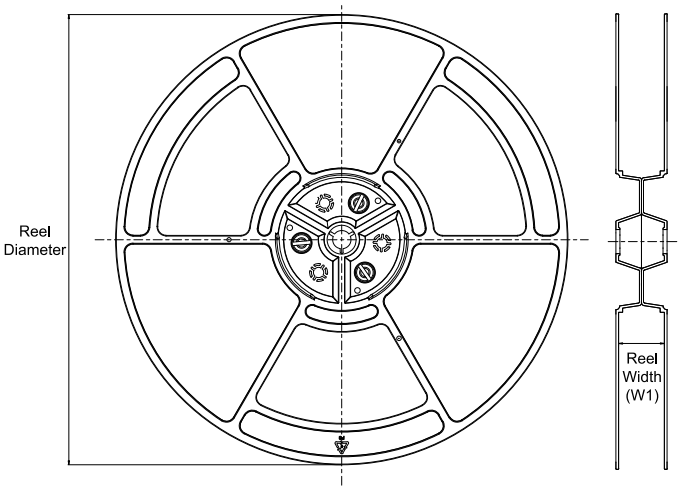
Figure 12-1 Soldering Temperature Curve

Table 12-1 Soldering Temperature Parameters

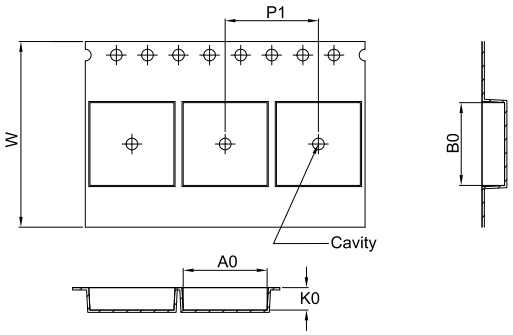
Profile Feature	Pb-Free Soldering
Ramp-up rate (T_L = 217°C to peak T_P)	3°C/s max
Time t_s of preheat temp (T_{smin} = 150°C to T_{smax} = 200°C)	60~120 seconds
Time t_L to be maintained above 217°C	60~150 seconds
Peak temperature T_P	260°C
Time t_P within 5°C of actual peak temp	30 seconds max
Ramp-down rate (peak T_P to T_L = 217°C)	6°C/s max
Time from 25°C to peak temperature T_P	8 minutes max

13 Tape and Reel Information

REEL DIMENSIONS

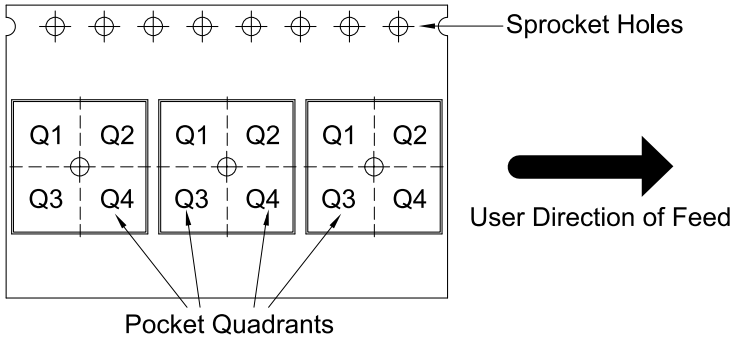


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CA-IS2062A	LGA16 4.65 x 5.2	A	16	3000	330	12.4	4.95	5.5	1.3	8.0	12.0	Q1

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