CA-IF1028A LIN transceiver with integrated voltage regulator

1. Features

- **AEC-Q100 Qualified for Automotive Application**
- **Meets LIN2.0、LIN2.1、LIN2.2、LIN2.2A and ISO 17987-4:2016(12V) Physical-layer (EPL) Standards**
- **Compliant to SAE J2602-1 and SAE J2602-2 LIN Physical-layer Specification**
- **Designed to Support 12V Applications with Wide Operating Supply Range:**
  - 5.5V to 28V supply range (V_{BAT})
- **Support up to 20kbps LIN Transmission Data Rate**
- **Operating Mode:**
  - Normal operation
  - Low-power Standby （typ.22μA）
  - Low-power Sleep（typ.14μA）
  - Power-off
- **Wake-up from Low-power Mode:**
  - Remote wake-up via LIN bus
  - wake-up via EN pins
- **Integrated 30kΩ LIN pull-up Resistor**
- **Power-up/down Glitch-free Operation on LIN bus and RXD output**
- **Integrated Protection Increases Robustness**
  - ±42V fault-tolerant LIN bus
  - 42V load dump protection
  - Enhanced ESD protection
  - Undervoltage protection on V_{BAT}
  - Transmitter dominant timeout prevents lockup
  - V_{CC} output voltage short and LIN bus short circuit protection functions.
  - Thermal shutdown
  - System level fail-safe protection for the unpowered node or ground disconnection
- **Voltage regulator offering 5 V or 3.3 V, 100 mA capability(SOIC8) and 125 mA capability(DFN8)**
- **–40°C to 150°C Junction Temperatures Range**
- **Available in SOIC8 and DFN8 Packages**

2. Applications

- Body electronics
- Automotive gateway
- Infotainment and cluster
- Hybrid electric vehicles and powertrain systems

3. General Description

The CA-IF1028A family of device is Local Interconnect Network (LIN) transceiver with integrated wake-up and protection features for automotive applications. LIN is low-speed universal asynchronous receiver transmitter (UART) communication protocol used to support in-vehicle networks. The CA-IF1028A transceiver controls the LIN bus state via the TXD input and reports the bus state on output RXD between the protocol controller and physical LIN networks. These device features slew-rate control and wave-shaping to reach a very low level of electromagnetic emission (EME) within a broad frequency range.

CA-IF1028A devices are designed to support 12V automotive applications with 5.5V to 28V wide V_{BAT} input voltage operating range and have up to ±42V fault protection on LIN bus, with integrated ESD protection, these devices help to reduce external components in the design.

Also, these devices feature low-power Sleep mode, as well as wake-up capability over LIN bus, or via the EN pin. In the event of a ground shift or supply voltage disconnection, the devices can prevent back-feed current through LIN to V_{BAT}.

CA-IF1028A integrates a low dropout regulator (LDO), providing 5V or 3.3V voltage output, with power supply currents up to 100mA (SOIC8) and 125 mA (DFN8) to power other devices.

Table 3-1. Device Information

Part number	Package	Package size(NOM)
CA-IF10285AS-Q1	SOIC8(S)	4.9mm x 3.9mm
CA-IF10285AD-Q1	DFN8(D)	3mm x 3mm
CA-IF10283AS-Q1	SOIC8(S)	4.9mm x 3.9mm
CA-IF10283AD-Q1	DFN8(D)	3mm x 3mm

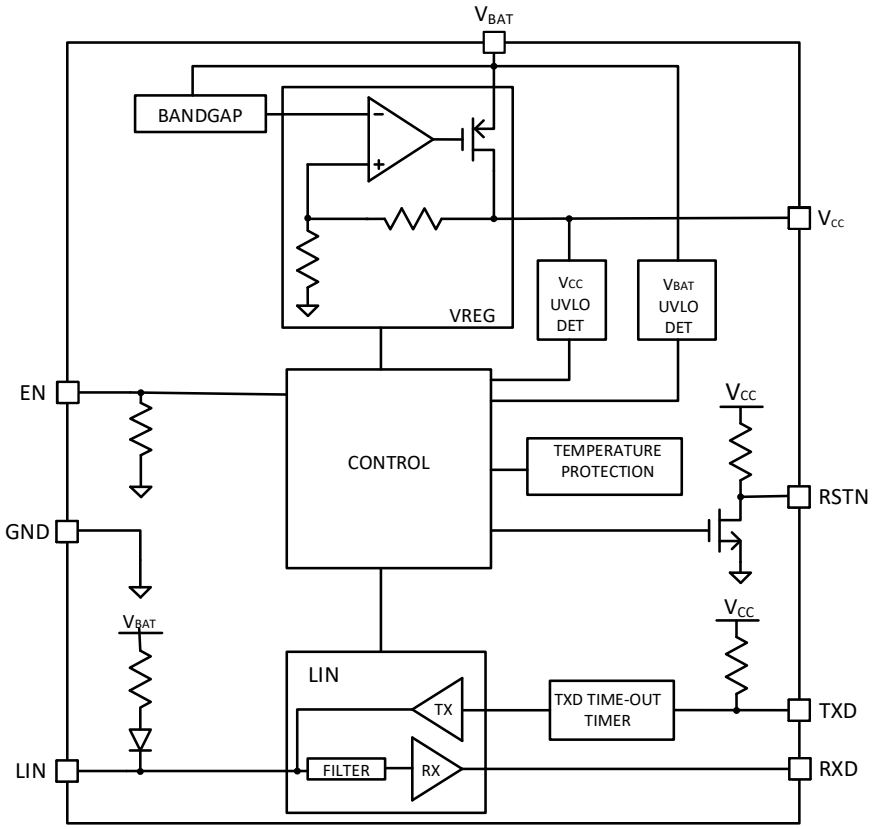


Figure3- 1. Simplified Block Diagram

4. Ordering Information

Table 4-1. Ordering Information

型号	V_{CC} 电压(LDO 输出)	Features	Package
CA-IF10285AS-Q1	5V	Automotive qualified part	SOIC8(S)
CA-IF10285AD-Q1	5V	Automotive qualified part	DFN8(D)
CA-IF10283AS-Q1	3.3V	Automotive qualified part	SOIC8(S)
CA-IF10283AD-Q1	3.3V	Automotive qualified part	DFN8(D)

Table of Contents

5. Revision History

Revision Number	Description	Page Changed
V1.0	Initial Version	NA

6. Pin Configuration and Functions

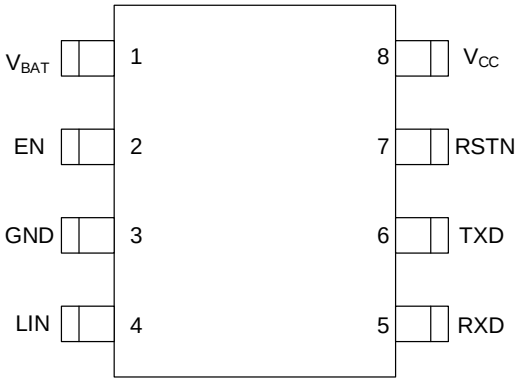


Figure6- 1. SOIC8 Pin Configuration

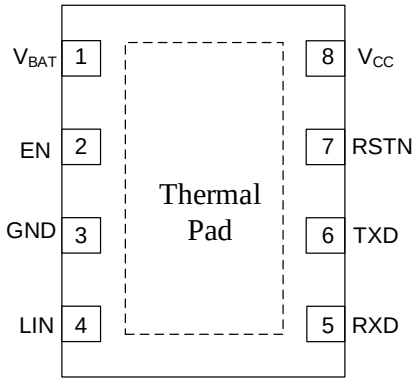


Figure6- 2. DFN8 Pin Configuration

Table 6-1. CA-IF1028A Pin Configuration and Description

Pin Name	Pin #	Type	Description
V_{BAT}	1	Power	Battery voltage input. Bypass V_{BAT} to ground with at least 0.1μF ceramic capacitor as close as possible to the device.
EN	2	Digital I/O	Enable input port.
GND	3	GND	Ground
LIN	4	Bus I/O	LIN bus input/output.
RXD	5	Digital I/O	Data receive output. The RXD reads back information from the LIN bus in normal operation mode and indicates a wake-up event in Standby mode, RXD is low if a wake event occurred.
TXD	6	Digital I/O	Transmit data input. TXD is a CMOS compatible input from microcontroller with an internal pulled up resistor to V_{CC}. Set this pin to “low” to drive a dominant stat on LIN bus.
RSTN	7	Digital I/O	Output reset port, RSTN is high when V_{CC} outputs normally; RSTN is low when V_{CC} is under voltage
V_{CC}	8	Digital I/O	Integrated LDO output

7. Specifications

7.1. Absolute Maximum Ratings1

Symbol	PARAMETER	TEST CONDITIONS	Min.	Max.	Unit
V_{BAT}	Supply voltage range	To GND, To LIN	-0.3	42	V
V_{CC}	LDO Output Valtage	To GND	-0.3	7	V
TXD	TXD voltage range	To GND	-0.3	V_{CC}+0.3	V
RXD	RXD voltage range	To GND	-0.3	V_{CC}+0.3	V
RSTN	RSTN voltage range	To GND	-0.3	V_{CC}+0.3	V
EN	EN voltage range	To GND	-0.3	V_{CC}+0.3	V
LIN	LIN voltage range	To GND, To V_{BAT}	-42	42	V
T_{vJ}	Virtual junction temperature range		-40	150	℃
T_{STG}	Storage temperature range		-55	150	℃

Note:

1. The stresses listed under “Absolute Maximum Ratings” are stress ratings only, not for functional operation condition. Exposure to absolute maximum rating conditions for extended periods may cause permanent damage to the device.

7.2. ESD Ratings

PARAMETER	TEST CONDITIONS		Value	单位
HBM ESD	LIN, V_{BAT} pins to GND		±8000	V
	V_{CC}, RXD, EN, RSTN, TXD pins to GND		±8000	
CDM ESD	Other pins to GND		±2000	V
System Level ESD	LIN and V_{BAT}	IEC 61000-4-2: contact discharge, without power-up	±6000	V

7.3. Recommended Operating Conditions

PARAMETER		Min.	Max.	Unit
V_{BAT}	Battery voltage range	5.5	28	V
V_{LIN}	LIN bus voltage range	0	28	V
V_{LOGIC}	Logic voltage range (RSTN、RXD、EN 和 TXD)	0	5.5	V
T_A	Operation Temperature Range	-40	125	℃

7.4. Recommended Operating Conditions

PARAMETER		SOIC8	DFN8	Unit
$R_{\theta JA}$	Junction-to-ambient thermal resistance	126	89	℃/W

7.5. Electrical Characteristics

Over recommended operating conditions, T_A = –40°C to 125°C (unless otherwise noted), V_{BAT}=12V.

7.5.1. DC Characteristics (Power Supply V_{BAT})

PARAMETER		TEST CONDITIONS	Min.	Typ.	Max.	Unit
I_{BAT}	V_{BAT} Current	Standby mode：V_{LIN}=V_{BAT}		22	52	μA
		Sleep mode：V_{LIN}=V_{BAT}		14	28	μA
		Normal mode(recessive): V_{LIN}=V_{BAT} V_{RXD}=V_{CC} V_{RSTN}=HIGH		135	850	μA
		Normal mode (dominant):V_{BAT}=12V V_{RXD}=0 V_{RSTN}=HIGH		1.5	4	mA

7.5.2. Power on reset(V_{BAT})

PARAMETER		TEST CONDITIONS	Min.	Typ.	Max.	Unit
$V_{th(det)pon}$	power-on detection threshold voltage			4.05	5.25	V
$V_{th(det)poff}$	power-off detection threshold voltage		3	3.7	4.2	V
$V_{hys(det)pon}$	power-on detection hysteresis voltage		50	350		mV

7.5.3. DC characteristic (V_{CC})

PARAMETER		TEST CONDITIONS		Min.	Typ.	Max.	Unit
V_{CC}	LDO outeput supply voltage	V_{CC}=5V, V_{BAT}=12V; I_{VCC}=-100mA to 0mA(SOIC8)， I_{VCC}=-125mA to 0mA(DNF-8), V_{CC} power supply current capability, See Figure8- 3 and Figure8- 4		4.9	5	5.1	V
		V_{CC}=3.3V, V_{BAT}=12V; I_{VCC}=-100mA to 0mA(SOIC8) I_{VCC}=-125mA to 0mA(DNF-8), See Figure8- 3 and Figure8- 4		3.234	3.3	3.366	V
I_{olim}	Output current limit	V_{CC}=0V to 5.5V		-500	-360	-150	mA
V_{uvd}	Under voltage detection voltage	$V_{CC(nom)}$=5V, Ramp Down		4.3	4.5	4.75	V
		$V_{CC(nom)}$=3.3V, Ramp Down		2.7	2.95	3.135	V
V_{uvr}	Under voltage recovery voltage	$V_{CC(nom)}$=5V, Ramp Up		4.4	4.6	4.9	V
		$V_{CC(nom)}$=3.3V, Ramp Up		2.8	3.1	3.234	V
$R_{(VBAT-VCC)}$[1]	resistance between pin VBAT and pin V_{CC}	$V_{CC(nom)}$=5V;V_{BAT}=4.5V to 5.5V;I_{VCC}=-70mA to -5mA;LDO regulator in saturation;	T_{vj}=85℃		5	7	Ω
			T_{vj}=150℃		5.7	9	Ω
C_o[1]	Output capacitance	equivalent series resistance <5Ω		1	10		uF

Note：
1. The test data is based on bench test and design simulation.

7.5.4. TXD Pin

PARAMETER		TEST CONDITIONS	Min.	Typ.	Max.	Unit
$V_{th(sw)}$	Switching threshold voltage	V_{CC}=2.97V to 5.5V	0.3xV_{CC}		0.7xV_{CC}	V
$V_{hys(i)}$	Hysteresis voltage	V_{CC}=2.97V to 5.5V	200			mV
R_{pu}	TXD pull-up resistor		5	12	25	kΩ

7.5.5. RXD Pin

PARAMETER		TEST CONDITIONS	Min.	Typ.	Max.	Unit
I_{OL}	Low-level output current	Normal mode： V_{RXD}= V_{CC} -0.4V;V_{LIN}= V_{BAT}			-0.4	mA
I_{LH}	High-level leakage current	Normal mode： V_{RXD}=0.4V;V_{LIN}=0V	0.4			mA

7.5.6. EN Pin

PARAMETER		TEST CONDITIONS	Min.	Typ.	Max.	Unit
$V_{th(sw)}$	Switching threshold voltage		0.8		2	V
R_{pd}	Pull-down resistance		50	130	400	kΩ

7.5.7. RSTN Pin

PARAMETER		TEST CONDITIONS	Min.	Typ.	Max.	Unit
R_{pu}	Pull-up resistance	V_{RSTN}=V_{CC}-0.4V; V_{CC}=2.97V to 5.5V	3	6	12	kΩ
I_{OL}	LOW-level output current	V_{RSTN}=0.4V; V_{CC}=2.97V to 5.5V;-40℃<T_{vj}<195℃	3.2	11	40	mA
V_{OL}	LOW-level output voltage	V_{CC}=2.5V to 5.5V;-40℃<T_{vj}<195℃	0		0.5	V
V_{OH}	HIGH-level output voltage	-40℃<T_{vj}<195℃	0.8xV_{CC}		V_{CC}+0.3	V

7.5.8. LIN Pin

PARAMETER		TEST CONDITIONS	Min.	Typ.	Max.	Unit
I_{BUS_LIM}	Driver output current limitation @dominant	V_{TXD}=0V;V_{LIN}=V_{BAT}=18V	40		150	mA
$I_{BUS\_PAS\_rec}$	Receiver input leakage current@ recessive	V_{TXD}=V_{CC} ;V_{LIN}= 18V;V_{BAT}=5.5V			20	μA
$I_{BUS\_PAS\_dom}$	Receiver input leakage current@ dominant	Normal mode; V_{TXD}=V_{CC};V_{LIN}= 0V;V_{BAT}=12V	-600			μA
$V_{SerDiode}$[1]	Voltage drop on the serial diode	in pull-up path with R_{slave}， $I_{SerDiode}$=10μA	0.4		1	V
$I_{BUS\_NO\_GND}$	Bus current @ loss ground	V_{BAT}=18V; V_{LIN}= 0V	-750		10	μA
$I_{BUS\_NO\_BAT}$	Bus current @ loss battery	V_{BAT}=0V; V_{LIN}= 18V			8	μA
V_{BUSdom}	LIN receiver dominant state	V_{BAT}=5.5V to 18V			0.4V_{BAT}	V
V_{BUSrec}	LIN receiver recessive state	V_{BAT}=5.5V to 18V	0.6V_{BAT}			V
V_{BUS_CNT}	LIN receiver center threshold	V_{BAT}=5.5V to 18V;V_{BUS_CNT}=(V_{BUSdom}+ V_{BUSrec})/2	0.45V_{BAT}	0. 5V_{BAT}	0.55V_{BAT}	V
V_{HYS}	LIN receiver hysteresis voltage	V_{BAT}=5.5V to 18V;V_{HYS}=V_{BUSrec} -V_{BUSdom}			0.175V_{BAT}	V
R_{slave}		Resistance between LIN and V_{BAT}，VLIN=0V;V_{BAT}=12V	20	30	60	kΩ
C_{LIN}[1]	Slave resistance				30	pF
$V_{O(DOM)}$	LIN dominant output	Normal mode;V_{TXD}=0V;V_{BAT}= 7V			1.4	V
		Normal mode;V_{TXD}=0V;V_{BAT}= 18V			2.0	V

Note：
1. The test data is based on bench test and design simulation.

7.5.9. Duty cycle

PARAMETER		TEST CONDITIONS	Min.	Typ.	Max.	Unit
$\delta1^{1,2}$	Duty cycle 1	$V_{th(rec)(max)}$=0.744xV_{BAT}; $V_{th(dom)(max)}$=0.581xV_{BAT}; t_{bit}=50μs; V_{BAT}=7V~18V，see Figure8- 1	0.396			
		$V_{th(rec)(max)}$=0.76xV_{BAT}; $V_{th(dom)(max)}$=0.593xV_{BAT}; t_{bit}=50μs; V_{BAT}=5.5V~7V，see Figure8- 1	0.396			
$\delta2^{2,3}$	Duty cycle 2	$V_{th(rec)(min)}$=0.422xV_{BAT}; $V_{th(dom)(min)}$=0.284xV_{BAT}; t_{bit}=50μs; V_{BAT}=7.6V~18V，see Figure8- 1			0.581	
		$V_{th(rec)(min)}$=0.41xV_{BAT}; $V_{th(dom)(min)}$=0.275xV_{BAT}; t_{bit}=50μs; V_{BAT}=6.1V~7.6V，see Figure8- 1			0.581	
$\delta3^{1,2}$	Duty cycle 3	$V_{th(rec)(max)}$=0.778xV_{BAT}; $V_{th(dom)(max)}$=0.616xV_{BAT}; t_{bit}=96μs; V_{BAT}=7V~18V，see Figure8- 1	0.417			
		$V_{th(rec)(max)}$=0.797xV_{BAT}; $V_{th(dom)(max)}$=0.630xV_{BAT}; t_{bit}=96μs; V_{BAT}=5.5V~7V，see Figure8- 1	0.417			
$\delta4^{2,3}$	Duty cycle 14	$V_{th(rec)(min)}$=0.389xV_{BAT}; $V_{th(dom)(min)}$=0.251xV_{BAT}; t_{bit}=96μs; V_{BAT}=7.6V~18V，see Figure8- 1			0.590	
		$V_{th(rec)(min)}$=0.378xV_{BAT}; $V_{th(dom)(min)}$=0.242xV_{BAT}; t_{bit}=96μs; V_{BAT}=6.1V~7.6V，see Figure8- 1			0.590	

Note：

1. δ1, δ3=$\frac{t_{bus(rec)(\min)}}{2\times t_{bit}}$
2. LIN bus load condition：(1) C_{BUS}=1nF, R_{BUS}=1kΩ；(2) C_{BUS}=6.8nF, R_{BUS}=660Ω；(3) C_{BUS}=10nF, R_{BUS}=500Ω
3. δ2, δ4=$\frac{t_{bus(rec)(\max)}}{2\times t_{bit}}$

7.5.10. Thermal Shutdown

PARAMETER		TEST CONDITIONS	Min.	Typ.	Max.	Unit
$T_{th(act)otp}$ [1]	Thermal shutdown temperature		165	180	195	℃
$T_{th(rel)otp}$ [1]	Thermal shutdown temperature recovery		126	138	150	℃

Note：

1. The test data is based on bench test and design simulation.

7.5.11. Switching Characteristics

PARAMETER		TEST CONDITIONS	Min.	Typ.	Max.	Unit
$t_{P(RX)}$	receiver propagation delay	Riseand fall，C_{RXD}=20pF			6	μs
$t_{P(RX)sym}$	receiver propagation delay symmetry	C_{RXD}=20pF	-2		2	μs
$t_{wake(dom)LIN}$	LIN dominant wake-up time	Sleep mode	30	80	150	μs
$t_{to(dom)TXD}$	TXD-dominant timeout	V_{TXD}=0V	6	13	20	ms
t_{msel}	mode select time		3	11.5	20	μs
$t_{det(uv)(vcc)}$	undervoltage detection time on pin V_{cc}	C_{RSTN}=20pF	1	8	15	μs
t_{rst}	RSTN reset time		2		8	ms

8. Parameter Measurement Information

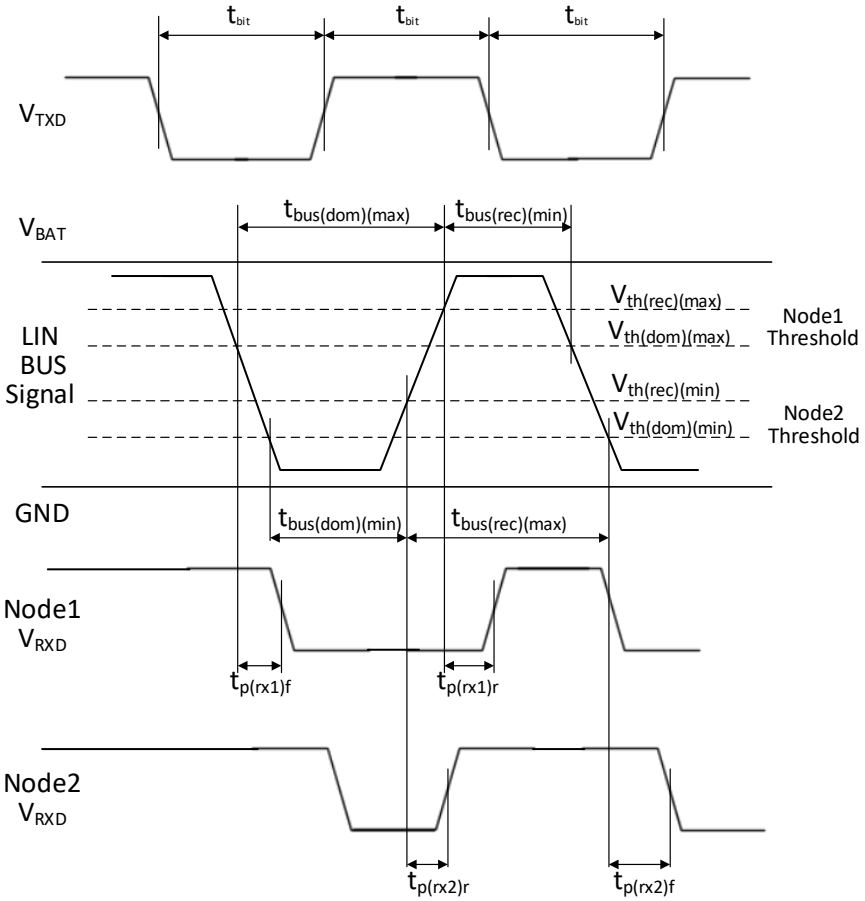


Figure8- 1. LIN Bus Transmission Timing Diagram

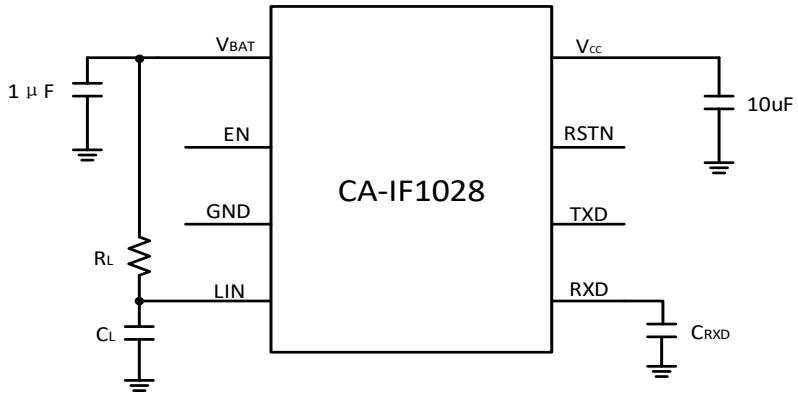


Figure8- 2. Switch characteristic testing circuit

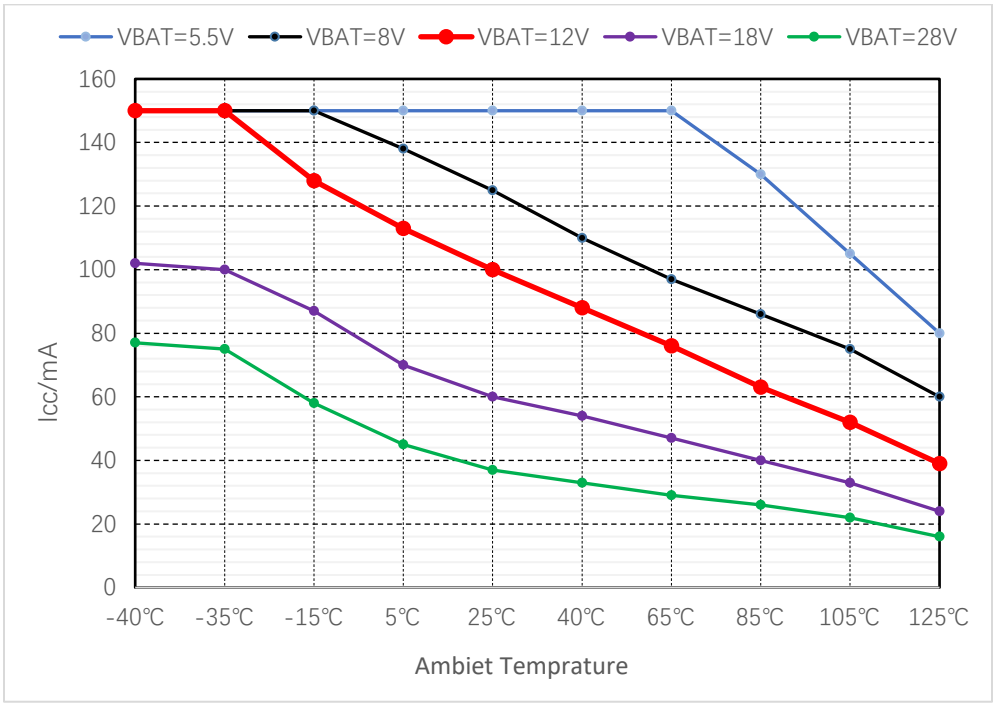


Figure8- 3. V_{CC} power supply current capability derating curve（SOIC8）

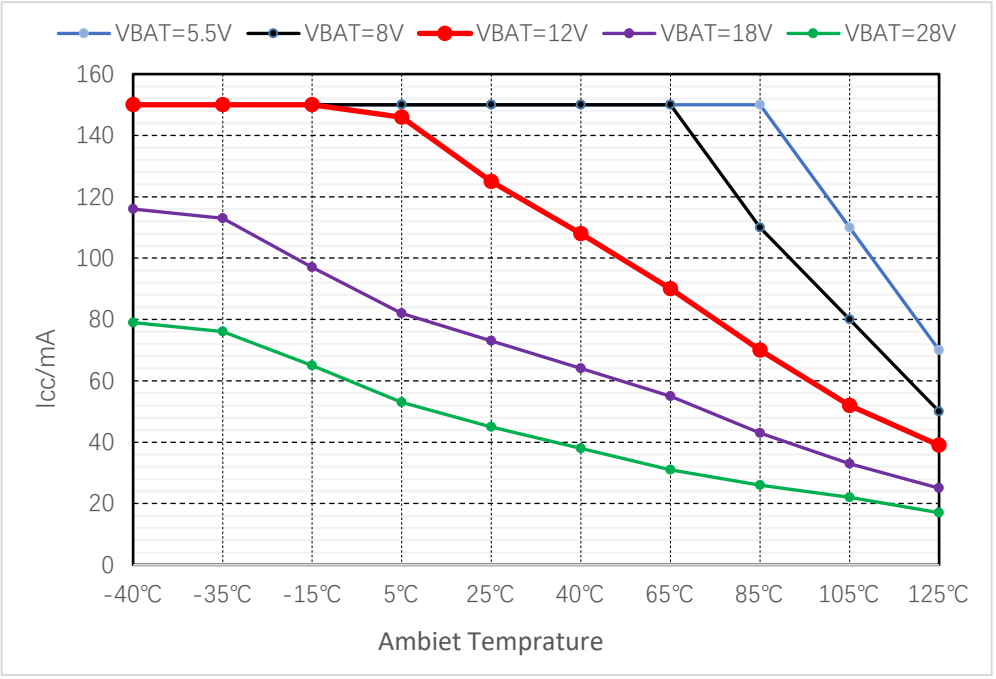


Figure8- 4. V_{CC} power supply current current capability derating curve（DFN8）

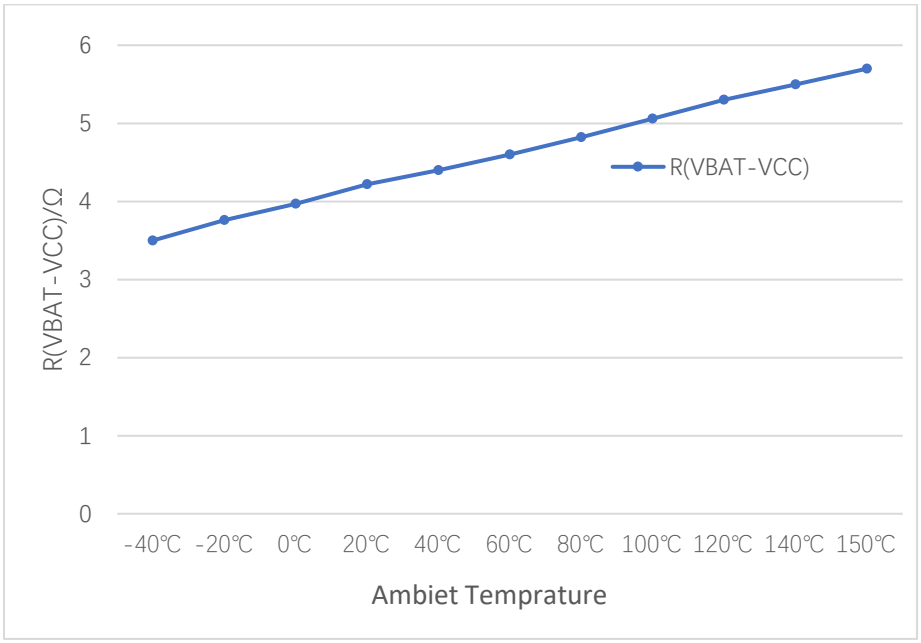


Figure8- 5. $R_{(VBAT-VCC)}$ Typical values vs. temperature changes

9. Detailed Description

9.1. Overview

The CA-IF1028A devices is fault-protected Local Interconnect Network (LIN) transceiver, meets the LIN 2.x/ISO 17987-4:2016/SAE J2602 physical layer standard. These devices are designed for harsh automotive applications with a number of integrated robust protection features that improve the reliability of end equipment. The extended fault-protected voltage range of ±42V on LIN bus line and 5.5V to 28V wide input voltage operating range allow for use in +12V automotive and truck applications. Dominant timeout prevents the bus from being blocked by a hung-up microcontroller. The LIN driver output is short-circuit current-limited and protected against excessive power dissipation by thermal shutdown circuitry that disable the transmitter to protect the device.

The LIN bus has two valid states: dominant and recessive. In the dominant state, LIN bus voltage level close to GND level; In the recessive state, LIN bus voltage level pulled up to the supply voltage V_{BAT} by bus termination. The CA-IF1028A transceiver can operate up to 20kbps data rate and the LIN driver converts the transmit data streams on the TXD input to LIN bus signals with optimized slew rates in order to minimize the level of electromagnetic emission on the LIN networks. The LIN receiver output reads back the information from the LIN bus to the microcontroller.

CA-IF1028A devices integrates LDO, which can provide power to microcontrollers or other peripheral devices through the V_{CC} pin. CA-IF10285AS/D-Q1 LDO output voltage is divided into 5V, CA-IF10283AS/D-Q1 LDO output voltage is divided into 3.3V; Its power supply current can reach up to 100mA (SOIC8) and 125 mA (DFN8). In application, the output current of LDO should be appropriately used based on VBAT voltage and environmental temperature, as shown in Figure8- 3 and Figure8- 4.

9.2. Short-circuit Protection

CA-IF1028A has V_{CC} output voltage short circuit protection and LIN bus short circuit protection functions.

When the V_{CC} output is short to GND, the internal circuit limits the maximum current to within I_{Olim} through current limiting, thereby preventing the chip from burning due to excessive power consumption;

When the LIN bus voltage is short to the V_{BAT} power supply and the chip is in dominant state, the transmitter internally limits the maximum current to IBUS through current limiting within I_{BUS_LIM} to prevent the chip burnout due to excessive power consumption.

9.3. Thermal Shutdown

In OFF mode, normal mode, and Standby mode, when the junction temperature exceeds the shutdown junction temperature $T_{th\ (act)\ otp}$, the chip will enter the OFF mode, that is, turn off the LDO function, and RSTN will become low level; When the junction temperature drops below $T_{th(rel)otp}$, the chip enters Standby mode again and LDO outputs normally.

In Sleep mode, the LDO and transmitter are already turned off, and even if the over temperature protection is triggered, the chip remains in Sleep mode.

9.4. VCC Under voltage detection voltage (Reset on pin RSTN)

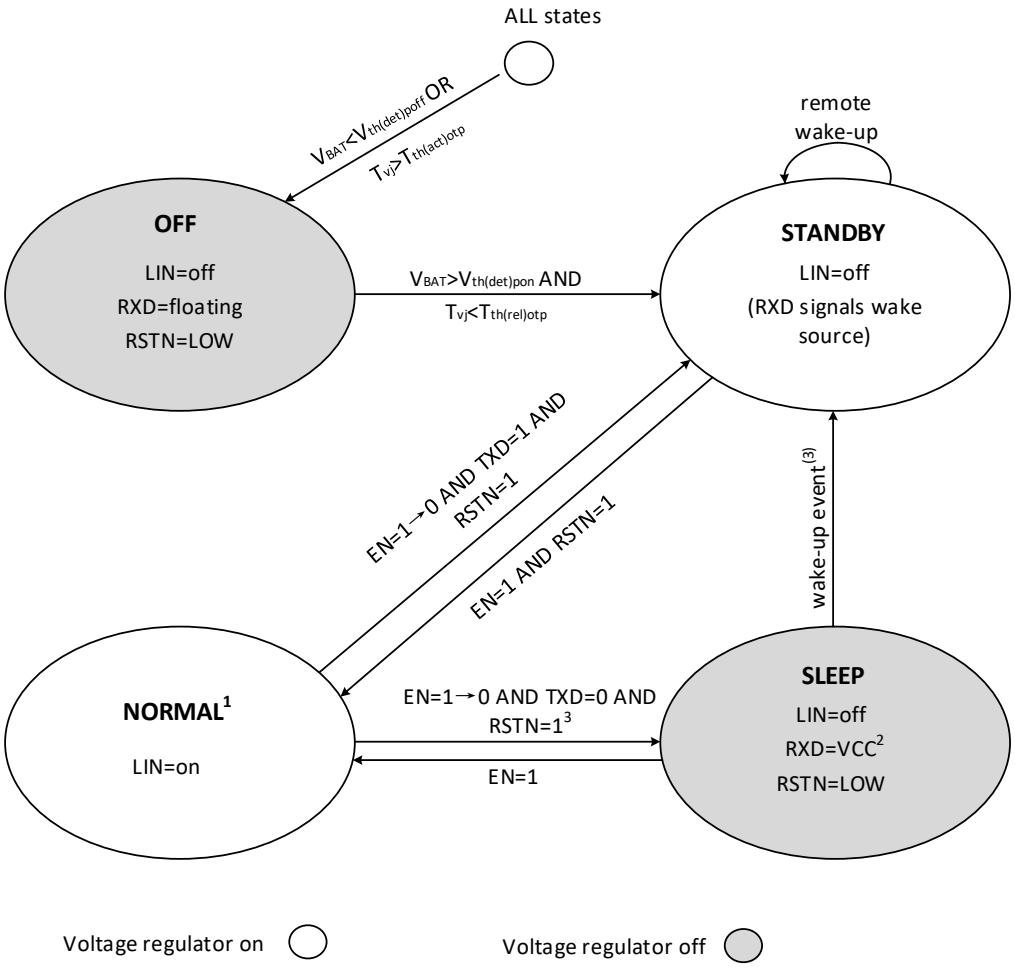
The output voltage on pin V_{CC} is monitored continuously. a system reset signal is generated When $V_{CC} < V_{uvd}$ and duration exceeds $T_{det\ (UV)\ (VCC)}$, pin RSTN output pulled low. Pin RSTN will go HIGH again once the voltage on V_{CC} exceeds the undervoltage recovery threshold (V_{uvr}) for t_{rst}.

9.5. Dominant timeout

The CA-IF1028A family of devices features a transmitter-dominant timeout($t_{to(dom)TXD}$) that prevents erroneous LIN controllers from clamping the bus to a dominant level by maintaining a permanently low TXD signal. When TXD remains in the dominant state (low) for longer than $t_{to(dom)TXD}$, the transmitter is disabled, releasing the bus to a recessive state. After a dominant timeout fault, the transmitter is re-enabled when receiving a rising edge driving TXD. The transmitter-dominant timeout limits the minimum possible data rate.

9.6. Operate modes

The CA-IF1028A supports four operating modes: Normal, Standby, Sleep and Off. See Figure9- 1 for more details about the CA-IF1028A operating modes.



Note：
1. In Normal mode, the LIN transmitter is enabled - but if EN and/or RSTN go LOW, the LIN transmitter will be disabled. Remote wake-up signaling will be activated.
2. Until V_{CC} drops below 2V.
3. If a wake-up event and a go-to-sleep event occur simultaneously, the device will switch directly to Standby mode without initiating a reset.

Figure9- 1. State Diagram

Sleep mode:

Sleep mode features extremely low power consumption. The CA-IF1028A switches to Sleep mode from Normal mode during the mode select window if TXD and EN are both Low, provided RSTN = 1.

The voltage regulator and the LIN physical layer are disabled in Sleep mode. Pin RSTN is forced LOW. Remote wake-up detection is active.

Standby mode:

When CA-IF1028A is in Sleep mode and detects a remote wake-up event, or when it is in normal mode and detects EN=H to L and TXD=H with RSTN=H (V_{CC} voltage output is normal), or when it is in OFF mode and detects that V_{BAT} is not under voltage and the chip is not over temperature, the chip enters Standby mode.

When in Standby mode, the transmitter is turned off and RXD represents a wake-up event.

Normal mode:

if the EN pin is pulled HIGH while the CA-IF1028A is in Standby mode (with RSTN = 1) or Sleep mode, the device will enter Normal mode. The LIN physical layer and the voltage regulator are enabled in Normal mode.

The high level of the bus represents recessive, while the low level represents dominant. After detecting the data flow on the LIN bus input pin, the receiver outputs it to the microcontroller through the RXD pin.

Off mode:

The CA-IF1028A switches to Off mode from all normal and Standby modes if the battery supply voltage drops below the power-off detection threshold ($V_{th(det)poff}$) or the junction temperature exceeds the overtemperature protection activation threshold ($T_{th(act)otp}$). The voltage regulator and the LIN physical layer are disabled in Off mode, and pin RSTN is forced LOW.

9.7. Remote Wake-up

The bus wake-up, also called remote wake-up, changes the transceiver's operation mode from Sleep mode to Standby mode. A falling edge on the LIN Bus, followed by a valid dominant bus signal for t > $t_{wake(dom)LIN}$, bus results in a bus wake-up event. A transition to Standby mode is performed with the subsequent rising edge on the LIN bus(the change from dominant to recessive), see Figure9- 2.

When an effective remote wake-up event occurs, the chip enters Standby mode and RXD is continuously low to send an interrupt request to the microcontroller.

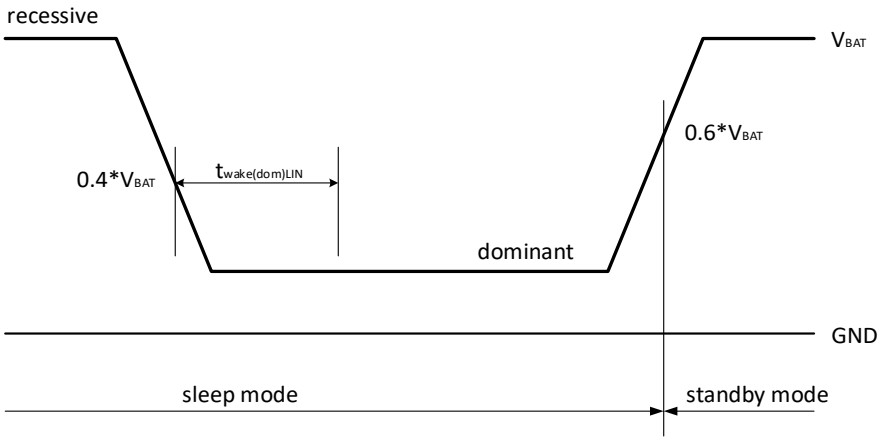


Figure9- 2. Remote Wake-up

10. Application Information

The LIN interface is a single wire bidirectional bus used for in-vehicle networks. The CA-IF1028A LIN transceiver is the interface between the microcontroller and physical LIN bus. Every LIN network consists of a master node and one or more slave nodes. To configure the CA-IF1028A transceiver for master node applications, a 1kΩ termination resistor and a diode must be connected between LIN bus and battery power supply V_{BAT} , connect 1nF bypass capacitor between LIN and GND, see Figure 10-1. As there is an internal pull-up resistor with a serial diode structure to V_{BAT} for the CA-IF1028A LIN transmitter, so no external pull-up components are required for LIN slave node applications, a 220pF bypass capacitor is needed between LIN and GND.

The CA-IF1028A devices support 3.3V and 5.0V logic input, allowing operation with a variety of microcontrollers with common I/O voltage levels. The receive data outputs RXD behavior for allowing the output level to the microcontroller supply voltage.The CA-IF1028A devices output pins RXD and RSTN integrate Pull-up resistor. When the microcontroller port pin is connected, no additional pull-up resistor is required.

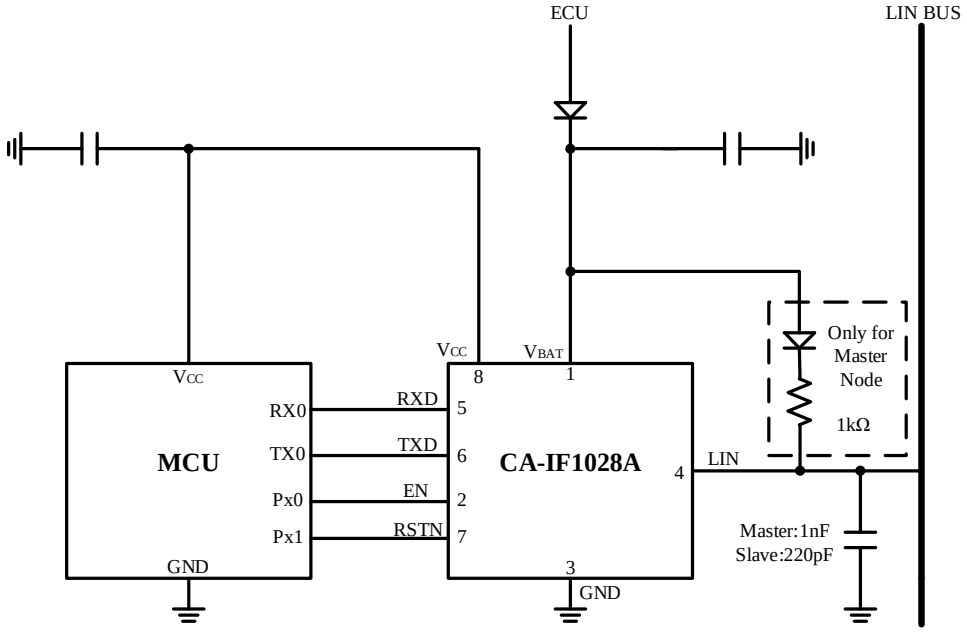


Figure 10- 1. Typical Application Circuit in LIN Bus

11. Package Information

11.1 SOIC8 Packege Outline

Dimensions in millimeters

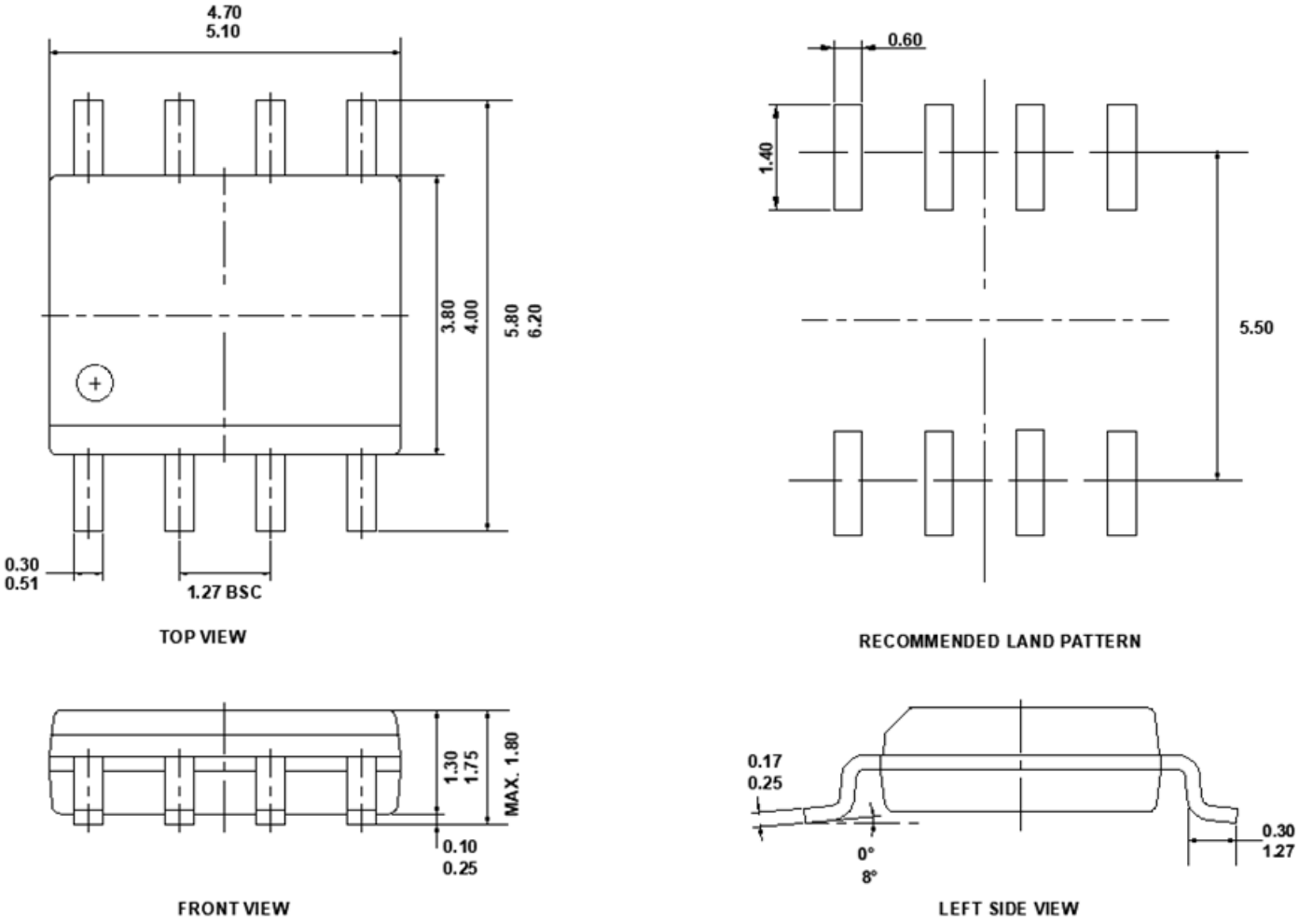
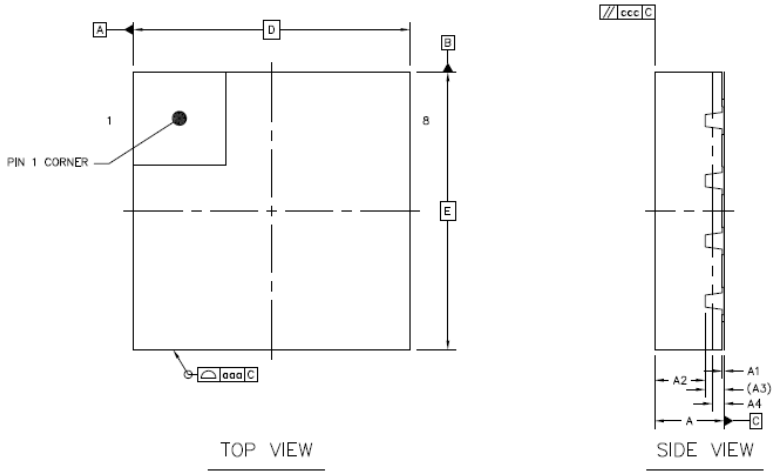


Figure 11- 1. SOIC8 Package Outline

11.2 DFN8 Package Outline

Dimensions in millimeters



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.55	---
L/F THICKNESS		A3		0.203 REF	
SIDE WETTABLE DEPTH		A4	0.075	---	0.18
LEAD WIDTH		b	0.25	0.3	0.35
BODY SIZE	X	D		3 BSC	
	Y	E		3 BSC	
LEAD PITCH		e		0.65 BSC	
EP SIZE	X	D2	1.5	1.6	1.7
	Y	E2	2.3	2.4	2.5
LEAD LENGTH		L	0.3	0.4	0.5
SIDE WETTABLE WIDTH		L1	0.01	---	0.09
LEAD TIP TO EXPOSED PAD EDGE		K		0.3 REF	
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		ccc		0.1	
LEAD OFFSET		bbb		0.1	
		ddd		0.05	
EXPOSED PAD OFFSET		fff		0.1	

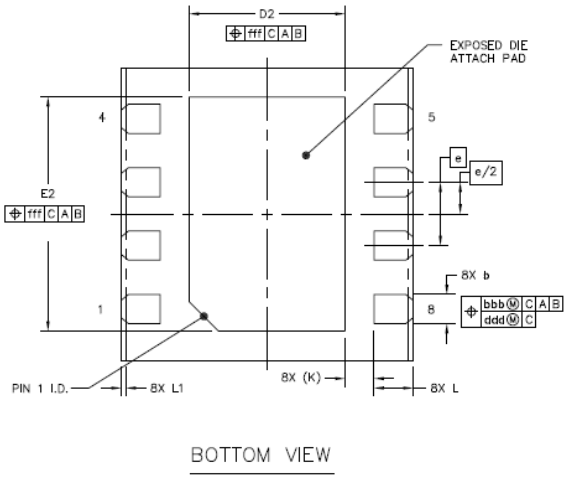


Figure 11- 2. DFN8 Package Outline

12. Soldering Temperature

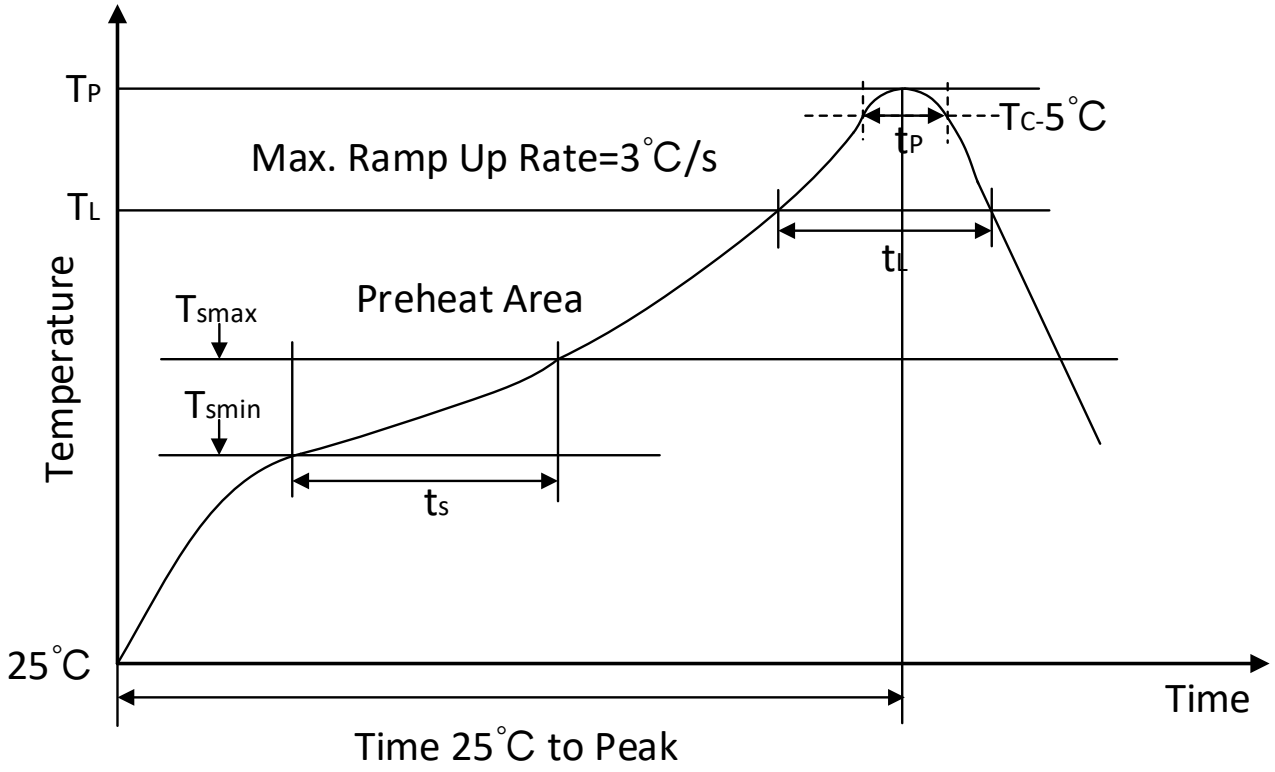
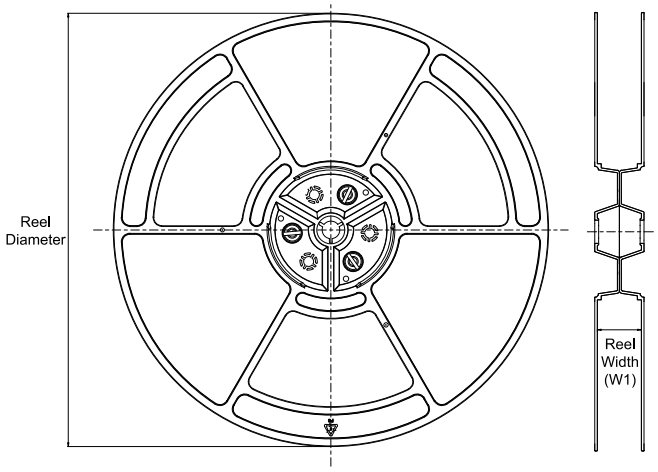


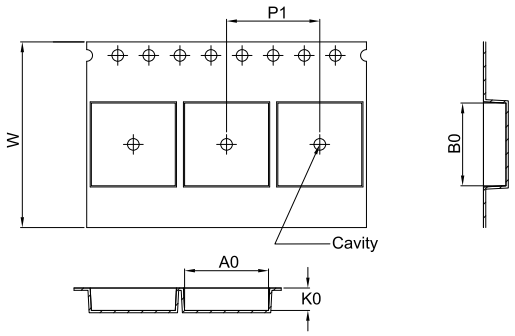
Figure12- 1. Soldering Temperature (reflow) Profile

Table 12-1. Soldering Temperature Parameter

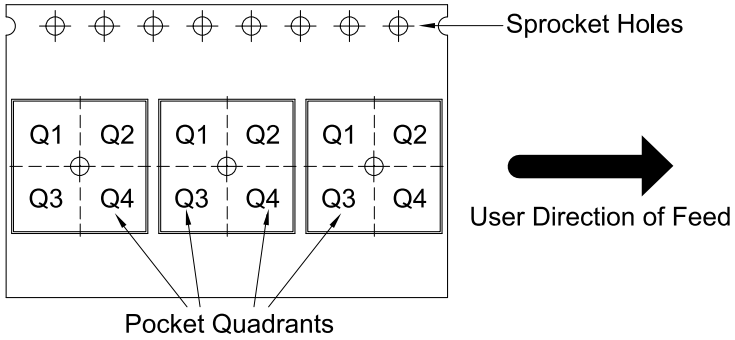
Profile Feature	**Pb-Free Assembly**
Average ramp-up rate(217 ℃ to Peak)	3℃/second max
Time of Preheat temp(from 150 ℃ to 200 ℃	60-120 second
Time to be maintained above 217 ℃	60-150 second
Peak temperature	260 +5/-0 ℃
Time within 5 ℃of actual peak temp	30 second
Ramp-down rate	6 ℃/second max.
Time from 25℃ to peak temp	8 minutes max

13. Tape and Reel Information





A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CA-IF10285AS-Q1	SOIC	S	8	2500	330	12.4	6.4	5.4	2.1	8	12	Q1
CA-IF10283AS-Q1	SOIC	S	8	2500	330	12.4	6.4	5.4	2.1	8	12	Q1
CA-IF10285AD-Q1	DFN	D	8	3000	330	12.4	3.3	3.3	1.1	8	12	Q1
CA-IF10283AD-Q1	DFN	D	8	3000	330	12.4	3.3	3.3	1.1	8	12	Q1

14. Important Statement

The above information is for reference only and used for helping Chipanalog customers with design, research and development. Chipanalog reserves the rights to change the above information due to technological innovation without advance notice.

All Chipanalog products pass ex-factory test. As for specific practical applications, customers need to be responsible for evaluating and determining whether the products are applicable or not by themselves. Chipanalog's authorization for customers to use the resources are only limited to development of the related applications of the Chipanalog products. In addition to this, the resources cannot be copied or shown, and Chipanalog is not responsible for any claims, compensations, costs, losses, liabilities and the like arising from the use of the resources.

Trademark information

Chipanalog Inc.® and Chipanalog® are registered trademarks of Chipanalog.

http://www.chipanalog.com