

CA-IS376x High-Speed Six-Channel Digital Isolators

1. Features

- **Data Rate: DC to 150Mbps**
- **Accepts 2.5V to 5.5V Supplies**
- **Wide Operating Temperature Range: -40°C to 125°C**
- **Default Output *High* (CA-IS376xHB) and *Low* (CA-IS376xLB) Options**
- **No Start-Up Initialization Required**
- **±50 kV/μs typical CMT**
- **Low Power Consumption**
 - 1.5mA per channel at 1Mbps with $V_{DD} = 5.0V$
 - 6.6mA per channel at 100Mbps with $V_{DD} = 5.0V$
- **Best in Class Propagation Delay and Skew**
 - 12ns typical propagation delay
 - 1ns pulse width distortion
 - 2ns propagation delay skew (chip -to-chip)
 - 5ns minimum pulse width
- **Up to 3.75kV_{RMS} isolation rating**
- **High lifetime: >40 years**
- **Three-state input with enable port**
- **Schmitt trigger inputs**
- **Narrow-body SSOP16(B) Package**
- **Safety regulatory approvals**
 - VDE certification according to DIN EN IEC 60747-17(VDE 0884-17):2021-10
 - UL certification according to UL 1577
 - CQC certification according to GB4943.1-2022
 - TUV certification

2. Applications

- Industrial Automation
- Motor Control
- Medical Systems
- Isolated Power Supplies
- Solar Inverters
- Isolated ADC, DAC

3. General Description

The CA-IS376x devices are high-performance six-channel, unidirectional digital isolators with up to 3.75kV_{RMS} isolation rating and ultra-fast data rate. The CA-IS376x devices offer high electromagnetic immunity and low emissions at low power consumption while isolating different ground domains and block high-voltage/high-current transients from sensitive or human interface circuitry. Each isolation channel has a logic input and output buffer separated by capacitive silicon dioxide (SiO₂) insulation barrier, the integrated Schmitt trigger on each input provide excellent noise immunity.

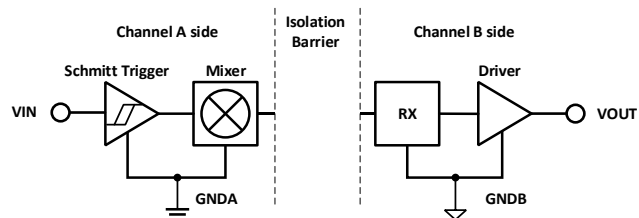
The CA-IS376x family offers all possible unidirectional channel configurations to accommodate any 6-channel design digital I/O applications, especial for the multiple SPI devices isolation. The CA-IS3760 features six channels transferring digital signals in one direction; The CA-IS3761 device has five forward and one reverse-direction channels; The CA-IS3762 device offers four forward and two reverse-direction channels; The CA-IS3763 provides further design flexibility with three channels in each direction. All devices of this family feature default outputs. When the input is either not powered or is open-circuit, the default output is low for devices with suffix L and high for devices with suffix H, see the Ordering Information for suffixes associated with each option.

The CA-IS376x series devices are specified over the -40°C to +125°C operating temperature range and are available in 16-pin SSOP narrow body package.

Device information

Part number	Package	Package size (NOM)
CA-IS3760 CA-IS3761 CA-IS3762 CA-IS3763	SSOP16(B)	4.90 mm × 3.90 mm

Simplified Channel Structure



GNDA and GNDB are the isolated grounds for A side and B side respectively.

4. Ordering Information

Table 4-1. Ordering Information

Part Number	Number of Inputs A Side	Number of Inputs B Side	Default Output	Isolation Rating (kV _{rms})	Output Enable	Package
CA-IS3760LB	6	0	Low	3.75	No	SSOP16
CA-IS3760HB	6	0	High	3.75	No	SSOP16
CA-IS3761LB	5	1	Low	3.75	No	SSOP16
CA-IS3761HB	5	1	High	3.75	No	SSOP16
CA-IS3762LB	4	2	Low	3.75	No	SSOP16
CA-IS3762HB	4	2	High	3.75	No	SSOP16
CA-IS3763LB	3	3	Low	3.75	No	SSOP16
CA-IS3763HB	3	3	High	3.75	No	SSOP16

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5. Revision History

Revision Number	Description	Revision Date	Page Changed
Version 1.0	N/A		N/A
Version 1.01	Changed V_{IORM} to 1414V, changed V_{IOWM} AC RMS value to 1000V and DC value to 1414V. Updated Power Ratings table.		7, 11, 12, 13
Version 1.02	Added CA-IS3760HB, CA-IS3761LB, CA-IS3761HB, CA-IS3763HB parts. Revised pin descriptions. Updated 7.5, 7.9		1,2 4 6,10,11,12
Version 1.03	Changed $V_{IT+(IN)}$ minimum value to 2.0V, changed $V_{IT-(IN)}$ maximum value to 0.8V; removed $V_{I(HYS)}$.		9
Version 1.04	Changed POD and tape reel information	2022/12/15	18,20
Version 1.05	Change DTI to 28um	2023/3/27	1,7,16
Version 1.06	Update VDE certification information	2023/9/13	7,8
Version 1.07	Updated TUV and UL certification information	2024.04.01	9
Version 1.08	Add TUV Certification standard of IEC 62368-1 Change the TUV Certification number to the Client reference number Update the recommended land pattern	2024/09/30	7,8 8 18
Version 1.09	Updated TUV Certification number of IEC 62368-1 standard	2024/12/17	8

6. Pin Configuration and Description

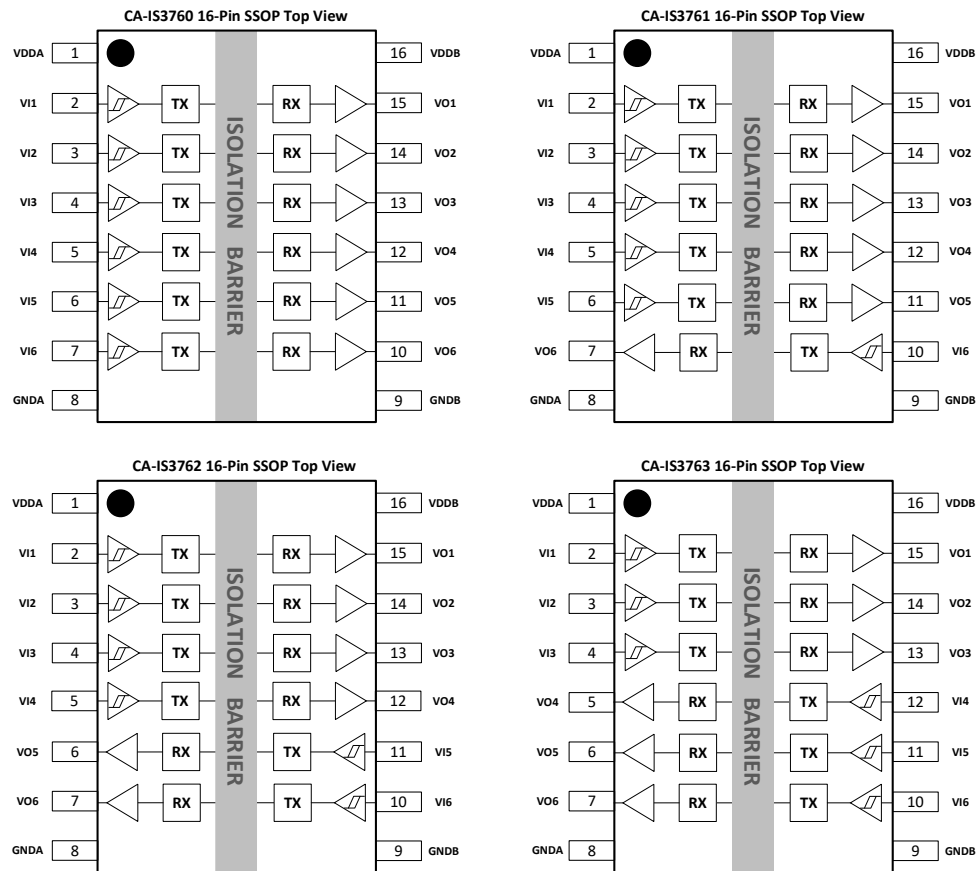


Figure 6-1. CA-IS376x pin configuration

Table 6-1. CA-IS376x pin description

16-SSOP Pin#				Name	Type	Description
CA-IS3760	CA-IS3761	CA-IS3762	CA-IS3763			
1	1	1	1	VDDA	Supply	Power supply for side A.
2	2	2	2	VI1	Digital I/O	Digital input 1 on side A, corresponds to logic output 1 on side B.
3	3	3	3	VI2	Digital I/O	Digital input 2 on side A, corresponds to logic output 2 on side B.
4	4	4	4	VI3	Digital I/O	Digital input 3 on side A, corresponds to logic output 3 on side B.
5	5	5	12	VI4	Digital I/O	Digital input 4 on side A/B, corresponds to logic output 4 on side B/A.
6	6	11	11	VI5	Digital I/O	Digital input 5 on side A/B, corresponds to logic output 5 on side B/A.
7	10	10	10	VI6	Digital I/O	Digital input 6 on side A/B, corresponds to logic output 6 on side B/A.
8	8	8	8	GNDA	Ground	Ground reference for side A.
9	9	9	9	GNDB	Ground	Ground reference for side B.
10	7	7	7	VO6	Digital I/O	Digital output 6 on side B/A, VO6 is the logic output for the VI6 input on side A/B.
11	11	6	6	VO5	Digital I/O	Digital output 5 on side B/A, VO5 is the logic output for the VI5 input on side A/B.
12	12	12	5	VO4	Digital I/O	Digital output 4 on side B/A, VO4 is the logic output for the VI4 input on side A/B.
13	13	13	13	VO3	Digital I/O	Digital output 3 on side B, VO3 is the logic output for the VI3 input on side A.
14	14	14	14	VO2	Digital I/O	Digital output 2 on side B, VO2 is the logic output for the VI2 input on side A.
15	15	15	15	VO1	Digital I/O	Digital output 1 on side B, VO1 is the logic output for the VI1 input on side A.
16	16	16	16	VDDB	Supply	Power supply for side B.

7. Specifications

7.1. Absolute Maximum Ratings¹

Parameters		Minimum value	Maximum value	Unit
V_{DDA}, V_{DDB}	Power supply voltage ²	-0.5	7.0	V
V_{IN}	Voltage at VI_x , VO_x , EN_x	-0.5	$V_{DD-} + 0.5^3$	V
I_O	Output current	-20	20	mA
T_J	Junction temperature		150	°C
T_{STG}	Storage temperature range	-65	150	°C
Notes: 1. The stresses listed under “Absolute Maximum Ratings” are stress ratings only, not for functional operation condition. Exposure to absolute maximum rating conditions for extended periods may cause permanent damage to the device. 2. All voltage values are with respect to the local ground terminal (GNDA or GNDB) and are peak voltage values. 3. Maximum voltage must not be exceed 7 V.				

7.2. ESD Ratings

		Numerical value	Unit
V_{ESD} Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ¹	±6000	V
	Charged device model (CDM), per JEDEC Specification JESD22-C101, all pins ²	±2000	V

7.3. Recommended Operating Conditions

PARAMETER		MIN	TYPE	MAX	UNIT
V_{DDA}, V_{DDB}	Supply voltage on side A, B	2.375	3.3/5.0	5.50	V
$V_{DD(UVLO+)}$	V_{DD} Undervoltage-Lockout Threshold When Supply Voltage is Rising	1.95	2.24	2.375	V
$V_{DD(UVLO-)}$	V_{DD} Undervoltage-Lockout Threshold When Supply Voltage is Falling	1.88	2.10	2.325	V
$V_{HYS(UVLO)}$	V_{DD} Undervoltage-Lockout Threshold Hysteresis	70	140	250	mV
I_{OH}	High-level Output Current	$V_{DDO}^1 = 5V$	-4		mA
		$V_{DDO} = 3.3V$	-2		
		$V_{DDO} = 2.5V$	-1		
I_{OL}	Low-level Output Current	$V_{DDO} = 5V$		4	mA
		$V_{DDO} = 3.3V$		2	
		$V_{DDO} = 2.5V$		1	
V_{IH}	High-level Input Voltage	2.0			V
V_{IL}	Low-level Input Voltage			0.8	V
DR	Data Rate	0		150	Mbps
T_A	Ambient Temperature	-40	27	125	°C
Note: 1. V_{DDO} = Output-side supply V_{DD} .					

7.4. Thermal Information

Thermal Metric		CA-IS376x	Unit
		SSOP16(B)	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	110	°C/W

7.5. Power Rating

Parameters		Test conditions	MIN	TYPE	MAX	Unit
CA-IS3760						
P _D	Maximum Power Dissipation	V _{DDA} = V _{ddb} = 5.5 V, C _L = 15 pF, T _J = 150°C, Input a 75-MHz 50% duty cycle square wave.			494	mW
P _{DA}	Maximum Power Dissipation on Side-A				49	mW
P _{DB}	Maximum Power Dissipation on Side-B				445	mW
CA-IS3761						
P _D	Maximum Power Dissipation	V _{DDA} = V _{ddb} = 5.5 V, C _L = 15 pF, T _J = 150°C, Input a 75-MHz 50% duty cycle square wave.			494	mW
P _{DA}	Maximum Power Dissipation on Side-A				113	mW
P _{DB}	Maximum Power Dissipation on Side-B				381	mW
CA-IS3762						
P _D	Maximum Power Dissipation	V _{DDA} = V _{ddb} = 5.5 V, C _L = 15 pF, T _J = 150°C, Input a 75-MHz 50% duty cycle square wave.			494	mW
P _{DA}	Maximum Power Dissipation on Side-A				180	mW
P _{DB}	Maximum Power Dissipation on Side-B				314	mW
CA-IS3763						
P _D	Maximum Power Dissipation	V _{DDA} = V _{ddb} = 5.5 V, C _L = 15 pF, T _J = 150°C, Input a 75-MHz 50% duty cycle square wave.			494	mW
P _{DA}	Maximum Power Dissipation on Side-A				247	mW
P _{DB}	Maximum Power Dissipation on Side-B				247	mW

7.6. Insulation Specifications

Parameters		Test conditions	Value	Unit
			B	
CLR	External Clearance	Shortest terminal-to-terminal distance through air	4	mm
CPG	External Creepage	Shortest terminal-to-terminal distance across the package surface	4	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	28	μm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	>600	V
Material group		Per IEC 60664-1	I	
Overvoltage category per IEC 60664-1		Rated mains voltage ≤ 150 V _{RMS}	I-IV	
		Rated mains voltage ≤ 300 V _{RMS}	I-III	
		Rated mains voltage ≤ 600 V _{RMS}	n/a	
DIN EN IEC 60747-17 (VDE 0884-17) ¹				
V _{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	566	V _{PK}
V _{IOWM}	Maximum operating isolation voltage	AC voltage; time-dependent dielectric breakdown (TDDb) test	400	V _{RMS}
		DC voltage	566	V _{DC}
V _{IOTM}	Maximum transient isolation voltage	V _{TEST} = V _{IOTM} , t=60 s (certified); V _{TEST} = 1.2 × V _{IOTM} , t=1 s (100% product test)	5300	V _{PK}
V _{IMP}	Maximum impulse voltage	1.2/50 μs waveform per IEC 62368-1	4070	V _{PK}
V _{IOSM}	Maximum surge isolation voltage ²	V _{IOSM} ≥ 1.3 × V _{IMP} ; Tested in oil (qualification test) , 1.2/50 μs waveform per IEC 62368-1	5300	V _{PK}
q _{pd}	Apparent charge ³	Method a, after input/output safety test of the subgroup 2/3, V _{ini} = V _{IOTM} , t _{ini} = 60 s; V _{pd(m)} = 1.2 × V _{IORM} , t _m = 10 s	≤5	pC
		Method a, after environmental test of the subgroup 1, V _{ini} = V _{IOTM} , t _{ini} = 60 s; V _{pd(m)} = 1.6 × V _{IORM} , t _m = 10 s	≤5	
		Method b, at routine test (100% production test) and preconditioning (type test) V _{ini} = 1.2 × V _{IOTM} , t _{ini} = 1 s; V _{pd(m)} = 1.5 × V _{IORM} , t _m = 1 s	≤5	
C _{IO}	Barrier capacitance, input to output ⁴	V _{IO} = 0.4 × sin (2πft), f = 1 MHz	~0.5	pF
R _{IO}	Isolation resistance ⁴	V _{IO} = 500 V, T _A = 25°C	>10 ¹²	Ω
		V _{IO} = 500 V, 100°C ≤ T _A ≤ 125°C	>10 ¹¹	
		V _{IO} = 500 V at T _S = 150°C	>10 ⁹	
Pollution degree			2	
UL 1577				
V _{ISO}	Maximum withstanding isolation voltage	V _{TEST} = V _{ISO} , t = 60 s (qualification) V _{TEST} = 1.2 × V _{ISO} , t = 1 s (100% production test)	3750	V _{RMS}
Notes:				
1. This coupler is suitable for “safe electrical insulation” only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.				
2. Devices are immersed in oil during surge characterization test.				
3. The characterization charge is discharging charge (pd) caused by partial discharge.				
4. Capacitance and resistance are measured with all pins on field-side and logic-side tied together.				

7.7. Safety-Related Certifications

VDE	UL	CQC	TUV
Certified according to DIN EN IEC 60747-17 (VDE 0884-17):2021-10; EN IEC 60747- 17:2020+AC:2021	Certified according to UL 1577 Component Recognition Program	Certified according to GB 4943.1-2022	Certified according to EN 61010-1 and EN 62368-1
Basic Isolation: V_{IORM} : 566V _{pk} V_{IOTM} : 5300V _{pk} V_{IOSM} : 5300V _{pk}	3750 V _{RMS} ;	SSOP16: Basic insulation (Altitude ≤ 5000 m)	EN 61010-1 3750 V _{RMS} EN 62368-1 3750 V _{RMS}
Certificate number: 40052786 (basic isolation)	Certificate number: E511334	Certificate number: CQC24001453031	Client reference number: 2253313

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7.8. Electrical Characteristics

 $V_{DDA} = V_{ddb} = 5\text{ V} \pm 10\%$, $T_A = -40\text{ to }125^\circ\text{C}$ (over recommended operating conditions, unless otherwise specified)

Parameters	Test conditions	MIN	TYPE	MAX	UNIT
V_{OH} High-level Output Voltage	$I_{OH} = -4\text{mA}$; See Figure 8-2	$V_{DDO}^{1-0.4}$	4.8		V
V_{OL} Low-level Output Voltage	$I_{OL} = 4\text{mA}$; See Figure 8-2		0.2	0.4	V
$V_{IT+(IN)}$ Rising input switching threshold		2.0			V
$V_{IT-(IN)}$ Falling input switching threshold				0.8	V
I_{IH} High-Level Input Leakage Current	$V_{IH} = V_{DDA}$ at INx or ENx			20	μA
I_{IL} Low-Level Input Leakage Current	$V_{IL} = 0\text{ V}$ at INx	-20			μA
Z_O Output Impedance ²			50		Ω
CMTI Common-mode Transient Immunity	$V_I = V_{DDI}^{1-0.4}$ or 0 V, $V_{CM} = 1200\text{V}$; See Figure 8-3		50		$\text{kV}/\mu\text{s}$
C_i Input Capacitance ³	$V_I = V_{DD}/2 + 0.4 \times \sin(2\pi ft)$, $f = 1\text{ MHz}$, $V_{DD} = 5\text{ V}$		2		pF

Notes:

- V_{DDI} = Input-side supply V_{DD} , V_{DDO} = Output-side supply V_{DD} .
- The nominal output impedance of each isolator driver is $50\ \Omega \pm 40\%$.
- Measured from pin to Ground.

 $V_{DDA} = V_{ddb} = 3.3\text{ V} \pm 10\%$, $T_A = -40\text{ to }125^\circ\text{C}$ (over recommended operating conditions, unless otherwise specified)

Parameters	Test conditions	MIN	TYPE	MAX	UNIT
V_{OH} High-level Output Voltage	$I_{OH} = -2\text{mA}$; See Figure 8-2	$V_{DDO}^{1-0.4}$	3.1		V
V_{OL} Low-level Output Voltage	$I_{OL} = 2\text{mA}$; See Figure 8-2		0.2	0.4	V
$V_{IT+(IN)}$ Rising input switching threshold		2.0			V
$V_{IT-(IN)}$ Falling input switching threshold				0.8	V
I_{IH} High-Level Input Leakage Current	$V_{IH} = V_{DDA}$ at INx or ENx			20	μA
I_{IL} Low-Level Input Leakage Current	$V_{IL} = 0\text{ V}$ at INx	-20			μA
Z_O Output Impedance ²			50		Ω
CMTI Common-mode Transient Immunity	$V_I = V_{DDI}^{1-0.4}$ or 0 V, $V_{CM} = 1200\text{V}$; See Figure 8-3		50		$\text{kV}/\mu\text{s}$
C_i Input Capacitance ³	$V_I = V_{DD}/2 + 0.4 \times \sin(2\pi ft)$, $f = 1\text{ MHz}$, $V_{DD} = 3.3\text{ V}$		2		pF

Notes:

- V_{DDI} = Input-side supply V_{DD} , V_{DDO} = Output-side supply V_{DD} .
- The nominal output impedance of each isolator driver is $50\ \Omega \pm 40\%$.
- Measured from pin to Ground.

 $V_{DDA} = V_{ddb} = 2.5\text{ V} \pm 10\%$, $T_A = -40\text{ to }125^\circ\text{C}$ (over recommended operating conditions, unless otherwise specified)

Parameters	Test conditions	MIN	TYPE	MAX	UNIT
V_{OH} High-level Output Voltage	$I_{OH} = -1\text{mA}$; See Figure 8-2	$V_{DDO}^{1-0.4}$	2.3		V
V_{OL} Low-level Output Voltage	$I_{OL} = 1\text{mA}$; See Figure 8-2		0.2	0.4	V
$V_{IT+(IN)}$ Rising input switching threshold		2.0			V
$V_{IT-(IN)}$ Falling input switching threshold				0.8	V
I_{IH} High-Level Input Leakage Current	$V_{IH} = V_{DDA}$ at INx or ENx			20	μA
I_{IL} Low-Level Input Leakage Current	$V_{IL} = 0\text{ V}$ at INx	-20			μA
Z_O Output Impedance ²			50		Ω
CMTI Common-mode Transient Immunity	$V_I = V_{DDI}^{1-0.4}$ or 0 V, $V_{CM} = 1200\text{V}$; See Figure 8-3		50		$\text{kV}/\mu\text{s}$
C_i Input Capacitance ³	$V_I = V_{DD}/2 + 0.4 \times \sin(2\pi ft)$, $f = 1\text{ MHz}$, $V_{DD} = 2.5\text{ V}$		2		pF

Notes:

- V_{DDI} = Input-side supply V_{DD} , V_{DDO} = Output-side supply V_{DD} .
- The nominal output impedance of each isolator driver is $50\ \Omega \pm 40\%$.
- Measured from pin to Ground.

7.9. Supply Current Characteristics
 $V_{DDA} = V_{ddb} = 5\text{ V} \pm 10\%$, $T_A = -40$ to 125°C (over recommended operating conditions, unless otherwise specified).

Parameters	Test conditions		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
CA-IS3760							
Supply Current – DC Signal	V _{IN} = 0V (CA-IS3760L); V _{IN} = V _{DDA} (CA-IS3760H)		I _{DDA}	2.0	2.9	mA	
			I _{ddb}	3.9	5.7		
	V _{IN} = V _{DDA} (CA-IS3760L); V _{IN} = 0V(CA-IS3760H)		I _{DDA}	7.0	10.7		
			I _{ddb}	4.1	6.1		
Supply Current – AC Signal	All Channels Switching with 50% Duty Cycle Square Wave Clock Input with 5V Amplitude; C _L = 15 pF for Each Channel.	1Mbps (500kHz)	I _{DDA}	4.5	6.8		
		10Mbps (5MHz)	I _{ddb}	6.3	9.3		
			I _{DDA}	4.8	7.2		
		100Mbps (50MHz)	I _{ddb}	26.9	40.6		
			I _{DDA}	6.4	9.5		
		I _{ddb}	59.0	80			
CA-IS3761							
Supply Current – DC Signal	V _{IN} = 0V (CA-IS3761L); V _{IN} = V _{DDI} ¹ (CA-IS3761H)		I _{DDA}	2.3	3.4	mA	
			I _{ddb}	3.6	5.3		
	V _{IN} = V _{DDI} ¹ (CA-IS3761L); V _{IN} = 0V(CA-IS3761H)		I _{DDA}	6.5	9.9		
			I _{ddb}	4.6	6.9		
Supply Current – AC Signal	All Channels Switching with 50% Duty Cycle Square Wave Clock Input with 5V Amplitude; C _L = 15 pF for Each Channel.	1Mbps (500kHz)	I _{DDA}	4.5	6.7		
		10Mbps (5MHz)	I _{ddb}	5.7	8.4		
			I _{DDA}	5.1	7.6		
		100Mbps (50MHz)	I _{ddb}	19.8	29.9		
			I _{DDA}	10.6	16.3		
		I _{ddb}	45.6	62.1			
CA-IS3762							
Supply Current – DC Signal	V _{IN} = 0V (CA-IS3762L); V _{IN} = V _{DDI} ¹ (CA-IS3762H)		I _{DDA}	2.8	4.5	mA	
			I _{ddb}	3.8	5.8		
	V _{IN} = V _{DDI} ¹ (CA-IS3762L); V _{IN} = 0V(CA-IS3762H)		I _{DDA}	6.2	9.9		
			I _{ddb}	5.6	8.7		
Supply Current – AC Signal	All Channels Switching with 50% Duty Cycle Square Wave Clock Input with 5V Amplitude; C _L = 15 pF for Each Channel.	1Mbps (500kHz)	I _{DDA}	5.4	8.3		
		10Mbps (5MHz)	I _{ddb}	6.3	9.5		
			I _{DDA}	13.1	18.3		
		100Mbps (50MHz)	I _{ddb}	21.0	31.5		
			I _{DDA}	26.0	36.9		
		I _{ddb}	44.7	72.2			
CA-IS3763							
Supply Current – DC Signal	V _{IN} = 0V (CA-IS3763L); V _{IN} = V _{DDI} ¹ (CA-IS3763H)		I _{DDA}	2.9	4.4	mA	
			I _{ddb}	2.9	4.4		
	V _{IN} = V _{DDI} ¹ (CA-IS3763L); V _{IN} = 0V(CA-IS3763H)		I _{DDA}	5.5	8.4		
			I _{ddb}	5.5	8.4		
Supply Current – AC Signal	All Channels Switching with 50% Duty Cycle Square Wave Clock Input with 5V Amplitude; C _L = 15 pF for Each Channel.	1Mbps (500kHz)	I _{DDA}	4.3	6.5		
		10Mbps (5MHz)	I _{ddb}	4.3	6.5		
			I _{DDA}	5.7	8.4		
		100Mbps (50MHz)	I _{ddb}	5.7	8.4		
			I _{DDA}	19.9	30.0		
		I _{ddb}	19.9	30.0			
Note:							
1. V _{DDI} = Input-side supply V _{DD} .							

$V_{DDA} = V_{DDB} = 3.3\text{ V} \pm 10\%$, $T_A = -40\text{ to }125^\circ\text{C}$ (over recommended operating conditions, unless otherwise specified)

Parameters	Test conditions		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
CA-IS3760							
Supply Current – DC Signal	$V_{IN} = 0V$ (CA-IS3760L); $V_{IN} = V_{DDA}$ (CA-IS3760H)		I_{DDA}		1.9	2.8	mA
			I_{DDB}		3.6	5.4	
	$V_{IN} = V_{DDA}$ (CA-IS3760L); $V_{IN} = 0V$ (CA-IS3760H)		I_{DDA}		6.8	10.5	
			I_{DDB}		3.9	5.7	
Supply Current – AC Signal	All Channels Switching with 50% Duty Cycle Square Wave Clock Input with 3.3V Amplitude; $C_L = 15\text{ pF}$ for Each Channel.	1Mbps (500kHz)	I_{DDA}		4.4	6.7	
		10Mbps (5MHz)	I_{DDB}		5.2	7.5	
			I_{DDA}		4.6	7.0	
		I_{DDB}		18.3	24.6		
		100Mbps (50MHz)	I_{DDA}		6.1	9.0	
			I_{DDB}		38.3	51.8	
CA-IS3761							
Supply Current – DC Signal	$V_{IN} = 0V$ (CA-IS3761L); $V_{IN} = V_{DDI}^1$ (CA-IS3761H)		I_{DDA}		2.2	3.2	mA
			I_{DDB}		3.4	5.0	
	$V_{IN} = V_{DDI}^1$ (CA-IS3761L); $V_{IN} = 0V$ (CA-IS3761H)		I_{DDA}		6.3	9.7	
			I_{DDB}		4.4	6.5	
Supply Current – AC Signal	All Channels Switching with 50% Duty Cycle Square Wave Clock Input with 3.3V Amplitude; $C_L = 15\text{ pF}$ for Each Channel.	1Mbps (500kHz)	I_{DDA}		4.3	6.5	
		10Mbps (5MHz)	I_{DDB}		4.8	7.1	
			I_{DDA}		4.8	7.1	
		I_{DDB}		13.9	18.9		
		100Mbps (50MHz)	I_{DDA}		8.6	12.2	
			I_{DDB}		30.1	40.8	
CA-IS3762							
Supply Current – DC Signal	$V_{IN} = 0V$ (CA-IS3762L); $V_{IN} = V_{DDI}^1$ (CA-IS3762H)		I_{DDA}		2.7	4.3	mA
			I_{DDB}		3.6	5.6	
	$V_{IN} = V_{DDI}^1$ (CA-IS3762L); $V_{IN} = 0V$ (CA-IS3762H)		I_{DDA}		6.0	9.7	
			I_{DDB}		5.4	8.4	
Supply Current – AC Signal	All Channels Switching with 50% Duty Cycle Square Wave Clock Input with 3.3V Amplitude; $C_L = 15\text{ pF}$ for Each Channel.	1Mbps (500kHz)	I_{DDA}		4.9	7.7	
		10Mbps (5MHz)	I_{DDB}		5.6	8.5	
			I_{DDA}		10.0	14.3	
		I_{DDB}		15.2	22.7		
		100Mbps (50MHz)	I_{DDA}		18.5	26.2	
			I_{DDB}		30.4	48.1	
CA-IS3763							
Supply Current – DC Signal	$V_{IN} = 0V$ (CA-IS3763L); $V_{IN} = V_{DDI}^1$ (CA-IS3763H)		I_{DDA}		2.7	4.1	mA
			I_{DDB}		2.7	4.1	
	$V_{IN} = V_{DDI}^1$ (CA-IS3763L); $V_{IN} = 0V$ (CA-IS3763H)		I_{DDA}		5.3	8.1	
			I_{DDB}		5.3	8.1	
Supply Current – AC Signal	All Channels Switching with 50% Duty Cycle Square Wave Clock Input with 3.3V Amplitude; $C_L = 15\text{ pF}$ for Each Channel.	1Mbps (500kHz)	I_{DDA}		4.1	6.2	
		10Mbps (5MHz)	I_{DDB}		4.1	6.2	
			I_{DDA}		5.1	7.4	
		I_{DDB}		5.1	7.4		
		100Mbps (50MHz)	I_{DDA}		13.6	18.7	
			I_{DDB}		13.6	18.7	
Note:							
1. V_{DDI} = Input-side supply V_{DD} .							

CA-IS3760, CA-IS3761, CA-IS3762, CA-IS3763
Version 1.09

Shanghai Chipanalog Microelectronics Co., Ltd.

 $V_{DDA} = V_{ddb} = 2.5\text{ V} \pm 10\%$, $T_A = -40\text{ to }125^\circ\text{C}$ (over recommended operating conditions, unless otherwise specified)

Parameters	Test conditions		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
CA-IS3760							
Supply Current – DC Signal	$V_{IN} = 0V$ (CA-IS3760L); $V_{IN} = V_{DDA}$ (CA-IS3760H)		I_{DDA}		1.9	2.7	mA
			I_{DDB}		3.6	5.2	
	$V_{IN} = V_{DDA}$ (CA-IS3760L); $V_{IN} = 0V$ (CA-IS3760H)		I_{DDA}		6.8	10.4	
			I_{DDB}		3.8	5.5	
Supply Current – AC Signal	All Channels Switching with 50% Duty Cycle Square Wave Clock Input with 2.5V Amplitude; $C_L = 15$ pF for Each Channel.	1Mbps (500kHz)	I_{DDA}		4.3	6.6	
			I_{DDB}		4.8	6.9	
		10Mbps (5MHz)	I_{DDA}		4.6	6.9	
			I_{DDB}		14.7	19.8	
		100Mbps (50MHz)	I_{DDA}		5.7	8.5	
			I_{DDB}		28.9	39.0	
CA-IS3761							
Supply Current – DC Signal	$V_{IN} = 0V$ (CA-IS3761L); $V_{IN} = V_{DDI}^1$ (CA-IS3761H)		I_{DDA}		2.1	3.2	mA
			I_{DDB}		3.3	4.8	
	$V_{IN} = V_{DDI}^1$ (CA-IS3761L); $V_{IN} = 0V$ (CA-IS3761H)		I_{DDA}		6.3	9.6	
			I_{DDB}		4.3	6.4	
Supply Current – AC Signal	All Channels Switching with 50% Duty Cycle Square Wave Clock Input with 2.5V Amplitude; $C_L = 15$ pF for Each Channel.	1Mbps (500kHz)	I_{DDA}		4.3	6.4	
			I_{DDB}		4.5	6.6	
		10Mbps (5MHz)	I_{DDA}		4.6	6.9	
			I_{DDB}		11.4	15.5	
		100Mbps (50MHz)	I_{DDA}		7.6	10.8	
			I_{DDB}		23.1	31.2	
CA-IS3762							
Supply Current – DC Signal	$V_{IN} = 0V$ (CA-IS3762L); $V_{IN} = V_{DDI}^1$ (CA-IS3762H)		I_{DDA}		2.6	4.2	mA
			I_{DDB}		3.5	5.5	
	$V_{IN} = V_{DDI}^1$ (CA-IS3762L); $V_{IN} = 0V$ (CA-IS3762H)		I_{DDA}		6.0	9.6	
			I_{DDB}		5.3	8.3	
Supply Current – AC Signal	All Channels Switching with 50% Duty Cycle Square Wave Clock Input with 2.5V Amplitude; $C_L = 15$ pF for Each Channel.	1Mbps (500kHz)	I_{DDA}		4.8	7.4	
			I_{DDB}		5.2	8.0	
		10Mbps (5MHz)	I_{DDA}		8.6	12.4	
			I_{DDB}		12.6	18.6	
		100Mbps (50MHz)	I_{DDA}		14.8	21.2	
			I_{DDB}		23.3	36.3	
CA-IS3763							
Supply Current – DC Signal	$V_{IN} = 0V$ (CA-IS3763L); $V_{IN} = V_{DDI}^1$ (CA-IS3763H)		I_{DDA}		2.7	4.0	mA
			I_{DDB}		2.7	4.0	
	$V_{IN} = V_{DDI}^1$ (CA-IS3763L); $V_{IN} = 0V$ (CA-IS3763H)		I_{DDA}		5.2	8.0	
			I_{DDB}		5.2	8.0	
Supply Current – AC Signal	All Channels Switching with 50% Duty Cycle Square Wave Clock Input with 2.5V Amplitude; $C_L = 15$ pF for Each Channel.	1Mbps (500kHz)	I_{DDA}		4.0	6.1	
			I_{DDB}		4.0	6.1	
		10Mbps (5MHz)	I_{DDA}		4.8	7.0	
			I_{DDB}		4.8	7.0	
		100Mbps (50MHz)	I_{DDA}		11.3	16.0	
			I_{DDB}		11.3	16.0	
Note:							
1. V_{DDI} = Input-side supply V_{DD} .							

7.10. Timing Characteristics

$V_{DDA} = V_{ddb} = 5\text{ V} \pm 10\%$, $T_A = -40$ to 125°C (over recommended operating conditions, unless otherwise specified)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DR Data Rate		0		150	Mbps
PW _{min} Minimum Pulse Width				5.0	ns
t _{PLH} , t _{PHL} Propagation Delay Time	See Figure 8-1	5.0	12.0	15.0	ns
PWD Pulse Width Distortion t _{PLH} - t _{PHL}			0.2	4.5	ns
t _{sk(o)} Channel-to-Channel Output Skew Time ¹	Same-direction channels		0.4	2.5	ns
t _{sk(pp)} Part-to-Part Output Skew Time ²			2.0	4.5	ns
t _r Output Signal Rise Time	See Figure 8-1		2.5	4.0	ns
t _f Output Signal Fall Time	See Figure 8-1		2.5	4.0	ns
t _{DO} Default Output Delay Time from Input Power Loss	See Figure 8-2		8	12	ns
t _{SU} Start-up Time			15	40	μs

Notes:

- tsk(o) is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
- tsk(pp) is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

$V_{DDA} = V_{ddb} = 3.3\text{ V} \pm 10\%$, $T_A = -40$ to 125°C (over recommended operating conditions, unless otherwise specified)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DR Data Rate		0		150	Mbps
PW _{min} Minimum Pulse Width				5.0	ns
t _{PLH} , t _{PHL} Propagation Delay Time	See Figure 8-1	5.0	12.0	15.0	ns
PWD Pulse Width Distortion t _{PLH} - t _{PHL}			0.2	4.5	ns
t _{sk(o)} Channel-to-Channel Output Skew Time ¹	Same-direction channels		0.4	2.5	ns
t _{sk(pp)} Part-to-Part Output Skew Time ²			2.0	4.5	ns
t _r Output Signal Rise Time	See Figure 8-1		2.5	4.0	ns
t _f Output Signal Fall Time	See Figure 8-1		2.5	4.0	ns
t _{DO} Default Output Delay Time from Input Power Loss	See Figure 8-2		8	12	ns
t _{SU} Start-up Time			15	40	μs

Notes:

- tsk(o) is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
- tsk(pp) is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

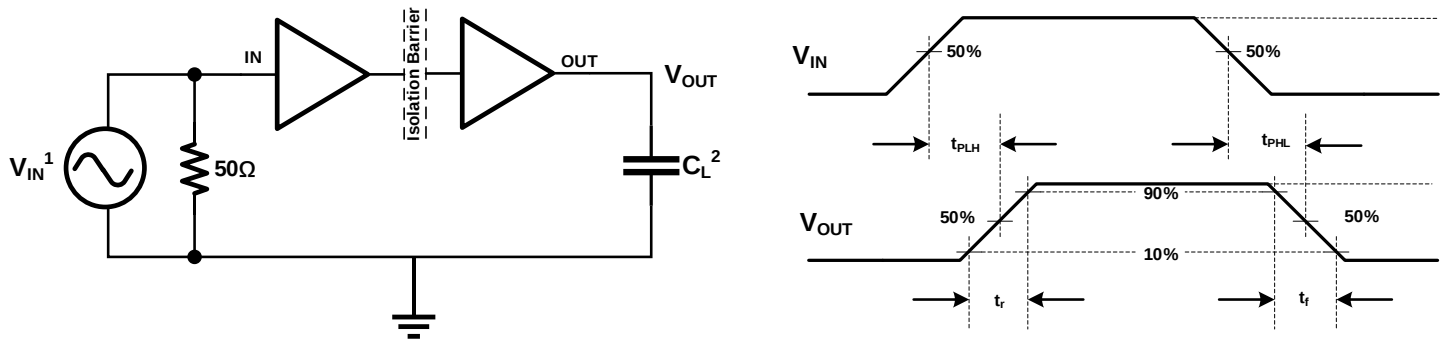
$V_{DDA} = V_{ddb} = 2.5\text{ V} \pm 10\%$, $T_A = -40$ to 125°C (over recommended operating conditions, unless otherwise specified)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DR Data Rate		0		150	Mbps
PW _{min} Minimum Pulse Width				5.0	ns
t _{PLH} , t _{PHL} Propagation Delay Time	See Figure 8-1	5.0	12.0	15.0	ns
PWD Pulse Width Distortion t _{PLH} - t _{PHL}			0.2	4.5	ns
t _{sk(o)} Channel-to-Channel Output Skew Time ¹	Same-direction channels		0.4	2.5	ns
t _{sk(pp)} Part-to-Part Output Skew Time ²			1.0	5.0	ns
t _r Output Signal Rise Time	See Figure 8-1		2.5	4.0	ns
t _f Output Signal Fall Time	See Figure 8-1		2.5	4.0	ns
t _{DO} Default Output Delay Time from Input Power Loss	See Figure 8-2		8	12	ns
t _{SU} Start-up Time			15	40	μs

Notes:

- tsk(o) is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
- tsk(pp) is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

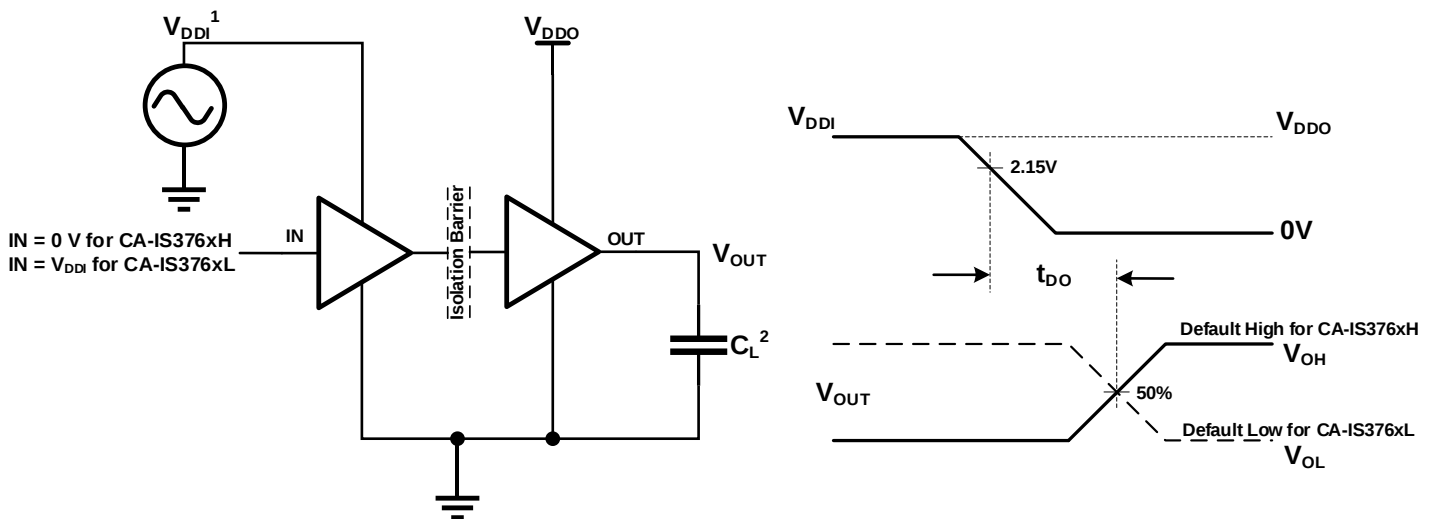
8. Parameter Measurement Information



Notes:

1. A square wave generator provide V_{IN} input signal with the following characteristics: frequency $\leq 100\text{kHz}$, 50% duty cycle, $t_r \leq 3\text{ns}$, $t_f \leq 3\text{ns}$, $Z_{out} = 50\Omega$. At the input, 50Ω resistor is required to terminate input generator signal. It is not needed in actual application.
2. $C_L = 15\text{pF}$ and includes external circuit (instrumentation and fixture etc.) capacitance. Since the load capacitance influence the output rising time, it's a key factor in the timing characteristic measurement.

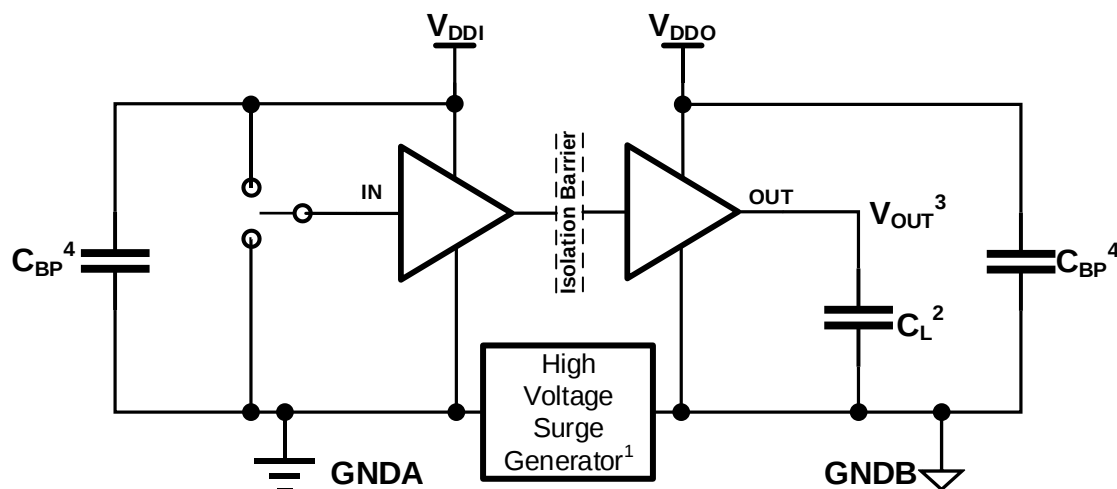
Figure 8-1. Switching Characteristics Test Circuit and Voltage Waveforms



Notes:

1. Power Supply Ramp Rate = 10 mV/ns . V_{DDI} should ramp over 2.375V , and less than 5.5V .
2. $C_L = 15\text{pF}$ and includes external circuit (instrumentation and fixture etc.) capacitance. Since the load capacitance influence the output rising time, it's a key factor in the timing characteristic measurement.

Figure 8-2. Default Output Delay Time Test Circuit and Voltage Waveforms



Notes:

1. The High Voltage Surge Generator generates repetitive high voltage surges with > 1kV amplitude, rise time <10ns and fall time <10ns, to reach common-mode transient noise with > 150kV/μs slew rate.
2. $C_L = 15\text{pF}$ and includes external circuit (instrumentation and fixture etc.) capacitance.
3. Pass-fail criteria: the output must remain stable.
4. C_{BP} (0.1 ~ 1μF) is bypass capacitance.

Figure 8-3. Common-Mode Transient Immunity Test Circuit

9. Detailed Description

9.1. Overview

The CA-IS376x are a family of six-channel digital galvanic isolators using Chipanalog's full differential capacitive isolation technology. These devices have an ON-OFF keying (OOK) modulation scheme to transfer digital signals across the SiO₂ based isolation barrier between circuits with different power domains. The transmitter sends a high frequency carrier across the barrier to represent one digital state and sends no signal to represent the other digital state. The receiver demodulates the signal and recovery input signal at output through a buffer stage. With this OOK architecture, CA-IS376x family of devices build a robust data transmission path between different power domains without any special start-up initialization requirements. These devices also incorporate advanced full differential techniques to minimize the radiated emissions due the high frequency carrier and IO buffer switching.

9.2. Functional Block Diagram

The conceptual block diagram of a digital capacitive isolator, Figure 9-1, shows a functional block diagram of a typical channel; Figure 9-2 shows the operating waveform of a typical channel. Each channel of the CA-IS376x is unidirectional, only passes data in one direction as indicated in the functional diagram. Each device of this family features six unidirectional channels that operate independently with guaranteed data rates from DC up to 150Mbps.

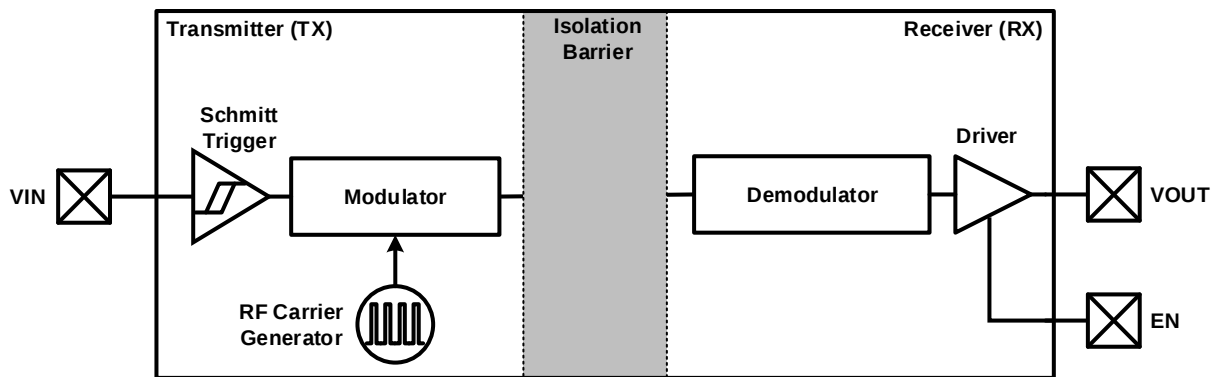


Figure 9-1. Functional Block Diagram of a Single Channel

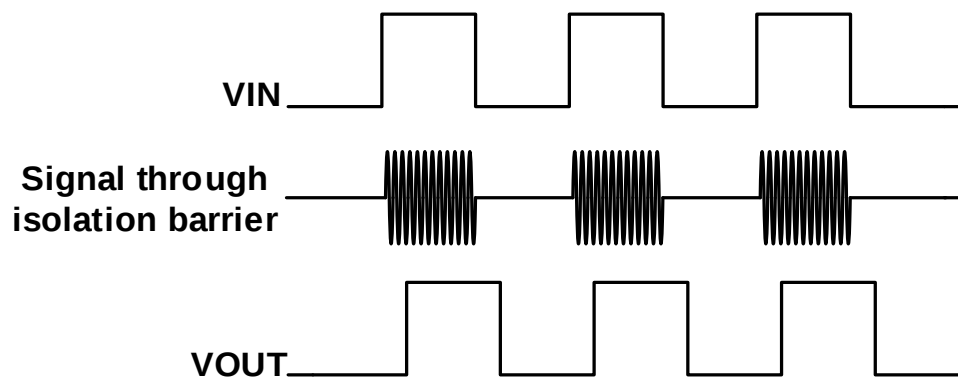


Figure 9-2. Conceptual Operation Waveforms of a Single Channel

9.3. Device Operation Modes

Table 9-1 lists the operation modes for the CA-IS376x devices.

Table 9-1. Operation Mode

V_{DDI}^1	V_{DDO}^1	INPUT (Ax/Bx) ²	OPERATION
PU	PU	H	Normal operation mode: Each channel output follows the logic state of its input.
		L	
		Open	Default output mode: When input V _{Ix} is open, the corresponding channel output goes to its default logic state. Default is <i>High</i> for CA-IS376xH and Low for CA-IS376xL.
PD	PU	X	Default output mode: When V _{DDI} is unpowered, a channel output assumes the logic state based on its default option. Default is <i>High</i> for CA-IS376xH and Low for CA-IS376xL.
X	PD	X	If the output side V _{DDO} is unpowered, a channel output is undetermined. ⁴

Notes:

- V_{DDI} = Input-side supply V_{DD}; V_{DDO} = Output-side supply V_{DD}; PU = Powered up ($V_{DD} \geq V_{DD(UVLO+)}$); PD = Powered down ($V_{DD} \leq V_{DD(UVLO-)}$); X = Irrelevant; H = High level; L = Low level; Z = High Impedance.
- A strongly driven input signal can weakly power the floating V_{DD} through an internal protection diode and cause undetermined output.

10. Application and Implementation

Unlike optocouplers, which require external components to improve performance, provide bias, or limit current, the CA-IS376x devices only require two external bypass capacitors to operate. To reduce ripple and the chance of introducing data errors, bypass VDDA and VDDB pins with 0.1μF to 1μF low-ESR ceramic capacitors to GNDA and GNDB respectively. Place the bypass capacitors as close to the power supply input pins as possible. The CA-IS37xx input is compatible with TTL levels, absorbs only microampere input leakage current, and can be driven without an external buffer circuit. The output resistance is 50Ω (rail to rail output) and forward and reverse channel configurations are available. Figure 10-1 shows typical operating circuit of the CA-IS37xx series products.

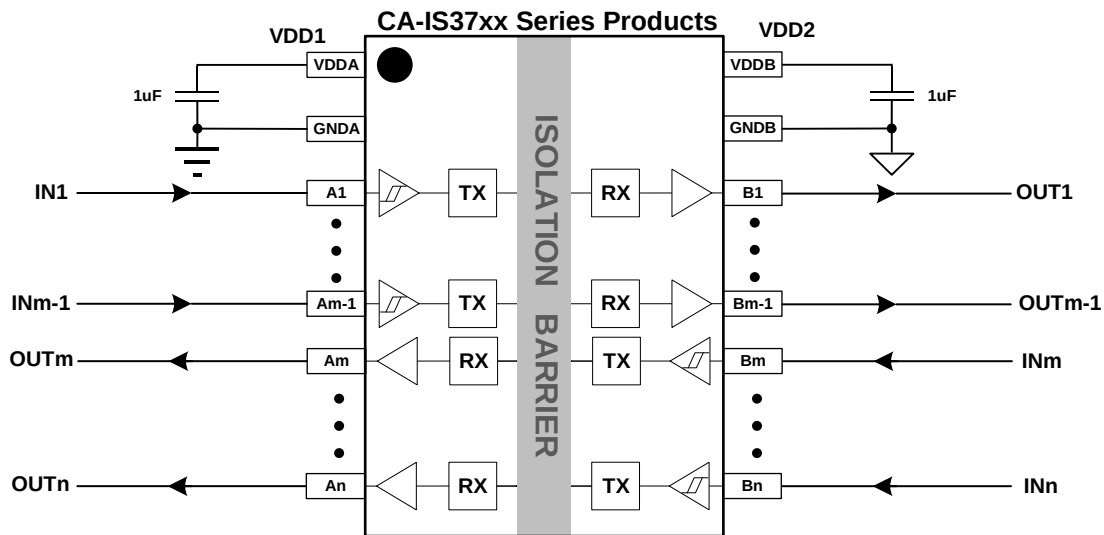
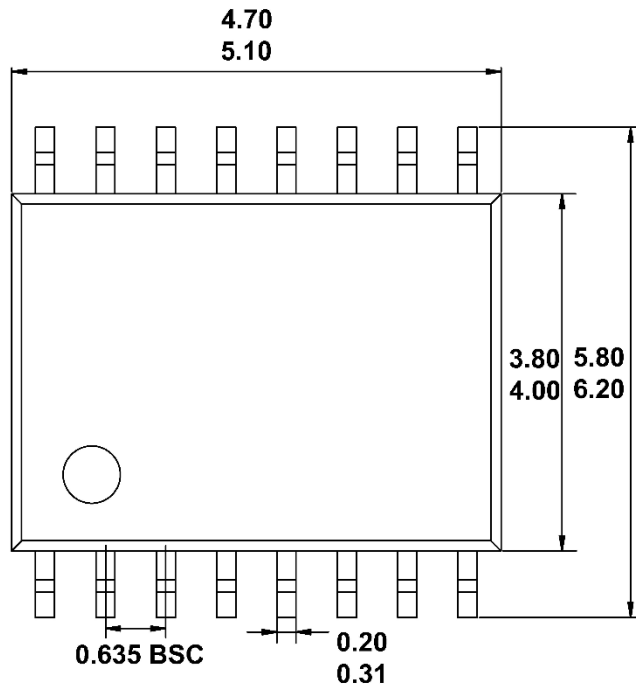


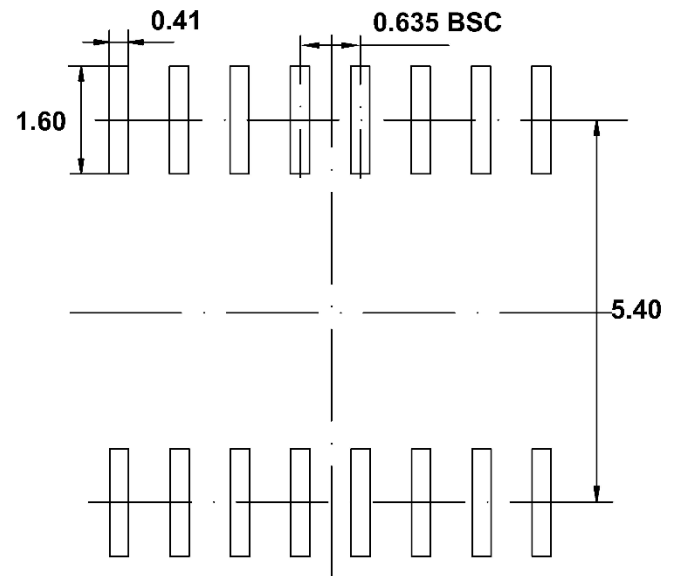
Figure 10-1. Typical Applications for the CA-IS37xx Series Digital Isolators

11. Package Information

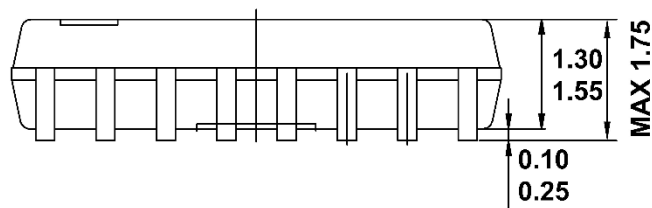
16-Pin Narrow Body SSOP Package Outline



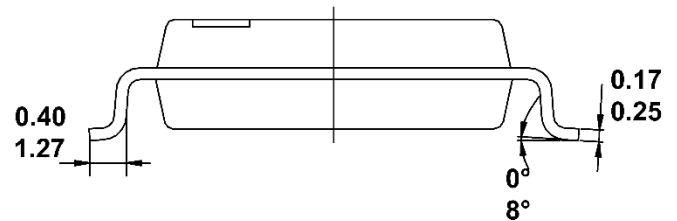
TOP VIEW



RECOMMENDED LAND PATTERN



BOTTOM VIEW



LEFT SIDE VIEW

Figure11-1 SSOP16(B) Package

12. Soldering Temperature (reflow) Profile

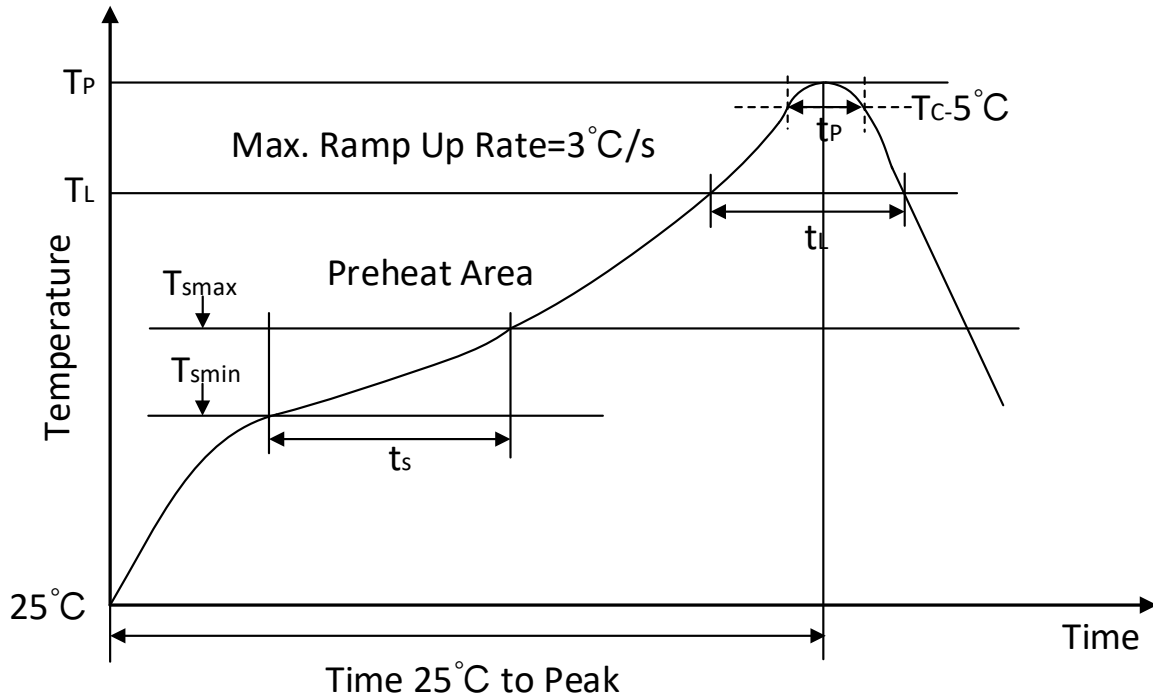
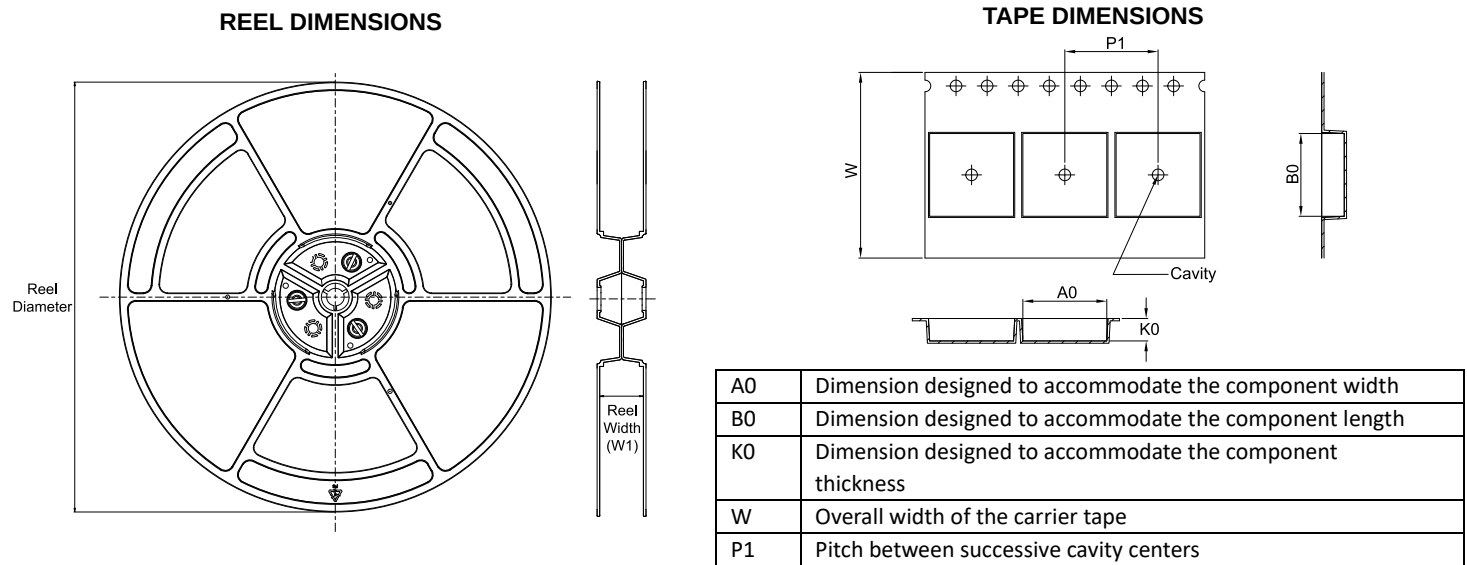


Figure. 12-1 Soldering Temperature (reflow) Profile

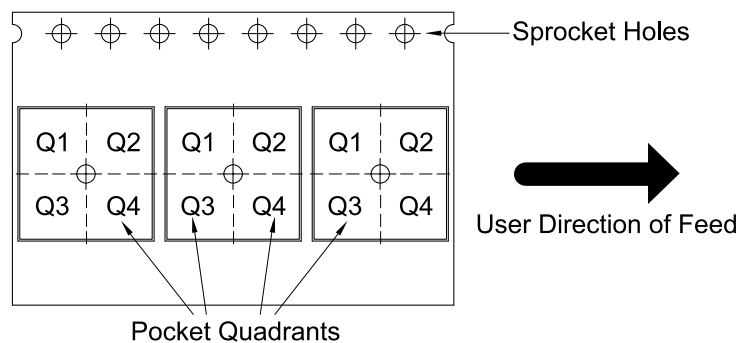
Table 12-1 Soldering Temperature Parameter

Profile Feature	Pb-Free Assembly
Average ramp-up rate(217 °C to Peak)	3°C/second max
Time of Preheat temp(from 150 °C to 200 °C)	60-120 second
Time to be maintained above 217 °C	60-150 second
Peak temperature	260 +5/-0 °C
Time within 5 °C of actual peak temp	30 second
Ramp-down rate	6 °C/second max.
Time from 25°C to peak temp	8 minutes max

13. Tape and Reel Information



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CA-IS3760LB	SSOP16	B	16	2500	330	12.4	6.40	5.40	2.10	8.00	12.00	Q1
CA-IS3760HB	SSOP16	B	16	2500	330	12.4	6.40	5.40	2.10	8.00	12.00	Q1
CA-IS3761LB	SSOP16	B	16	2500	330	12.4	6.40	5.40	2.10	8.00	12.00	Q1
CA-IS3761HB	SSOP16	B	16	2500	330	12.4	6.40	5.40	2.10	8.00	12.00	Q1
CA-IS3762LB	SSOP16	B	16	2500	330	12.4	6.40	5.40	2.10	8.00	12.00	Q1
CA-IS3762HB	SSOP16	B	16	2500	330	12.4	6.40	5.40	2.10	8.00	12.00	Q1
CA-IS3763LB	SSOP16	B	16	2500	330	12.4	6.40	5.40	2.10	8.00	12.00	Q1
CA-IS3763HB	SSOP16	B	16	2500	330	12.4	6.40	5.40	2.10	8.00	12.00	Q1

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