

#### CA-IF1044A-Q1 Version 0.75,2024/04/18

## CA-IF1044Ax Automotive CAN Transceiver with Standby Mode

11

#### 1. Features

- Meets the ISO 11898-2:2016 and ISO 11898-5:2007 physical layer standards
- Support classic CAN and 5 Mbps CAN FD
- Low-Current Standby Mode: 7.5uA
- Ideal passive behavior when unpowered
  - Bus and logic terminals are high impedance (no load)
  - Power up/down with glitch free operation on bus and RXD output
- The I/O voltage range supports 3.3V and 5V microcontrollers (MCU)
- Integrated protection increases robustness
  ±58V fault-tolerant CANH and CANL
  - ±30V extended common-mode input range (CMR)
  - Undervoltage protection on V<sub>CC</sub> and V<sub>IO</sub> supply terminals
  - Transmitter dominant timeout prevents lockup, data rates down to 4 kbps
  - Thermal shutdown protection (TSD)
- Typical loop delay: 110ns
- Common-mode input voltage of the receiver: ±30V
- –55°C to 150°C Junction Temperatures Range
- Available in SOIC8 and DFN8 packages
- AEC-Q100 Qualified and –40°C to 125°C Grade 1 operating temperature range

#### 2. Applications

- Body electronics
- Power system
- Automotive gateway
- Advanced driver assistance systems (ADAS)
- In-vehicle infotainment system
- Thermal management module
- On-board sensor module

#### 3. General Description

The CA-IF1044Ax devices are control area network (CAN) transceivers with integrated protection for industrial and

automotive applications. These devices are designed for using in CAN FD (flexible data rate) networks up to 5 Mbps data rate and feature ±42V extended fault protection on the CAN bus for equipment where overvoltage protection is required. This family of CAN transceivers also incorporate an input common-mode range(CMR) of ±30V, exceeding the ISO 11898 specification of -2V to +7V, well suited for applications where ground planes from different systems are shifting relative to each other.

The CA-IF1044Ax series devices include a dominant timeout to prevent bus lockup caused by controller error or by a fault on the TXD input. When the TXD remains in the dominant state (low) for longer than  $t_{DOM}$ , the driver is switched to the recessive state, releasing the bus and allowing other nodes to communicate. The transceivers feature a STB pin for two modes of operation: normal high-speed mode and standby mode for low current consumption. Also, the CA-IF1044AVx devices in this family provide low level translation to simplify the interface with 5V, or 3.3V low voltage CAN controllers.

The CA-IF1044Ax family of devices is available in a standard 8-pin narrow-body SOIC package and small size 8-pin DFN package, operates over the -55°C to +150°C junction temperature range. AEC-Q100 qualified for automotive applications.

#### Table 3-1. Device Information

Part number	Package	Package size(NOM)
CA-IF1044AS-Q1	SOIC8	4.9mm x 3.9mm
CA-IF1044AVS-Q1	30108	4.9mm x 3.9mm
CA-IF1044AD-Q1	DFN8	3.0mm x 3.0mm
CA-IF1044AVD-Q1	DENO	3.0mm x 3.0mm
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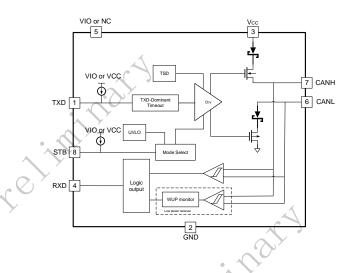
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#### Simplified Block Diagram



## en Anningt **Ordering Information** 4.

#### Table 4-1. Ordering Information

Part Number	Features	Package	
CA-IF1044AS-Q1	Pin 5 = NC	SOIC8	
CA-IF1044AVS-Q1	With low level translation, Pin 5 = $V_{IO}$	SOIC8	_
CA-IF1044AD-Q1	Pin 5 = NC	DFN8	_
CA-IF1044AVD-Q1	With low level translation, Pin 5 = V <sub>I0</sub>	DFN8	
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### CA-IF1044A-Q1 Version 0.75,2025/04/18

## **Table of Contents**

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1.	Featu	res	1
2.	Applic	ations	1
3.	Gener	al Description	
4.		ing Information	
5.	Revisi	on History	3
6.	Pin Co	nfiguration and Functions	4
7.	Specif	ications	5
	7.1.	Absolute Maximum Ratings	
	7.2.	ESD Ratings	5
	7.3.	Recommended Operating Conditions	5
	7.4.	Thermal Information	5
	7.5.	Electrical Characteristics	6
	7.6.	Switching Characteristics	8
8.	Param	eter Measurement Information	9
9.	Detail	ed Description	13
	9.1.	CAN Bus Status	13 🔨
	9.2.	Receiver	13
•	9.3.	Transmitter	14

	9.4.	Prot	ection Functions	
		9.4.1.	Undervoltage Lockout	15
		9.4.2.	Fault Protection	16
		9.4.3.	Thermal Shutdown	
		9.4.4.	Current-Limit	16
		9.4.5.	Transmitter-Dominant Timeout	
	9.5.	Unp	owered Device	17
	9.6.	Floa	ting Terminals	17
	9.7.	Ope	rating Mode	17
		9.7.1.	Normal Mode	17
		9.7.2.	Standby and Wake-up	17
10.		Applic	ation Information	18
11.		Packa	ge Information	20
12.	(	<b>N</b> .Z	- ring Temperature (reflow) Profile	
13.	$\sim$	/	and Reel Information	
	Ý	-		
14.		Apper	ndix	24
15.		Impor	tant Statement	25

#### **Revision History** 5.

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#### CA-IF1044A-Q1 Version 0.75,2025/04/18

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#### Proliminary 6. **Pin Configuration and Functions** 25° STB TXD 8 1 CANH GND 2 7 vcc CANL 3 6 RXD 4 VIO or NC 5 Figure 6-1. CA-IF1044Ax Pin Configuration

#### Table 6-1. CA-IF1044Ax Pin Configuration and Description

	Pi	n #	-1		
	CA-IF1044S-Q1 CA-IF1044D-Q1	CA-IF1044VS-Q1 CA-IF1044VD-Q1	Pin Name	Туре	Description
		1	TXD	Digital I/O	Transmit Data Input, Drive TXD high to set the driver in the recessive state. Drive TXD low to set the driver in the dominant state. TXD is a CMOS/TTL compatible input from a CAN controller with an internal pull-up to $V_{CC}$ or $V_{IO}$ .
	2	2	GND	GND	Ground.
	3	3	V <sub>CC</sub>	Power	+5V Supply Voltage. Bypass $V_{CC}$ to GND with an at least $0.1\mu$ F capacitor.
	4	4	RXD	Digital I/O	Receive Data Output, RXD is LOW for dominant bus state and HIGH for recessive bus state. RXD is a CMOS/TTL compatible output from the physical bus lines CANH and CANL.
	5	-	NC	NC	No connect.
	-	5	Vio	Power	Logic Supply Input. V <sub>IO</sub> is the logic supply voltage for the input/output between the CAN transceiver and controller. V <sub>IO</sub> allows full compatibility from +1.8V to +5.5V logic on all digital lines. Bypass to GND with a 0.1 $\mu$ F capacitor. Connect V <sub>IO</sub> to V <sub>CC</sub> for 5V logic compatibility.
	6	6	CANL	Bus I/O	CAN bus line low.
	7	7	CANH	Bus I/O	CAN bus line high.
	8	8	STB	Digital I/O	Standby Mode. A logic-high on STB pin or leave it open to select the standby mode. In standby mode, the transceiver is not able to transmit data and the receiver is in low-power mode. A logic-low on STB pin puts the transceiver in normal operating mode.
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#### CA-IF1044A-Q1 Version 0.75,2025/04/18

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7. **Specifications** 

#### 7.1. **Absolute Maximum Ratings**

e - <sup>1</sup>		Y		C 7
	PARAMETER	MIN	MAX	UNIT
V <sub>cc</sub>	5V Bus Supply Voltage Range	-0.3	7	$\mathcal{O}$ v
V <sub>IO</sub>	Logic Supply Voltage Range	-0.3	7	V
V <sub>BUS</sub>	CAN Bus I/O voltage range (CANH,CANL)	-42	42	V
V(DIFF)	Max differential voltage between CANH and CANL	-42	42	V
V <sub>(Logic_Input)</sub>	Logic input terminal voltage range (TXD, S)	-0.3	+7 and < VIO+0.3	V
V <sub>(Logic_Output)</sub>	Logic output terminal voltage range (RXD)	-0.3	+7 and < VIO+0.3	V
I <sub>O(RXD)</sub>	RXD (receiver) terminal output current	-8	8	mA
TJ	Virtual junction temperature range	-55	150	°C
T <sub>STG</sub>	Storage temperature range	-65	150	°C
Noto				

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Note:

The stresses listed under "Absolute Maximum Ratings" are stress ratings only, not for functional operation condition. Exposure to absolute 1. maximum rating conditions for extended periods may cause permanent damage to the device.

#### 7.2. **ESD** Ratings

Parameters	TEST CO	TEST CONDITIONS		
CA-IF1044Ax	~ ^			
HBM <sup>1</sup> ESD	All pins	/	±8000	V
CDM ESD	All pins		±2000	V
System Level ESD	CAN bus terminals (CANH, CANL) to GND	IEC 61000-4-2: unpowered contact discharge.	±6000 <sup>2</sup>	V
Note: 1. Per AEC Q100-002, HBM s 2. Testing on System Board L	tressing shall be in accordance with the ANSI/	/ESDA/JEDEC JS-001 specification.	JOI .	

Testing on System Board Level.

#### 7.3. **Recommended Operating Conditions**

	PARAMETER			TYP MAX	UNIT
V <sub>cc</sub>	Supply Voltage Range		4,5	5.5	V
V <sub>IO</sub>	Logic Supply Voltage Range		3.0	5.5	V
I <sub>OH(RXD)</sub>	RXD terminal high level output current		-2		mA
I <sub>OL(RXD)</sub>	RXD terminal low level output current			2	mA
7.4. Thern	nal Information	4			
	Thermal Metric		DFN8	SOIC8	UNIT
R <sub>0JA</sub>	Junction to Ambient	~0,	40	170	°C/W

#### Thermal Information 7.4.

7.4.	Thermal Information	A			. 11
	Thermal Metric	DFN8		SOIC8	UNIT
R <sub>0JA</sub>	Junction to Ambient	40		170	°C/W
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#### 7.5. **Electrical Characteristics**

## Over recommended operating conditions, $T_A = -40^{\circ}$ C to 125°C (unless otherwise noted).

	PARAMETER	TEST CONDITIONS	MIN	ТҮР	MAX	UNI
POWER	7					2
$\sim 0^{\prime}$		TXD=0V, STB=0V, $R_{L}$ = 60 $\Omega$ (dominant)		45	70	mA
		see Figure 8-1			<u>y</u>	
		TXD=0V, STB=0V, RL=50 Ohm (dominant) see Figure 8-1		50	80	mA
~		TXD=0V, STB=0V, CANH=-12V (dominant)				
		see Figure 8-1		Z) ×	110	mA
l <sub>cc</sub>	5V Supply Current	TXD=V <sub>cc</sub> or V <sub>10</sub> , STB=0V, RL=50 Ohm (recessive)	5	4	7	
		see Figure 8-1				m/
		TXD = STB = V <sub>IO</sub> (standby, CA-IF1044Vx), RL = 50 Ohm		0.5	5	μA
	$\sim \gamma$	see Figure 8-1		0.5	5	
		TXD = STB = $V_{CC}$ (standby, CA-IF1044S-Q1/CA-IF1044D-		7.5	17	μA
		Q1), RL = 50 Ohm, see Figure 8-1				
10	I/O Supply Current	TXD = 0V, STB = 0V, RXD open (CA-IF1044Vx)		160	300	μA
10	., e capp., ea	TXD= V <sub>IO</sub> , STB= V <sub>IO</sub> , RXD open (CA-IF1044Vx)		7	12	μ/
/ <sub>uv_vcc</sub>	V <sub>cc</sub> UVLO Threshold	Rising		4.1	4.45	V
uv_vcc	V <sub>cc</sub> UVLO Threshold	Falling	3.7	3.9	4.25	V
/HYS	V <sub>CC</sub> UVLO Hysteresis voltage	Hysteresis voltage		200		m
	V <sub>IO</sub> UVLO Voltage(CA-IF1044AVS-					
~	Q1)	Rising		2.65	2.85	v
	/V <sub>CC_sd</sub> UVLO Voltage(CA-	Nishig		2.05	2.05	v
/uv_ <sub>vio</sub> /	IF1044AS-Q1)					
uv_vcc_sd	V <sub>IO</sub> UVLO Voltage(CA-IF1044AVS-	$\sim$		1		
	Q1)	Falling		25	2.7	v
	/V <sub>CC_sd</sub> UVLO Voltage(CA-				2.7	
	IF1044AS-Q1)			0		
	V <sub>10</sub> UVLO Hysteresis voltage (CA-			/		
/HYS(UV_VIO/	IF1044AVS-Q1)	Hysteresis voltage	$\cdot \circ$	150		m
'CC_sd)	/V <sub>CC_sd</sub> UVLO Hysteresis voltage (CA-		$\sim$			
	IF1044AS-Q1)		ý í			
	RFACE (Mode select input, STB)		07141			
ин	High-level input voltage	$\sim$	0.7xV <sub>cc</sub> <sup>1</sup>		0.01/ 1	V
/ <sub>IL</sub>	Low-level input voltage				0.3Xv <sub>CC</sub> <sup>1</sup>	V
IH	High-level input leakage current	$STB = V_{CC} = V_{IO} = 5.5V$	-2		2	μ/
L	Low-level input leakage current	STB = 0V, V <sub>CC</sub> = V <sub>IO</sub> = 5.5V	-20		-2	μ
ek(off)	Unpowered leakage current	STB=5.5V, V <sub>CC</sub> = V <sub>IO</sub> = 0V	-1		1	μ
	RFACE (CAN transmit data input, TX		0 = 1			$\mathbf{e}$
ин	High-level input voltage		0.7Xv <sub>CC</sub> <sup>1</sup>		A	V
/ <sub>IL</sub>	Low-level input voltage				$0.3 X v_{Cc}^{1}$	ν v
н	High-level input leakage current	$TXD = V_{CC} = V_{IO} = 5.5V$	-2.5	0	~ T	μ
IL	Low-level input leakage current	$TXD = 0V, V_{CC} = V_{10} = 5.5V$	-200	-100	-60	μ/
ek(off)	Unpowered leakage current	$TXD = 5.5V, V_{CC} = V_{IO} = 0V$	110	160	240	μ
	Input capacitance	$V_{IN} = 0.4 \text{*sin}(4E6 \pi \text{*t}) + 2.5V$		5		pl
i	FACE (CAN receive data output, RXD)		1			V
Ci OGIC INTER		lo = -2mA	0.8Xv <sub>CC</sub> <sup>1</sup>			
о <b>GIC INTER</b> И <sub>ОН</sub>	High-level output voltage	lo = -2mA lo = +2mA	0.8Xv <sub>CC</sub> <sup>1</sup>	<u> </u>	0.2Xvcc1	v
і <b>OGIC INTER</b> Ион Иоц	High-level output voltage	lo = +2mA	4	0	0.2Xv <sub>CC</sub> <sup>1</sup>	-
Сі OGIC INTER Ион Иоц ek(off)	High-level output voltage Low-level output voltage Unpowered leakage current		0.8Xv <sub>cc</sub> <sup>1</sup>	0	0.2Xv <sub>CC</sub> <sup>1</sup>	-
Сі OGIC INTER /он /оL lek(off) Dver-temper	High-level output voltage Low-level output voltage Unpowered leakage current rature protection	lo = +2mA	4			μ/
Сі OGIC INTER / <sub>ОН</sub> / <sub>OL</sub> lek(off)	High-level output voltage Low-level output voltage Unpowered leakage current	lo = +2mA	4	0 185 15		۷ 44 °C



## **Electrical Characteristics (continued)**

## Over recommended operating conditions, $T_A = -40^{\circ}$ C to 125°C (unless otherwise noted)

Over recom	mended operating conditions, $T_A =$	–40°C to 125°C (unless otherwise noted).			1
•	PARAMETER	TEST CONDITIONS	MIN 1	ΎΡ ΜΑΧ	UNIT
CAN BUS DR	IVER			$\bigcirc$	X
V <sub>Q(DOM)</sub>	Bus output voltage (dominant)	TXD = low, STB = 0V, $R_L$ =50 -65 $\Omega$ , CL=open, RCM=open, CANH, see Figure 8-1	2.75	4.5	V
		TXD = low, STB = 0V, $R_L$ = 50 -65 $\Omega$ , CL=open, RCM=open, CANL, see Figure 8-1	0.5	2.25	V
7		TXD = low, STB=0V, RL=45-50 Ohm, RCM open, see Figure 8-1	1.4	3.3	V
V OD(DOM)	Bus output differential voltage (dominant)	TXD = low, STB=0V, RL=50-65 Ohm, RCM open, see Figure 8-1	1,5	3.0	V
		TXD = low, STB = 0V, RL=2240 Ohm, RCM open, see Figure 8-1	1.5	5.0	V
V <sub>O(REC)</sub>	Bus output voltage (recessive)	TXD=V <sub>CC</sub> or V <sub>10</sub> , V <sub>CC</sub> = V <sub>10</sub> , STB=0V, RL=open, RCM=open, CANH,CANL, see Figure 8-1	2 0.5	«V <sub>cc</sub> 3	V
M	Bus output differential voltage	TXD = high, STB=0V, $R_{L}$ =60 $\Omega$ , CL=open, RCM=open, see Figure 8-1	-120	12	mV
V <sub>OD(REC)</sub>	(recessive)	TXD = high, STB=0V, no load, CL=open, RCM=open, see Figure 8-1	-50	50	mV
		STB=V <sub>IO</sub> , RL open, RCM open, CANH	-0.1	0.1	V
V <sub>O(STB)</sub>	Bus output at standby mode	STB= V <sub>10</sub> , RL open, RCM open, CANL	-0.1	0.1	V )
	1	STB= V <sub>IO</sub> , RL open, RCM open, CANH-CANL	-0.2	0.2	V
~	3	TXD = low, STB=0V, CANL open, V CANH= -5V to 40V, see	-		
	Short-circuit current (dominant)	Figure 8-7	115		m۸
los(ss_dom)	Short-circuit current (dominant)	TXD = low, STB=0V, CANH open, V <sub>CANL</sub> = -5V to 40V, see Figure 8-7		115	mA
IOS(SS_rec)	Short-circuit current (recessive)	TXD = high, STB=0V , $V_{BSU}$ = CANH = CANL = -27V to 32V, see Figure 8-7	-6	6	mA
V <sub>SYM</sub>	Transient symmetry (dominant or recessive)	$R_L$ = 60 Ω, STB=0V, $R_{CM}$ open, $C_{split}$ =4.7nF, RCM open , TXD = 250kHz, 1MHz, 2.5M Hz, see Figure 8-1	0.9	1.1	V/V
V <sub>SYM_DC</sub>	DC Output symmetry (dominant or recessive)	RL =60 Ω, STB = 0, $R_{CM}$ open, see Figure 8-1	-0.4	0.4	V
CAN RECEIV	ER A		Y	4	
V <sub>CM</sub>	Common-mode input range	Regular mode and standby mode, RXD output valid, see Figure8-2	-30	+30	V
	Input differential threshold voltage at	STB = 0V, $V_{CM}$ from -20V to 20V, see Figure 8-2	500	900	mV
V <sub>IT</sub>	normal mode	STB=0V, V <sub>CM</sub> from -30V to 30V, see Figure 8-2	400	1000	mV
V <sub>IT(STB)</sub>	Input differential threshold at standby mode	STB = high, Vcm from -12V to 12V(3≤Vio≤5.5V, no VIO ignore), see Figure8-2	400	1150	mV
	Input differential threshold voltage at	STB=0V, V <sub>CM</sub> from -20V to 20V, see Figure 8-2	0.9	9	
V <sub>DIFF_D</sub>	normal mode (dominant)	STB=0V, V <sub>CM</sub> from -30V to 30V, see Figure 8-2	1	9	N Y
	Input differential threshold voltage at	STB=0V, V <sub>CM</sub> from -20V to 20V, see Figure 8-2	-4	0.5	V.
V <sub>DIFF_R</sub>	normal mode (recessive)	STB=0V, V <sub>CM</sub> from -30V to 30V, see Figure 8-2	-4	0.4	V
V <sub>DIFF_D(STB)</sub>	Input differential threshold voltage at standby mode (dominant)	STB=high, see Figure 8-2	1.15	9	V
V <sub>DIFF_R(STB)</sub>	Input differential threshold voltage at standby mode (recessive)	STB=high, see Figure 8-2	-4	0.4	v
V <sub>DIFF</sub> (HYST)	Input differential threshold hysteresis	normal mode	100	)	mV
R <sub>IN</sub>	CANH/CANL input resistance	) TXD = high, STB = 0, V <sub>CM</sub> = -30V to 30V	10	40	kΩ
R <sub>DIFF</sub>	Differential input resistance	$TXD = high, STB = 0, V_{CM} = -30V \text{ to } 30V$	20	80	kΩ
RDIFF (M)	Input resistance matching	V <sub>CANH</sub> = V <sub>CANL</sub> =5V	-2	2	%
	Input Leakage Current	$V_{IO} = V_{CC} = 0V, V_{CANH} = V_{CANL} = 5V$		8	μA
C <sub>IN</sub>	Input capacitance	CANH or CANL to GND, TXD=Vcc, Vio = Vcc, STB = 0	·	24	μ <del>Λ</del> pF
	Differential input capacitance	CANH to CANL, TXD = High		12	pF
C <sub>IN_DIFF</sub>	Bincientiai input capacitance			12	۲F

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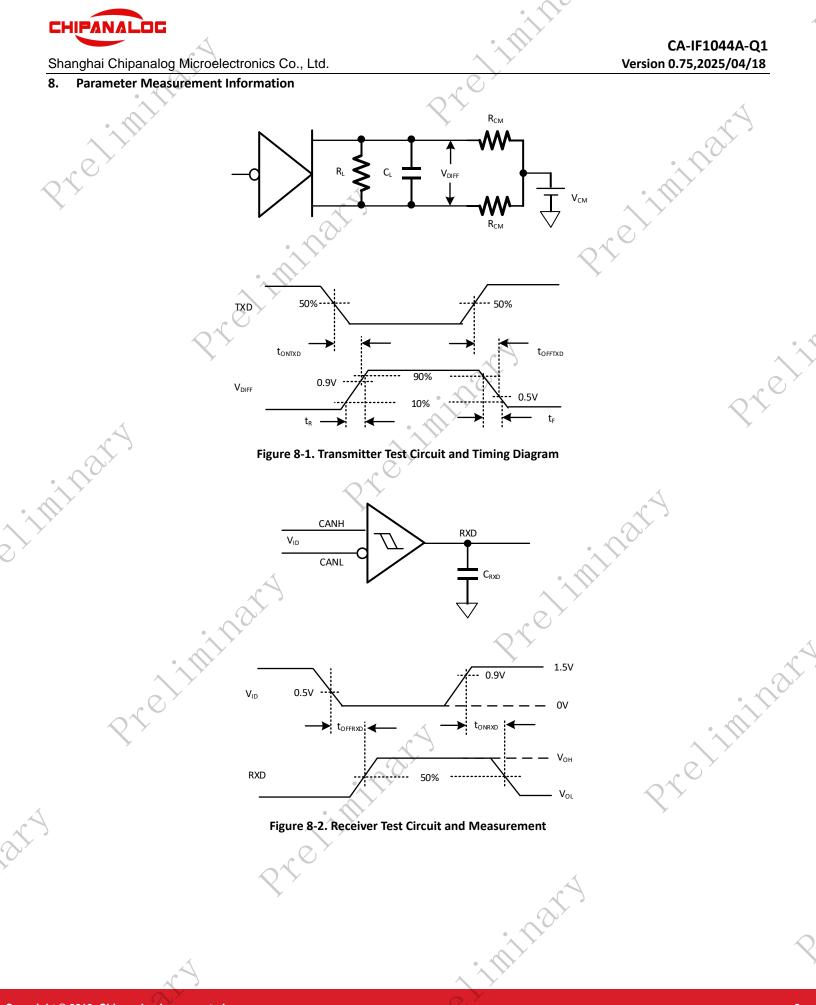
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#### 7.6. **Switching Characteristics**

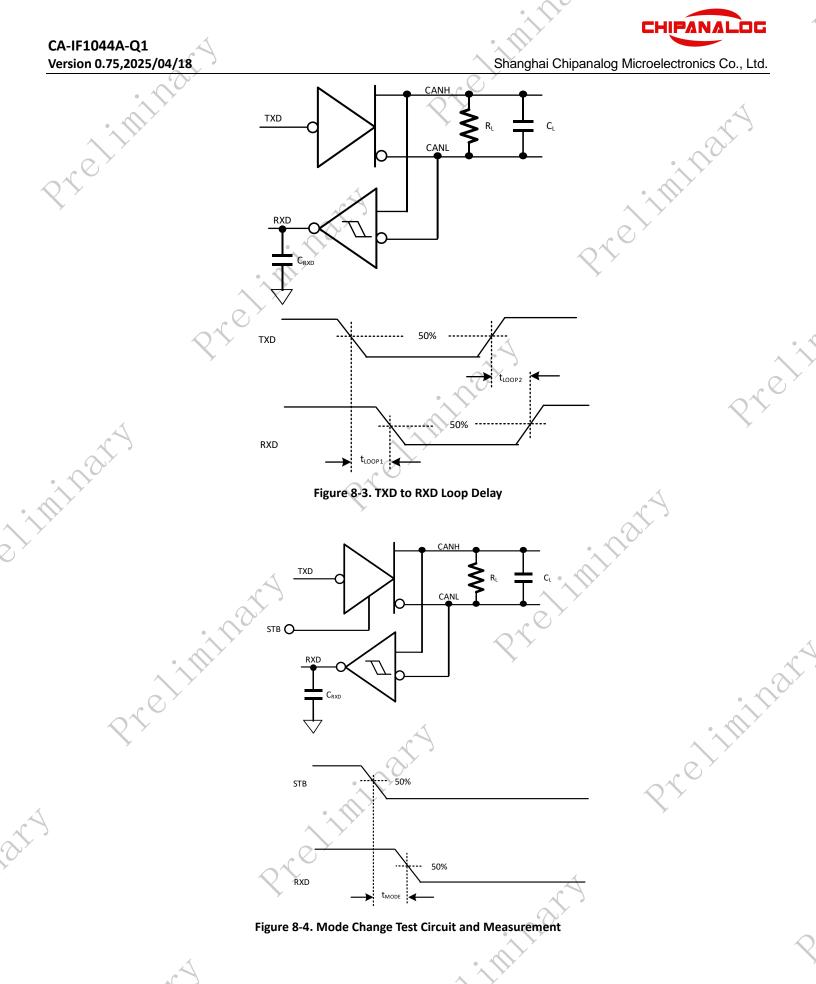
CONTROMTXD propagation delay (recessive to dominant)STB = 0, R_1=600, C_1=100pF, see Figure 8-138nsCONTROMTXD propagation delay (dominant to recessive)STB = 0, R_1=600, C_1=100pF, see Figure 8-145nsCONTROMTXD-dominant TimeoutR_=600, C_1=00pF, see Figure 8-52.56.810msRECEIVERSTB = 0, C_{RXD}=15pF, see Figure 8-273nsRECEIVERSTB = 0, C_{RXD}=15pF, see Figure 8-273nsRECEIVERGomman to recessive)STB = 0, C_{RXD}=15pF, see Figure 8-275nsRECEIVERTotal loop delay, driver input (TXD) to receiver output (RXD), recessive to dominantR_=600, C_1=100pF, see Figure 8-3110185nsDEVICETotal loop delay, driver input (TXD) to receiver output (RXD), dominant to receiver output (RXD), dominant to receiver output (RXD), dominant to receiver output (RXD), dominant to see Figure 8-41245 $\mu$ sTotal loop delay, or from standby to normal standby or from standby to normalsee Figure 8-40.51.8 $\mu$ sTwe normalStB = 0, R_=600, C_1=100pF, C_RXD =15pF, see Figure 8-40.810msTotal loop 20 onsSTB = 0, R_=600, C_1=100pF, C_RXD =15pF, see155210nsMarcotBit time on CAN bus output pins with tarrxD) = 500 nsSTB = 0, R_=600, C_1=100pF, C_RXD =15pF, see155210nsBit time on RXD output pins with tarrxD) = 200 nsSTB = 0, R_=600, C_1=100pF, C_RXD =15pF, see120220nsBit time on RXD output pins	DNIXOTXD propagation delay (recessive to dominant)STB = 0, R <sub>1</sub> =600, C <sub>1</sub> =100pF, see Figure 8-138nsOPTRIDTXD propagation delay (dominant to recessive)STB = 0, R <sub>1</sub> =600, C <sub>1</sub> =100pF, see Figure 8-145nsECELVERTXD-dominant TimeoutR <sub>1</sub> =600, C <sub>1</sub> =100pF, see Figure 8-52.56.810msECELVERSTB = 0, C <sub>RXD</sub> =15pF, see Figure 8-273nsCMIRDRXD propagation delay (recessive to dominant)STB = 0, C <sub>RXD</sub> =15pF, see Figure8-275nsECELVERTotal loop delay, driver input (TXD) to receiver output (RXD), dominant to receiver output RXD), dominant to receiver output RXD, dominant to receiver outpu		PARAMETER	TEST CONDITIONS	MIN	ТҮР	MAX 🔿	
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RECEIVERRXD propagation delay (recessive to dominant)STB = 0, $C_{RXD}$ =15pF, see Figure8-273nsRXD Propagation delay (dominant to recessive)STB = 0, $C_{RXD}$ =15pF, see Figure8-275nsDEVICETotal loop delay, driver input (TXD) to receiver output (RXD), recessive to dominantRL=600, CL=100pF, see Figure 8-3110185nsItioop2Total loop delay, driver input (TXD) to receiver output (RXD), recessive to dominantRL=600, CL=100pF, see Figure 8-3110185nsItioop2Total loop delay, driver input (TXD) to receiver output (RXD), dominant to recessiveRL=600, CL=100pF, see Figure 8-3115185nsItioop2Total loop delay, driver input (TXD) to recessivesee Figure 8-40.51.8µsItioop2Total loop delay, driver input (TXD) to recessivesee Figure 8-40.51.8µsItioop2Filter time for a valid wake-up patternsee Figure 8-40.51.8µsItione on CAN bus output pins with tar(txD) = 200 nsSTB = 0, RL=600, CL=100pF, CRXD =15pF, see Figure 8-6135210nsItiotheuaBit time on CAN bus output pins with tar(txD) = 200 nsSTB = 0, RL=600, CL=100pF, CRXD =15pF, see Figure 8-6120220nsItiot(rod)Bit time on RXD output pins with tar(txD) = 200 nsSTB = 0, RL=600, CL=100pF, CRXD =15pF, see Figure 8-6120220nsItiot(rod)Bit time on RXD output pins with tar(txD) = 500 nsSTB = 0, RL=600, CL=100pF, CRXD =15pF, see Fi	<b>EECEIVER</b> ONENDRXD propagation delay (recessive to dominant)STB = 0, $C_{RXD}=15pF$ , see Figure8-273nsOFFRUDRXD Propagation delay (dominant to recessive)STB = 0, $C_{RXD}=15pF$ , see Figure8-273ns <b>DEVICE</b> Total loop delay, driver input (TXD) to receiver output (RXD), recessive to dominantR <sub>L</sub> =60 $\Omega$ , C <sub>L</sub> =100pF, see Figure 8-3110185ns <b>DEVICE</b> Total loop delay, driver input (TXD) to receiver output (RXD), dominant to recessiveR <sub>L</sub> =60 $\Omega$ , C <sub>L</sub> =100pF, see Figure 8-3110185ns <b>Deop2</b> Total loop delay, driver input (TXD) to recessiveRL=60 $\Omega$ , C <sub>L</sub> =100pF, see Figure 8-3115185ns <b>Mode</b> Mode change time, from normal to standby or from standby to normalsee Figure 8-40.51.8µs <b>WE</b> , FILTEROUTBus wake-up timeoutsee Figure 8-40.810ms <b>D TIMING</b> STB = 0, R <sub>L</sub> =60 $\Omega$ , C <sub>L</sub> =100pF, C <sub>RXD</sub> =15pF, see Figure 8-6135530ns <b>D TIMING</b> STB = 0, R_L=60 $\Omega$ , C <sub>L</sub> =100pF, C <sub>RXD</sub> =15pF, see Figure 8-6135210ns <b>D TIMING</b> STB = 0, R_L=60 $\Omega$ , C <sub>L</sub> =100pF, C <sub>RXD</sub> =15pF, see Figure 8-6120220ns <b>D TIMING</b> STB = 0, R_L=60 $\Omega$ , C <sub>L</sub> =100pF, C <sub>RXD</sub> =15pF, see Figure 8-6120220ns <b>D TIMING</b> STB = 0, R_L=60 $\Omega$ , C <sub>L</sub> =100pF, C <sub>RXD</sub> =15pF, see Figure 8-6120220ns <b>D TIMING</b> STB = 0, R_L=60 $\Omega$ , C <sub>L</sub> =100PF, C <sub>RXD</sub> =15pF, see Figure 8-6120220ns <b>D TIMING</b> <td>t<sub>DOM</sub></td> <td>TXD-dominant Timeout</td> <td>R<sub>L</sub>=60 Ω, C<sub>L</sub> open, see Figure 8-5</td> <td>2.5</td> <td>6.8</td> <td>10</td> <td>ms</td>	t <sub>DOM</sub>	TXD-dominant Timeout	R <sub>L</sub> =60 Ω, C <sub>L</sub> open, see Figure 8-5	2.5	6.8	10	ms
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CorFRADRXD Propagation delay (dominant to recessive)STB = 0, $C_{RXD} = 15pF$ , see Figure8-275nsDEVICETotal loop delay, driver input (TXD) to receiver output (RXD), recessive to dominant $R_L = 60\Omega$ , $C_L = 100pF$ , see Figure 8-3110185nsTotal loop delay, driver input (TXD) to receiver output (RXD), dominant to recessive $R_L = 60\Omega$ , $C_L = 100pF$ , see Figure 8-3110185nsTotal loop delay, driver input (TXD) to receiver output (RXD), dominant to recessive $R_L = 60\Omega$ , $C_L = 100pF$ , see Figure 8-3115185nsMode change time, from normal to standby or from standby to normalsee Figure 8-40.51.8 $\mu$ sTwe, FLITERFilter time for a valid wake-up patternsee Figure 8-40.810msFW, FLITERBit time on CAN bus output pins with tarrixoj = 500 nsSTB = 0, $R_L = 60\Omega$ , $C_L = 100pF$ , $C_{RXD} = 15pF$ , see155210nsBit time on RXD output pins with tarrixoj = 200 nsSTB = 0, $R_L = 60\Omega$ , $C_L = 100pF$ , $C_{RXD} = 15pF$ , see120220nsHold(x)Bit time on RXD output pins with tarrixoj = 200 nsSTB = 0, $R_L = 60\Omega$ , $C_L = 100pF$ , $C_{RXD} = 15pF$ , see120220nsHold(x)Bit time on RXD output pins with tarrixoj = 200 nsSTB = 0, $R_L = 60\Omega$ , $C_L = 100pF$ , $C_{RXD} = 15pF$ , see120220nsHold(x)Bit time on RXD output pins with tarrixoj = 200 nsSTB = 0, $R_L = 60\Omega$ , $C_L = 100pF$ , $C_{RXD} = 15pF$ , see120220nsHold(x)Bit time on RXD output pins with<	OFFRIO    RXD Propagation delay (dominant to recessive)    STB = 0, C <sub>RXD</sub> =15pF, see Figure 8-2    75    ns      DEVICE    Total loop delay, driver input (TXD) to receiver output (RXD), recessive to dominant    R <sub>1</sub> =60Ω, C <sub>1</sub> =100pF, see Figure 8-3    110    185    ns      Isoop2    Total loop delay, driver input (TXD) to receiver output (RXD), dominant to recessive    R <sub>1</sub> =60Ω, C <sub>1</sub> =100pF, see Figure 8-3    110    185    ns      MODE    Mode change time, from normal to standby or from standby to normal    see Figure 8-4    0.5    1.8    µs      WK_FILTER    Filter time for a valid wake-up pattern    see Figure 8-4    0.8    10    ms      D TIMING    Bit time on CAN bus output pins with tar(trxo) = 500 ns    STB = 0, R <sub>1</sub> =60Ω, C <sub>1</sub> =100pF, C <sub>RXD</sub> =15pF, see Figure 8-6    155    210    ns      bitchust    Bit time on RXD output pins with tar(trxo) = 200 ns    STB = 0, R <sub>1</sub> =60Ω, C <sub>1</sub> =100pF, C <sub>RXD</sub> =15pF, see Figure 8-6    120    220    ns      bit(nd)    Bit time on RXD output pins with tar(trxo) = 200 ns    STB = 0, R <sub>1</sub> =60Ω, C <sub>1</sub> =100pF, C <sub>RXD</sub> =15pF, see Figure 8-6    120    220    ns      bit(nd)    Bit time on RXD output pins with tar(trxo) = 200 ns    STB = 0, R <sub>1</sub> =60Ω, C <sub>1</sub> =100pF, C <sub>RXD</sub> =15pF, see Figure 8-6    120    220    ns <td></td> <td></td> <td>STB = 0, <math>C_{RXD}</math>=15pF, see Figure8-2</td> <td></td> <td>73</td> <td></td> <td>ns</td>			STB = 0, $C_{RXD}$ =15pF, see Figure8-2		73		ns
Image: constraint of the constr	Image: constraint of the constr							
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termtermFigure 8-6trecReceiver timing symmetry with $t_{BIT(TXD)}$ STB = 0, $R_L=60\Omega$ , $C_L=100$ pF, $C_{RXD}=15$ pF, see Figure 8-6-6540nsReceiver timing symmetry with $t_{BIT(TXD)}$ STB = 0, $R_L=60\Omega$ , $C_L=100$ pF, $C_{RXD}=15$ pF, see Figure 8-6-6540ns	tBIT(TXD) = 200 ns  Figure 8-6    Receiver timing symmetry with tBIT(TXD) = 500ns  STB = 0, RL=60Ω, CL=100pF, CRXD =15pF, see Figure 8-6  -65  40  ns    Receiver timing symmetry with tBIT(TXD)  STB = 0, RL=60Ω, CL=100pF, CRXD =15pF, see  -65  40  ns		Bit time on RXD output pins with	STB = 0, R <sub>L</sub> =60Ω, C <sub>L</sub> =100pF, C <sub>RXD</sub> =15pF, see	120	-		-
Figure 8-6  -65  40  ns    Receiver timing symmetry with t <sub>BIT(TXD)</sub> STB = 0, RL=60Ω, CL=100pF, CRXD =15pF, see  40  ns	rec  = 500ns  Figure 8-6  -65  40  ns    Receiver timing symmetry with t <sub>BIT(TXD)</sub> STB = 0, RL=60Ω, CL=100pF, CRXD =15pF, see  45  45	t <sub>bit(rxd)</sub>		Figure 8-6	120		220	ns
= 500ns  Figure 8-6    Receiver timing symmetry with t <sub>BIT(TXD)</sub> STB = 0, RL=60Ω, CL=100pF, CRXD =15pF, see	= 500ns  Figure 8-6    Receiver timing symmetry with t <sub>BIT(TXD)</sub> STB = 0, RL=60Ω, CL=100pF, CRXD =15pF, see		Receiver timing symmetry with tBIT(TXD)	STB = 0, R <sub>L</sub> =60Ω, C <sub>L</sub> =100pF, C <sub>RXD</sub> =15pF, see	65			
		t <sub>rec</sub>	= 500ns	Figure 8-6	-65		40	ns
Figure 8-6 -45 15 ns	rec = 200ns Figure 8-6 -45 15 ns		Receiver timing symmetry with tBIT(TXD)	STB = 0, R <sub>L</sub> =60Ω, C <sub>L</sub> =100pF, C <sub>RXD</sub> =15pF, see	45			
		t <sub>rec</sub>	= 200ns	Figure 8-6	-45		15	ns
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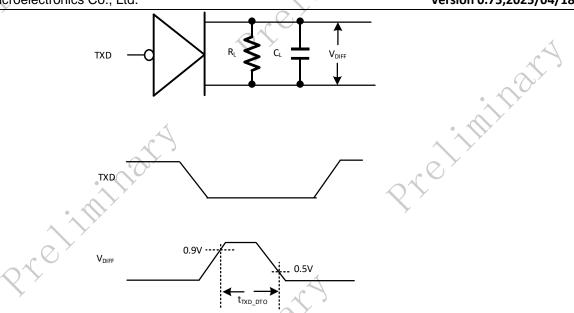


Figure 8-5. Transmitting Dominant Timeout Timing Diagram

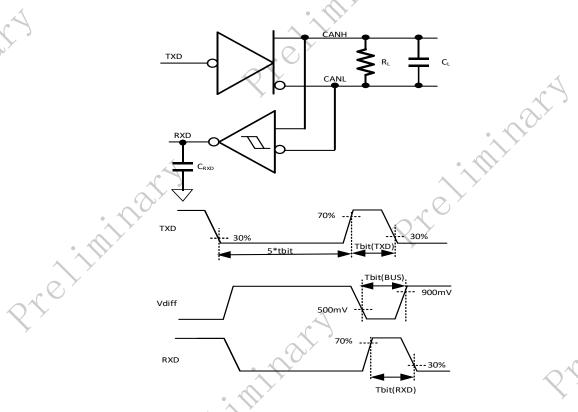
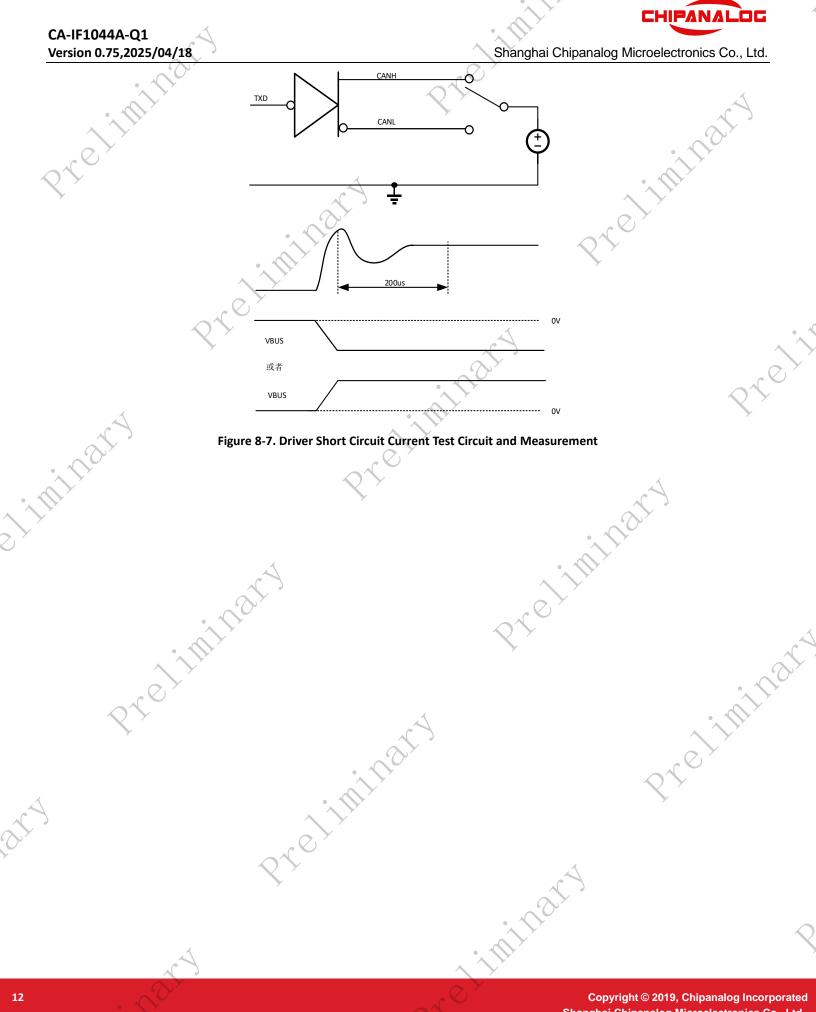


Figure 8-6. CAN FD Timing Parameter Measurement

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#### CA-IF1044A-Q1 Version 0.75,2025/04/18

#### 9. Detailed Description

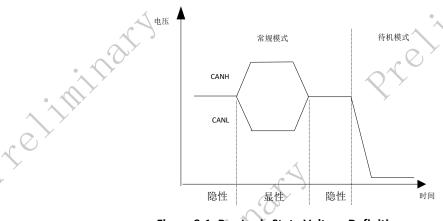
The CA-IF1044Ax family of devices is fault-protected Controller Area Network (CAN) transceiver, meets the ISO11898-2 (2016) high speed CAN physical layer standard. These devices are designed for harsh industrial and automotive applications with a number of integrated robust protection features set that improve the reliability of end equipment. All devices are fault protected up to ±58V for the bus pins, making them ideal for applications where overvoltage protection is required. A common-mode voltage ranges of ±30V enables communication in noisy environments where there are ground plane differences between different systems. Dominant timeout prevents the bus from being blocked by a hung-up microcontroller, and the outputs CANH and CANL are short-circuit current-limited and protected against excessive power dissipation by thermal shutdown circuitry that places the driver outputs in a high-impedance state.

A separate input  $V_{IO}$  allows the CA-IF1044AVx devices to communicate with logic systems down to 3.3V while operating up to a +5V bus supply. This provides a reduced input voltage threshold to the TXD and STB inputs, and provides a logic-high output at RXD compatible with the microcontroller's supply rail. The logic compatibility eliminates external logic level translator and longer propagation delay due to level shifting. Connect  $V_{IO}$  to  $V_{CC}$  to operate with +5V logic systems.

The CA-IF1044Ax devices can operate up to 5Mbps data rate and support CAN FD. However, the maximum data rate is limited by the bus loading, number of nodes, cable length etc. factors, for CAN network design, margin must be given for signal loss across the system and cabling, parasitic loadings, timing, network imbalances, ground offsets and signal integrity thus a practical maximum data rate, number of nodes often lower than the theoretical value.

#### 9.1. CAN Bus Status

The CAN bus has two states: dominant and recessive. In the dominant state (a zero bit, used to determine message priority), CANH-CANL are defined to be logic '0' when the voltage across them is between +1.5V and +3V (higher than 0.9V). In the recessive state (a 1-bit and the state of the idle bus), the driver is defined to be logic '1' when differential voltage is between -120mV and +12mV, or when it is near zero(lower than 0.5V), see Figure 9-1 for the bus logic state voltage definition.





#### 9.2. Receiver

The receiver of CA-IF1044Ax family of devices includes a main receiver to support normal bi-directional communication and a low-power receive channel to monitor the bus line and detect the wakeup event on the bus line during standby mode. In normal operation (STB = low), the main receiver reads the differential input from the bus line (CANH and CANL) and transfers this data as a single-ended output RXD to the CAN controller. The internal comparator senses the difference voltage  $V_{DIFF}$  = ( $V_{CANH}-V_{CANL}$ ), with respect to an internal threshold of 0.7V. If  $V_{DIFF}$  > 0.9V, a logic-low is present on RXD; If  $V_{DIFF}$  < 0.5V, a logichigh is present. The CANH and CANL common-mode range is ±30V in normal mode. See Figure 9-2 for the receiver input bias circuit.

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Drive the STB pin high or leave it open for operating at standby mode, in this case, the main receiver is disabled and the low-power receive channel is enabled. This switches the receiver to a low current and low-speed state. The bus line is monitored by a low-power differential comparator to detect and recognize a wakeup event on the bus line. RXD is logic High until a valid wake-up is received. Once a valid remote wake-up event occurred, RXD transition to logic Low.

RXD is a logic-high when CANH and CANL are shorted or terminated and un-driven in both normal mode and standby mode, see Table 9-1 for more details about the receiver truth table.

Table 9-1. Receiver Truth Table

	•		
DEVICE MODE	$V_{iD} = V_{CANH} - V_{CANL}$	BUS STATE	RXD
	V <sub>ID</sub> ≥0.9V	Dominant	Low
Normal STB = Low	0.5V < V <sub>ID</sub> <0.9V	Indeterminate	Indeterminate
STB - LOW	$V_{ID} \le 0.5V$	Recessive	High
Standby	V <sub>ID</sub> > 1.15V	Dominant	Low if a remote wake event occurred, otherwise output High.
STB = High or open	0.4V < V <sub>ID</sub> <1.15V	Indeterminate	Indeterminate
	$V_{ID} \leq 0.4V$	Recessive	High
Any	Open (V <sub>ID</sub> ≈ 0V)	Open	High

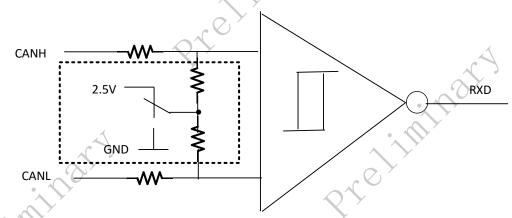


Figure 9-2. Receiver Input/Transmitter Output Bias Circuit

## 9.3. Transmitter

In normal operation (STB = Low), the transmitter converts a single-ended input signal (TXD) from the local CAN controller to differential outputs for the bus lines CANH and CANL. The truth table for the transmitter is provided in Table 9-2. The CA-IF1044x family of devices protects the transmitter output stage against a short-circuit to a positive or negative voltage by limiting the driver current. Thermal shutdown further protects the devices from excessive temperatures that may result from a short circuit. The transmitter returns to normal operation once the short is removed and the junction temperature drops at least the thermal shutdown hysteresis temperature below the thermal shutdown temperature of the device.

Drive the STB pin high for standby mode, the transmitter is disabled and put the bus in high-impedance with internal weak pull-down to ground, see Figure 9-2.



#### CA-IF1044A-Q1 Version 0.75,2025/04/18

Table 9-2. Transmitter Truth Table (When Not Connected to the Bus)

	II	NPUT		ούτι	PUT	
	STB	TXD	TXD LOW TIME	CANH	CANL	BUS STATE
	NY Y	Low	< t <sub>DOM</sub>	High	Low	Dominant
	C Low	Low	> t <sub>DOM</sub>	V <sub>cc</sub> /2	V <sub>cc</sub> /2	Recessive
$\mathcal{Q}$	×	High or Open	x	V <sub>cc</sub> /2	V <sub>cc</sub> /2	Recessive
×	High or Open	Х	x	High-Z	High-Z	Bias to GND

Note: X = Don't care, High-Z = High impedance.

#### 9.4. Protection Functions

#### 9.4.1. Undervoltage Lockout

Both the CA-IF1044AS-Q1/CA-IF1044AD-Q1 and the CA-IF1044AVx family of devices have undervoltage detection on  $V_{CC}$  supply terminal. For CA-IF1044AS-Q1/CA-IF1044AD-Q1, when the supply voltage  $V_{CC}$  is less than  $V_{UN_vCC}$  and greater than  $Vuv_vcc_sd$ , if STB = high, will put the device into low-power standby mode; if STB = low, will put the device into shutdown mode. If the supply voltage  $V_{CC}$  is less than  $Vuv_vcc_sd$ , will put the device into shutdown and disable both receiver and driver, leave the bus in high-impedance. See Table 9-3 for more details.

#### Table 9-3. CA-IF1044AS-Q1/CA-IF1044AD-Q1 Undervoltage Lockout

	V <sub>cc</sub>		BUS OUTPUT	RXD
× 1	> V <sub>UV_VCC</sub>	Normal	Per TXD	Mirrors Bus
	$V_{UV_VCC} > V_{CC} > Vuv_vcc_sd$	Standby	Weak pull-down to GND	According to the wake-up status
	< Vuv_vcc_sd	Protected state	High-Z	High-Z

The CA-IF1044AVx devices also feature undervoltage detection on  $V_{IO}$  supply terminal, if the supply voltage  $V_{IO}$  is less than  $V_{UV\_VIO}$ , will disable both receiver and driver, put the device into shutdown mode. When  $V_{IO}$  is in valid level but  $V_{CC}$  is less than  $V_{UN\_VCC}$ , if STB = high, will place the device into low-power standby mode; if STB = low, will put the device into shutdown mode. See Table 9-4 for the undervoltage lockout status of CA-IF1044Vx.

#### Table 9-4. CA-IF1044AVx Undervoltage Lockout

V <sub>cc</sub>	V <sub>IO</sub>	DEVICE STATE	BUS OUTPUT	RXD
$\mathbf{Q}^{\mathbf{Y}}$	5 M	Standby (STB = high)	Bias to GND	According to the wake-up status
> Vuv_vcc	> V <sub>UV_IO</sub>	Normal(STB = GND)	Per TXD	According to BUS
< V <sub>UV_VCC</sub>	> V <sub>UV_10</sub>	Standby	Bias to GND	According to the wake-up status
> V <sub>UV_VCC</sub> or < V <sub>UV_VCC</sub>	< V <sub>UV_IO</sub>	Protected state	High-Z	High-Z

Once the undervoltage condition is cleared and the supply voltage has returned to a valid level, the devices transition to normal mode after the  $t_{MODE}$  time has expired. The host controller should not attempt to send or receive messages until the  $t_{MODE}$  time has expired.

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#### CA-IF1044A-Q1 Version 0.75,2025/04/18

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#### 9.4.2. Fault Protection

The CA-IF1044Ax devices has an internal ±42V overvoltage protection circuit on the driver output and receiver input to protect the devices from accidental shorts between a local power supply and the data lines of the transceivers. This level of protection is present whether the transceiver is powered or un-powered.

#### 9.4.3. Thermal Shutdown

If the junction temperature of the devices exceed the thermal shutdown threshold  $T_{TSD}$  (185°C), the device turns off the CAN driver circuits thus blocking the TXD-to-bus transmission path. The CAN bus terminals are biased to the recessive level during a thermal shutdown, and the receiver-to-RXD path remains operational. The shutdown condition is cleared when the junction temperature drops at least the thermal shutdown hysteresis temperature below the thermal shutdown threshold.

#### 9.4.4. Current-Limit

The CA-IF1044Ax protect the transmitter output stage against a short-circuit to a positive or negative voltage by limiting the driver current. However, this will cause large supply current and dissipation. Thermal shutdown further protects the devices from excessive temperatures that may result from a short circuit. The transmitter returns to normal operation once the short is removed.

#### 9.4.5. Transmitter-Dominant Timeout

The CA-IF1044Ax family of devices features a transmitter-dominant timeout ( $t_{DOM}$ ) that prevents erroneous CAN controllers from clamping the bus to a dominant level by maintaining a continuous low TXD signal. When TXD remains in the dominant state (low) for greater than  $t_{DOM}$ , the transmitter is disabled, releasing the bus to a recessive state (see Figure 9-3). After a dominant timeout fault, the transmitter is re-enabled when receiving a rising edge at TXD. The transmitter-dominant timeout limits the minimum possible data rate to 4kbps.

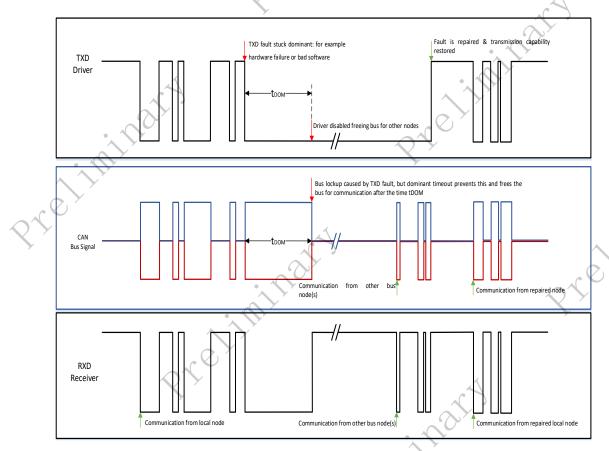


Figure 9-3. Transmitter-Dominant Timeout Protection



#### 9.5. Unpowered Device

The device is designed to be 'ideal passive' or 'no load' to the CAN bus if it is unpowered. The bus terminals (CANH, CANL) have extremely low leakage currents when the device is unpowered to avoid loading down the bus.

#### 9.6. Floating Terminals

These devices have internal pull-up on critical terminals to place the device into known states if the terminals float. The TXD terminal is pulled up to  $V_{cc}$  or  $V_{lo}$  to force a recessive input level if the terminal floats. The pin STB is also pulled up to force the device into standby mode if the terminal floats.

#### 9.7. Operating Mode

All devices have two operating modes: normal mode and standby mode. Operating mode selection is made via the STB input.

#### 9.7.1. Normal Mode

Select the normal mode of devices operation by setting STB terminal to logic-low. The CAN driver and receiver are fully operational and CAN communication is bi-directional. The driver translates a digital input on TXD to a differential output on CANH and CANL. The receiver translates the differential signal from CANH and CANL to a single-ended output on RXD.

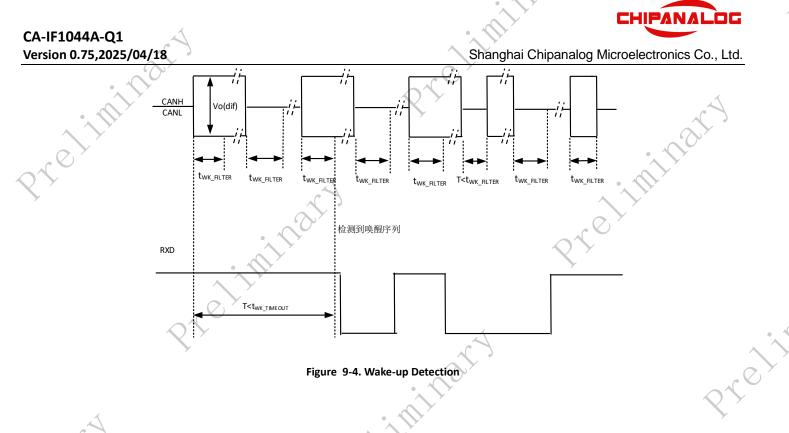
#### 9.7.2. Standby and Wake-up

Drive STB pin high or leave it open for standby mode, which switches the transmitter off and disables the main receiver. The low-power receive channel is enabled and put the device to a low current and low-speed monitor state. Thus the supply current is reduced during standby mode. The bus line is monitored by the low-power bus monitor, a low-speed differential comparator, to detect and recognize a wakeup event on the bus line, see Table 9-5.

#### Table 9-5. Operating Mode

STB	MODE	DRIVER	RECEIVER
Low	Normal	Enabled	Enabled
High or open	Standby	Disabled	Low-power receive channel is enabled and monitor the bus line.

To improve the system operation reliability and prevent false wake-up, the CA-IF1044Ax devices' receiver features wakeup timeout detection and filtered CAN bus status wake-up detection according to the ISO 11898-2:2016 standard. This means, for a valid dominant or recessive to be considered, the bus must be kept in that state for more than the  $t_{WK\_FILTER}$  time. For a remote wake-up event to successfully occur, a dominant bus level greater than  $t_{WK\_FILTER}$  must be detected and received by the low-power receive channel first to initiate a wake-up event. Then the low-power monitor will wait for a valid dominant state, other bus traffic does not reset the bus monitor. Once the low-power receive channel detects a successful wake-up event (a series of valid dominant - recessive - dominant pulses) within the timeout value t  $\leq t_{WK\_TIMEOUT}$ , RXD pulls low. CAN controller can drive the STB low based on this wake-up signal from RXD for normal operation. RXD is high until a valid wake-up is received during standby mode, see Figure 9-4 for more details.



#### 10. Application Information

The CA-IF1044Ax CAN transceivers are typically used in applications with a host microprocessor or FPGA that includes the data link layer portion of the CAN protocol. Figure 10-1, Figure 10-2 show the typical application circuit for the CA-IF1044AS-Q1/CA-IF1044AD-Q1 and CA-IF1044AVx, respectively. In Figure 10-2, connect the  $V_{10}$  to the MCU logic-supply.

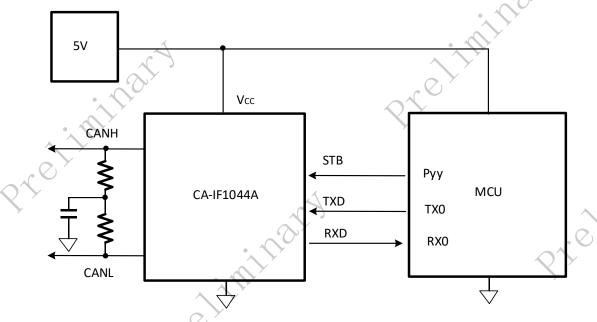


Figure 10-1. Typical Application Circuit for the CA-IF1044AS-Q1/CA-IF1044AD-Q1

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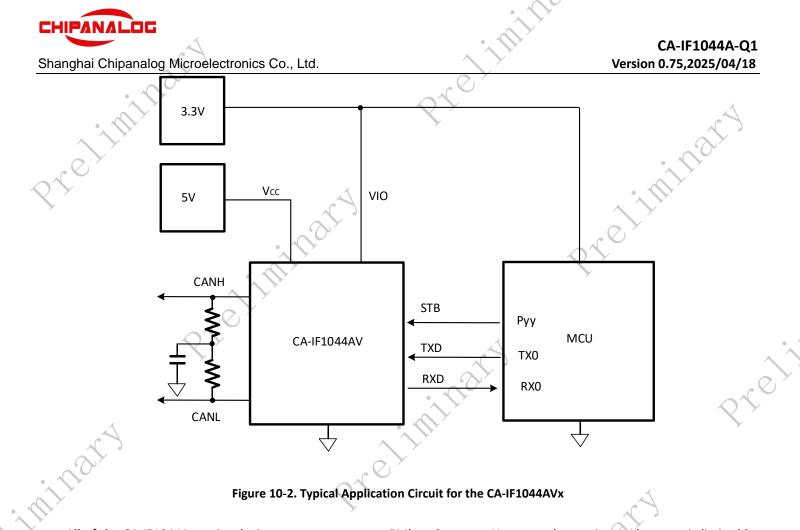


Figure 10-2. Typical Application Circuit for the CA-IF1044AVx

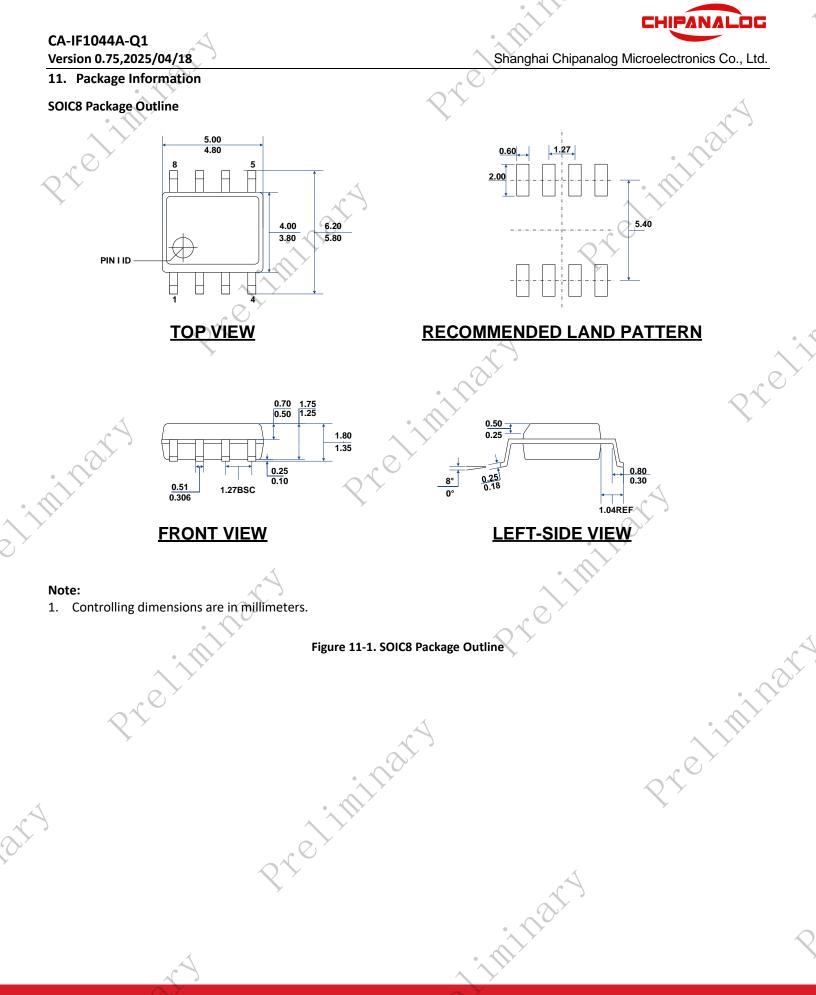
All of the CA-IF1044Ax series devices can operate up to 5Mbps data rate. However, the maximum data rate is limited by the bus loading, number of nodes, cable length etc. For CAN network design, margin must be given for signal loss across the system and cabling, parasitic loadings, timing, network imbalances, ground offsets and signal integrity thus a practical maximum data rate, number of nodes often lower. The ISO11898 Standard specifies a maximum of 30 nodes, with careful design, and consider of high input impedance of the CA-IF1044Ax, designers can have many more nodes on the CAN bus. Prelimit

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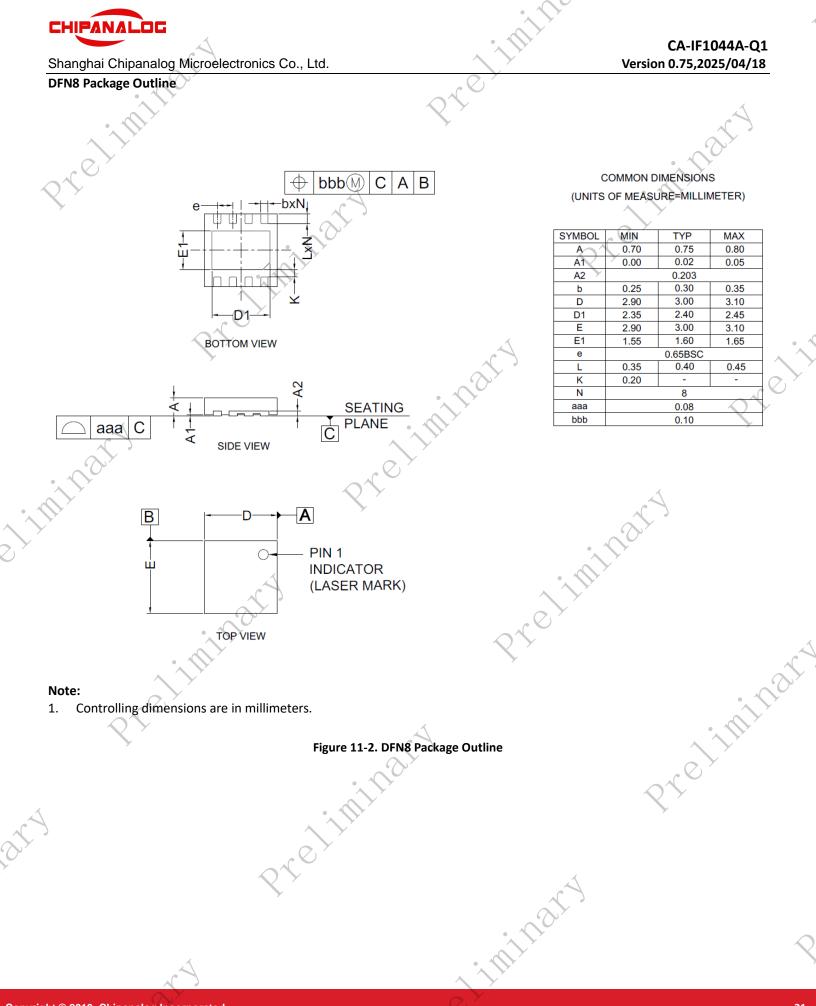
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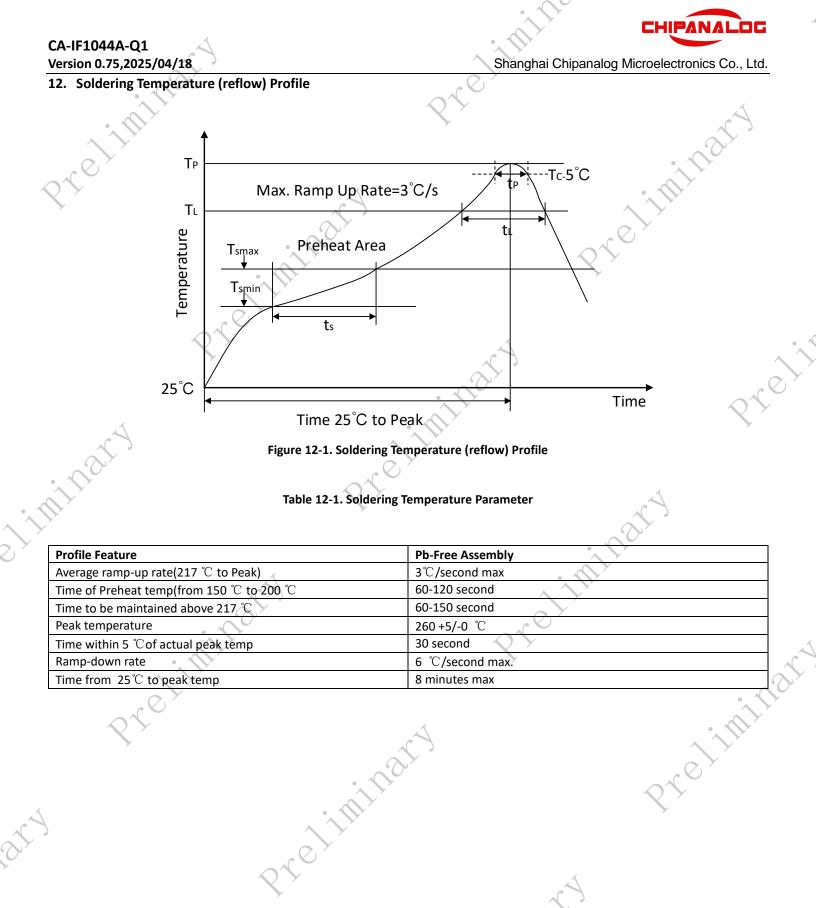
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#### CA-IF1044A-Q1 Version 0.75,2025/04/18

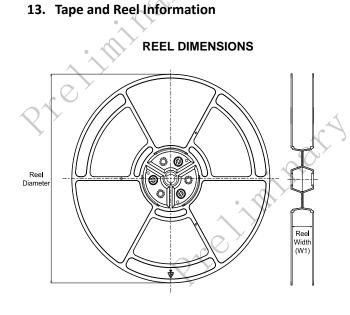


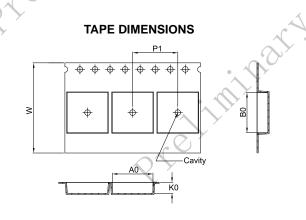


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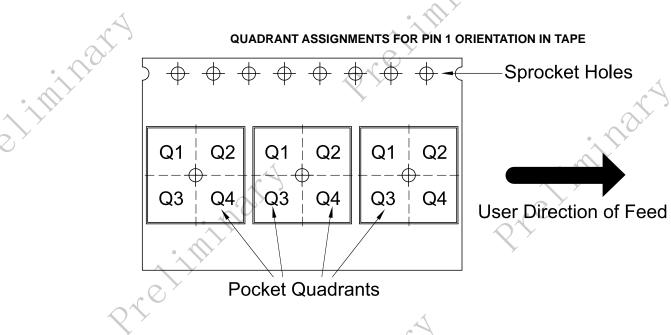
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A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
К0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

#### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

L							R	> >		, 1 00			- AS
~	2 ×	Poc	ket C	Quadra	ants							• • •	
27	_			*,	All dimensions	s are nominal							
Device	Packag e Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant	
CA-IF1044AS-Q1	SOIC8	S	8	2500	330	12.4	6.40	5.40	2.10	8.00	12.00	Q1	
CA-IF1044AVS-Q1	SOIC8	S	8	2500	330	12.4	6.40	5.40	2.10	8.00	12.00	Q1	_
CA-IF1044AD-Q1	DFN8	D	8	3000	330	12.4	3.35	3.35	1.13	8.00	12.00	Q1	
CA-IF1044AVD-Q1	DFN8	D	8	3000	330	12.4	3.35	3.35	1.13	8.00	12.00	Q1	
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## CA-IF1044A-Q1

Version 0.75,2025/04/18

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14. Appendix

Table 14-1. Comparison Table of Parameter Symbols in	CO11000 2.201C Chandend and CA IF1011 Detected
Ianie 14-1 ( omnarison Janie of Parameter Symbols in	$\mathbf{N}$

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ISO 11898-2:2016			CA-IF1044 Datasheet
Parameter	Note	Symbol	Parameter
HS-PMA dominant output characteristics	-1		
Single ended voltage on CAN_H	Vcan_h		
Single ended voltage on CAN_L	VCAN_L	Vo(dom)	dominant output voltage
Differential voltage on normal bus load			
Differential voltage on effective resistance during arbitration	VDiff	Vod(dom)	dominant differential output voltage
Optional: Differential voltage on extended bus load range	-		<b>&gt;</b>
HS-PMA driver symmetry			1
Driver symmetry	Vsym	Vsym	transmitter voltage symmetry
Maximum HS-PMA driver output current		1	1
Absolute current on CAN_H	ICAN_H		
Absolute current on CAN_L	ICAN_L	- los(ss_dom)	dominant short-circuit output current
HS-PMA recessive output characteristics, bus biasing active/inactive	. ^		
Single ended output voltage on CAN_H	Vcan_H		
Single ended output voltage on CAN_L	Vcan_l	VO(REC)	recessive output voltage
Differential output voltage	VDiff	VOD(REC)	recessive differential output voltage
Optional HS-PMA transmit dominant timeout	,		4
Transmit dominant timeout, long			
Transmit dominant timeout, short	tdom	tdom	TXD dominant time-out time
HS-PMA static receiver input characteristics, bus biasing active/inact	tive		• •
Recessive state differential input voltage range			
Dominant state differential input voltage range	VDiff	Vit	differential receiver threshold voltage
HS-PMA receiver input resistance (matching)	-		
Differential internal resistance	RDiff	RDIFF	differential input resistance
Single ended internal resistance	Rcan_h Rcan_l	RIN	input resistance
Matching of internal resistance	m <sub>R</sub>	Rdiff(m)	input resistance deviation
HS-PMA implementation loop delay requirement			
Loop delay	time	tloop2	delay time from TXD HIGH to RXD HIGH
	tLoop	tloop1	delay time from TXD LOW to RXD LOW
Optional HS-PMA implementation data signal timing requirements Mbit/s up to 5 Mbit/s	for use with	bit rates above	e 1 Mbit/s up to 2 Mbit/s and above 2
Transmitted recessive bit width @ 2 Mbit/s / @ 5 Mbit/s, intended	<b>t</b> Bit(Bus)	tbit(B∪S)	transmitted recessive bit width
Received recessive bit width @ 2 Mbit/s / @ 5 Mbit/s	tBit(RXD)	tbit(RXD)	bit time on pin RXD
Receiver timing symmetry @ 2 Mbit/s / @ 5 Mbit/s	ΔtRec	ΔtRec	receiver timing symmetry
HS-PMA maximum ratings of V <sub>CAN_H</sub> , V <sub>CAN_L</sub> and V <sub>Diff</sub>	-		4
Maximum rating V <sub>Diff</sub>	VDiff	V(DIFF)	voltage between pin CANH and pin CANL
General maximum rating $V_{\text{CAN}\_\text{H}}$ and $V_{\text{CAN}\_\text{L}}$	Vcan_h	V(BUS)	voltage on CANH, CANL pin
	VCAN_L		I VOICAGE UN CANIL, CANL PILL

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