CA-IS305xC 3.75kV$_{RMS}$/5kV$_{RMS}$ Isolated CAN Transceivers

1 Features

- **Meets the ISO 11898-2 physical layer standards**
- **Integrated protection increases robustness**
  - 3.75kV$_{RMS}$ (DUB8) or 5kV$_{RMS}$ (SOIC8-WB/SOIC16-WB) withstand isolation voltage for 60s (galvanic isolation)
  - ±150kV/μs typical CMTI
  - ±52V fault-tolerant CANH and CANL
  - ±30V extended common-mode input range (CMR)
  - Transmitter dominant timeout prevents lockup, data rates down to 5.5kbps
  - Thermal shutdown
- **Supports up to 1Mbps classic CAN and 5Mbps CAN FD (flexible data rate)**
- **Low loop delay: 165ns (typical), 255ns (maximum)**
- **3.0V to 5.5V I/O voltage range, supports 3V, 3.3V and 5V CAN controller interface**
- **Ideal passive behavior when unpowered**
- **Wide operating temperature range: -40°C to 125°C**
- **Wide-body SOIC8-WB(G), SOIC16-WB(W) packages and DUB8(U) package.**
- **Safety Regulatory Approvals**
  - VDE certification according to DIN EN IEC 60747-17(VDE 0884-17):2021-10
  - UL according to UL 1577
  - CQC according to GB4943.1-2022
  - TUV certification

2 Applications

- Industrial Controls
- Building Automation
- Security and Protection System
- Transportation
- Medical
- Telecom
- HVAC

3 General Description

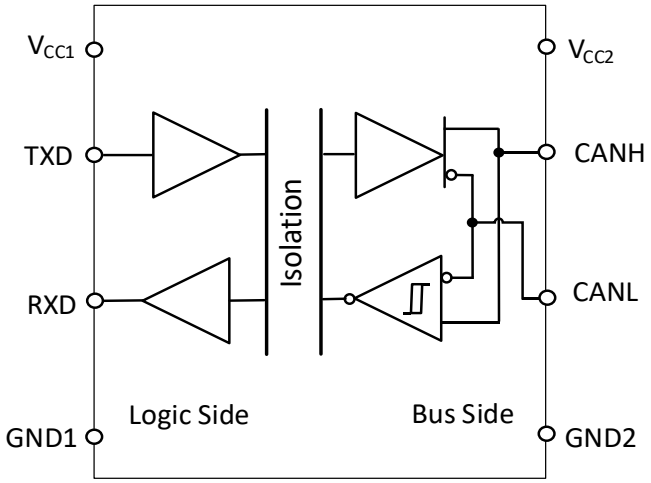
The CA-IS305xC family of devices is galvanically-isolated controller area network (CAN) transceiver that has superior isolation and CAN performance to meet the needs of the industrial applications. All devices of this family have the logic input and output buffers separated by a silicon oxide (SiO_2) insulation barrier that provides galvanic isolation. Isolation improves communication by breaking ground loops and reduces noise where there are large differences in ground potential between ports. Both the CA-IS3050C and the CA-IS3052C are available in wide-body SOIC8 and SOIC16, but offer different pinout; also, the CA-IS3050C is available DUB8 package. The SOIC16-WB is the industry standard isolated CAN package while the SOIC8-WB and DUB8 are much smaller packages that further reduce the board space in addition to reduced components due to integration of isolation and CAN with protection features. The CA-IS3050CU provides up to 3.75kV$_{RMS}$ (60s) of galvanic isolation; The CA-IS3050CG/W and CA-IS3052CG/W provide up to 5kV$_{RMS}$ (60s) of galvanic isolation.

These transceivers operate up to 5Mbps data rate and feature integrated protection for robust communication, including current limit, thermal shutdown, and the extended ±52V fault protection on the CAN bus for equipment where overvoltage protection is required. The dominant timeout detection prevents bus lockup caused by controller error or by a fault on the TXD input. These CAN receivers also incorporate an input common-mode range (CMR) of ±30V, exceeding the ISO 11898 specification of -2V to +7V. All devices operate over -40°C to +125°C temperature range.

Device information

Part Number	Package	Package size (Nominal value)
CA-IS3050CG	SOIC8-WB(G)	5.85 mm × 7.50 mm
CA-IS3052CG		
CA-IS3050CW	SOIC16-WB(W)	10.30 mm × 7.50 mm
CA-IS3052CW		
CA-IS3050CU	DUB8(U)	9.20mm × 6.62mm

Simplified functional block diagram



4 Ordering Information

Table 4-1 Ordering Information

Part #	V_{CC1} (V)	V_{CC2} (V)	Data Rate (Mbps)	Galvanic Isolation (V_{RMS})	Package
CA-IS3050CG	3.0~5.5	4.5~5.5	5	5000	SOIC8-WB
CA-IS3050CW	3.0~5.5	4.5~5.5	5	5000	SOIC16-WB
CA-IS3052CG	3.0~5.5	4.5~5.5	5	5000	SOIC8-WB
CA-IS3052CW	3.0~5.5	4.5~5.5	5	5000	SOIC16-WB
CA-IS3050CU	3.0~5.5	4.5~5.5	5	3750	DUB8

Contents

5 Revision history

Revision Number	Description	Revised Date	Page Changed
Version 1.00	Initial version	2024/07/18	N/A
Version 1.01	Update UL certification number Add TUV certification information Add CQC certification information	2025/03/01	1, 8

6 Pin Configuration and Functions

6.1 CA-IS3050Cx Pin Configuration and Functions

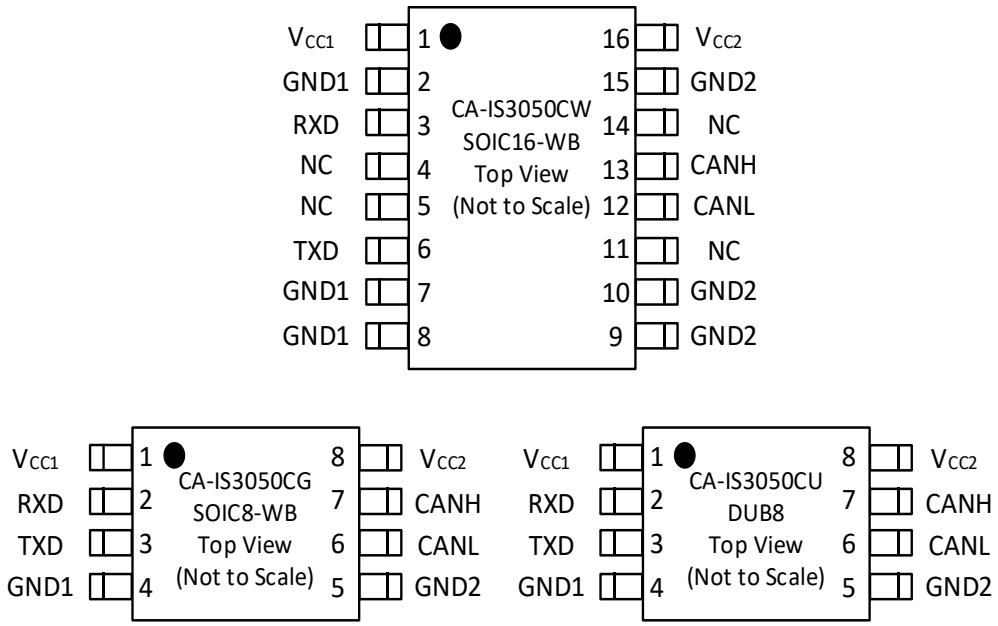


Figure 6-1 CA-IS3050Cx Pin Configuration

Table 6-1 CA-IS3050Cx Pin Configuration and Description

Pin name	Pin number		Type	Description
	SOIC16-WB	SOIC8-WB /DUB8		
V_{CC1}	1	1	Power supply	Power supply input for the logic side. Bypass V_{CC1} to GND1 with a 0.1μF capacitor as close to the device as possible.
GND1	2, 7, 8	4	Ground	Logic side ground.
RXD	3	2	Digital I/O	Receiver output. RXD is high when the bus is in the recessive state. RXD is low when the bus is in the dominant state.
NC	4, 5,	–	–	Inside the chip this pin is not connected, in applications it can be connected to V_{CC1} or GND1 or floating.
NC	11, 14	–	–	Inside the chip this pin is not connected, in applications it can be connected to V_{CC2} or GND2 or floating.
TXD	6	3	Digital I/O	Transmitter data input. CANH and CANL are in the dominant state when TXD is low. CANH and CANL are in the recessive state when TXD is high.
GND2	9, 10, 15	5	Ground	Bus side ground.
CANL	12	6	Bus I/O	Low-level CAN differential line.
CANH	13	7	Bus I/O	High-level CAN differential line.
V_{CC2}	16	8	Power supply	Power supply input for the bus side. Bypass V_{CC2} to GND2 with a 0.1μF capacitor as close to the device as possible.

6.2 CA-IS3052Cx Pin Configuration and Functions

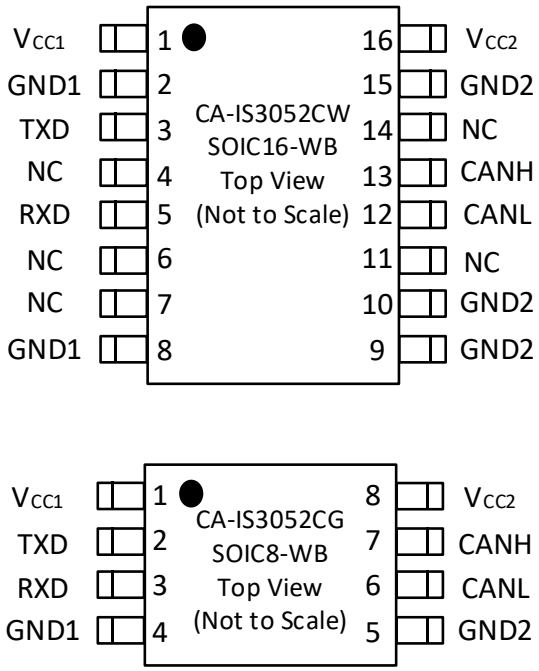


Figure. 6-2 CA-IS3052Cx Pin Configuration

Table 6-2 CA-IS3052Cx Pin Configuration and Description

Pin name	Pin number		Type	Description
	SOIC16-WB	SOIC8-WB		
V_{CC1}	1	1	Power supply	Power supply input for the logic side. Bypass V_{CC1} to GND1 with 0.1μF capacitor as close to the device as possible.
GND1	2, 8	4	Ground	Logic side ground.
TXD	3	2	Digital I/O	Transmitter data input. CANH and CANL are in the dominant state when TXD is low. CANH and CANL are in the recessive state when TXD is high.
NC	4, 6, 7,	–	–	Inside the chip this pin is not connected, in applications it can be connected to V_{CC1} or GND1 or floating.
NC	11, 14	–	–	Inside the chip this pin is not connected, in applications it can be connected to V_{CC2} or GND2 or floating.
RXD	5	3	Digital I/O	Receiver output. RXD is high when the bus is in the recessive state. RXD is low when the bus is in the dominant state.
GND2	9, 10, 15	5	Ground	Bus side ground.
CANL	12	6	Bus I/O	Low-level CAN differential line.
CANH	13	7	Bus I/O	High-level CAN differential line.
V_{CC2}	16	8	Power supply	Power supply input for the bus side. Bypass V_{CC2} to GND2 with 0.1μF capacitor as close to the device as possible.

7 Specifications

7.1 Absolute Maximum Ratings[1]

Parameters		Minimum value	Maximum value	Unit
V_{CC1} or V_{CC2}	Power supply voltage[2]	–0.5	6.0	V
TXD or RXD to GND1	Logic side voltage (RXD, TXD)	–0.5	V_{CC1} + 0.5[3]	V
CANH or CANL to GND2 CANH to CANL	CANH or CANL to GND2 Bus side differential voltage between CANH and CANL	–52	52	V
I_O	Receiver output current	–15	15	mA
T_J	Junction temperature		150	°C
T_{STG}	Storage temperature range	–65	150	°C

Notes:
1. The stresses listed under "Absolute Maximum Ratings" are stress ratings only, not for functional operation condition. Exposure to absolute maximum rating conditions for extended periods may cause permanent damage to the device.
2. All voltage values except differential I/O bus voltages are with respect to the local ground (GND1 or GND2) and are peak voltage values.
3. Maximum voltage must not be exceeded 6 V.

7.2 ESD Ratings

			Numerical value	Unit
V_{ESD}	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, bus pins to GND2	±8000	V
		Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all other pins[1]	±4000	
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[2]	±1500	

Notes:
1. Per JEDEC document JEP155, 500V HBM allows safe manufacturing of standard ESD control process.
2. Per JEDEC document JEP157, 250V CDM allows safe manufacturing of standard ESD control process.

7.3 Recommended Operating Conditions

Parameters			MIN	TYP	MAX	Unit
V_{CC1}	Logic side power voltage		3.0	3.3	5.5	V
V_{CC2}	Bus side power voltage		4.5	5	5.5	V
V_I or V_{IC}	Voltage at bus pins (separately or common mode)		–30		30	V
V_{IH}	Input high voltage	Driver (TXD)	0.7 x V_{CC1}			V
V_{IL}	Input low voltage	Driver (TXD)			0.3 x V_{CC1}	V
V_{ID}	Differential input voltage		–30		30	V
I_{OH}	High-level output current	Driver	–70			mA
		Receiver	–4			
I_{OL}	Low-level output current	Driver			70	mA
		Receiver			4	
T_A	Ambient temperature		–40		125	°C
T_J	Junction temperature		–40		150	°C
P_D	Total power dissipation	V_{CC1} = 5.5V, V_{CC2} = 5.25V, T_A = 125°C, R_L = 60Ω, TXD input is 500 kHz, 50% duty cycle square wave			242	mW
P_{D1}	Logic side power dissipation				19	mW
P_{D2}	Bus side power dissipation				223	mW
$T_{J(shutdown)}$	Thermal shutdown temperature[1]			190		°C

Note:
1. Extended operation in thermal shutdown may affect device reliability.

7.4 Thermal Information

Heat meter		SOIC8-WB	SOIC16-WB	DUB8	Unit
$R_{\theta JA}$	Junction-to-ambient thermal resistance	110.1	86.5	73.3	°C/W
$R_{\theta JC}$	Junction-to-case thermal resistance	51.7	49.6	63.2	°C/W

7.5 Insulation Specifications

Parameters		Test conditions	Value		Unit
			SOIC8-WB / SOIC16-WB	DUB8	
CLR	External clearance[1]	Shortest terminal-to-terminal distance through air	8	6.1	mm
CPG	External creepage[1]	Shortest terminal-to-terminal distance across the package surface	8	6.8	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	28	28	μm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11)；IEC 60112	>600	>600	V
	Material group	Per IEC 60664-1	I	I	
Overvoltage category per IEC 60664-1		Rated mains voltage ≤ 150 V_{RMS}	I-IV	I-IV	
		Rated mains voltage ≤ 300 V_{RMS}	I-IV	I-III	
		Rated mains voltage ≤ 600 V_{RMS}	I-IV	N/A	
		Rated mains voltage ≤ 1000 V_{RMS}	I-III	N/A	
DIN V VDE V 0884-17:2021-10[2]					
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	1414	566	V_{PK}
V_{IOWM}	Maximum operating isolation voltage	AC voltage; time-dependent dielectric breakdown (TDDB) test	1000	400	V_{RMS}
		DC voltage	1414	566	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t=60 s (certified); $V_{TEST} = 1.2 \times V_{IOTM}$, t=1 s (100% product test)	7070	5300	V_{PK}
V_{IMP}	Maximum impulse voltage	1.2/50-μs waveform per IEC 62368-1	9846	4077	V_{PK}
V_{IOSM}	Maximum surge isolation voltage[3]	$V_{IOSM} \geq 1.3 \times V_{IMP}$; Tested in oil (qualification test), 1.2/50-μs waveform per IEC 62368-1	12800	5300	V_{PK}
q_{pd}	Apparent charge[4]	Method a, after input/output safety test of the subgroup 2/3, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)} = 1.2 \times V_{IORM}$, t_m = 10 s	≤5	≤5	pC
		Method a, after environmental test of the subgroup 1, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)} = 1.6 \times V_{IORM}$, t_m = 10 s (SOIC8-WB and SOIC16-WB) $V_{pd(m)} = 1.3 \times V_{IORM}$, t_m = 10 s(DUB8)	≤5	≤5	
		Method b1, at routine test (100% production test) and preconditioning (type test) $V_{ini} = 1.2 \times V_{IOTM}$, t_{ini} = 1 s; $V_{pd(m)} = 1.875 \times V_{IORM}$, t_m = 1 s (certificated, SOIC8-WB and SOIC16-WB) $V_{pd(m)} = 1.5 \times V_{IORM}$, t_m = 1 s (certificated, DUB8)	≤5	≤5	
C_{IO}	Barrier capacitance, input to output[5]	V_{IO} = 0.4 × sin (2πft), f = 1 MHz	~0.5	~0.5	pF
R_{IO}	Isolation resistance[5]	V_{IO} = 500 V, T_A = 25°C	$>10^{12}$	$>10^{12}$	Ω
		V_{IO} = 500 V, 100°C ≤ T_A ≤ 125°C	$>10^{11}$	$>10^{11}$	
		V_{IO} = 500 V at T_S = 150°C	$>10^{9}$	$>10^{9}$	
	Pollution degree		2	2	
UL 1577					
V_{ISO}	Maximum withstanding isolation voltage	$V_{TEST} = V_{ISO}$, t = 60 s (qualification) $V_{TEST} = 1.2 \times V_{ISO}$, t = 1 s (100% production test)	5000	3750	V_{RMS}
Notes:					

1. Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications.
2. This coupler is suitable for safe electrical insulation only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
3. Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
4. Apparent charge is electrical discharge caused by a partial discharge (pd).
5. All pins on each side of the barrier tied together creating a two-terminal device.

7.6 Safety-Related Certifications

VDE	UL		TUV
Certified according to DIN EN IEC 60747-17(VDE 0884-17):2021-10; EN IEC 60747-17:2020+AC:2021	Certified according to UL 1577 Component Recognition Program	Certified according to GB4943.1-2022	Certified according to EN 61010-1 and EN 62368-1
CA-IS3050C / CA-IS3052C (SOIC8-WB/ SOIC16-WB, reinforced isolation) V_{IORM}: 1414V_{PK} V_{IOTM}: 7070V_{PK} V_{IOSM}: 12800V_{PK} CA-IS3050CU (DUB8, basic isolation) V_{IORM}: 566V_{PK} V_{IOTM}: 5300V_{PK} V_{IOSM}: 5300V_{PK}	Single Protection SOIC8-WB: 5000V_{RMS}; SOIC16-WB: 5000V_{RMS} DUB8: 3750V_{RMS}	Reinforced insulation: SOIC8-WB / SOIC16-WB Basic insulation: DUB8 (Altitude ≤ 5000m)	EN 61010-1 5000V_{RMS} (SOIC8-WB / SOIC16-WB) 3750V_{RMS} (DUB8) EN 62368-1 5000V_{RMS} (SOIC8-WB / SOIC16-WB) 3750V_{RMS} (DUB8)
Certificate number: 40057278 (Reinforced) 40052786 (Basic)	Certificate number: E511334	Certificate number: SOIC8-WB: CQC24001434134 SOIC16-WB: Pending DUB8: CQC24001452683	Client reference number: 2253313

7.7 Electrical Characteristics

over recommended operating conditions (unless otherwise noted). All typical values are at 25°C with V_{CC1} = V_{CC2} = 5V.

Parameters		Test conditions	MIN	TYP	MAX	Unit
Power supply voltage						
V_{CC1_UVLO+} UVLO power up start up		V_{CC1}	2.55	2.7	2.85	V
V_{CC1_UVLO-} UVLO power drop reset		V_{CC1}	2.35	2.5	2.65	
V_{CC2_UVLO+} UVLO power up start up		V_{CC2}	3.9	4.2	4.45	
V_{CC2_UVLO-} UVLO power drop reset		V_{CC2}	3.8	4.0	4.35	
Power supply current						
I_{CC1} Logic side power supply current		V_I = V_{CC1}, V_{CC1} = 5V		1.8	2.8	mA
		V_I = 0V, V_{CC1} = 5V		3	4	
I_{CC2} Bus side power supply current	Dominant	V_I = 0V， R_L = 60Ω		44	73	mA
	Recessive	V_I = V_{CC1}		3	12	
Driver						
$V_{O(D)}$ Bus output voltage (dominant)	CANH	V_I = 0V, R_L = 60Ω; see Figure 8-1 and Figure 8-2.	2.75	3.4	4.5	V
	CANL		0.5		2.25	
$V_{O(R)}$ Bus output voltage (recessive)		V_I = V_{CC1}, R_L = 60Ω; see Figure 8-1 and Figure 8-2.	2	2.5	3	V
$V_{OD(D)}$ Differential output voltage (dominant)		V_I = 0V, R_L = 60Ω; see Figure 8-1, Figure 8-2 and Figure 8-3.	1.5		3	V
		V_I = 0V, R_L = 45Ω; see Figure 8-1, Figure 8-2 and Figure 8-3.	1.4		3	V
$V_{OD(R)}$ Differential output voltage (recessive)		V_I = V_{CC1}, R_L = 60Ω; see Figure 8-1 and Figure 8-2.	–12		12	mV
		V_I = V_{CC1}, no-load.	–50		50	mV
$V_{OC(D)}$ Common mode output voltage (dominant)		See Figure 8-7	2	2.5	3	V
$V_{OC(pp)}$ Peak to peak common mode output voltage				0.3		V
I_{IH} High-level input current, TXD input		TXD= V_{CC1}			20	μA
I_{IL} Low-level input current, TXD input		TXD = 0V	–20			μA
$I_{OS(SS)}$ Short-circuit steady-state output current		TXD=Low, V_{CANH} = –30V, CANL open; see Figure 8-10.	–105	–67		mA
		TXD=High, V_{CANH} = 30V, CANL open; see Figure 8-10.		1.25	5	
		TXD=High, V_{CANL} = –30V, CANH open; see Figure 8-10.	–5	–1.25		
		TXD=Low, V_{CANL} = 30V, CANH open; see Figure 8-10.		83	105	
Receiver						
V_{IT+} Positive-going bus input threshold voltage		-20V ≤ V_{CM} ≤ 20V			0.9	V
V_{IT-} Negative-going bus input threshold voltage			0.5			V
V_{IT+} Positive-going bus input threshold voltage		-30V ≤ V_{CM} ≤ 30V			1.0	V
V_{IT-} Negative-going bus input threshold voltage			0.4			V
V_{HYS} Hysteresis voltage				120		mV
V_{OH} High-level output voltage		V_{CC1} = 5V, I_{OH} = –4mA; see Figure 8-6.	4.6	4.8		V
		V_{CC1} = 5V, I_{OH} = –20μA; see Figure 8-6.	4.9	5		
		V_{CC1} = 3.3V, I_{OH} = –4mA; see Figure 8-6.	2.9	3.1		V
		V_{CC1} = 3.3V, I_{OH} = –20μA; see Figure 8-6.	3.2	3.3		
V_{OL} Low-level output voltage		I_{OL} = 4mA; see Figure 8-6.		0.2	0.4	V
		I_{OL} = 20μA; see Figure 8-6.		0	0.1	
C_I CANH or CANL input capacitance to ground		V_{TXD} = V_{CC1}, V_I = 0.4 x sin(2πft) + 2.5V, f = 1MHz		20		pF
C_{ID} Differential input capacitance		V_{TXD} = V_{CC1}, V_I = 0.4 x sin(2πft),		10		pF

		f = 1MHz				
R_{IN}	CANH and CANL input capacitance	$V_{TXD} = V_{CC1}$	15		40	kΩ
R_{ID}	Differential input resistance	$V_{TXD} = V_{CC1}$	30		80	kΩ
$R_{I(m)}$	Input resistance matching $(1 – [R_{IN(CANH)} / R_{IN(CANL)}]) \times 100\%$	$V_{CANH} = V_{CANL}$	–5%	0%	5%	
CMTI	Common mode transient immunity	V_I = 0V or V_{CC1}; see Figure 8-12.	±100	±150		kV/μs

7.8 Switching Characteristics

over recommended operating conditions (unless otherwise noted). All typical values are at 25°C with $V_{CC1} = V_{CC2} = 5V$.

Parameters		Test conditions		MIN	TYP	MAX	Unit
Device							
t_{loop1}	Total loop delay, driver input (TXD) to receiver output (RXD), recessive to dominant	see Figure 8-8.			165	255	ns
t_{loop2}	Total loop delay, driver input (TXD) to receiver output (RXD), dominant to recessive				185	255	ns
Driver							
t_{PLH}	TXD propagation delay (recessive to dominant)	see Figure 8-4.			85	140	ns
t_{PHL}	TXD propagation delay (dominant to recessive)				65	110	
t_r	Differential driver output rise time				45	70	
t_f	Differential driver output fall time				60	100	
t_{TXD_DTO}[1]	TXD dominant timeout	C_L = 100pF; see Figure 8-9.		2	5	8	ms
Receiver							
t_{PLH}	RXD propagation delay (recessive to dominant)	see Figure 8-6.			75	145	ns
t_{PHL}	RXD Propagation delay (dominant to recessive)				95	165	
t_r	RXD Output signal rise time				2.5		
t_f	RXD Output signal fall time				2.5		
FD TIMING							
$T_{bit(BUS)}$	Bit time on CAN bus output pins	R_L = 60Ω, C_L=100pF, C_{RXD}=15pF, see Figure 8-11	$T_{bit(TXD)}$ = 500ns	435		530	ns
			$T_{bit(TXD)}$ = 200ns	155		210	ns
$T_{bit(RXD)}$	Bit time on RXD output pins		$T_{bit(TXD)}$ = 500ns	400		550	ns
			$T_{bit(TXD)}$ = 200ns	120		220	ns
Δt_{re}	Receiver timing symmetry		$T_{bit(TXD)}$ = 500ns	-65		40	ns
			$T_{bit(TXD)}$ = 200ns	-45		15	ns

Note:

1. The TXD dominant time out (t_{TXD_DTO}) disables the driver of the transceiver once the TXD has been dominant longer than (t_{TXD_DTO}) which releases the bus lines to recessive preventing a local failure from locking the bus dominant.
2. $\Delta t_{rec} = T_{bit(RXD)} – T_{bit(BUS)}$

8 Parameter Measurement Information

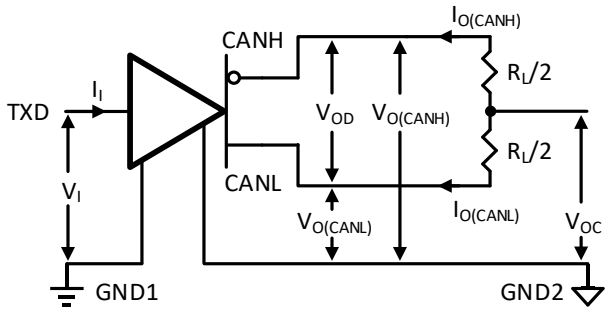


Figure. 8-1 Driver Voltage and Current Definition

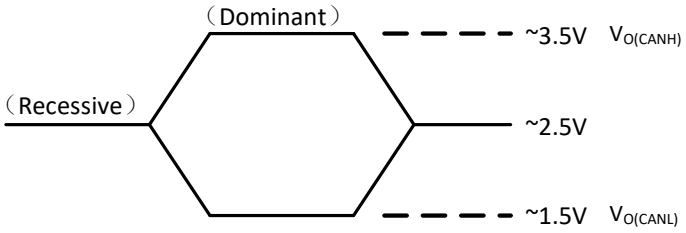


Figure. 8-2 Bus Logic State Voltage Definition

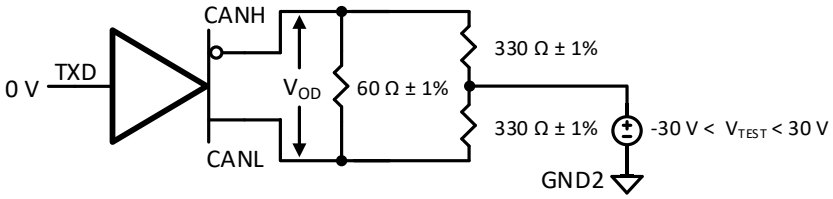
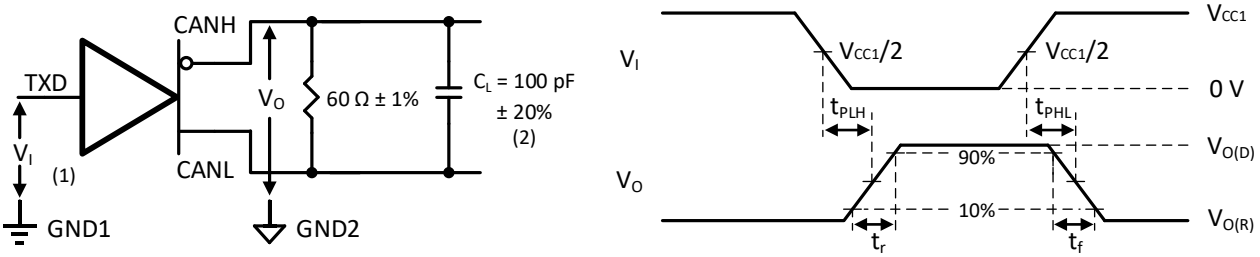


Figure. 8-3 Driver V_{OD} with Common Mode Loading Test Circuit



Notes:

1. The input pulse is supplied by a generator with characteristics: PRR ≤ 125 kHz, 50% duty cycle; rise time t_r≤6 ns, fall time t_f≤6 ns; Z_O = 50 Ω.
2. Load capacitance C_L includes external circuit (instrumentation and fixture etc.) capacitance.

Figure. 8-4 Transmitter Test Circuit and Timing Diagram

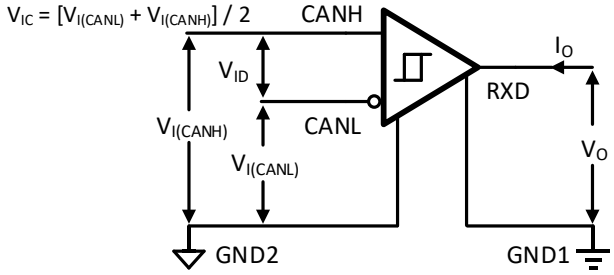
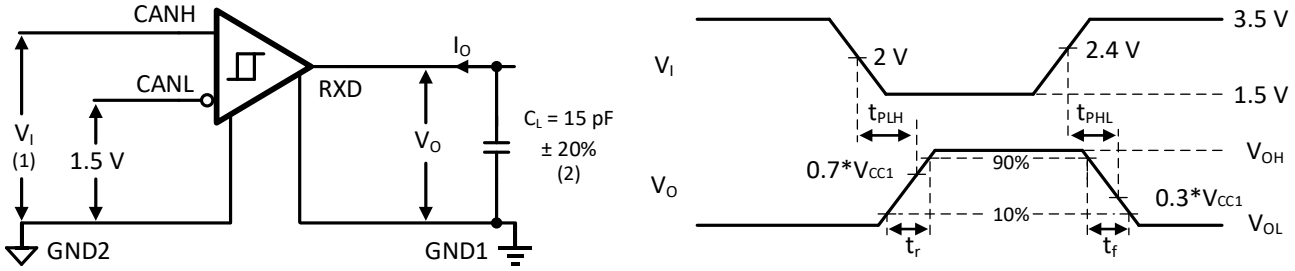


Figure. 8-5 Receiver Voltage and Current Definition



Notes:

1. The input pulse is supplied by a generator with characteristics: PRR ≤ 125 kHz, 50% duty cycle; rise time t_r≤6 ns, fall time t_f≤6 ns; Z_O = 50 Ω.
2. Load capacitance C_L includes external circuit (instrumentation and fixture etc.) capacitance.

Figure. 8-6 Receiver Test Circuit and Timing Diagram

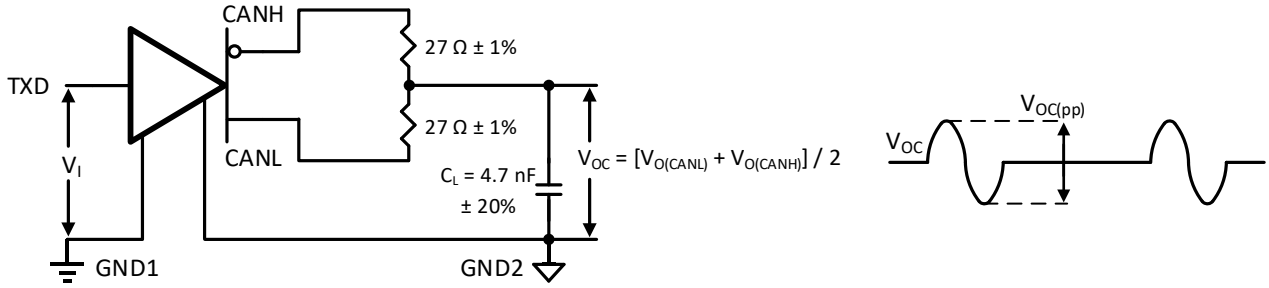


Figure. 8-7 Peak-to-Peak Output Voltage Test Circuit and Waveform

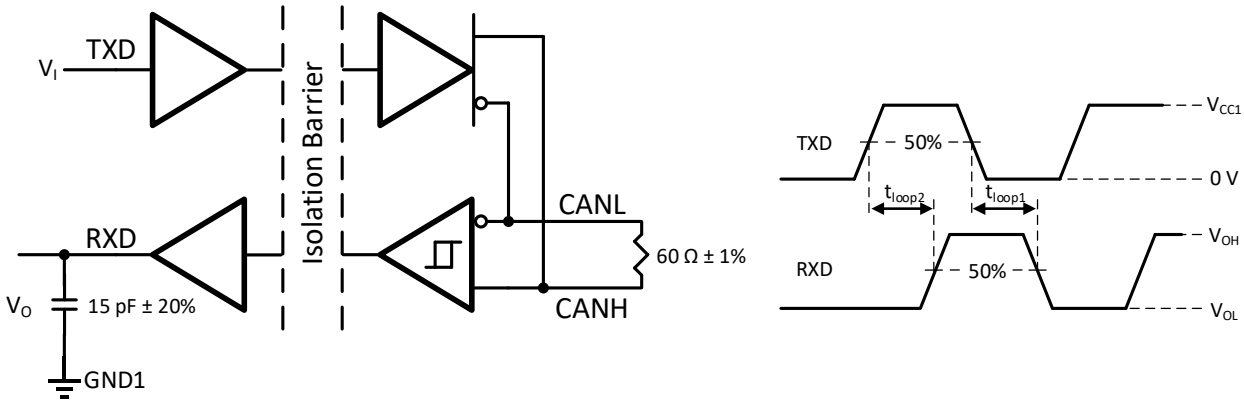
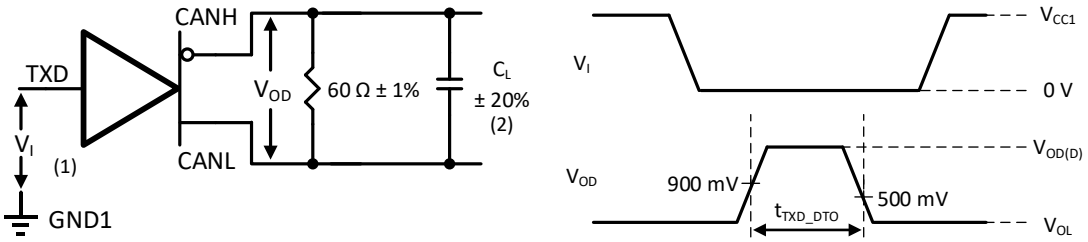


Figure. 8-8 TXD to RXD Loop Delay



Notes:

1. The input pulse is supplied by a generator with characteristics: PRR ≤ 125 kHz, 50% duty cycle; rise time t_r≤6 ns, fall time t_f≤6 ns; Z_O = 50 Ω.
2. Load capacitance C_L includes external circuit (instrumentation and fixture etc.) capacitance.

Figure. 8-9 Transmitting Dominant Timeout Timing Diagram

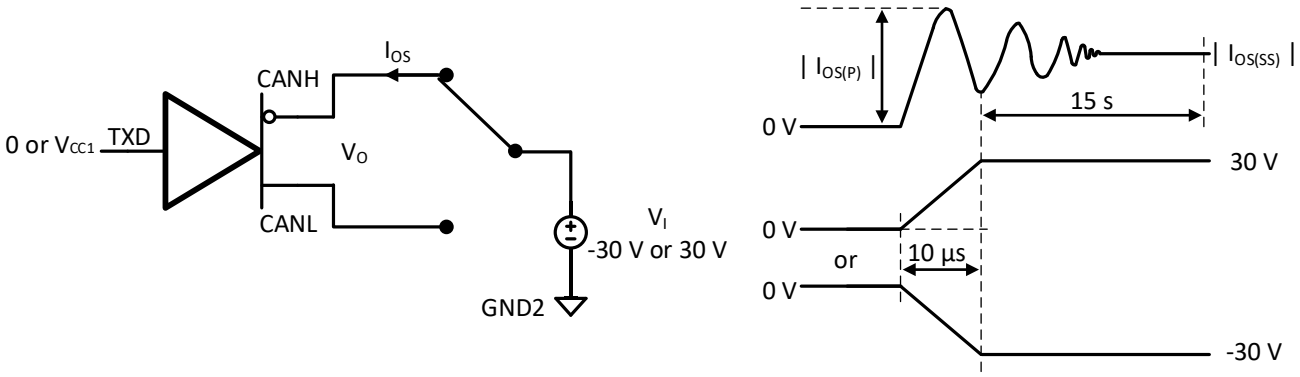


Figure. 8-10 Driver Short Circuit Current Test Circuit and Measurement

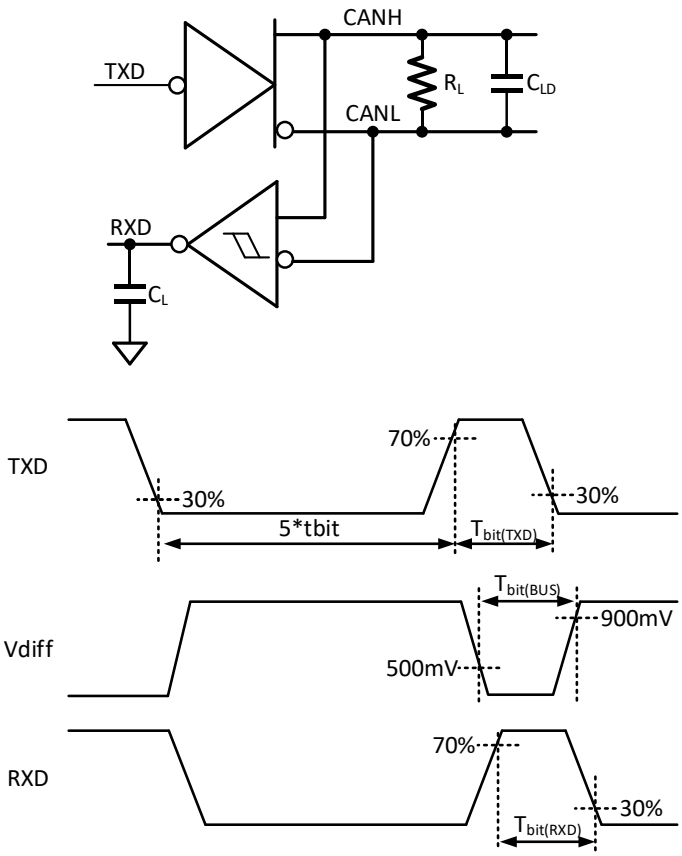


Figure. 8-11 CAN FD Timing Parameter Measurement

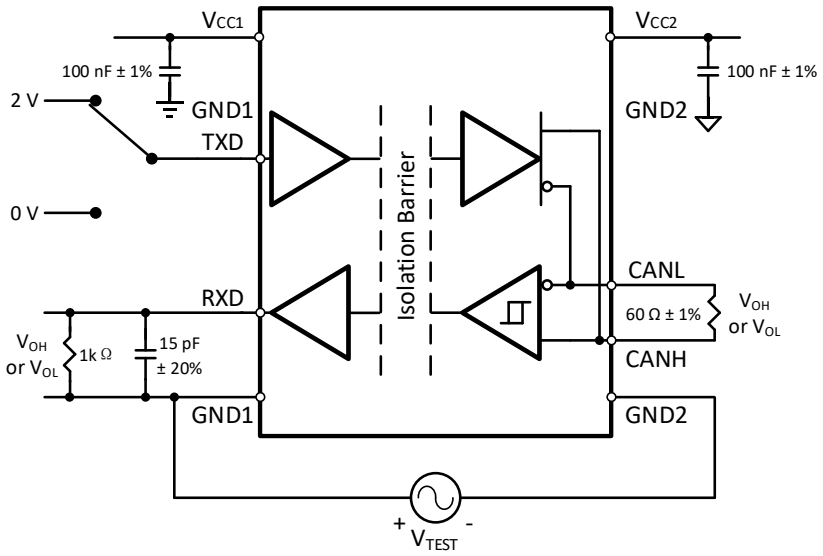


Figure. 8-12 Common-Mode Transient Immunity Test Circuit

9 Detailed Description

9.1 Overview

The CA-IS305xC isolated controller area network (CAN) transceivers provide up to 3.75kV$_{RMS}$ (DUB8 package) and 5kV$_{RMS}$ (SOIC8-WB/SOIC16-WB package) of galvanic isolation between the cable side (bus-side) of the transceiver and the controller side (logic-side). These devices feature up to ±150kV/μs common mode transient immunity, allow up to 5Mbps communication across an isolation barrier. Robust isolation coupled with high standoff voltage and increased speeds enables efficient communication in noisy environments, making them ideal for communication with the microcontroller in a wide range of applications such as solar inverters, circuit breakers, motor drives, PLC communication modules, telecom rectifiers, elevators, HVACs and EV charging infrastructures. Interfacing with CAN protocol controllers is simplified by the 3.0V to 5.5V wide supply voltage range (V_{CC1}) on the controller side of the device. This supply voltage sets the interface logic levels between the transceiver and controller. The supply voltage range for the CAN bus side of the device is 4.5V to 5.5V (V_{CC2}). The receiver input common-mode range is ±30V, exceeding the ISO 11898 specification of -2V to +7V, and the fault tolerant is up to ±52V. Dominant timeout prevents the bus from being blocked by a hung-up microcontroller, and the outputs CANH and CANL are short-circuit current-limited, protected against excessive power dissipation by thermal shutdown circuitry that places the driver outputs in a high-impedance state.

9.2 CAN Bus Status

The CAN bus has two states: dominant and recessive. In the dominant state (a zero bit, used to determine message priority), CANH – CANL are defined to be logic '0' when the voltage across them is between +1.5V and +3V (higher than 0.9V). In the recessive state (a 1-bit and the state of the idle bus), the driver is defined to be logic '1' when differential voltage is between -50mV and +50mV. See Figure 8-2.

9.3 Receiver

The receiver demodulates the differential input from the bus line (CANH and CANL) and transfers it as a single-ended output on RXD pin. The internal comparator senses the differential voltage $V_{ID} = (V_{CANH} – V_{CANL})$ from bus. If $V_{ID} > V_{IT+}$, a logical low is present on RXD pin; If $V_{ID} < V_{IT–}$, a logical high is present on RXD pin. RXD is a logical high when CANH and CANL are open, short or on idle state. See Table 9-1.

Table 9-1 Receiver Truth Table

$V_{ID}=V_{CANH}-V_{CANL}$		BUS STATE	RXD
V_{CM} = –20V to +20V	V_{CM} = –30V to +30V		
$V_{ID} \geq 0.9V$	$V_{ID} \geq 1V$	Dominant	Low
$0.5V < V_{ID} < 0.9V$	$0.4V < V_{ID} < 1V$	Indeterminate	Indeterminate
$V_{ID} \leq 0.5V$	$V_{ID} \leq 0.4V$	Recessive	High
Open ($V_{ID} \approx 0V$)		Open	High

9.4 Transmitter

Table 9-2 Transmitter Truth Table[1]

V_{CC1}	V_{CC2}	INPUT	TXD LOW TIME	OUTPUT		BUS STATE
		TXD[2]		CANH	CANL	
Power up	Power up	Low	< t_{TXD_DTO}	High	Low	Dominant
		Low	> t_{TXD_DTO}	$V_{CC2}/2$	$V_{CC2}/2$	Recessive
		High or Open	X	$V_{CC2}/2$	$V_{CC2}/2$	Recessive
Power up	Power down	X	X	Hi-Z	Hi-Z	Hi-Z
Power down	Power up	X	X	$V_{CC2}/2$	$V_{CC2}/2$	Recessive

Note:

1. X = Don't care; Hi-Z = high impedance.
2. The input of TXD is weakly pulled-up internally.

The transmitter converts a single-ended input signal (TXD) from the local CAN controller to differential outputs for the bus lines CANH and CANL. The truth table for the transmitter is provided in Table 9-2.

CANH and CANL outputs are short-circuit current limited and are protected against excessive power dissipation by thermal shutdown circuitry that places the driver outputs in a high-impedance state.

9.5 Protection Functions

9.5.1 Signal Isolation and Protection

The CA-IS305xC devices integrated digital galvanic isolators using Chipanalog's capacitive isolation technology based on the ON-OFF keying (OOK) modulation scheme, allow data transmission between the controller side and cable side of the transceiver with different power domains. The driver outputs/receiver inputs are also protected from ±8kV electrostatic discharge (ESD) to GND2 on the bus side, as specified by the Human Body Model (HBM).

9.5.2 Thermal Shutdown

If the junction temperature of the CA-IS305xC device exceeds the thermal shutdown threshold $T_{J\ (shutdown)}$ (190°C, typ.), the device turns off the CAN driver circuits thus blocking the TXD-to-bus transmission path. The CAN bus terminals are biased to the recessive level during a thermal shutdown, and the receiver-to-RXD path remains operational. The shutdown condition is cleared when the junction temperature drops to normal operation temperature range of the device.

9.5.3 Current-Limit

The CA-IS305xC protect the transmitter output stage against a short-circuit to a positive or negative voltage by limiting the driver current. However, this will cause large supply current and dissipation. Thermal shutdown further protects the devices from excessive temperatures that may result from a short circuit. The transmitter returns to normal operation once the short is removed.

9.5.4 Transmitter-Dominant Timeout

The CA-IS305xC devices feature a transmitter-dominant timeout (t_{TXD_DTO}) that prevents erroneous CAN controllers from clamping the bus to a dominant level by maintaining a continuous low TXD signal. When TXD remains in the dominant state (low) for greater than t_{TXD_DTO}, the transmitter is disabled, releasing the bus to a recessive state. After a dominant timeout fault, the transmitter is re-enabled when receiving a rising edge at TXD. The CAN protocol allows a maximum of eleven successive dominant bits (on TXD) for the worst case, where five successive dominant bits are followed immediately by an error frame. So the minimum transmitted data rate can be calculated as: 11 bits/t_{TXD_DTO} = 11 bits / 2ms = 5.5kbps. The transmitter-dominant timeout limits the minimum possible data rate of the CA-IS305xC to 5.5kbps.

10 Application Information

The CAN bus has been a very popular serial communication standard in the industry due to its excellent prioritization and arbitration capabilities. In systems with different voltage domains, isolation is typically used to protect the low voltage side from the high voltage side in case of any faults. The CA-IS305xC family of devices is ideal for these kinds of applications, see Figure 10-1 the typical application circuit.

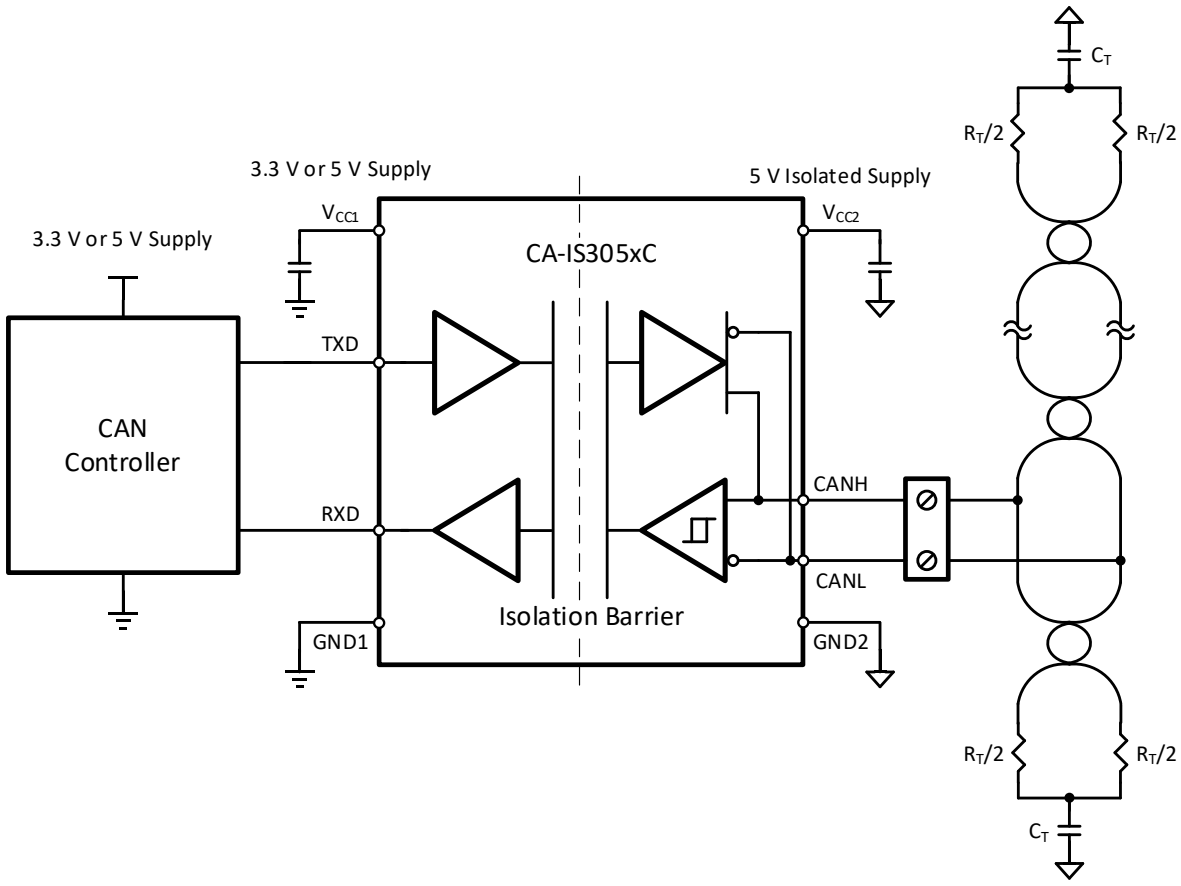


Figure. 10-1 Typical Application Circuit

These devices can operate up to 5Mbps data rate. However, the maximum data rate is limited by the bus loading, number of nodes, cable length etc. factors. For CAN network design, margin must be given for signal loss across the system and cabling, parasitic loadings, timing, network imbalances, ground offsets and signal integrity thus a practical maximum data rate, number of nodes often lower. The ISO11898 Standard specifies a maximum of 30 nodes. However, with careful design, and consider of high input impedance of the CA-IS305xC, designers can have many more nodes on the CAN bus. The differential input resistance of the CA-IS305xC is a minimum of 30kΩ. If 110 pcs CA-IS305xC transceivers are in parallel on a bus, this is equivalent to a 273Ω differential load. That transceiver load of 273Ω in parallel with the 60Ω (the two 120Ω termination resistors in parallel) gives a total 49Ω load on the bus. The driver differential output of CA-IS305xC devices is specified to provide at least 1.5V with a 60Ω load, and additionally specified with a differential output of 1.4V with a 45Ω load. Therefore, the CA-IS305xC theoretically can support over 110 transceivers on a single bus with design margin.

In multidrop CAN applications, it is important to maintain a single linear bus of uniform impedance that is properly terminated at each end. A star, ring, or tree configuration should never be used. Any deviation from the end-to-end wiring scheme creates a stub. High-speed data edges on a stub can create reflections back down to the bus. These reflections can cause data errors by eroding the noise margin of the system. Although stubs are unavoidable in a multidrop system, care should be

taken to keep these stubs as short as possible, especially when operating with high data rates. See Figure 10-2, the typical CAN Bus Operating Circuit, termination may be a single 120Ω resistor at the end of the bus, either on the cable or in a terminating node; or split termination, the two 60Ω termination resistors in parallel may be used if filtering and stabilization of the common mode voltage of the bus is desired.

To ensure reliable operation at all data rates and supply voltages, a 0.1μF bypass capacitor is recommended at logic-side and bus-side supply pins (V_{CC1} and V_{CC2}). The capacitors should be placed as close to the supply pins as possible. The PCB designer should follow some critical recommendations in order to get the best performance from the design. For the high-speed operating digital circuit boards, we recommend to use the standard FR-4 PCB material and a minimum of four layers is required to accomplish a low EMI PCB design. Layer order from top-to-bottom is: high-speed signal layer, ground plane, power plane, and low-frequency signal layer. Also, keep the input/output traces as short as possible, avoid using vias to make low-inductance paths for the signals.

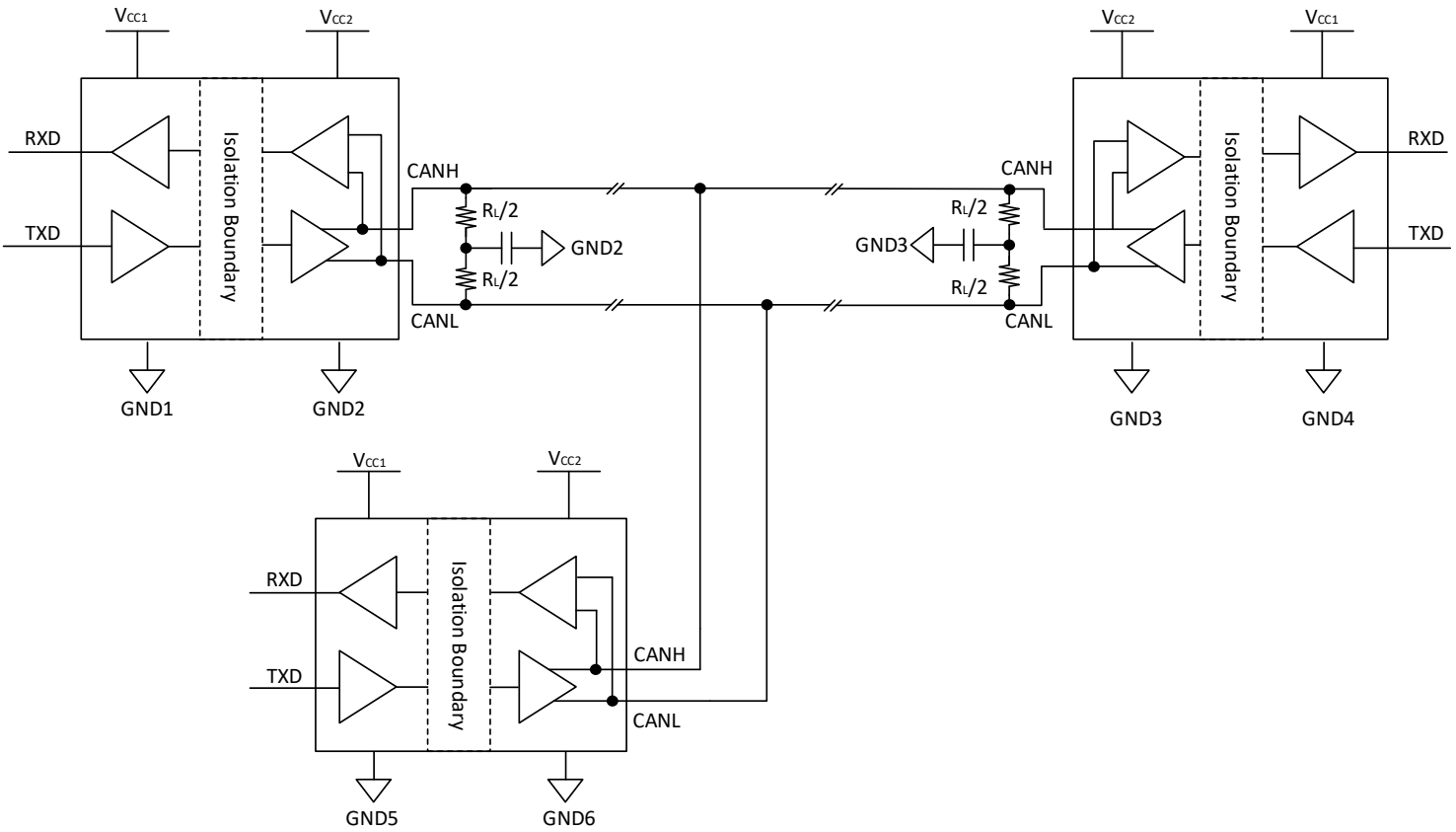
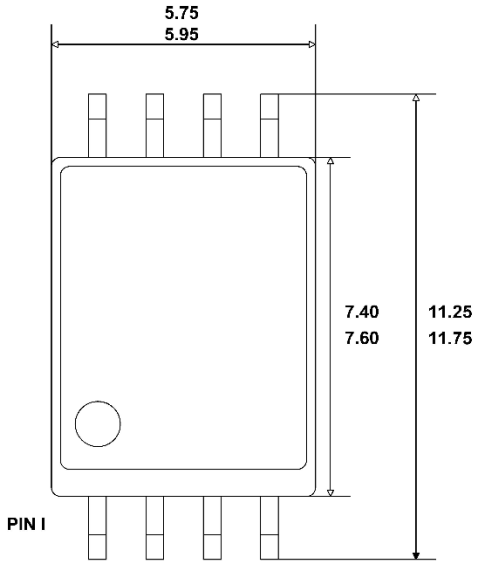


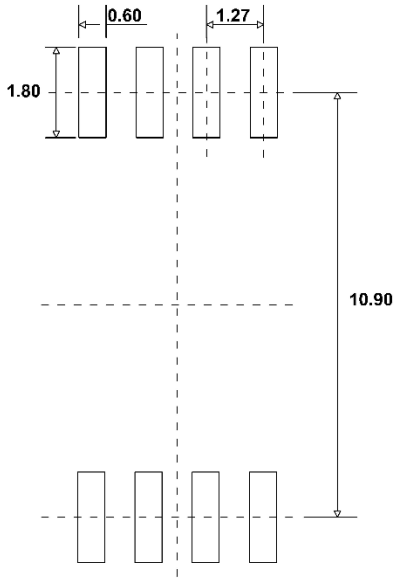
Figure. 10-2 Typical CAN Bus Operating Circuit

11 Package Information

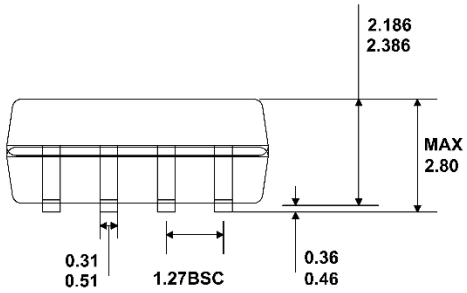
11.1 SOIC8-WB Package Outline



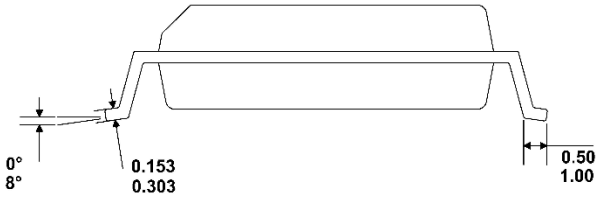
TOP VIEW



RECOMMENDED LAND PATTERN



FRONT VIEW

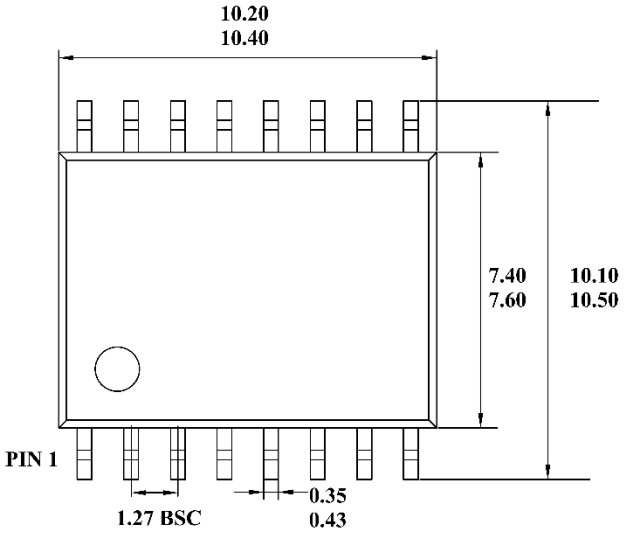


LEFT-SIDE VIEW

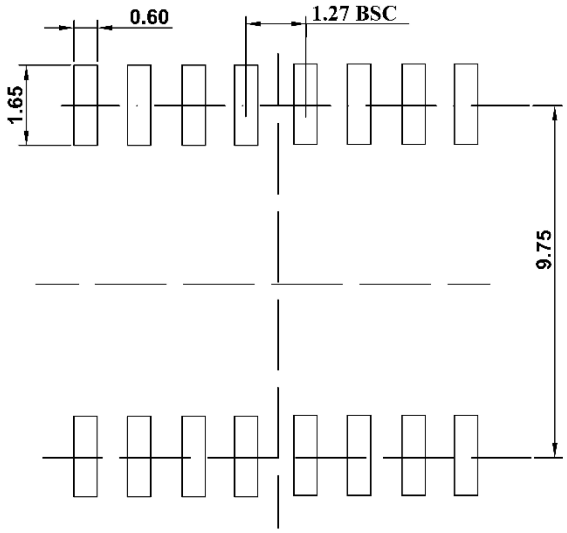
Note:

1. All dimensions are in millimeters; angles are in degrees.

11.2 SOIC16-WB Package Outline



TOP VIEW



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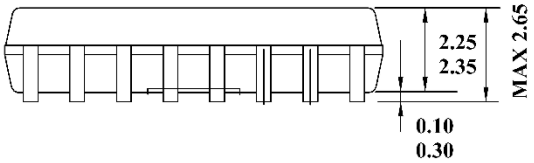
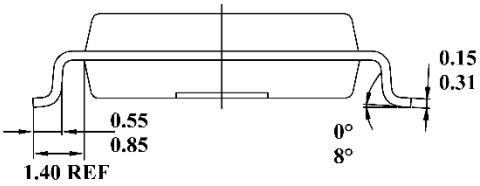


FRONT VIEW

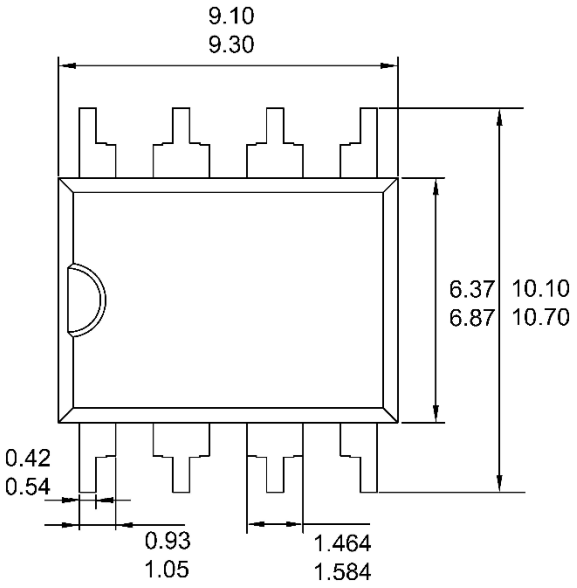


LEFT SIDE VIEW

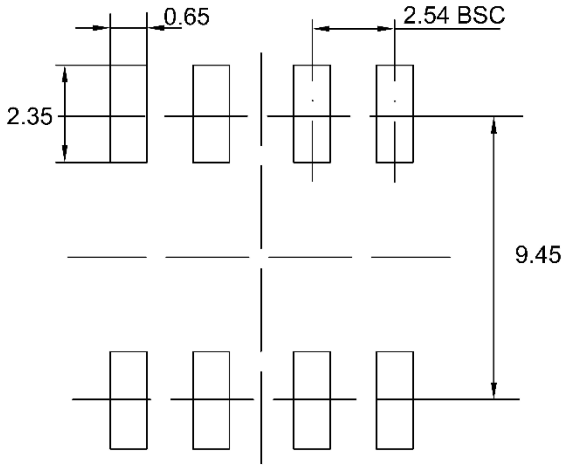
Note:

1. All dimensions are in millimeters; angles are in degrees.

11.3 DUB8 Package Outline



TOP VIEW



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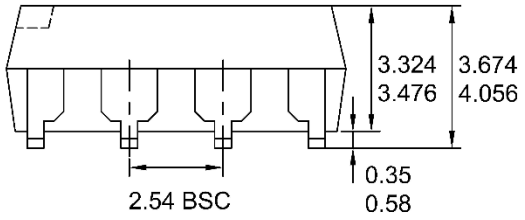
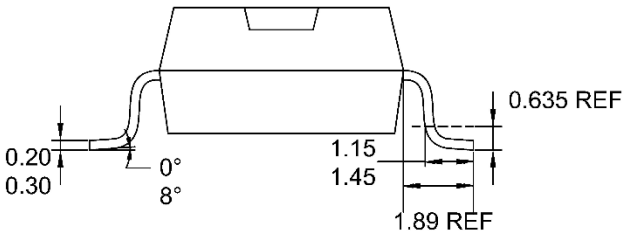


FRONT VIEW



LEFT-SIDE VIEW

Note:

1. All dimensions are in millimeters; angles are in degrees.

12 Soldering Temperature (reflow) Profile

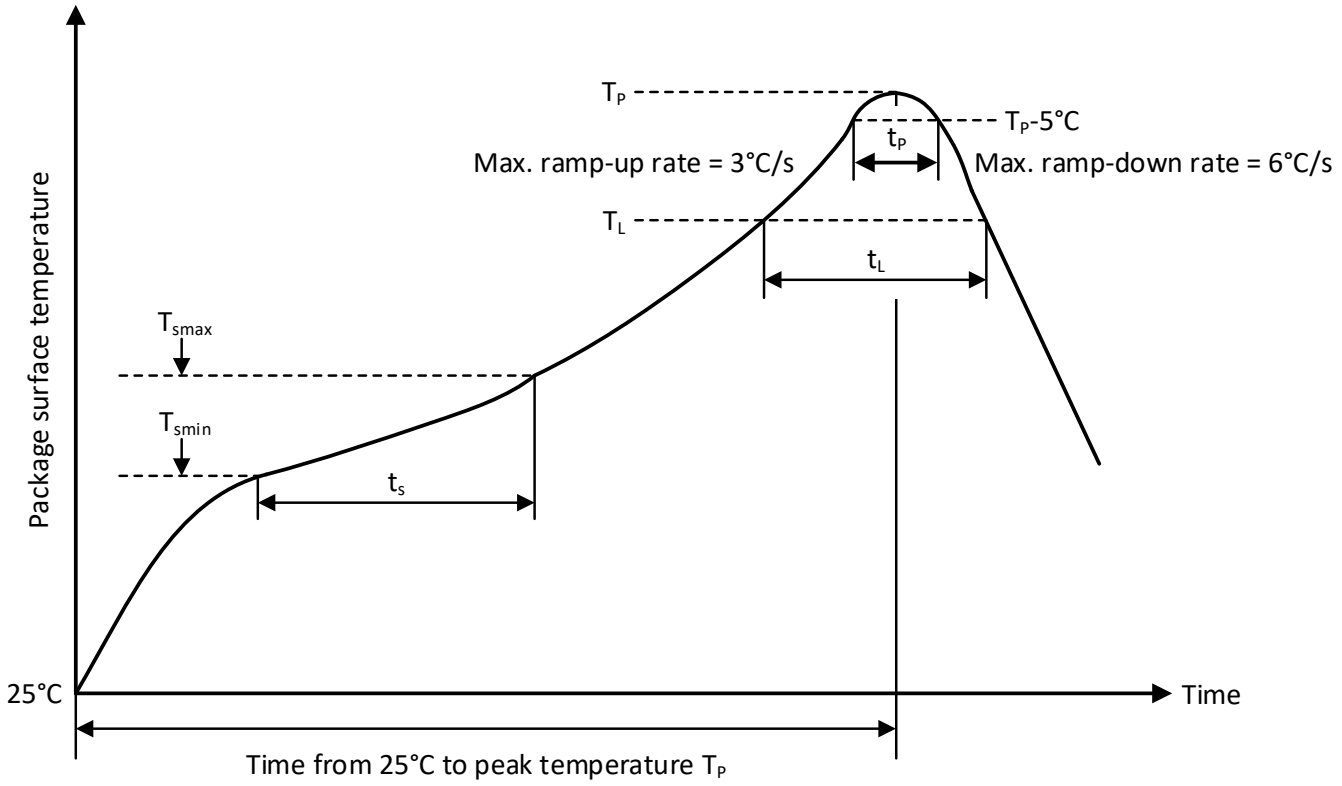
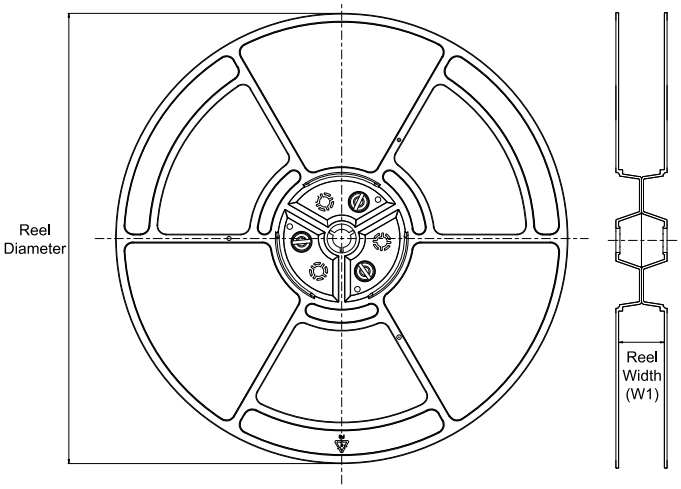


Figure. 12-1 Soldering Temperature (reflow) Profile

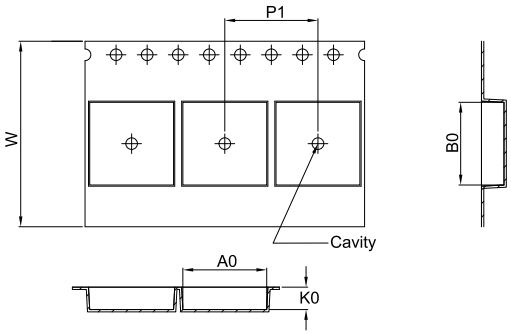
Profile Feature	Pb-Free Soldering
Ramp-up rate (T_L = 217°C to peak T_P)	3°C/s max
Time t_s of preheat temp (T_{smin} = 150°C to T_{smax} = 200°C)	60~120 seconds
Time t_L to be maintained above 217°C	60~150 seconds
Peak temperature T_P	260°C
Time t_P within 5°C of actual peak temp	30 seconds max
Ramp-down rate (peak T_P to T_L = 217°C)	6°C/s max
Time from 25°C to peak temperature T_P	8 minutes max

13 Tape and Reel Information

REEL DIMENSIONS

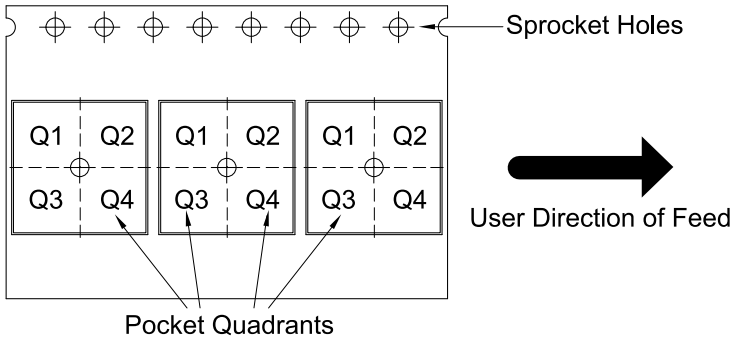


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CA-IS3050CW	SOIC	W	16	1000	330	16.4	10.90	10.70	3.20	12.00	16.00	Q1
CA-IS3050CG	SOIC	G	8	1000	330	16.4	11.95	6.15	3.20	16.00	16.00	Q1
CA-IS3052CW	SOIC	W	16	1000	330	16.4	10.90	10.70	3.20	12.00	16.00	Q1
CA-IS3052CG	SOIC	G	8	1000	330	16.4	11.95	6.15	3.20	16.00	16.00	Q1
CA-IS3050CU	DUB	U	8	800	330	24.4	10.90	9.60	4.30	16.00	24.00	Q1

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