CA-IS2092 Isolated RS-485 Transceiver with Integrated DC-DC Converter

1. Features

- **High-Performance and Compliant with RS-485 EIA/TIA-485 Standard**
  - 0.5Mbps data rate
  - 1/8-unit load enables up to 256 nodes on the bus
  - 3V to 5.5V supply voltage range, and the CA-IS2092VW provides individual logic supply input
- **Integrated DC-DC Converter for Cable-side Power**
  - 3.3V and 5V output options ($V_{ISO} \le V_{CC}$)
  - High integration with internal transformer
  - Soft-start reduces input inrush current
  - Overload and short-circuit protection
  - Thermal shutdown
- **Integrated Protection for Robust Communication**
  - 3.75kV_{RMS} withstand isolation voltage for 60s (galvanic isolation)
  - ±150kV/µs typical CMTI
  - High lifetime: >40 years
  - ±20-kV Human Body Model (HBM) ESD protection on bus I/O, ±6kV HBM ESD protection on logic I/O
  - True fail-safe guarantees known receiver output state
  - Wide operating temperature range: –40°C to 125°C
- **Wide-body SOIC16-WB(W) Package**
- **Safety Regulatory Approvals**
  - VDE certification according to DIN EN IEC 60747-17(VDE 0884-17):2021-10
  - UL certification according to UL 1577
  - CQC certification according to GB4943.1-2022
  - TUV certification

2. Applications

- Industrial Automation Equipment
- Grid infrastructure
- Solar inverter
- Motor drivers
- HVAC

3. General Description

The CA-IS2092x family of devices is galvanically-isolated RS-485 transceivers with built-in isolated DC-DC converter, that eliminates the need for a separate isolated power supply in space constrained isolated designs. All devices of this family have the logic input and output buffers separated by a silicon oxide (SiO_2) insulation barrier that provides up to 3.75kV_{RMS} (60s) of galvanic isolation and ±150kV/µs typical CMTI. Isolation improves data-communication quality by breaking ground loops and reduces noise where there are large differences in ground potential between ports. An integrated DC-DC converter generates the 3.3V or 5V operating voltage for the cable-side.

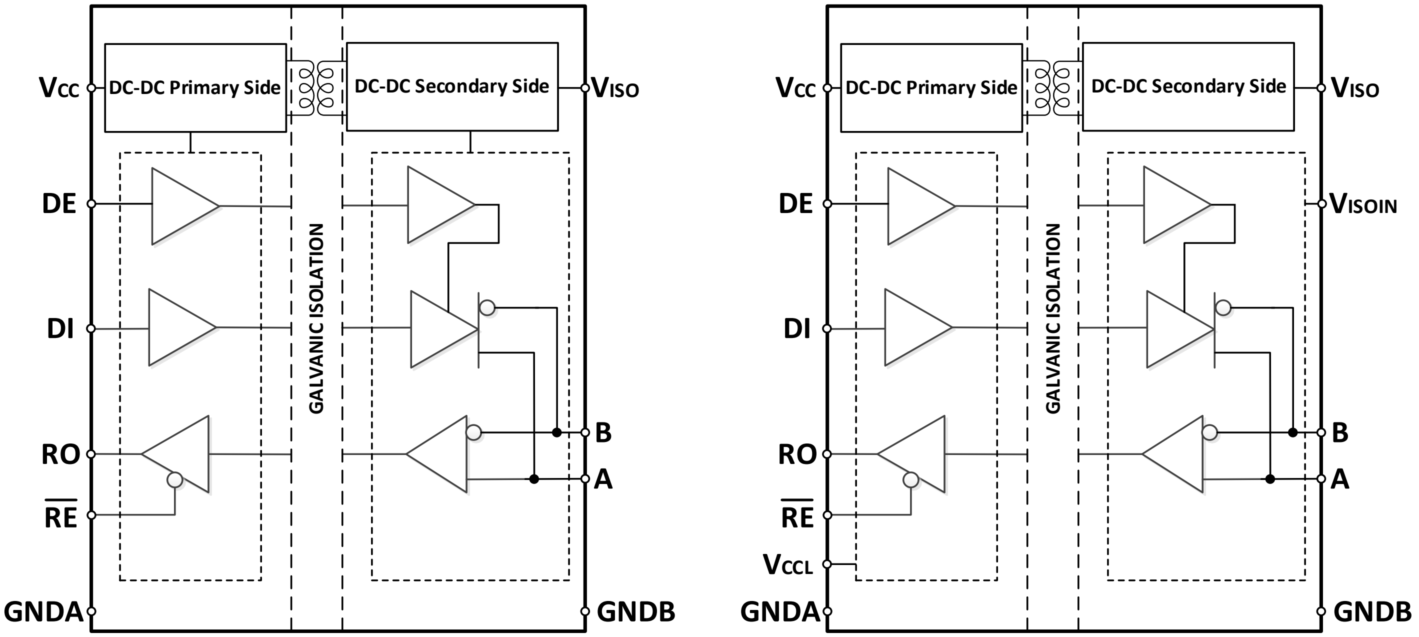
The CA-IS2092x family of devices is designed for multi-drop operation with high ESD protection of up to ±20kV HBM on the bus pins. The receiver is 1/8-unit load, allowing up to 256 transceivers (loads) on a common bus. These devices are half-duplex transceivers and the driver and receiver enable pins let any node at any given moment be configured in either transmit or receive mode which decreases cable requirements. The individual logic supply input of CA-IS2092VW allows fully compatible 2.5V to 5.5V logic on logic input/output lines.

The CA-IS2092x series devices are available in wide-body 16-pin SOIC package which are the industry standard isolated RS-485 package, and operate over -40°C to +125°C temperature range.

Device Information

PART NUMBER	PACKAGE	BODY SIZE (NOM)
CA-IS2092W CA-IS2092VW	SOIC16-WB(W)	10.30 mm × 7.50 mm

CA-IS2092x Function Diagram



CA-IS2092W

CA-IS2092VW

4. Ordering Information

Table 4-1. Ordering Information

Part Number	Full/half duplex	Data Rate (Mbps)	V_{ISO} (V)	V_{DDL}	Package
CA-IS2092W	Half-Duplex	0.5	3.3/5.0	N/A	SOIC16-WB(W)
CA-IS2092VW	Half-Duplex	0.5	3.3/5.0	Yes	SOIC16-WB(W)

Contents

5. Revision History

Revision Number	Description	Revised Date	Page Changed
Version 1.00	Preliminary Version		N/A
Version 1.01	Changed t_{PHZ} and t_{PLZ} value.		10
Version 1.02	Updated POD.	2023/12/19	25
Version 1.03	Changed UL certification information.	2023/05/23	7
Version 1.04	Updated VDE, TUV information	2023/09/19	6, 7
Version 1.05	Updated VDE, UL, CQC, TUV information Updated the test conditions of V_{IOSM}	2024/04/16	1, 6, 7
Version 1.06	1. Updated the writing method of the maximum load current I_{ISO} value and updated its annotation 2. Added notes to CMTI parameters	2024/05/13	9, 10
Version 1.07	Added TUV certification number of IEC62368-1 standard Updated VDE information of V_{IMP} and V_{IOSM} Updated recommended land pattern	2024/12/17	7 6-7 24

6. Pin Configuration and Description

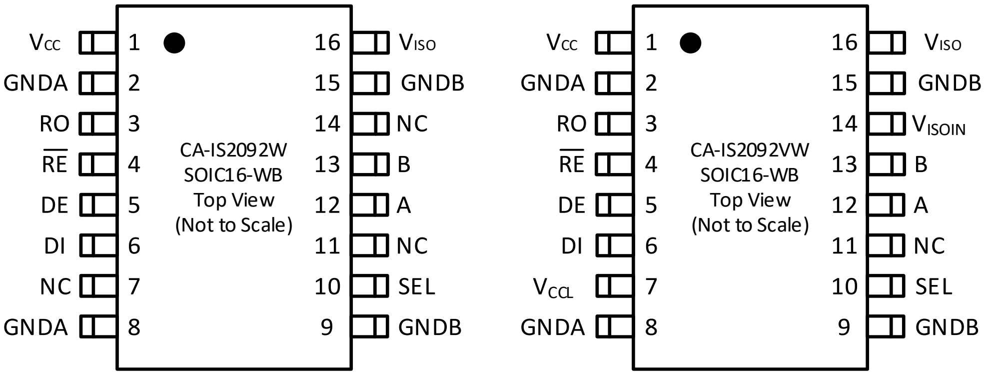


Figure 6-1. CA-IS2092W/CA-IS2092VW SOIC16 Top View

Table 6-1. CA-IS2092W/CA-IS2092VW Pin Description and Functions

Name	PIN Number		Type	Description
	CA-IS2092W	CA-IS2092VW		
V_{CC}	1	1	Power Supply	Logic-Side Power Input and DC-DC converter supply input. Bypass V_{CC} to GNDA with both 0.1µF and at least 10µF capacitors as close to the device as possible.
GNDA	2, 8	2, 8	GND	Logic-Side Ground. GNDA is the ground reference for digital signals of logic side.
RO	3	3	Digital I/O	Receiver Data Output. Drive $\overline{RE}$ low to enable receiver R_X. With $\overline{RE}$ low, RO is high when (V_A –V_B) > -20mV and is low when (V_A – V_B) < -200mV. RO is high impedance when $\overline{RE}$ is high.
$\overline{RE}$	4	4	Digital I/O	Receiver Output Enable. Driver $\overline{RE}$ low or connect to GNDA to enable R_X. Drive $\overline{RE}$ high to disable R_X. RO is high-impedance when $\overline{RE}$ is high.
DE	5	5	Digital I/O	Driver Output Enable. Drive DE high to enable bus driver outputs. Drive DE low or connect to GNDA to disable bus driver outputs. DE has an internal weak pull-down to GNDA.
DI	6	6	Digital I/O	Driver Input. With DE high, a logic low on DI forces the noninverting output (A) low and the inverting output (B) high; a logic high on DI forces the noninverting output high and the inverting output low.
V_{CCL}[1]	---	7	Power Supply	Logic-supply input. V_{CCL} is the logic supply voltage for logic-side input/output. Bypass to GNDA with a 1µF capacitor.
NC	7	---	---	No internal connection on logic side.
GNDB	9, 15	9, 15	GND	Cable Side Ground. GNDB is the ground reference for the RS-485 bus signals.
SEL[2]	10	10	Digital I/O	Output voltage V_{ISO} select pin: V_{ISO} = 5.0 V when SEL is shorted to V_{ISO}; V_{ISO} = 3.3 V when SEL is shorted to GNDB or floating;
NC	11, 14	11	---	No internal connection on cable side.
A	12	12	Bus I/O	Non-inverting RS-485 receiver input and driver output.
B	13	13	Bus I/O	Inverting RS-485 receiver input and driver output.
V_{ISOIN}	---	14	Power Supply	Cable side power supply input. Bypass V_{ISOIN} to GNDB with at least 1µF capacitor as close to the device as possible.
V_{ISO}	16	16	Power Supply	Isolated DC-DC power supply output. Cable Side Power supply. Bypass V_{ISO} to GNDB with both 0.1µF and at least 10µF capacitors as close to the device as possible.

Notes:

1. Logic-Supply Input. V_{CCL} can be different voltage from V_{CC} supply, which allows fully compatible +2.7V to +5.5V logic for digital input/output.
2. $V_{ISO} \leq V_{CC}$, this means if V_{CC} = 3.3V, SEL pin must be floating or connected to GNDB and set the V_{IOS} output to 3.3V; if V_{CC} = 5.0V, there is no connection limit for SEL pin.

7. Specifications

7.1. Absolute Maximum Ratings[1]

PARAMETER		MIN	MAX	UNIT
V_{CC}, V_{CCL}	Logic-side Supply Voltage[2]	-0.5	6.0	V
V_{ISO}, V_{ISOIN}	Cable-side Supply Voltage[2]	-0.5	6.0	V
V_{IO1}	Logic Voltage (DI, DE, $\overline{RE}$, RO)	-0.5	$V_{CC}/V_{CCL} + 0.5$[3]	V
V_{IO2}	Cable-side logic voltage (SEL)	-0.5	$V_{ISO}/V_{ISOIN} + 0.5$[3]	V
V_{BUS}	Voltage on bus I/Os (A, B)	-8	13	V
I_O	Output current on RO	-20	20	mA
T_J	Junction Temperature		150	°C
T_{STG}	Storage Temperature	-65	150	°C

Notes:

1. The stresses listed under "Absolute Maximum Ratings" are stress ratings only, not for functional operation condition. Exposure to absolute maximum rating conditions for extended periods may cause permanent damage to the device.
2. All voltage values except differential I/O bus voltages are with respect to the local ground (GNDA or GNDB) and are peak voltage values.
3. Maximum voltage must not exceed 6V.

7.2. ESD Ratings

PARAMETER			VALUE	UNIT
V_{ESD} Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001	Bus pins to GNDB	±20	kV
		Other pins on cable-side to GNDB	±6	
		All pins on logic-side to GNDA	±6	
	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins		±2	

7.3. Recommended Operating Conditions

PARAMETER		Min	Typ	Max	Unit
V_{CC}[1]	Supply voltage on logic side	3.15	3.3 or 5	5.5	V
V_{CCL}	Logic supply voltage	2.375	3.3 or 5	5.5	V
V_{OC}	Common mode voltage at bus pins: A, B, Y and Z	-7		12	V
V_{ID}	Differential input voltage V_{AB}	-12		12	V
RL	Differential load	54			Ω
V_{IH}	Input high voltage (DI, DE to GNDA)	2.0		V_{CC}/V_{CCL} +0.3	V
V_{IL}	Input low voltage (DI, DE to GNDA)	-0.3		0.8	V
V_{IH}	Input high voltage ($\overline{RE}$ to GNDA)	0.7 x V_{CC}/V_{CCL}		V_{CC}/V_{CCL} +0.3	V
V_{IL}	Input low voltage ($\overline{RE}$ to GNDA)	-0.3		0.3 x V_{CC} /V_{CCL}	V
DR	Data rate of the CA-IS2092W/CA-IS2092VW			0.5	Mbps
T_A	Ambient Temperature	-40		125	°C

Note:

1. $V_{ISO} \le V_{CC}$, this means if V_{CC} = 3.3V, SEL pin must be floating or connected to GNDB and set the V_{IOS} output to 3.3V; if V_{CC} = 5.0V, there is no connection limit for SEL pin.

7.4. Thermal Information

THERMAL METRIC		CA-IS2092x	Unit
		SOIC16-WB (W)	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	68.5	°C/W

7.5. Insulation Specifications

PARAMETER		TEST CONDITIONS	VALUE	UNIT
			W	
CLR	External clearance[1]	Shortest terminal-to-terminal distance through air	8	mm
CPG	External creepage[1]	Shortest terminal-to-terminal distance across the package surface	8	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	28	μm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	>600	V
	Material group	According to IEC 60664-1	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 150 V_{RMS}	I-IV	
		Rated mains voltage ≤ 300 V_{RMS}	I-IV	
		Rated mains voltage ≤ 600 V_{RMS}	I-IV	
		Rated mains voltage ≤ 1000 V_{RMS}	I-III	
DIN V VDE V 0884-17:2021-10[2]				
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	1414	V_{PK}
V_{IOWM}	Maximum operating isolation voltage	AC voltage; time-dependent dielectric breakdown (TDDB) test	1000	V_{RMS}
		DC voltage	1414	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t=60 s (qualification); $V_{TEST} = 1.2 \times V_{IOTM}$, t=1 s (100% product test)	7070	V_{PK}
V_{IMP}	Maximum impulse voltage	1.2/50 μs waveform per IEC 62368-1	9846	V_{PK}
V_{IOSM}	Maximum surge isolation voltage[3]	$V_{IOSM} \geq 1.3 \times V_{IMP}$; Tested in oil (qualification test) , 1.2/50 μs waveform per IEC 62368-1	12800	V_{PK}
q_{pd}	Apparent charge[4]	Method a, after input/output safety tests subgroup 2/3, $V_{ini} = V_{IOTM}$, $t_{ini} = 60s$; $V_{pd(m)} = 1.2 \times V_{IORM}$, $t_m = 10s$	≤5	pC
		Method a, after environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, $t_{ini} = 60s$; $V_{pd(m)} = 1.3 \times V_{IORM}$, $t_m = 10s$	≤5	
		Method b1, at routine test (100% production test) and preconditioning (sample test) $V_{ini} = 1.2 \times V_{IOTM}$, $t_{ini} = 1s$; $V_{pd(m)} = 1.5 \times V_{IORM}$, $t_m = 1s$	≤5	
C_{IO}	Barrier capacitance, input to output[5]	$V_{IO} = 0.4 \times \sin(2\pi ft)$, f = 1 MHz	~3.5	pF
R_{IO}	Isolation resistance, input to output[5]	$V_{IO} = 500V$, $T_A = 25°C$	$>10^{12}$	Ω
		$V_{IO} = 500V$, $100°C \leq T_A \leq 125°C$	$>10^{11}$	
		$V_{IO} = 500V$ at $T_S = 150°C$	$>10^{9}$	
	Pollution degree		2	
UL 1577				
V_{ISO}	Maximum withstanding isolation voltage	$V_{TEST} = V_{ISO}$, t = 60s (qualification), $V_{TEST} = 1.2 \times V_{ISO}$, t = 1s (100% production)	3750	V_{RMS}

NOTE:

1. Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications.
2. This coupler is suitable for safe electrical insulation only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
3. Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
4. Apparent charge is electrical discharge caused by a partial discharge (pd).
5. All pins on each side of the barrier tied together creating a two-terminal device.

7.6. Safety-Related Certifications

VDE	UL	CQC	TUV
Certified according to DIN EN IEC 60747-17(VDE 0884-17):2021-10; EN IEC 60747-17:2020+AC:2021	Certified according to UL 1577 Component Recognition Program	Certified according to GB4943.1-2011	Certified according to EN 61010-1 and EN 62368-1
Reinforced insulation: V_{IORM}: 1414V_{PK} V_{IOTM}: 7070V_{PK} V_{IOSM}: 12800V_{PK}	Single Protection 5000V_{RMS}	Reinforced insulation (Altitude ≤ 5000m)	EN 61010-1: 5000V_{RMS} EN 62368-1: 5000V_{RMS}
Certification number: 40057278 (Reinforced insulation)	Certification number: E511334	Certification number: CQC23001406424	Client reference number: 2253313

7.7. Electrical Characteristics

7.7.1. Driver

All typical specs are at V_{CC} = 5V, V_{CCL} = V_{CC}, V_{ISOIN} = V_{ISO}, T_A = 25°C, Min/Max specs are over recommended operating conditions unless otherwise specified.

Parameter		Test Condition	Min	Typ	Max	Unit
$\lvert V_{OD1} \rvert$	Driver differential output voltage	I_O = 0mA, unloaded bus. SEL = LOW or float		2.9		V
		I_O = 0mA, unloaded bus. SEL = HIGH	3.7	4.6		
$\lvert V_{OD2} \rvert$	Driver differential output voltage	R_L=54Ω, see Figure 8-1, SEL = LOW or float	1.5	2		V
		R_L=54Ω, see Figure 8-1, SEL = HIGH	2.1	3.6		
$\lvert V_{OD3} \rvert$	Driver differential output voltage with bus load	V_{test} = -7V to 12V, see Figure 8-1	1.5			V
$\Delta\lvert V_{OD} \rvert$	Change in differential output voltage between two states	R_L=54Ω, or R_L=100Ω, see Figure 8-1	-0.2		0.2	V
V_{OC}	Common-mode output voltage	R_L=54Ω, or R_L=100Ω, see Figure 8-1	1	$V_{ISO}/2$	3	V
ΔV_{OC}	Change in steady-state common-mode output voltage between two states	R_L=54Ω, or R_L=100Ω, see Figure 8-1	-0.2		0.2	V
I_{IH}, I_{IL}	Input leakage current	DI, DE = low or high	-20		20	μA
I_{os}	Short-circuit output current (V_O = HIGH)	DE = V_{CC}, DI = 0V or V_{CC}, V_A or V_B = -7V	-150		150	mA
		DE = V_{CC}, DI = 0V or V_{CC}, V_A or V_B = 12V				
CMTI[1]	Common mode transient immunity	V_{CM} = 1500V; See Figure 8-6	100	150		kV/μs

Notes:

1. The test data is based on bench test and design simulation.

7.7.2. Receiver

All typical specs are at V_{CC} = 5V, V_{CCL} = V_{CC}, V_{ISOIN} = V_{ISO}, T_A = 25°C, Min/Max specs are over recommended operating conditions unless otherwise specified.

	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output logic high voltage	V_{CC}=5V, I_{OH}=4mA	V_{CC}-0.4	4.8		V
		V_{CC}=3.3V, I_{OH}=-4mA	V_{CC}-0.4	3		
V_{OL}	Output logic low voltage	V_{CC}=5V, I_{OL}=4mA		0.2	0.4	V
		V_{CC}=3.3V, I_{OL}=4mA		0.2	0.4	
$V_{IT+(IN)}$	Positive-going input threshold voltage			-110	-50	mV
$V_{IT-(IN)}$	Negative-going input threshold voltage		-200	-140		mV
$V_{I(HYS)}$	Receiver input hysteresis			30		mV
I_I	Bus input current	V_A or V_B =12V, other inputs = 0 V		75	125	μA
		V_A or V_B =12V, V_{CC} = 0 V, other inputs = 0 V		80	125	
		V_A or V_B = -7 V, other inputs = 0 V	–100	–40		
		V_A or V_B = -7 V, V_{CC} = 0 V, other inputs = 0 V	–100	–40		
I_{IH}	Input current on $\overline{RE}$ pin	V_{IH} = V_{CC}	-20		20	μA
I_{IL}	Input current on $\overline{RE}$ pin	V_{IL} = 0 V	-20		20	μA
R_{ID}	Differential input resistance	Between A and B, -7V < V_{CM} < 12V	96			KΩ

7.8. Supply Current

All typical specs are at V_{CC} = 5V, V_{CCL} = V_{CC}, V_{ISOIN} = V_{ISO}, T_A = 25°C, Min/Max specs are over recommended operating conditions.

Parameter		Test Condition		Min	Typ	Max	Unit
Isolated Power Supply (without bus load across A and B, unless otherwise specified.)							
V_{ISO}	Isolated supply output	I_{ISO} = 0 to 130mA, V_{CC} = 5V, SEL = GNDB or V_{ISO}		4.75	5	5.25	V
		I_{ISO} = 0 to 75mA, V_{CC} = 3.3V, SEL = GNDB		3.13	3.3	3.47	
I_{ISO}	Maximum load current[1]	R_L = NC[2]	V_{CC} = 5V, SEL = GNDB or V_{ISO}	130			mA
			V_{CC} = 3.3V, SEL = GNDB	75			
		R_L = 100Ω	V_{CC} = 5V, SEL = V_{ISO}	80			
			V_{CC} = 5V, SEL = GNDB	105			
			V_{CC} = 3.3V, SEL = GNDB	40			
		R_L = 54Ω	V_{CC} = 5V, SEL = V_{ISO}	55			
			V_{CC} = 5V, SEL = GNDB	85			
			V_{CC} = 3.3V, SEL = GNDB	30			
$V_{ISO(LINE)}$	DC line regulation	I_{ISO} = 50mA, V_{CC} = 4.5 to 5.5V, SEL = GNDB or V_{ISO}			2		mV/V
		I_{ISO} = 50mA, V_{CC} = 3.15 to 3.6V, SEL = GNDB					
$V_{ISO(LOAD)}$	DC load regulation	I_{ISO} = 0 to 130mA, V_{CC} = 5V, SEL = GNDB or V_{ISO}			1%		
		I_{ISO} = 0 to 75mA, V_{CC} = 3.3V, SEL = GNDB					
EFF	Efficiency @ maximum load current	I_{ISO} = 130mA, C_{LOAD} = 0.1µF// 10µF	V_{CC} = 5V, SEL = V_{ISO}		53%		
			V_{CC} = 5V, SEL = GNDB		42%		
		I_{ISO} = 75mA, C_{LOAD} = 0.1µF// 10µF	V_{CC} = 3.3V, SEL = GNDB		47%		
Quiescent current, DE = V_{CC}, $\overline{RE}$ = 0V, DI = 0V							
I_{CC}	Supply current on logic side	R_L = NC[2]	V_{CC} = 3.3V, SEL = GNDB		17	28	mA
			V_{CC} = 5.0V, SEL = GNDB		15	22	
			V_{CC} = 5.0V, SEL = V_{ISO}		18	28	
		R_L = 54Ω	V_{CC} = 3.3V, SEL = GNDB		94	125	
			V_{CC} = 5.0V, SEL = GNDB		82	120	
			V_{CC} = 5.0V, SEL = V_{ISO}		140	200	
		R_L = 100Ω	V_{CC} = 3.3V, SEL = GNDB		65	95	
			V_{CC} = 5.0V, SEL = GNDB		55	80	
			V_{CC} = 5.0V, SEL = V_{ISO}		93	135	
		R_L = 120Ω	V_{CC} = 3.3V, SEL = GNDB		57	88	
			V_{CC} = 5.0V, SEL = GNDB		50	72	
			V_{CC} = 5.0V, SEL = V_{ISO}		83	120	
Average operating current, DE = V_{CC}, $\overline{RE}$ = 0V, DI = 250kHz square-wave, 50% duty cycle.							
I_{CC}	Supply current on logic side	R_L = 54Ω	V_{CC} = 3.3V, SEL = GNDB		92	125	mA
			V_{CC} = 5V, SEL = GNDB		85	120	
			V_{CC} = 5V, SEL = V_{ISO}		145	210	
		R_L = 100Ω	V_{CC} = 3.3V, SEL = GNDB		65	95	
			V_{CC} = 5V, SEL = GNDB		60	85	
			V_{CC} = 5V, SEL = V_{ISO}		100	145	
		R_L = 120Ω	V_{CC} = 3.3V, SEL = GNDB		60	85	
			V_{CC} = 5V, SEL = GNDB		55	80	
			V_{CC} = 5V, SEL = V_{ISO}		95	140	

Notes:

1. DE = V_{CC}, $\overline{RE}$ = 0V, DI = 0V or V_{CC}; The available output current from V_{ISO} will be reduced when T_A > 85˚C, see Figure7-14, Figure7-16, Figure7-18, the maximum output current of V_{ISO} vs. temperature.
2. R_L is bus load across A and B, R_L= NC means no-load connection between A and B.

7.9. Switching Characteristics

7.9.1. Driver

All typical specs are at V_{CC} = 5V, V_{CCL} = V_{CC}, V_{ISOIN} = V_{ISO}, T_A = 25°C, Min/Max specs are over recommended operating conditions unless otherwise specified.

Parameters		Test conditions	Min	Typ	Max	Unit
t_{PLH},t_{PHL}	Driver Propagation Delay	See Figure 8-2		100	250	ns
t_{PWD}	Driver output skew |t_{PLH} - t_{PHL}|			5	20	ns
t_r,t_f	Differential output rise/full time			150	500	ns
t_{PZH},t_{PZL}	Driver enable time	See Figure 8-3		300	800	ns
t_{PHZ},t_{PLZ}	Driver disable time			20	50	ns

7.9.2. Receiver

All typical specs are at V_{CC} = 5V, V_{CCL} = V_{CC}, V_{ISOIN} = V_{ISO}, T_A = 25°C, Min/Max specs are over recommended operating conditions unless otherwise specified.

Parameters		Test conditions	Min	Typ	Max	Unit
t_{PLH},t_{PHL}	Receiver propagation delay	See Figure 8-4.		50	100	ns
t_{PWD}	Receiver output skew |t_{PLH} - t_{PHL}|				12	ns
t_r,t_f	Receiver output rise/full time			2.5	4	ns
t_{PHZ},t_{PLZ}	Receiver disable time	See Figure 8-5.		20	50	ns
t_{PZH},t_{PZL}	Receiver enable time, DE = 0V			30	80	ns

7.10. Typical Operating Characteristics

All typical specs are at V_{CC} = 5V, V_{CCL} = V_{CC}, V_{ISOIN} = V_{ISO}, T_A = 25°C, Min/Max specs are over recommended operating conditions unless otherwise specified.

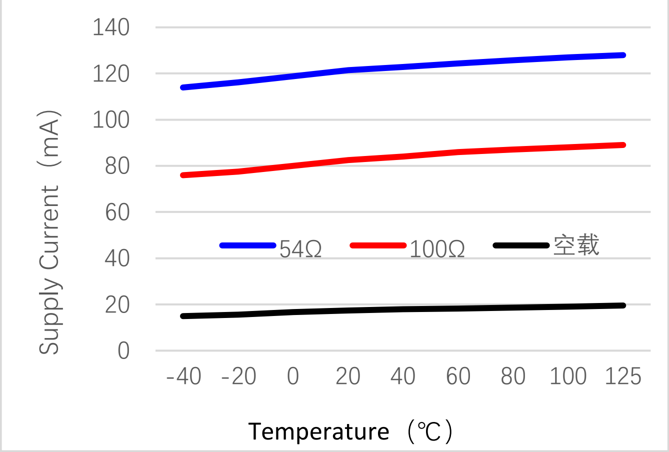


Figure 7-1.
Logic-side supply current (I_{CC}) at different bus load
V_{CC} = 5V, V_{ISO} = 5V, DR = 500kbps

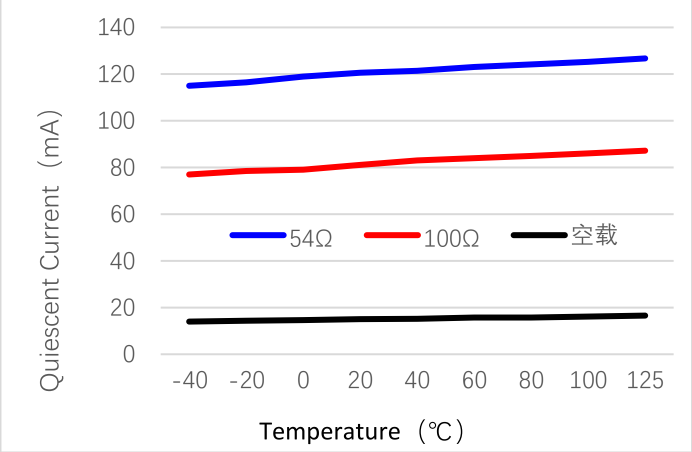


Figure 7-2.
Logic-side supply quiescent Current at different bus load
V_{CC} = 5V，V_{ISO} = 5V， DI = Low

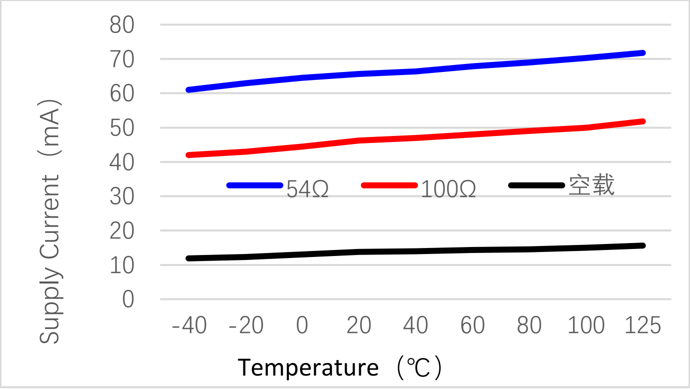


Figure 7-3.
Logic-side supply current (I_{CC}) at different bus load
V_{CC} = 5V, V_{ISO} = 3.3V, DR = 500kbps

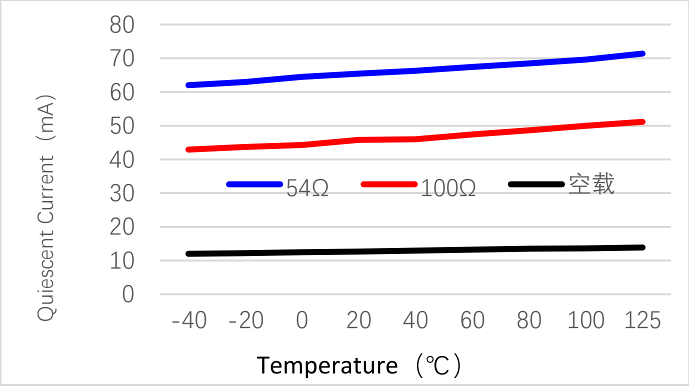


Figure 7-4.
Logic-side supply quiescent Current at different bus load
V_{CC} = 5V，V_{ISO} = 3.3V， DI = Low

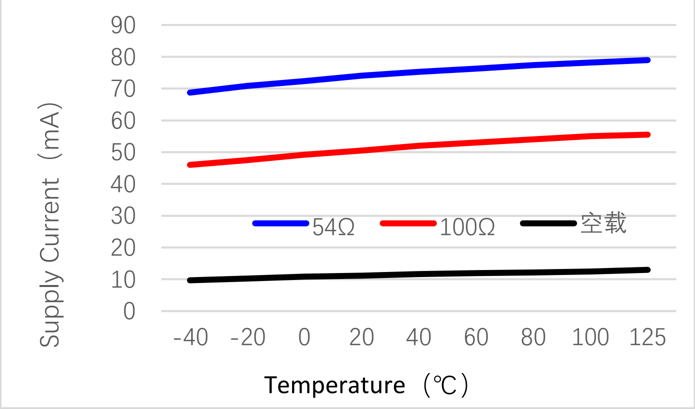


Figure 7-5.
Logic-side supply current (I_{CC}) at different bus load
V_{CC} = 3.3V, V_{ISO} = 3.3V, DR = 500kbps

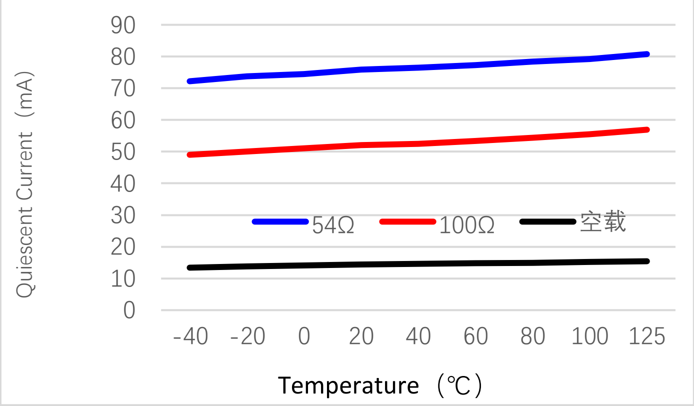


Figure 7-6.
Logic-side supply quiescent Current at different bus load
V_{CC} = 3.3V，V_{ISO} = 3.3V， DI = Low

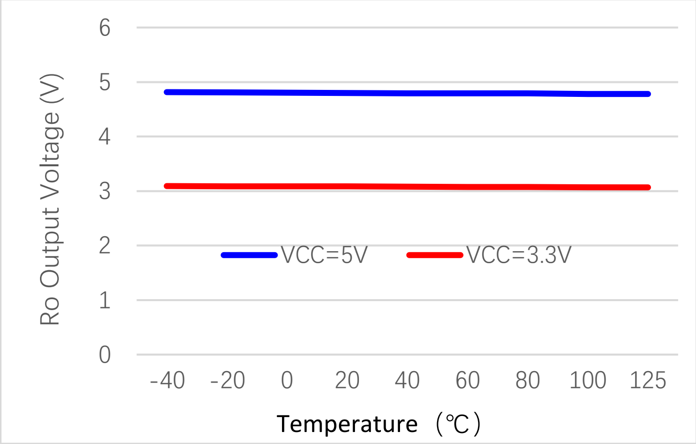


Figure 7-7.
R_O = High, R_O pull-down current is 4mA

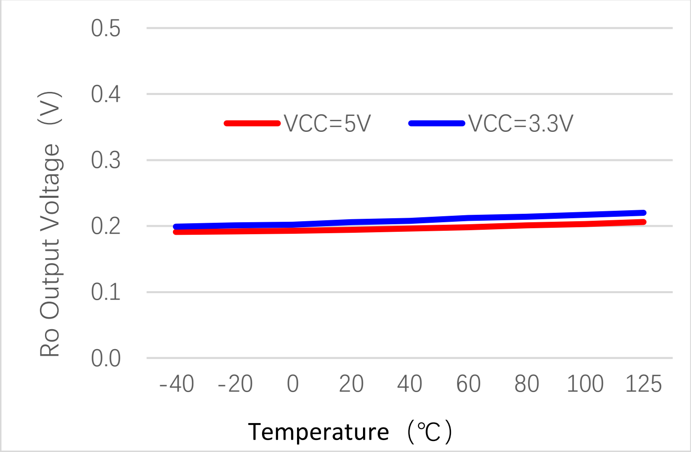


Figure 7-8.
R_O = Low, R_O pull-up current = 4mA

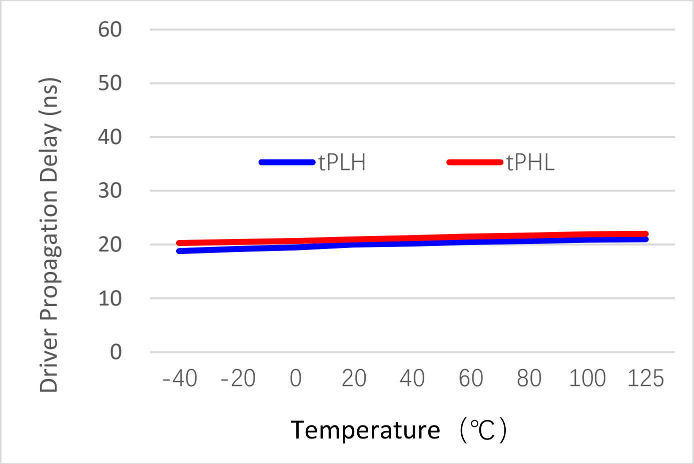


Figure 7-9. Driver propagation delay
V_{CC} = 3.3V, V_{ISO} = 3.3V, R_L = 54Ω

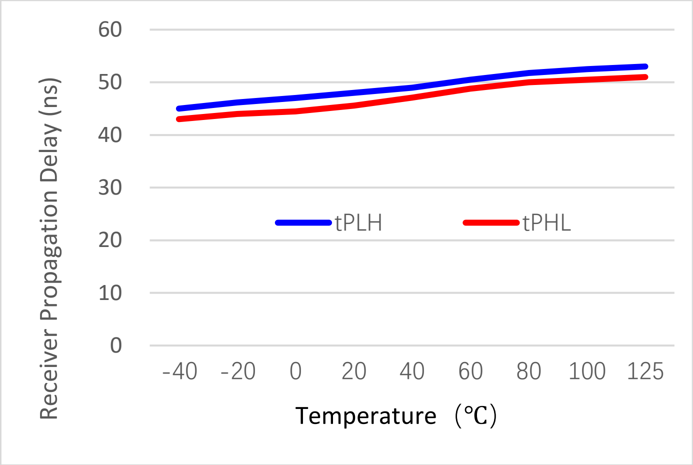


Figure 7-10. Receiver propagation delay
V_{CC} = 3.3V, V_{ISO} = 3.3V, R_L = 54Ω

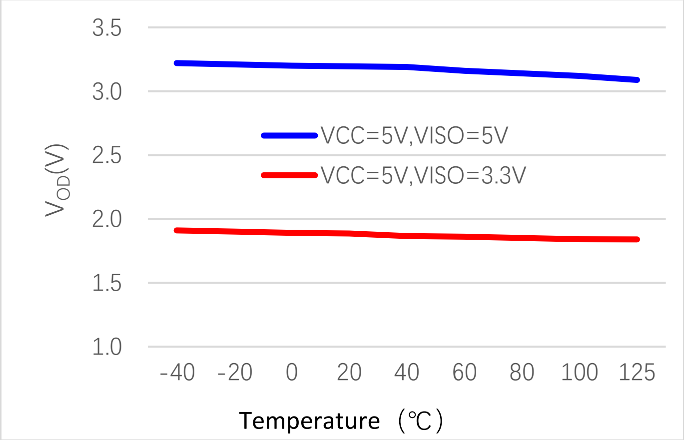


Figure 7-11.
Differential output voltage V_{OD}, R_L = 54Ω, V_{CC} = 5V

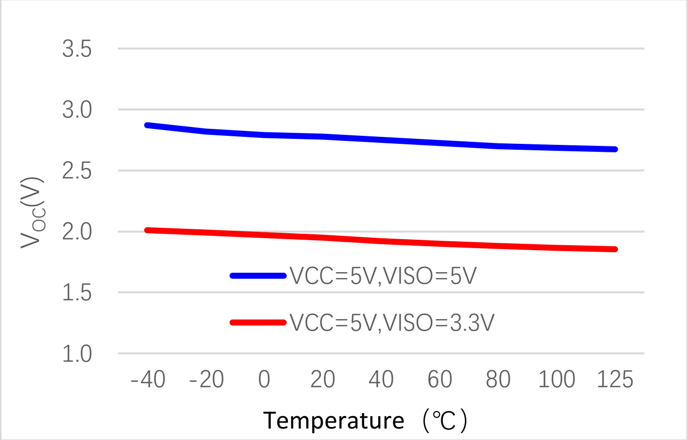


Figure 7-12.
Common-mode output voltage V_{OC}, R_L = 54Ω, V_{CC} = 5V

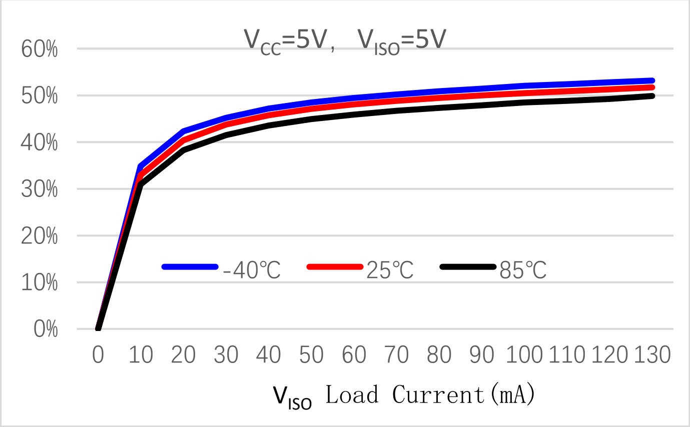


Figure 7-13.
Efficiency vs. load current (I_{ISO}) at different ambient temperature
V_{CC} = 5V, V_{ISO} = 5V, R_L = NC

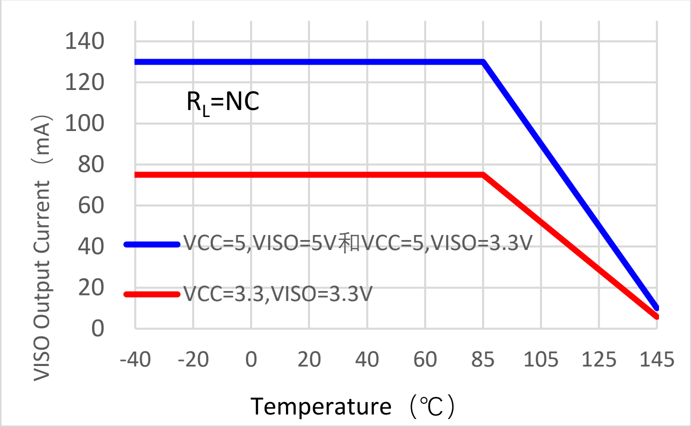


Figure 7-14.
Maximum output current from V_{ISO} vs. temperature with R_L = NC
Without data transmission

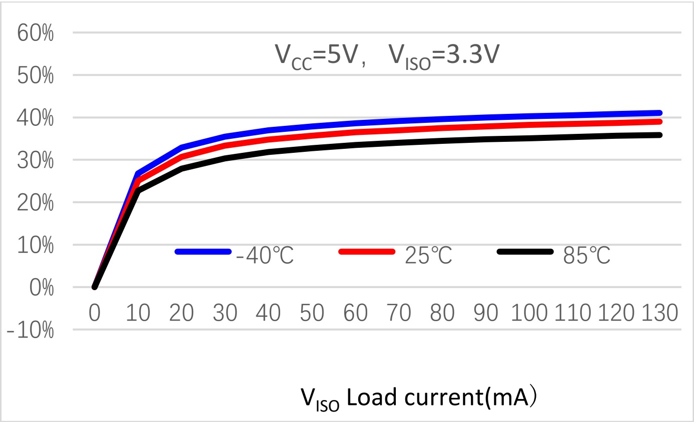


Figure 7-15.
Efficiency vs. load current (I_{ISO}) at different ambient temperature
V_{CC} = 5V, V_{ISO} = 3.3V, R_L = NC

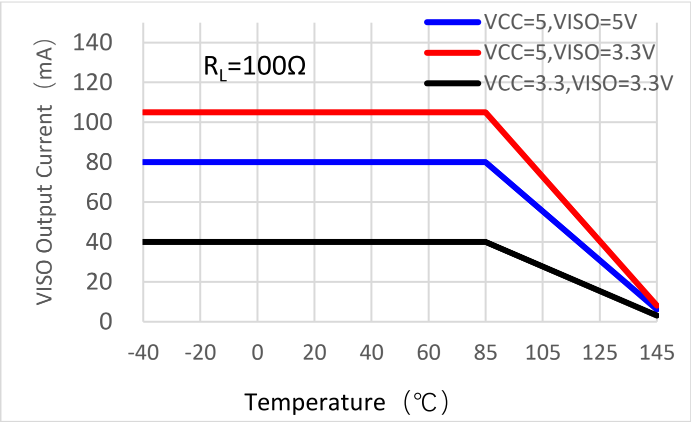


Figure 7-16.
Maximum output current from V_{ISO} vs. temperature with R_L = 100Ω
CA-IS2092x：DR = 500kbps, C_L = 2nF

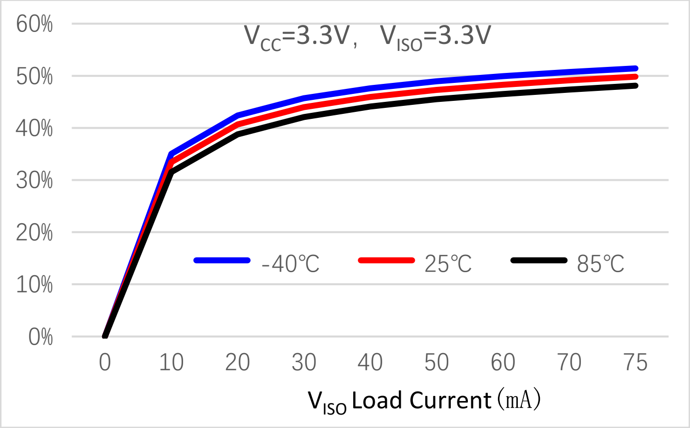


Figure 7-17.
Efficiency vs. load current (I_{ISO}) at different ambient temperature
V_{CC} = 3.3V, V_{ISO} = 3.3V, R_L = NC

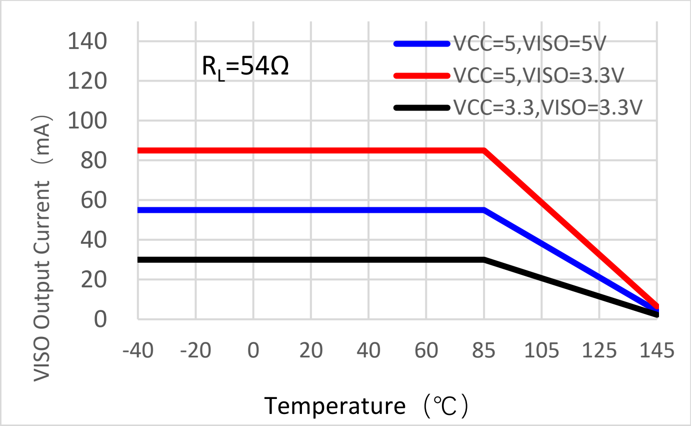


Figure 7-18.
Maximum output current from V_{ISO} vs. temperature with R_L = 54Ω
CA-IS2092x：DR = 500kbps, C_L = 2nF

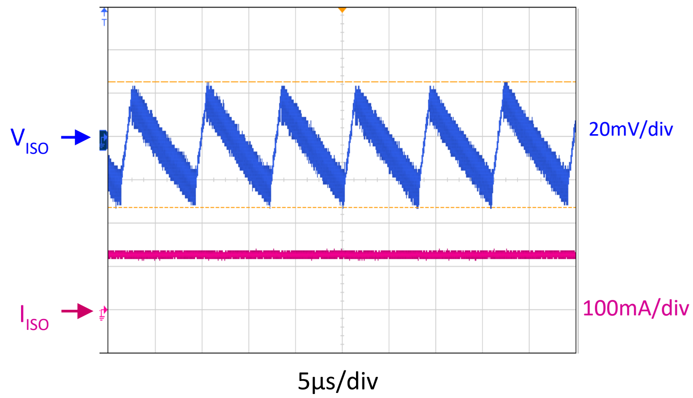


Figure 7-19.
V_{CC} = 5V, V_{ISO} = 5V, R_L = NC, I_{ISO} = 130mA
V_{ISO} Ripple Voltage: 58mV$_{P-P}$

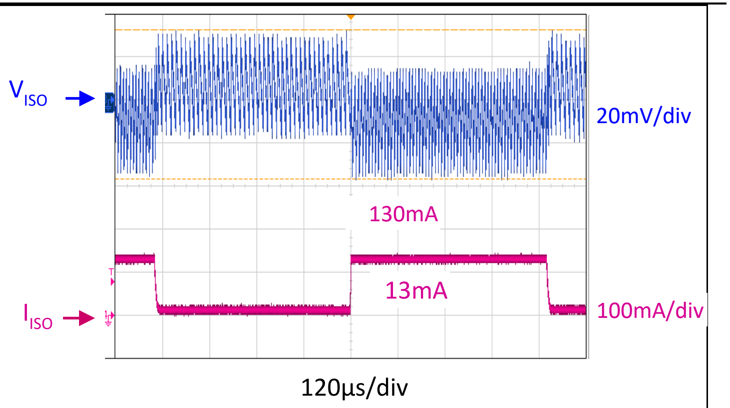


Figure 7-20.
V_{CC} = 5V, V_{ISO} = 5V, 13mA to 130mA I_{ISO} load transient, R_L = NC
V_{ISO} Ripple Voltage: 68mV$_{P-P}$

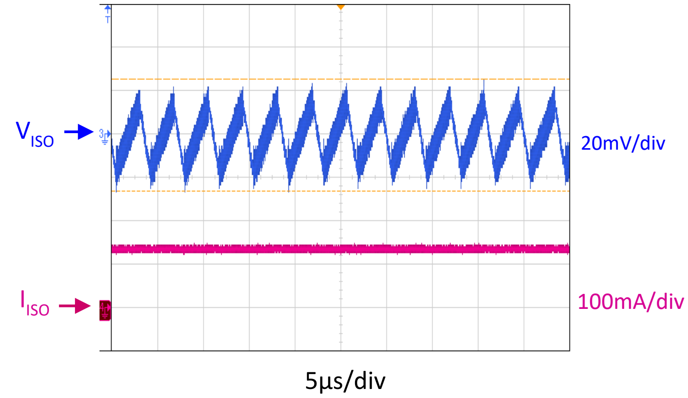


Figure 7-21.
V_{CC} = 5V, V_{ISO} = 3.3V, R_L = NC, I_{ISO} = 130mA
V_{ISO} Ripple Voltage: 51mV$_{P-P}$

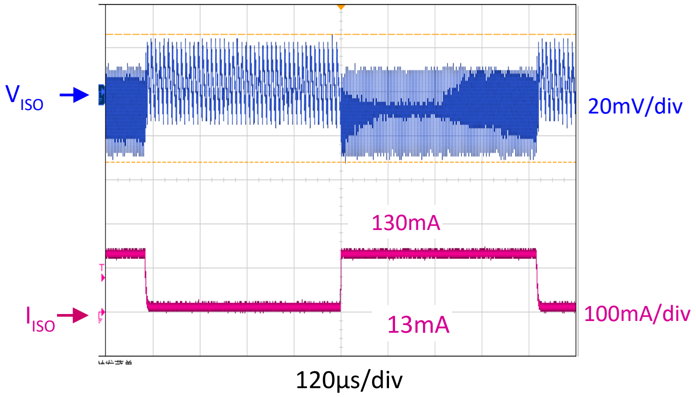


Figure 7-22.
V_{CC} = 5V, V_{ISO} = 3.3V, 13mA to 130mA I_{ISO} load transient, R_L = NC
V_{ISO} Ripple Voltage: 58mV$_{P-P}$

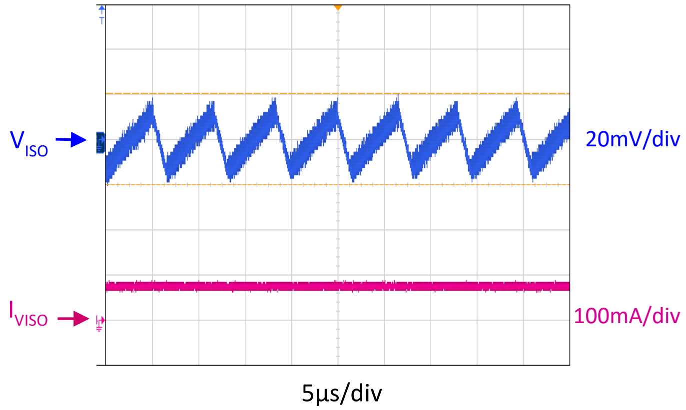


Figure 7-23.
V_{CC}=3.3V, V_{ISO}=3.3V, I_{ISO}= 75mA, R_L = NC
V_{ISO} Ripple Voltage: 40mV$_{P-P}$

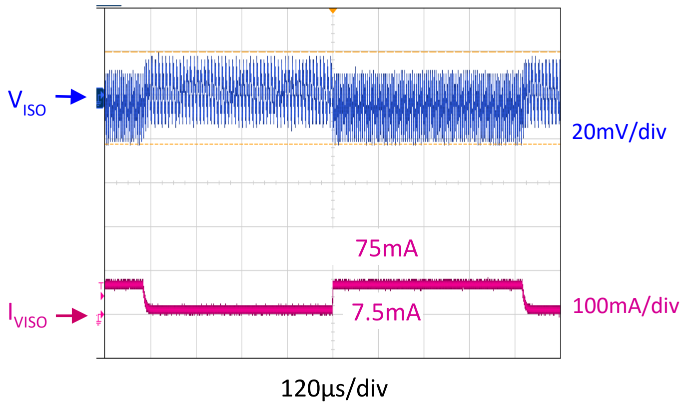


Figure 7-24.
V_{CC} = 3.3V, V_{ISO} = 3.3V,7.5mA to 75mA I_{ISO} load transient, R_L = NC
V_{ISO} Ripple Voltage: 42mV$_{P-P}$

8. Parameter Measurement Information

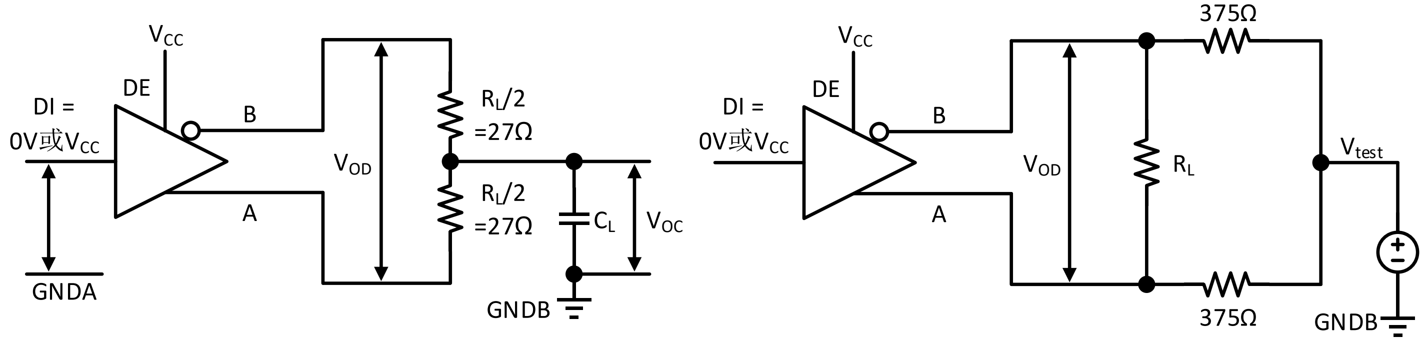


Figure 8-1. Driver DC Test Circuit

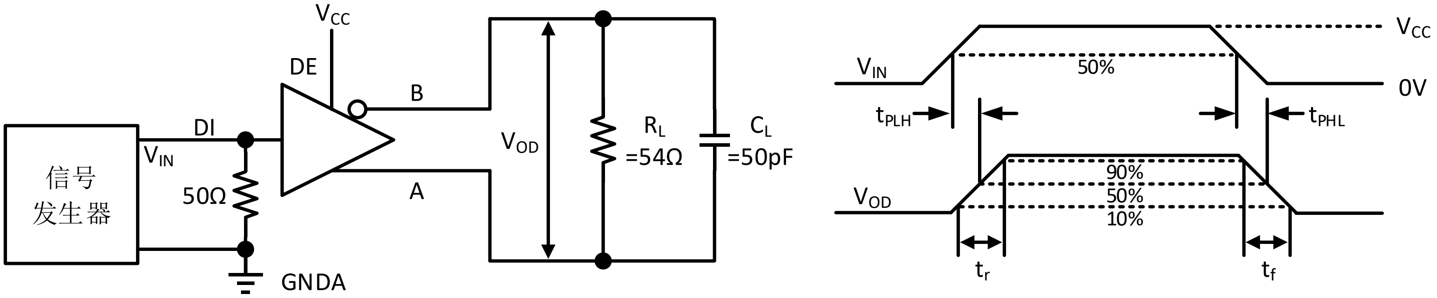


Figure 8-2. Driver Propagation Delays

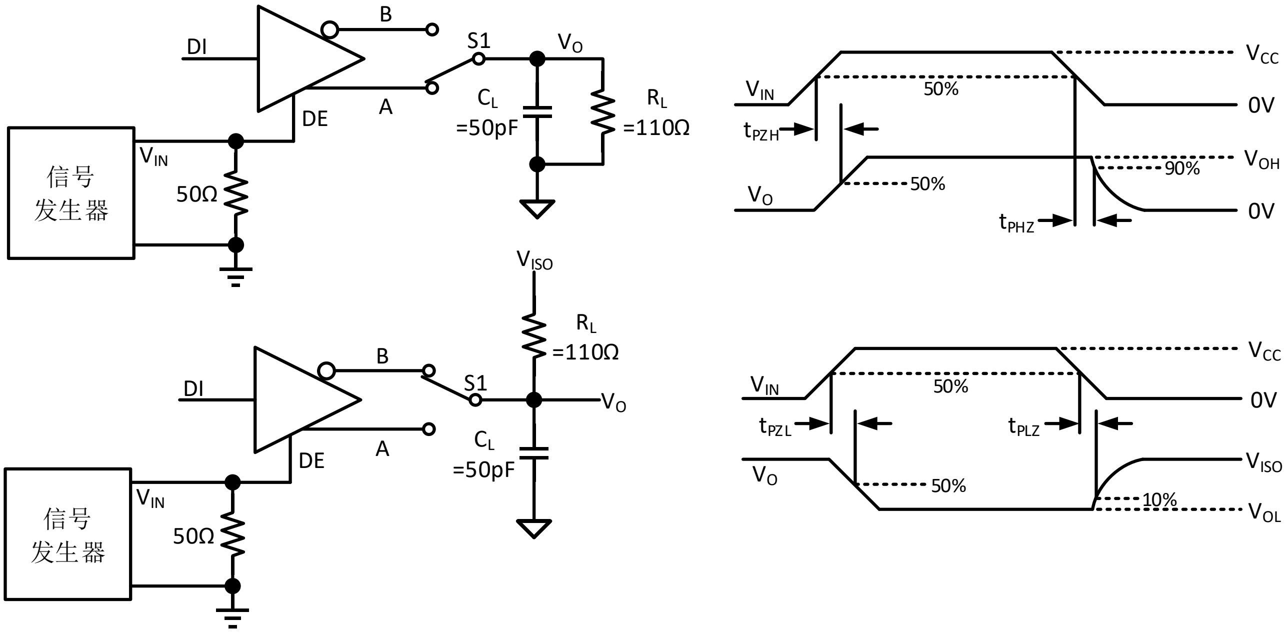


Figure 8-3. Driver Enable and Disable Times

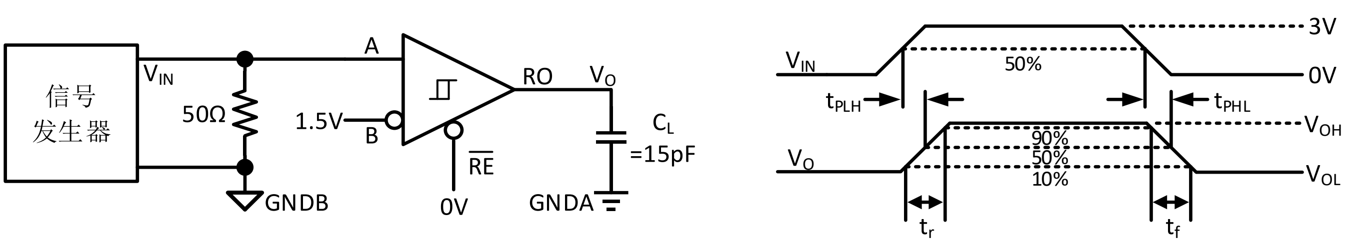


Figure 8-4. Receiver Propagation Delays

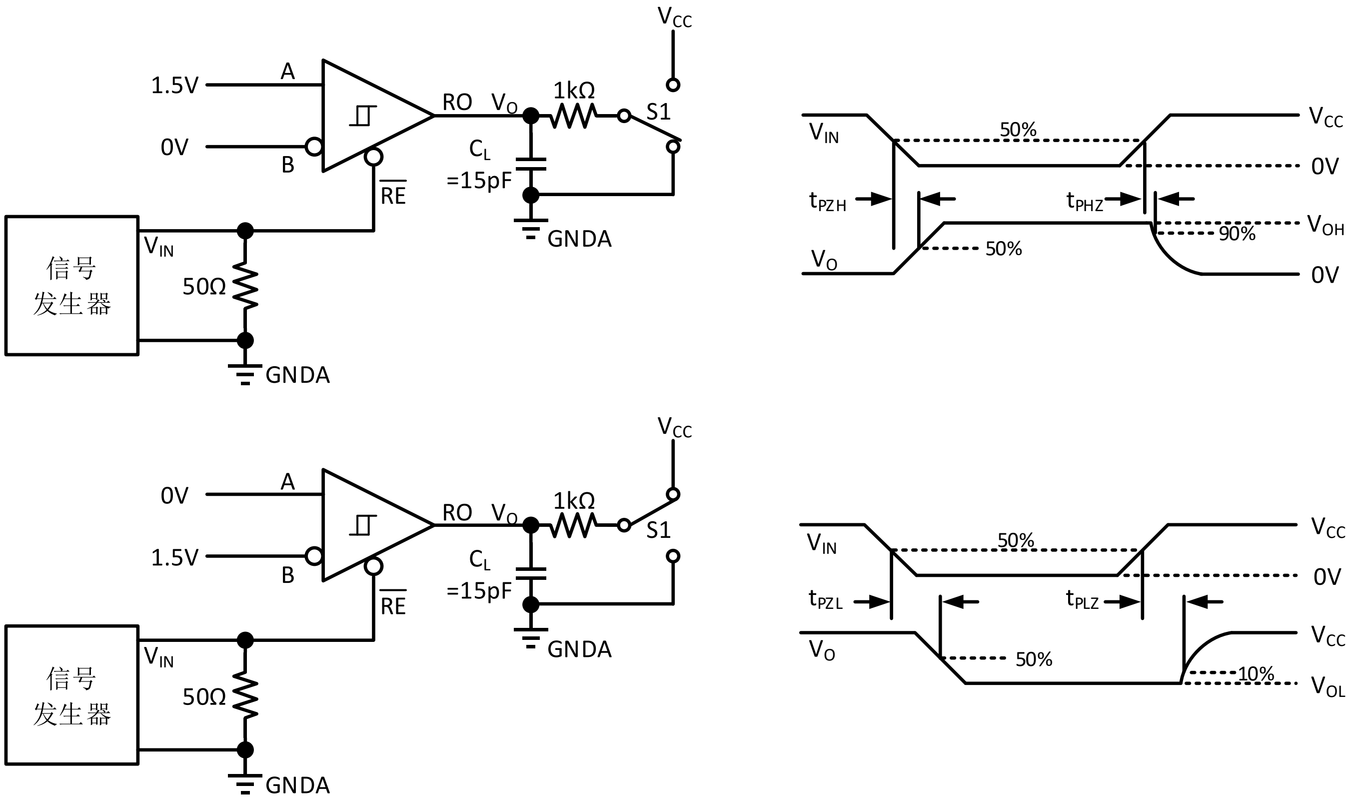


Figure 8-5. Receiver Enable and Disable Times

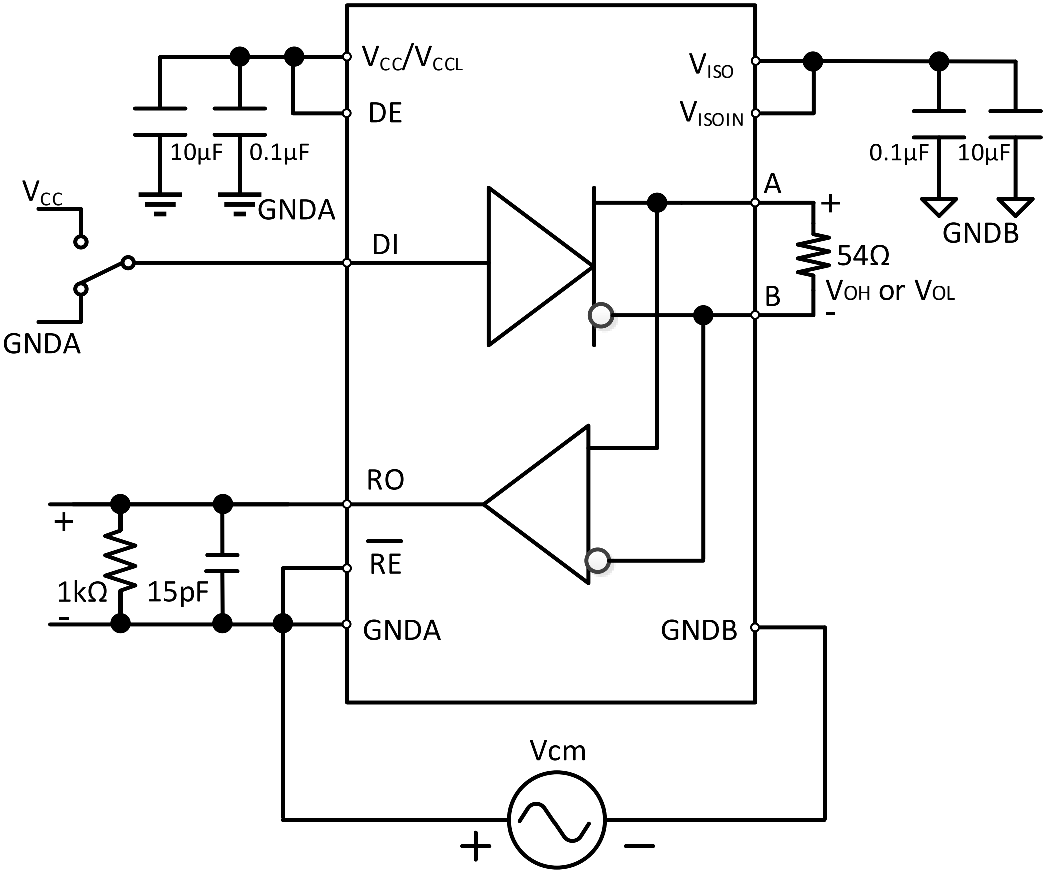


Figure 8-6. Common Mode Transient Immunity (CMTI) Test for the Half-duplex

9. Detailed Description

The CA-IS2092 isolated half-duplex RS-485 transceivers provide up to 3.75kV$_{RMS}$ of galvanic isolation between the cable side (bus-side) of the transceiver and the controller side (logic-side). These devices feature up to 150kV/µs common mode transient immunity, allow up to 0.5Mbps communication across an isolation barrier. Power isolation is achieved with an integrated DC-DC convertor to generate a regulated 3.3V or 5V supply for the cable-side circuit. These devices do not require any external components other than bypass capacitors and bus termination resistors to realize an isolated RS-485 port. Robust isolation coupled with extended ESD protection and increased speed enables efficient communication in noisy environments, making them ideal for long distance transmission and multi-drop communication in a wide range of applications such as motor drives, PLC communication modules, telecom rectifiers, elevators, HVACs etc. systems. Two mechanisms against excessive power dissipation caused by faults or bus contention. The first, over-current protection on the output stage, provides immediate protection against short circuits over the entire common-mode voltage range. The second, a thermal shutdown circuit, forces the driver outputs into a high-impedance state.

9.1. Logic Input

The CA-IS2092x devices include three logic inputs on the logic side: receiver enable, driver enable and driver digital input. The driver enable control DE pin has an internal weak pull-down to GNDA, while the digital input DI and receiver enable pins have an internal pull-up to V_{CC}/V_{CCL}, see Figure 9-1 the input equivalent circuit.

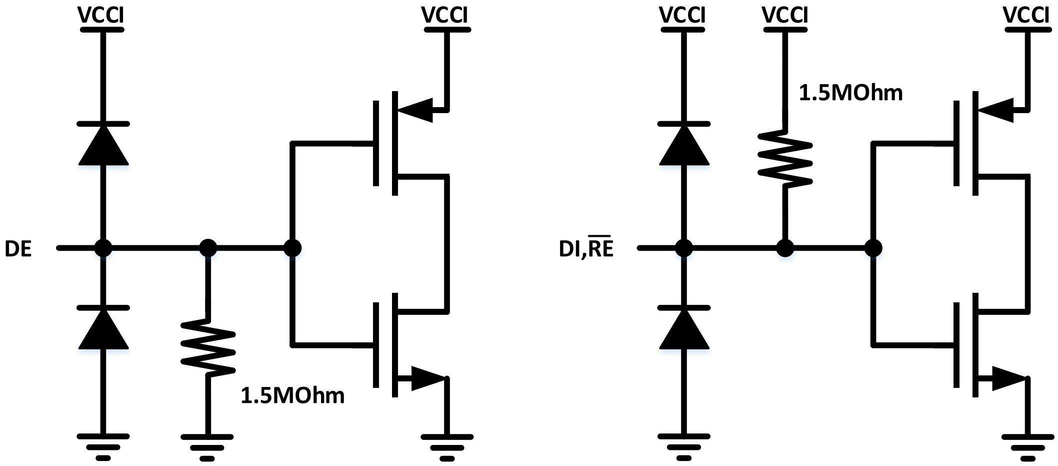


Figure 9-1. Input equivalent circuit

9.2. Fail-Safe Receiver

The receiver reads the differential input from the bus line (A and B) and transfers this data as a single-ended, logic-level output RO to the controller. Driving the enable input $\overline{RE}$ low to enable the receiver. Driving $\overline{RE}$ logic high to disable the receiver. RO is high impedance when $\overline{RE}$ is logic high. The $\overline{RE}$ pin has an internal pull-up resistor to V_{CC} for CA-IS2092W or V_{CCL} for CA-IS2092VW.

The CA-IS2092x family of RS-485 transceivers do not require external fail-safe bias resistors because a true fail-safe feature is integrated into the devices. In true fail-safe, the receiver's positive-going input threshold is $V_{IT+(IN)}$ (-110mV, typ. and -50mV, max.), if the differential receiver input voltage of V_A-V_B is greater than or equal to $V_{IT+(IN)}$, RO is logic high when $\overline{RE}$ is low; RO is logic low when V_A-V_B is less than or equal to $V_{IT-(IN)}$ in case the receiver is enabled; thereby eliminating the need for fail-safe bias resistors while complying fully with the RS-485 standard, see Table 9-1 the receiver truth table. Fail-safe feature is used to keep the receiver's output in a defined state when the receiver is not connected to the cable, the cable has an open or the cable has a short.

Table 9-1. Receiver Truth Table

DIFFERENTIAL INPUT: $V_{ID} = (V_A - V_B)$	ENABLE ($\overline{RE}$)	OUTPUT (RO)
$V_{IT+(IN)} \le V_{ID}$	L	H
$V_{IT-(IN)} < V_{ID} < V_{IT+(IN)}$	L	Indeterminate
$V_{ID} \le V_{IT-(IN)}$	L	L
X	H	Hi-Z
Open/Short/Idle	L	H
X	Open	Hi-Z

Notes:

1. X = don't care; H = high level; L = low level; Hi-Z = high impedance.
2. $\overline{RE}$ has an internal weak pull-up to V_{CC}.

9.3. Driver

The transmitter converts a single-ended input signal (DI) from the local controller to differential outputs on the bus lines A and B. The truth table for the transmitter is provided in Table 9-2, the driver enable control DE pin has an internal weak pull-down to GNDA, see Figure 9-1 the input equivalent circuit; while the digital input DI pin has an internal pull-up to V_{CC} for CA-IS2092W or V_{CCL} for CA-IS2092VW. The driver outputs and receiver inputs on the bus side are protected from ±20kV electrostatic discharge (ESD) to GNDB, as specified by the Human Body Model (HBM). The driver outputs also feature short-circuit protection and thermal shutdown.

Table 9-2. Transmitter Truth Table

T_X INPUT	ENABLE INPUT	OUTPUT	
(DI)	(DE)	A	B
H	H	H	L
L	H	L	H
X	L	Hi-Z	Hi-Z
X	OPEN	Hi-Z	Hi-Z
OPEN	H	H	L

Notes:

1. X = don't care; H = high level; L = low level; Hi-Z = high impedance.
2. DE pin has an internal weak pull-down to GNDA, and DI pin has an internal pull-up to V_{CC}/V_{CCL}.

9.4. Protection Functions

9.4.1. Signal Isolation and Power Isolation

The CA-IS2092x devices integrated digital galvanic isolators using Chipanalog's capacitive isolation technology based on the ON-OFF keying (OOK) modulation scheme, allow data transmission between the controller side and cable side of the transceiver with different power domains. Also, the power isolation is achieved with an integrated DC-DC convertor to generate a regulated 3.3V or 5V supply for the cable-side.

9.4.2. Undervoltage Lockout

Both CA-IS2092V and CA-IS2092VW have undervoltage detection on V_{CC} supply terminal, the CA-IS2092VW also features undervoltage detection on V_{CCL} supply terminal, that place the device in protected mode during an undervoltage event on V_{CCL} or/and V_{CC}, see Table 9-3 and Table 9-4. Once the undervoltage condition is cleared and the supply voltage has returned to a valid level, the devices transition to normal mode. The host controller should not attempt to send or receive messages until the device enters normal operation.

Table 9-3. CA-IS2092W Undervoltage Lockout

V_{CC}	DEVICE STATE	BUS OUTPUT	RXD
> $V_{CC(UVLO+)}$	Normal	Per TXD	Mirrors Bus
< $V_{CC(UVLO-)}$	Protected mode	High Impedance	High Impedance

Table 9-4. CA-IS2092VW Undervoltage Lockout

V_{CC}	V_{CCL}	DEVICE STATE	BUS OUTPUT	RXD
> $V_{CC(UVLO+)}$	> $V_{CCL(UVLO+)}$	Normal	Per TXD	Mirrors Bus
< $V_{CC(UVLO-)}$	> $V_{CCL(UVLO+)}$	Protected mode	High Impedance	High Impedance
> $V_{CC(UVLO+)}$	< $V_{CCL(UVLO-)}$	Protected mode	High Impedance	High Impedance
< $V_{CC(UVLO-)}$	< $V_{CCL(UVLO-)}$	Protected mode	High Impedance	High Impedance

9.4.3. Thermal Shutdown

If the junction temperature of the CA-IS2092x device exceeds the thermal shutdown threshold $T_{J(shutdown)}$ (180°C, typ.), the driver outputs go high-impedance state. The shutdown condition is cleared when the junction temperature drops to normal operation temperature range of the device (160°C, typ.).

9.4.4. Current Limiting

The CA-IS2092x protect the transmitter output stage against a short-circuit to a positive or negative voltage over the common mode voltage range of -7V to 12V by limiting the driver current. However, this will cause large supply current and dissipation. Thermal shutdown further protects the devices from excessive temperatures that may result from a short circuit fault. The transmitter returns to normal operation once the short is removed.

9.5. Isolated Supply Output

The integrated DC-DC converter provide up to 650mW of isolated power with +3.3V or +5V fixed output voltage configurations, depending on the SEL pin status, see Table 9-5 for the supply configurations of CA-IS2092x devices. Get the SEL pin fixed (connect to V_{ISO} or GNDB) before power on the transceivers.

Table 9-5. Supply Configuration

SEL INPUT	V_{CC}	V_{ISO}
Shorted to V_{ISO}	5 V	5V
Shorted to GNDB or floating	5 V	3.3V
Shorted to GNDB or floating	3.3 V [1]	3.3V [2]

Notes:

1. V_{DD} = 3.3 V, SEL shorted to V_{ISO} (essentially V_{ISO} = 5 V) is not recommended.
2. The SEL pin has a weak pull-down internally. However, for V_{ISO} = 3.3 V, the SEL pin should be connected to the GNDB externally, especially in the noisy system.

The maximum output current from V_{ISO} is shown as Table 9-6. Note that the I_{ISO} value in Table 9-6 is the maximum output current at +25°C with data rate x load capacitance < 0.5Mbps × 2nF. As the increase of temperature, especially when the temperature exceeds +85°C, the maximum load current will be decreased, see more details in Figure 9-2,Figure 9-6 and Figure 9-8.

Table 9-6. Maximum Output Current of V_{ISO} @ T_A = 25°C

Supply voltage V_{CC} (V)	V_{ISO} (V)	R_L (Ω) between A and B	I_{ISO} (mA)
4.5~5.5	5	NC[1]	130
4.5~5.5	3.3		130
3.15~3.6	3.3		75
4.5~5.5	5	100	80
4.5~5.5	3.3		105
3.15~3.6	3.3		40
4.5~5.5	5	54	55
4.5~5.5	3.3		85
3.15~3.6	3.3		30

Note:

1. NC means no-load connection between A and B

10. Applications Information

10.1. Overview

The CA-IS2092 family of half-duplex RS-485 transceivers commonly used for asynchronous data transmissions. For half-duplex devices, the driver and receiver enable pins allow for the configuration of different operating modes. Because of high peak currents flowing through V_{CC} and V_{ISO} supplies, bulk capacitance of typical 10µF (or at least 4.7µF) is recommended on both pins. Higher values of bulk capacitors are helpful to reduce noise and ripple further and enhance performance, see Figure 10-1 the typical application circuit. Make sure there is no data transmission during the CA-IS2092X power up.

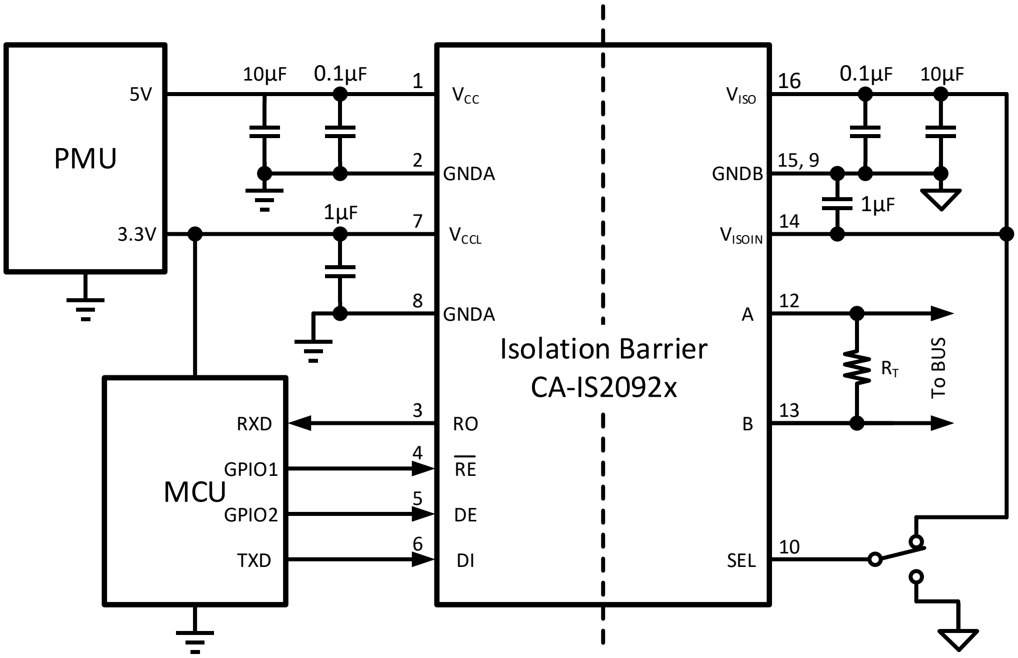


Figure 10-1. Typical application circuit

10.2. Typical Application

An RS-485 bus consists of multiple transceivers connecting in parallel to a bus cable. As seen in the following typical network application circuit, Figure 10-2. The maximum recommended data rate in the RS-485/RS422 network is 10Mbps, which can be achieved at a maximum cable length of 40ft (12m). The absolute maximum distance is 4000ft (1.2km) of cable, at which point, data rate is limited to 100kbps. These were the specifications made in the original RS-485 standard, new RS-485 transceivers and cables are pushing the limit of RS-485 far beyond its original definitions. However, the maximum data rate is still limited by the bus loading, number of nodes, cable length etc. factors. For RS-485 network design, margin must be given for signal loss across the system and cabling, parasitic loadings, timing, network imbalances, ground offsets and signal integrity thus a practical maximum data rate, number of nodes often lower. To minimize reflections, terminate the line at both ends with a termination resistor (120Ω in the typical application circuits), whose value matches the characteristic impedance (Z_0) of the cable, and keep stub lengths off the main line as short as possible. As a general rule moreover, termination resistors should be placed at both far ends of the cable. This method, known as parallel termination, generally allows for higher data rates over longer cable length.

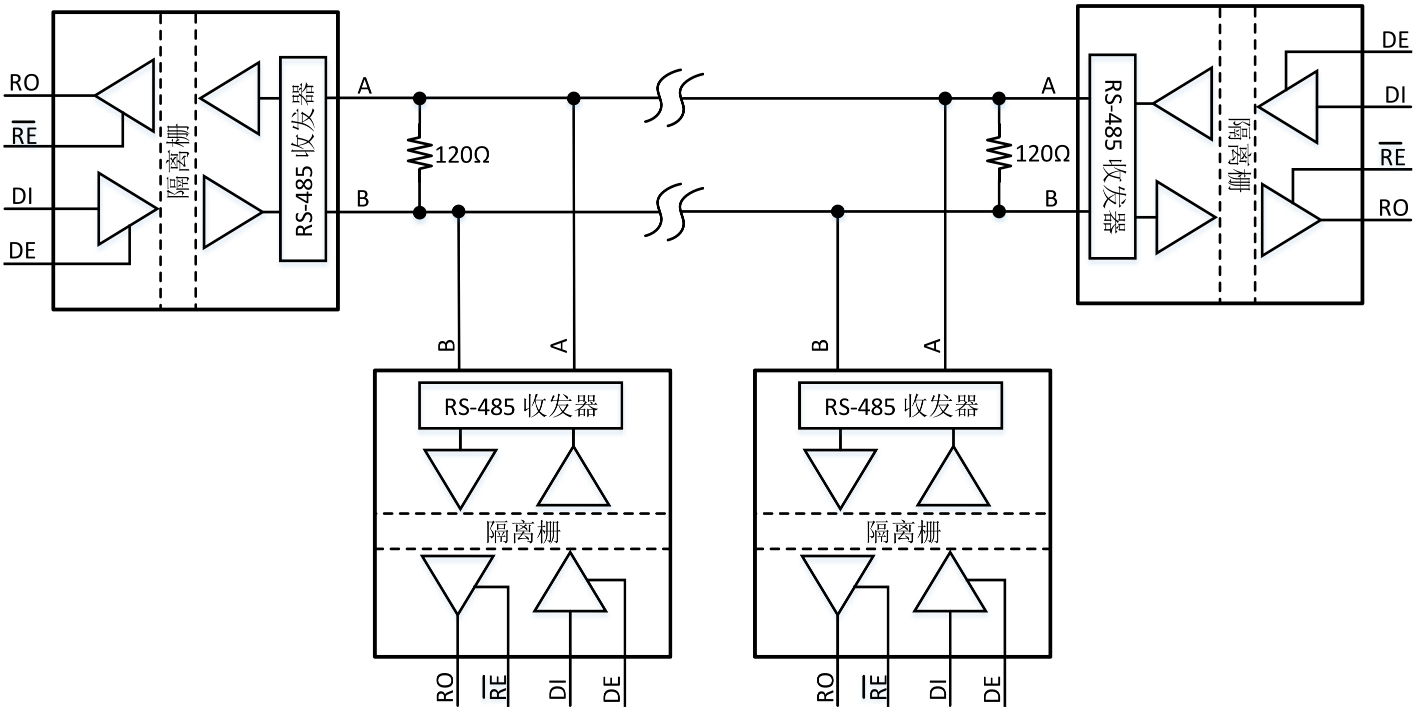


Figure 10-2. Typical isolated half-duplex RS-485 application circuit

10.3. 256 transceivers on the bus

The maximum number of transceivers and receivers allowed depends on how much each device loads down the system. All devices connected to an RS-485 network should be characterized in regard to multiples or fractions of unit loads. The maximum number of unit loads allowed one twisted pair, assuming a properly terminated cable with a characteristic impedance of 120Ω or more, is 32 (375Ω). The CA-IS2092x transceivers have a 1/8-unit load (96kΩ) receiver, which allows up to 256 transceivers, connected in parallel, on one communication line.

10.4. PCB Layout

Careful PCB layout is critical to achieve clean and stable communication operation. It is recommended to design an isolation channel underneath the isolator that is free from ground and signal planes. Any galvanic or metallic connection between the cable side and logic side will defeat the isolation. To make sure device operation is reliable at all data rates and supply voltages, the minimum 0.1µF//10µF decoupling capacitors between V_{CC} and GNDA, between V_{ISO} and GNDB are recommended. For the individual logic supply input V_{CCL} and V_{ISOIN}, we recommend to use a 1µF ceramic capacitors with X5R or X7R between V_{CCL} pin and GNDA, V_{ISOIN} and GNDB. Place the bypass capacitors, and the CA-IS2092x IC on the same PCB layer. Place decoupling capacitors as close as possible to the CA-IS2092x device pins, see Figure 10-3 recommended components placement for the PCB layout. The paths must be wide and short to minimize inductance, also any via holes must be avoided on these paths.

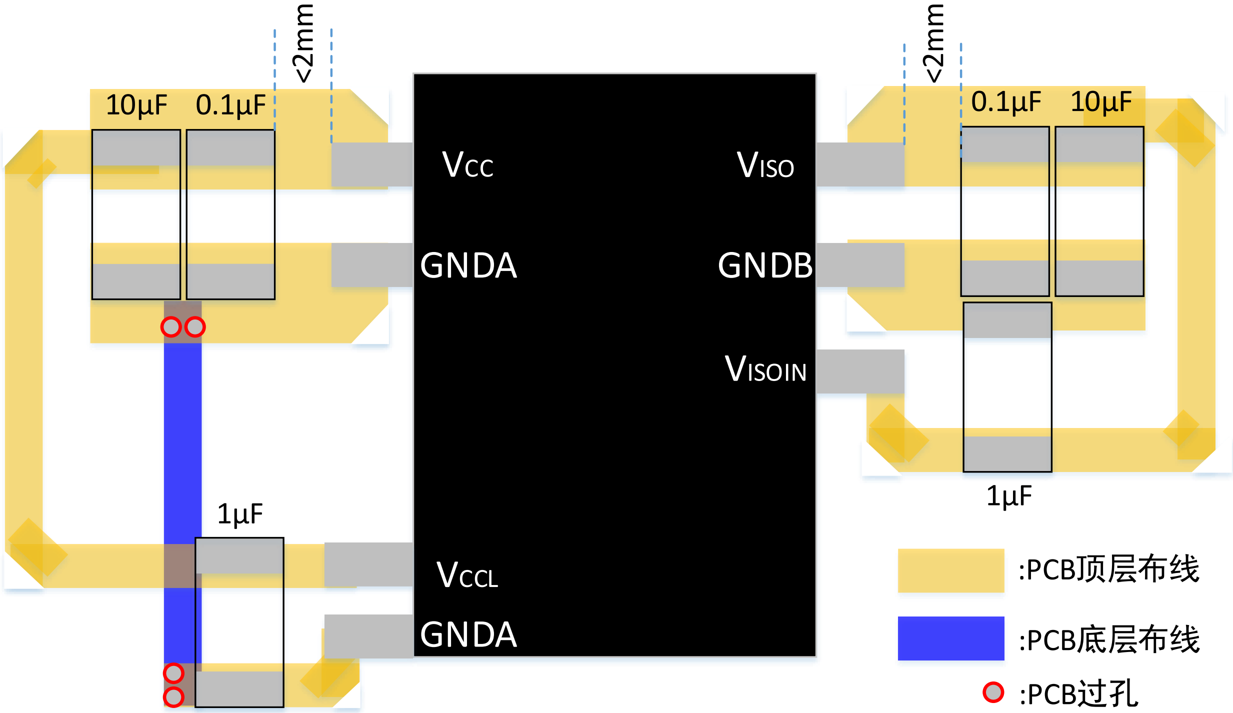
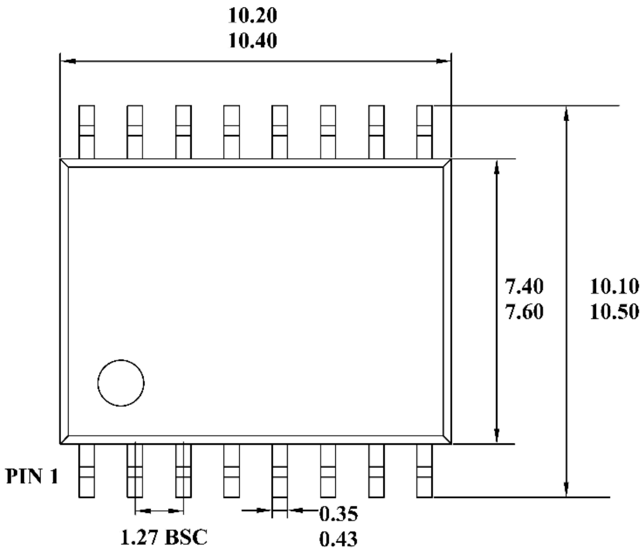


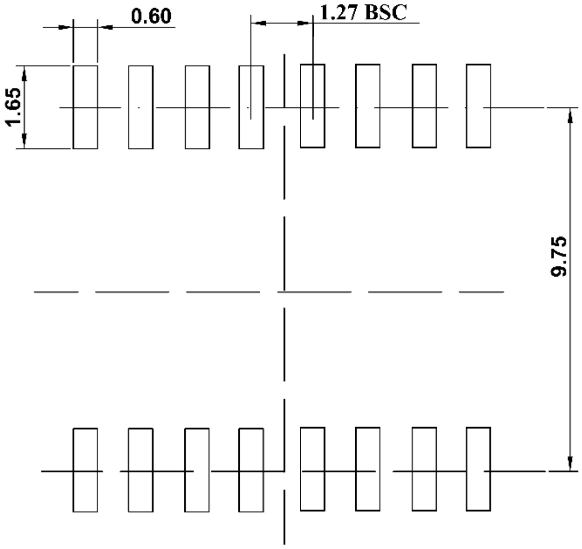
Figure 10-3. Recommended PCB Layout

11. Package Information

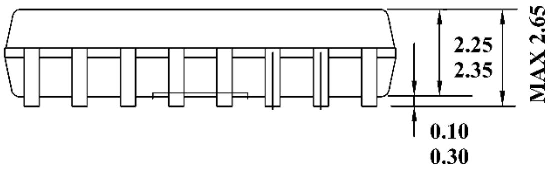
16-Pin Wide Body SOIC Package Outline



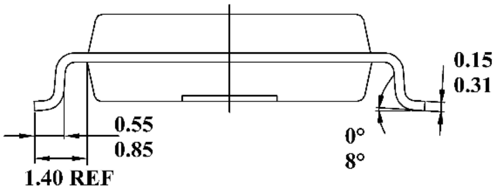
TOP VIEW



RECOMMENDED LAND PATTERN



FRONT VIEW



LEFT SIDE VIEW

Note:

1. All dimensions are in millimeters, angles are in degrees.

12. Soldering Temperature (Reflow) Profile

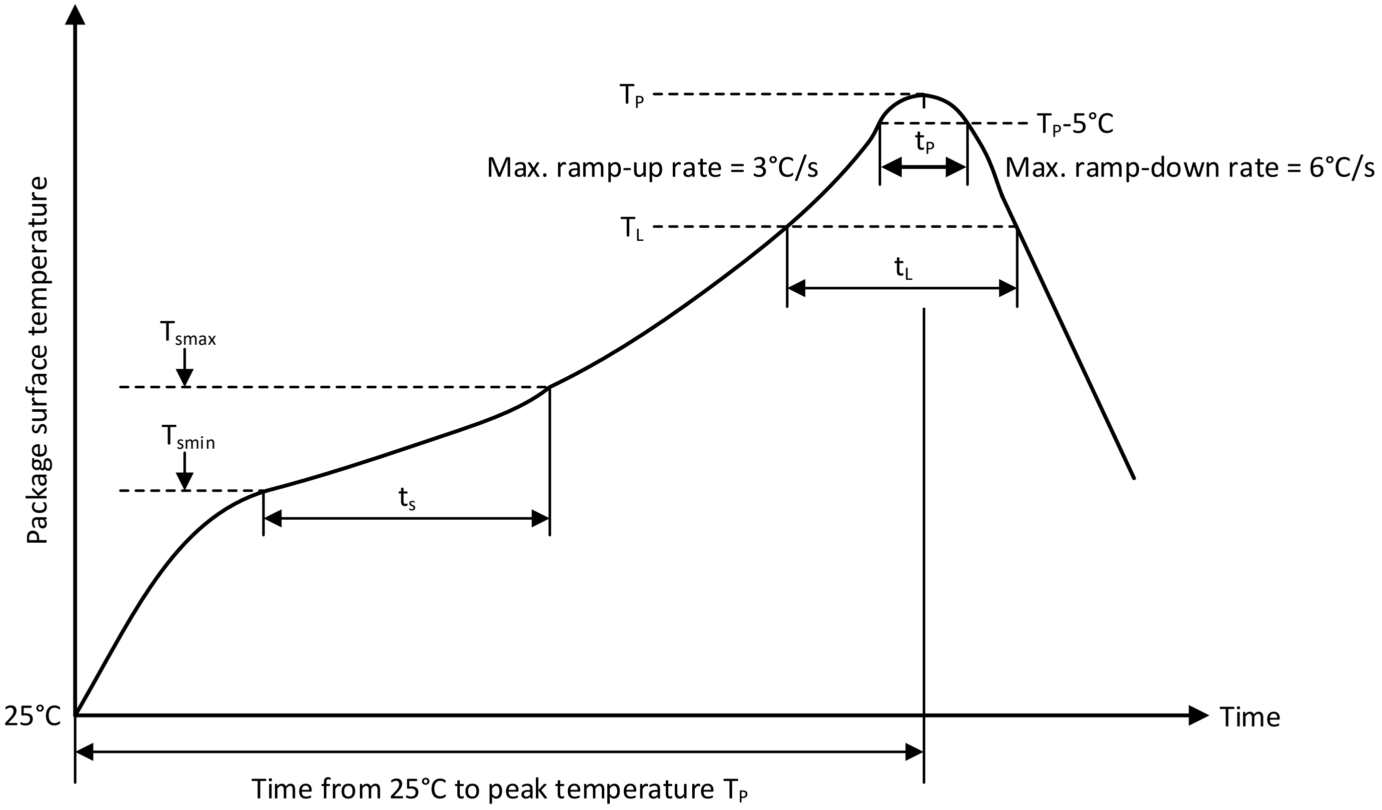
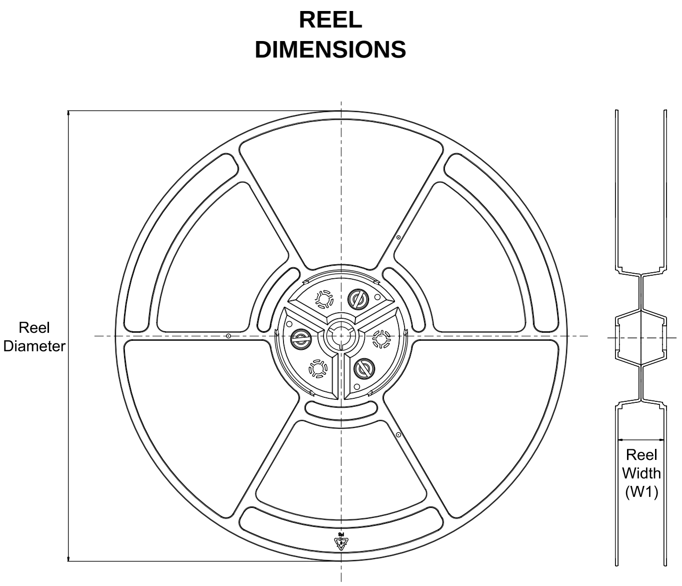


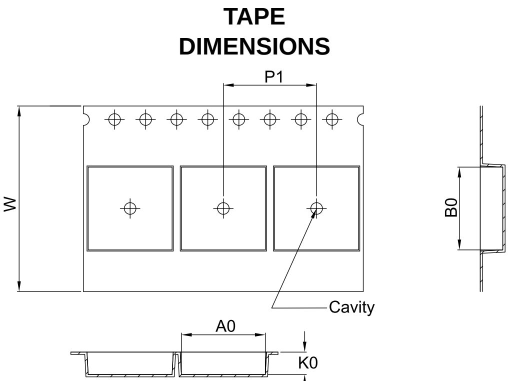
Figure. 12-1 Soldering Temperature (reflow) Profile

Table. 12-1 Soldering Temperature Parameter

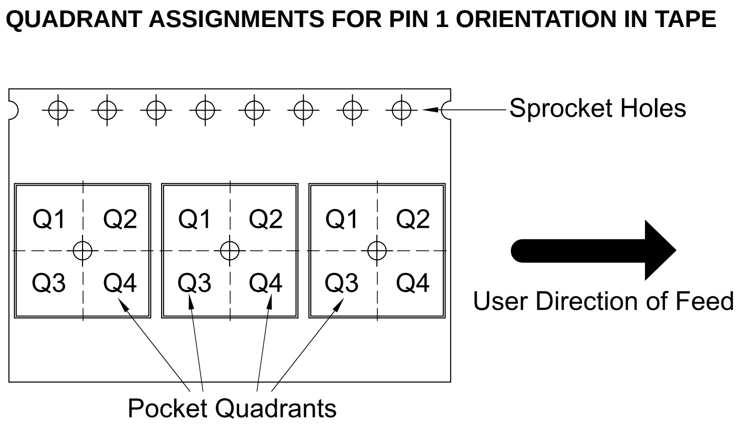
Profile Feature	Pb-Free Soldering
Ramp-up rate (T_L = 217°C to peak T_P)	3°C/s max
Time t_s of preheat temp (T_{smin} = 150°C to T_{smax} = 200°C)	60~120 seconds
Time t_L to be maintained above 217°C	60~150 seconds
Peak temperature T_P	260°C
Time t_P within 5°C of actual peak temp	30 seconds max
Ramp-down rate (peak T_P to T_L = 217°C)	6°C/s max
Time from 25°C to peak temperature T_P	8 minutes max

13. Tape And Reel Information





A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CA-IS2092W	SOIC	W	16	1000	330	16.4	10.9	10.7	3.2	12.0	16.0	Q1
CA-IS2092VW	SOIC	W	16	1000	330	16.4	10.9	10.7	3.2	12.0	16.0	Q1

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